MATERIALS SCIENCE

High-performance and scalable metal-chalcogenide semiconductors and devices via chalco-gel routes

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We report a general strategy for obtaining high-quality, large-area metal-chalcogenide semiconductor films from precursors combining chelated metal salts with chalcoureas or chalcoamides. Using conventional organic solvents, such precursors enable the expeditious formation of chalco-gels, which are easily transformed into the corresponding high-performance metal-chalcogenide thin films with large, uniform areas. Diverse metal chalcogenides and their alloys (MQ_x: M = Zn, Cd, In, Sb, Pb; Q = S, Se, Te) are successfully synthesized at relatively low processing temperatures (<400°C). The versatility of this scalable route is demonstrated by the fabrication of large-area thin-film transistors (TFTs), optoelectronic devices, and integrated circuits on a 4-inch Si wafer and 2.5-inch borosilicate glass substrates in ambient air using CdS, CdSe, and In_2Se_3 active layers. The CdSe TFTs exhibit a maximum field-effect mobility greater than 300 $cm^2 V^{-1} s^{-1}$ with an on/off current ratio of $>10^7$ and good operational stability (threshold voltage shift < 0.5 V at a positive gate bias stress of 10 ks). In addition, metal chalcogenide–based phototransistors with a photodetectivity of $>10^{13}$ Jones and seven-stage ring oscillators operating at a speed of ~2.6 MHz (propagation delay of < 27 ns per stage) are demonstrated.

INTRODUCTION

Because of increasing demands for large-area, high-performance electronics, high-mobility semiconducting materials that are compatible with conventional complementary metal-oxide semiconductor (CMOS) processing and that can form large-area films are required (*1*, *2*). In this regard, semiconducting materials, such as organic, metal-oxide, and low-dimensional layered semiconductors, have been extensively investigated because of their promising electrical properties and solution processability. In particular, low-dimensional layered semiconductors, such as graphene (*3*, *4*), transition metal dichalcogenides (TMDCs) (*5*–*8*), and colloidal nanocrystal semiconductors (*9*–*11*), have been used to realize high-performance electrical and optical devices including displays, sensors, and complex integrated systems (*7*, *12*–*14*). Before the industrial success of amorphous silicon-based thin-film transistor (TFT) technology, metal chalcogenides, such as CdS and CdSe, were considered as one of the most promising semiconductor material classes for early-stage TFT development (*15*, *16*). Recently, TMDCs have re-emerged as alternative channel materials because they exhibit excellent carrier mobilities (>100 $cm^2 V^{-1} s^{-1}$) with sizeable band gaps in the range of 1 to 2 eV, offering promise as active elements in future high-performance optoelectronic devices (*7*). In addition, recent reports on dimensional reduction approaches by dissolving metal chalcogenides in strongly coordinating or chemical-reducing environments, such as thiol-amines and hydrazine, enabled the low-cost deposition of some metal-chalcogenide films, which have inherent solubility limitations (*17*, *18*). For example, hydrazine as a highly reducing and basic solvent can generate thermally decomposable hydrazinium chalcometallates as soluble metal-chalcogenide precursors for some post-transition metal chalcogenides (*18*). Similarly, the dissolution of metal chalcogenides with thiol-amines has been recently reported with limited material choices (*17*). Although these advances are noteworthy, there are several remaining challenges, such as complex and toxic processes for solution syntheses, the limited materials choice with inherent chemical solubility, and the difficulty of area-scalable on-chip device integrity as in conventional CMOS processes.

Previously, our groups have reported that solution-processed inorganic semiconductor devices based on metal oxides and metal-chalcogenide nanocrystals could serve as a replacement for vacuum-deposited semiconductor devices (*19*–*21*). Although the possibility of solution-derived metal-chalcogenide devices has been proposed, the insufficient electrical performance and limited materials scope combined with the lack of underlying physicochemical mechanisms for generalized material synthesis, as well as the uniform production of a broad range of uniform area-scalable on-chip devices, remained as challenges. Here, we report a new strategy to expand the scope of high-performance and large-area solution-processable semiconductors via a generalized chalco-gel route. In particular, we used stabilized organochalcogen precursors (chalcoureas or chalcoamides) and chelated metal salts to access diverse metal chalcogenides and their alloys (MQ_x: M = Zn, Cd, In, Sb, Pb; Q = S, Se, Te), which can be converted into high-performance, large-area polycrystalline semiconducting films at relatively low temperatures (<400°C). This approach enables the preparation of a variety of metal-chalcogenide films by an environmentally benign solution process, and we demonstrate their viability in the scalable production of various uniform devices and integrated optoelectronics. The results reported here argue that chalco-gel–processed metal chalcogenides offer a general route to realize high-performance and extremely stable solution-processed semiconductor thin-film devices with marginal toxicity and heat input, offering compatibility with standard CMOS processing and large-scale on-chip device applications.

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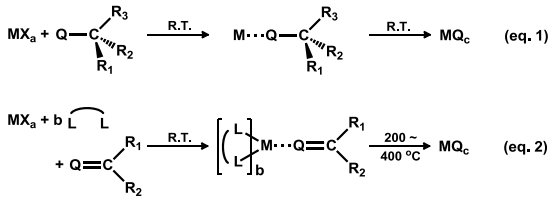
RESULTS

Key synthetic design of the metal-chalcogenide precursors

Unlike typical oxide sol-gel precursors having stable carbon-oxygen single bonds, the weak carbon-chalcogen bond in R-Q-M species (R = organic leaving group, Q = chalcogen, M = metal) generally results in uncontrolled condensation processes and rapid precipitation even at 25°C, thus impeding chalco-gel formation (Eq. 1). In particular, compared to C–O bonding [bond energy (D) ≈ 380 kJ/mol], the significant instability/weakness of C–Se (D ≈ 234 kJ/mol) and C–Te (D ≈ 200 kJ/mol) bonding has challenged the design of soluble metal-chalcogenide precursors with useful stability. As described in Eq. 2, we envisioned that organochalcogen stabilization could be achieved through the formation of strong C=Q double bonds or stabilizing resonance structures, which would favor stable metal-chalcogen coordination (*22*). In addition, chelating ligands that saturate the metal ion coordination sphere should retard possible side reactions between the organochalcogen ligand and the metal ion, which would promote uncontrolled condensation processes. Without a chelating stabilizer (for example, acetylacetonate), the precursor solution undergoes slow decomposition and precipitation at 25°C (Eq. 1). Overall, these synergetic improvements of thermodynamic and kinetic stability could be used for the solution-derived deposition of diverse metal-chalcogenide films with virtually unlimited metal-chalcogen combinations (table S1).



M = metal ion; X = anion; L-L = chelating ligand; Q = S, Se, Te; R_1, R_2, R_3 = organic group

Figure 1A illustrates a representative synthetic process for a CdSe precursor, as an example of CdSe thin-film formation. In the synthetic process, the formation of the precursor solution begins with a chelated metal complex and a stable organochalcogen precursor. The binding between the metal-organochalcogen and the metal-chelating ligand is confirmed with ^{113}Cd nuclear magnetic resonance (NMR) spectroscopy (Fig. 1B). The chemical shifts (δ) of 97.5 ppm (parts per million) and 105.4 ppm for thiourea- and selenourea-coordinated Cd(II), respectively,

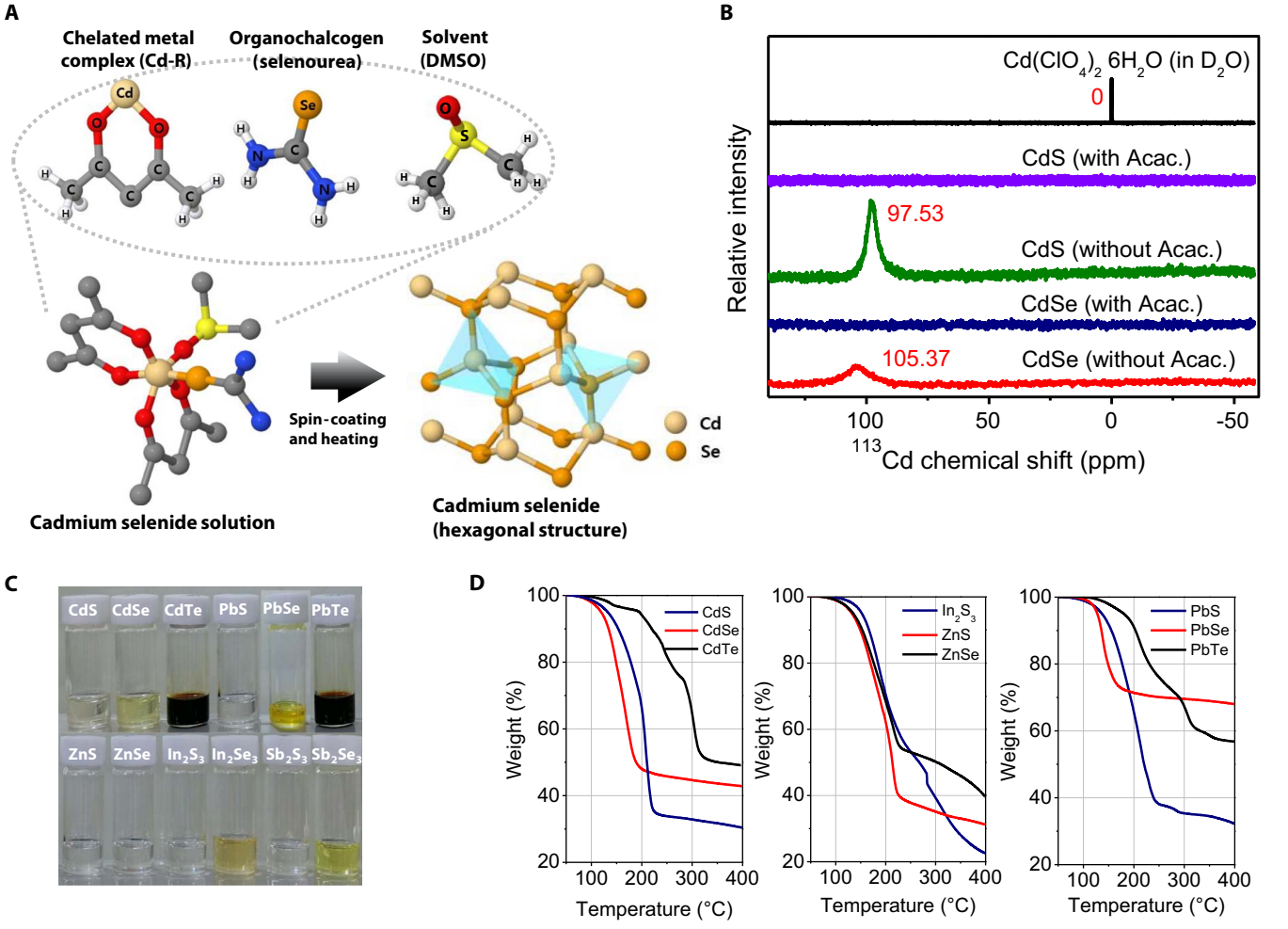


Fig. 1. Synthetic procedure for metal-chalcogenide precursor solutions and thin films. (**A**) Schematic illustration describing the chalco-gel–based synthesis of a CdSe precursor solution and thin-film formation. (**B**) NMR chemical shifts of ^{113}Cd compounds. (**C**) Photographic images of a series of metal (M = Cd, Pb, Zn, In, Sb)–chalcogenide (Q = S, Se, Te) solutions. (**D**) TGA of CdS, CdSe, CdTe, In_2S_3, ZnS, ZnSe, PbS, PbSe, and PbTe precursor solutions.

are well matched with literature data (*23*). The organochalcogen-coordinated Cd(II) acetylacetonate complex shows the disappearance of the ^{113}Cd resonance, consistent with known acetylacetonate-Cd(II) relaxation time/line broadening effects (*24*). The ^{1}H NMR spectrum in fig. S1 confirms the coordination of acetylacetonate to Cd(II). The strong hydrogen bonding between metal complexes or the direct linkage with the bidentate ligand is necessary for stable chalco-gel formation, which, in turn, facilitates useful solution processability (fig. S2). The precursor solutions for chalco-gels can be prepared with diverse polar solvents, including 2-methoxyethanol (2-ME), *N*,*N*′-dimethylformamide (DMF), dimethyl sulfoxide (DMSO), and *N*-methylformamide (NMF), which provide complete dissolution of the metal salts and organochalcogens.

The versatility of the present approach was demonstrated by formulating various metal-chalcogenide precursor solutions with corresponding metal-chalcogenide elements (MQ_x: M = Zn, Cd, In, Sb, Pb; Q = S, Se, Te) (Fig. 1C). Because of the strong affinity between soft metal cations (such as Pb^{2+}, Cd^{2+}, etc.) and soft chalcogen anions, the soluble precursors with soft metal cations are usually difficult to achieve with the reported solvent systems, such as hydrazine and thiol-amines (*17*). Further information on the precursors is provided in table S2. Figure 1D shows the thermogravimetric analysis (TGA) for various metal-chalcogenide solutions with DMSO as the solvent, measured in a flowing Ar atmosphere. As depicted, the gradational weight loss is accompanied by the decomposition process, which can be attributed to the evaporation of residual solvent and elimination of various organic compounds contained in the precursors. Note that the low-temperature (<350°C) decomposition of the metal-chalcogenide solutions indicates the viability of low temperature–processed materials using these metal-chalcogenide precursors. Depending on the choice of organochalcogen, metal salt anion, and chelating stabilizer, the chalco-gel with different residual solvent and chelating stabilizer compositions could show diverse thermal decomposition routes.

Characterization of the metal-chalcogenide thin films

First, it is important to demonstrate continuous and uniform thin-film formation with the present solution-based processing strategy. To characterize the thin films, various metal-chalcogenide solutions were spun onto Si wafer or borosilicate glass substrates with subsequent thermal annealing at a temperature of <400°C for 30 min under a nitrogen atmosphere. As confirmed by high-resolution transmission electron microscopy (HRTEM) images (Fig. 2A), smooth and continuous metal-chalcogenide films with thicknesses in the range of 14 to 18 nm are successfully obtained. The HRTEM cross-sectional image of a CdSe film demonstrates continuous film formation with a well-defined polycrystalline structure. Furthermore, atomic force microscopy (AFM) images of various metal-chalcogenide films show that the films have smooth surfaces with a root mean square roughness of 0.12 to 3.60 nm (fig. S3), which is favorable for bottom-up structure fabrication.

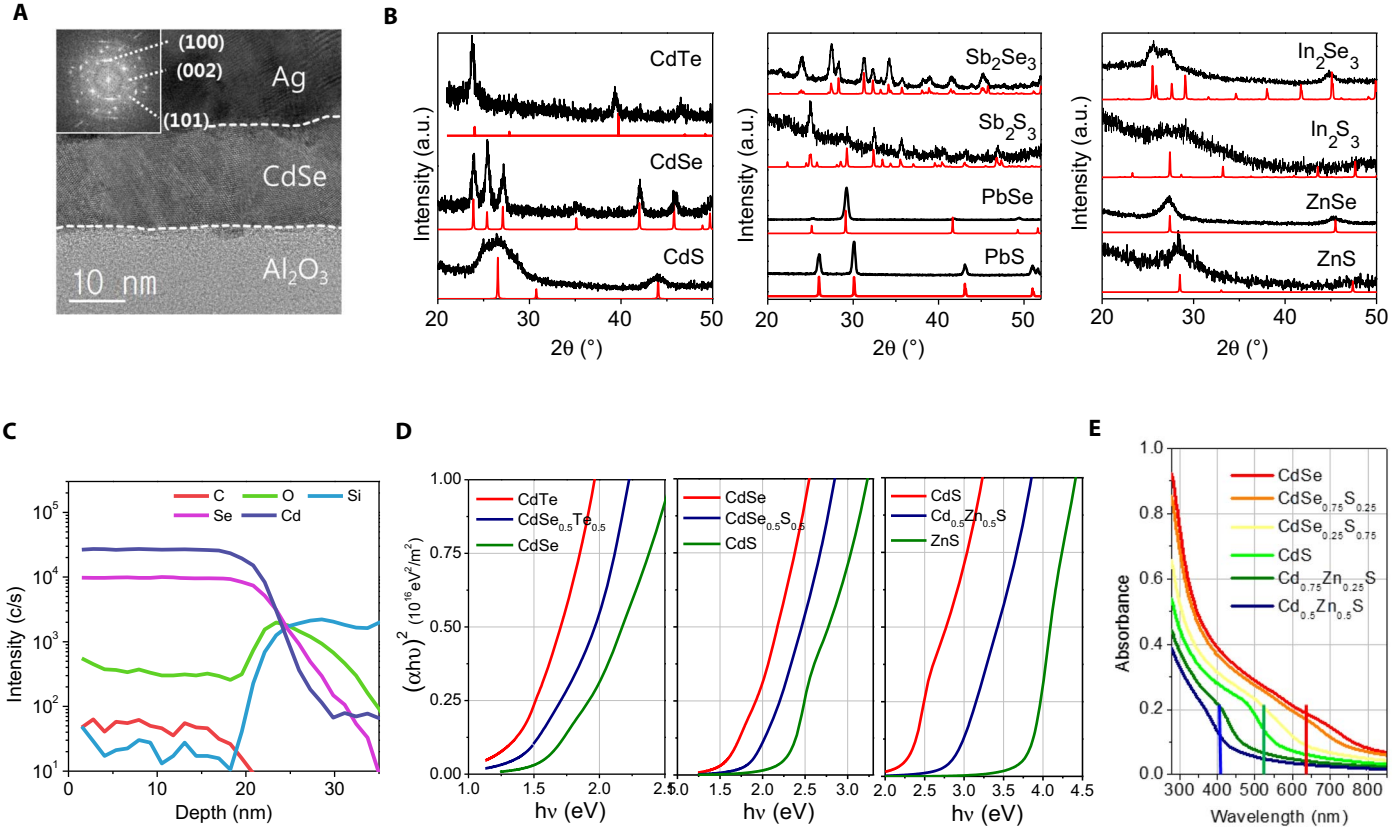


Fig. 2. Characterization of metal-chalcogenide thin films. (**A**) TEM cross-sectional image of a CdSe thin film on an Al_2O_3 gate dielectric (inset: the electron diffraction pattern obtained by FFT). (**B**) Measured (black line) and reference (red line) XRD peaks of metal-chalcogenide thin films: CdS, CdSe, CdTe, Sb_2S_3, Sb_2Se_3, PbS, PbSe, In_2S_3, In_2Se_3, ZnS, and ZnSe. (**C**) Secondary ion mass spectroscopy (SIMS) of a CdSe thin film on Si wafer. (**D**) Tauc plots for $CdSe_mTe_{1-m}$, CdS_mSe_{1-m}, and $Cd_mZn_{1-m}S$ (m = 0, 0.5, and 1, respectively) alloy films fabricated on glass substrates. (**E**) Optical absorbance spectra of CdZnSeS alloy thin films on glass substrates. Indicated R, G, and B color bars show laser source wavelengths of 406 nm (blue), 520 nm (green), and 638 nm (red), respectively.

As shown in field-emission scanning electron microscopy (FE-SEM) images (fig. S4), the metal-chalcogenide thin film is composed of a large number of small-sized grains. Polycrystallinity is further confirmed by electron diffraction patterns, which indicate multiple orientations of fine crystalline structures (fig. S6 and table S3). The electron diffraction pattern was obtained by the fast Fourier transformation (FFT) of the HRTEM image. The diffraction pattern distance values, which are the reciprocal of the *d*-spacings, are 2.69, 2.85, and 3.04 nm^{-1}, respectively (*25*). The calculated *d*-spacing values of 3.711, 3.503, and 3.279 Å correspond well to Miller indices of (100), (002), and (101), respectively, indicating the formation of fully hexagonal CdSe crystals. The grazing incidence x-ray diffraction (GIXRD) analysis also confirms the formation of polycrystalline structures in a large number of metal-chalcogenide thin films (Fig. 2B). The diffraction peaks identify the presence of cubic (CdS, ZnS), hexagonal (CdSe), wurtzite (ZnSe), and other crystal structures. The chemical composition of the CdSe film was investigated by SIMS (Fig. 2C), Rutherford backscattering spectroscopy (RBS), and x-ray photoelectron spectroscopy (XPS) (fig. S7). The chemical composition of the CdSe film obtained from RBS analysis is $Cd_{1.0}Se_{1.0}$, which is well matched to the theoretical value of a CdSe film, $Cd_{1.0}Se_{1.0}$ (*26*, *27*). Furthermore, the RBS spectra in fig. S7 confirm negligible carbon impurities in the chalco-gel–derived CdSe films. Considering the significant variation of relative sensitivity factor (RSF) in SIMS, the small carbon ion signal in the SIMS data roughly indicates relatively low carbon concentrations in the present CdSe thin films of no more than 0.5 atomic %, assuming similar RSF values between Se and C (*28*). Furthermore, surface analysis of the CdSe films by XPS reveals the lack of significant Se3*d* oxidation peaks at 59.2 eV, even after 400°C ambient air annealing treatment (fig. S7).

It can be seen from the present results that the solid solution formation with isostructural metal chalcogenides can be used to achieve finely tunable semiconductor optical properties, as plotted in Fig. 2 (D and E). The thin films of $CdSe_mTe_{1-m}$, CdS_mSe_{1-m}, and $Cd_mZn_{1-m}S$ (m = 0, 0.5, and 1, respectively) alloys were spun and annealed on borosilicate glass substrates at 400°C for 30 min under a nitrogen atmosphere. The absorption and transmission spectra (Fig. 2D and fig. S8) show significant absorption below the fundamental absorption edge. Because film crystallinity has significantly affected the slope of the transmission spectra (*29*, *30*), the films that have a high crystallinity typically show a sharp fall in transmission below the fundamental edge, as shown in fig. S8D. Such behavior in the optical spectra of the polycrystalline films has been reported in a previous report (*31*). A more detailed study of the $(\alpha\hbar\upsilon)^2$ versus E_G plot reveals the band gap of the metal-chalcogenide films. The Tauc plot (Fig. 2D) verifies that the solution-processed metal-chalcogenide alloy films have similar band gaps to the reported band gaps of CdTe, CdSe, CdS, and ZnS, which are 1.5 to 1.6 eV, 1.7 eV, 2.15 to 2.48 eV, and 3.51 to 3.84 eV, respectively (*32*–*35*). In the solid solutions of cadmium and zinc chalcogenides, the chalco-gel–processed metal-chalcogenide alloys demonstrate wide tunability of the band gap from the near-infrared to ultraviolet (UV) regions. The gradual shifts in transmittance onset and the corresponding band gap tunability are readily achieved by manipulating the metal and organochalogen compositions of the precursor solutions (Fig. 2D and fig. S8).

Electrical characterization of the TFTs

To ensure the successful translation of the present chalco-gel–based metal-chalcogenide semiconductors into electronic applications, we fabricated the chalco-gel–processed metal-chalcogenide semiconductor TFTs in ambient air. Figure 3 (A and B) and fig. S9 show the transfer and output characteristics of CdSe TFTs using a thermally grown SiO_2 gate dielectric (thickness of 200 nm) on a heavily doped Si wafer (bottom gate and top contact structure) with a channel length and a channel width of 100 and 1000 μm, respectively. The CdSe TFTs exhibit an n-type behavior with a maximum saturation and linear field-effect mobilities exceeding 300 and 200 $cm^2 V^{-1} s^{-1}$, respectively (average saturation and linear mobility of 206 ± 29 $cm^2 V^{-1} s^{-1}$ and 156 ± 22 $cm^2 V^{-1} s^{-1}$ from 19 different batches of devices), and a current modulation of $>10^7$ with a hysteresis level of 1 to 3 V. Here, the saturation and linear mobilities are characterized at drain biases of 40 and 4 V, respectively, along with a gate bias sweep of −40 to 40 V. Compared to recently reported highly crystalline inorganic semiconductor TFTs (*10*, *36*), we observe relatively lower mobility (50 to 100%) in the linear regime than in the saturation regime, which is possibly due to the smaller thickness of semiconductor films (14 to 18 nm) used in this experiment and their subsequent inherent defects or traps in bulk and grain boundaries, as well as less optimized source/drain contact structures (*37*–*39*). Nevertheless, the electrical characteristics of the present metal-chalcogenide semiconductors suggest that the benign solution-processed metal-chalcogenide TFTs outperform the vacuum-deposited metal-oxide TFTs and are comparable to those of laser-crystallized polycrystalline Si TFTs. We further investigated the relationships between the TFT device performance, the chemistry, and film properties. Specifically, solvent effects on film crystallinity and field-effect mobility were studied with various solvents, such as DMF, DMSO, and NMF. Furthermore, the influence of film thickness on the crystallinity and the field-effect mobility were also studied. Table S4 shows the electrical properties of CdSe TFTs with different solvents. With similar thicknesses of ~20 nm, the DMF-based TFT device has the lowest electron mobility value. The GIXRD results confirm poor crystallinity of the CdSe film grown with DMF (fig. S10). For NMF and DMSO, similar crystallinities are observed (fig. S10). As reported for lead halide perovskite film deposition, the formation of a stable intermediate complex between DMSO and the heavy metal ion may afford better chalco-gel stability and, subsequently, improved film quality (*40*). The importance of film crystallinity control is again clear with the thickness variation experiment. For the solution processing method, the film thickness can be generally controlled by the precursor concentration, deposition parameters (spin rate in spin-coating, bar pitch/coating speed in bar-coating, ambient coating conditions, etc.), and the number of multi-stacked layers. To demonstrate the controllability of thickness in the present chalco-gel route, we fabricated CdSe films with thicknesses in the range of 10 to 180 nm. Furthermore, their electrical properties were analyzed using a TFT structure. Here, the film thickness was controlled by changing the concentration of the CdSe precursor solutions with DMSO as the optimized solvent (0.2, 0.4, 0.8, 1.2, and 1.6 M). As confirmed by GIXRD in fig. S11 and SIMS in fig. S12, the fabricated CdSe films are crystalline, and no significant carbon or oxygen contamination is detected, regardless of the film thickness. Note that fig. S13 shows significant mobility changes with CdSe film thickness. In particular, the 10-nm-thick CdSe film exhibits an extremely low mobility of 0.7 $cm^2 V^{-1} s^{-1}$. With increasing channel thickness, a maximum mobility of 180 $cm^2 V^{-1} s^{-1}$ is obtained at a thickness of ~20 nm (0.4 M), which then gradually decreases. For the 10-nm-thick CdSe film, broad diffraction peaks are observed in the XRD spectra (fig. S11), indicating that the low concentration of precursor solution (0.2 M) yields small grains and possibly a discontinuous CdSe film morphology (fig. S14).

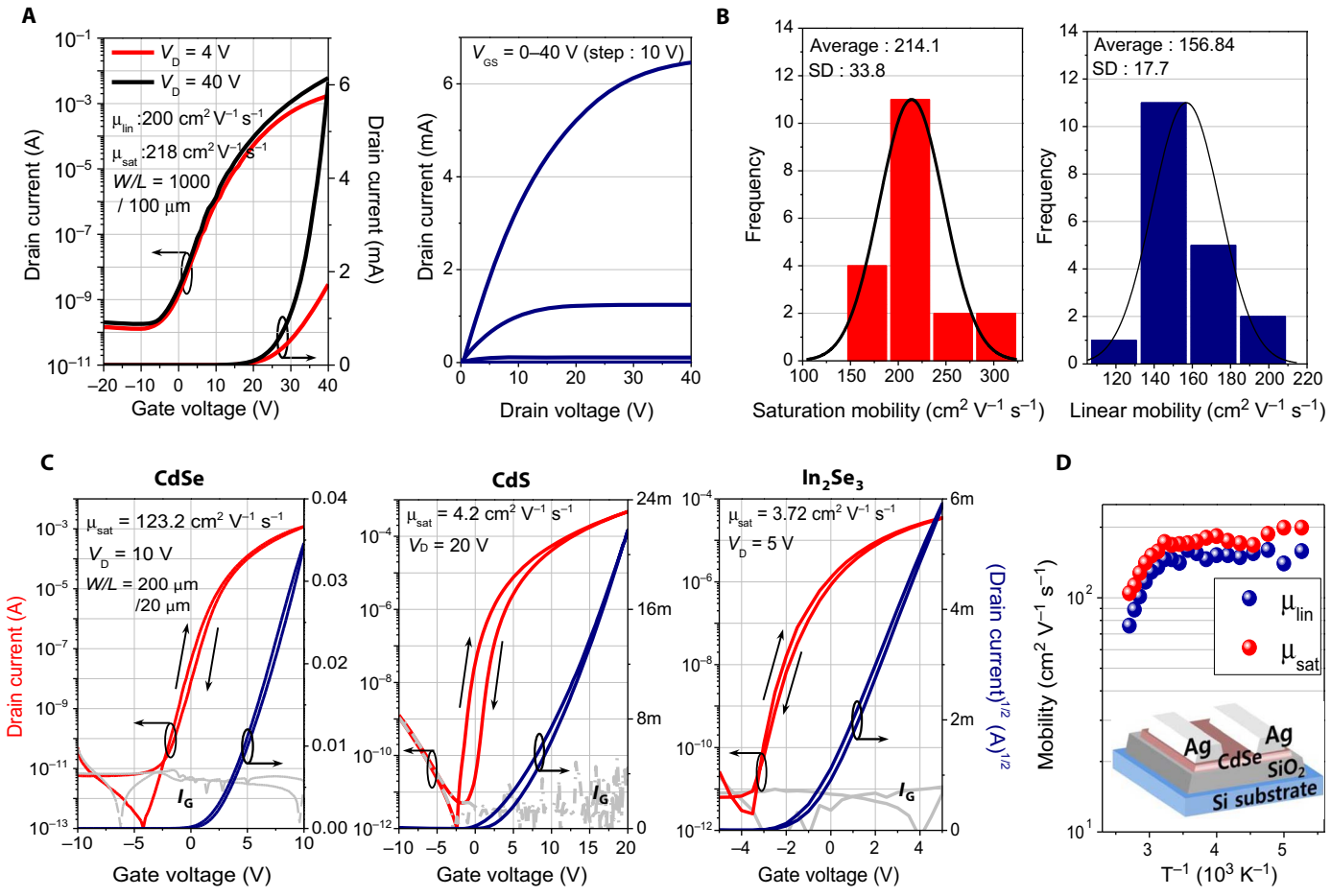


Fig. 3. Electrical characteristics of solution-processed metal-chalcogenide TFTs. Transfer and output characteristics of (**A**) CdSe TFTs using silicon dioxide gate dielectrics (*W*/*L* = 1000 μm/100 μm). (**B**) Saturation and linear mobility statistics of CdSe TFTs on silicon dioxide gate dielectrics. (**C**) CdSe, CdS, and In_2Se_3 TFTs (*W*/*L* = 200 μm/20 μm) using ALD-deposited Al_2O_3 gate dielectrics. (**D**) Temperature dependence of field-effect mobility for an n-channel CdSe TFT device fabricated on a SiO_2 gate dielectric.

With an optimized precursor concentration of 0.4 M, the mobility is substantially increased to 180 cm^2 V^{-1} s^{-1}. When the CdSe films are thicker than the optimum thickness, the mobility gradually decreases. Although similar grain size and crystallinity are observed for the 0.4 to 1.6 M precursor-derived CdSe films by GIXRD (fig. S11) and FE-SEM images (fig. S13), the decreasing mobility trend can be explained by the evolution of a large amount of gaseous species during the annealing process and subsequent formation of microporous structures within the film (*21*, *41*). Furthermore, it was reported that by stacking multiple layers, the formation of films having thicknesses of up to the micrometer scale is possible (*41*).

In realistic device fabrications, gate dielectrics, such as atomic layer–deposited (ALD) dense Al_2O_3 and reliable solution-processed metal-oxide gate dielectrics (Zr-doped Al_2O_3) (*42*), can be combined with conventional wet etching and photolithography for active channel and gate/source/drain electrode formation. Here, ALD and solution-deposited Al_2O_3 gate dielectrics exhibit low leakage current, high breakdown voltage, and stable dielectric properties at high frequencies, while providing uniform semiconductor film formation (fig. S15) (*42*). Various characterizations, such as field-effect mobility, threshold voltage, and subthreshold slope, were carried out in ambient air for the chalcogel–processed metal-chalcogenide TFTs having an inverted-staggered structure (Fig. 3C). The CdSe TFTs using ALD and solution-deposited Al_2O_3 gate dielectrics exhibited maximum saturation field-effect mobilities of >180 cm^2 V^{-1} s^{-1} (average saturation mobility of 125 ± 17 cm^2 V^{-1} s^{-1} from 100 devices), a threshold voltage (V_T) of 0.46 ± 0.98 V, a current modulation of >10^8, a hysteresis level of 0 to 0.5 V, and a subthreshold slope as steep as 0.2 V decade^{-1} (fig. S16). In this case, the field-effect mobility in the linear regime typically reaches 80 to 100% of the saturation mobility. For the versatile transformation of these materials into electronic devices, various metal-chalcogenide thin films, such as indium selenide (In_2Se_3) and cadmium sulfide (CdS), were also used as a channel layer. The In_2Se_3 and CdS films were thermally annealed at 350°C for 30 min under ambient air. The In_2Se_3 TFTs exhibited saturation and linear field-effect mobilities of >4.2 cm^2 V^{-1} s^{-1}, whereas the CdS TFTs exhibited saturation and linear field-effect mobilities of >3.7 cm^2 V^{-1} s^{-1}. For devices with high mobilities, such as >300 cm^2 V^{-1} s^{-1} (Fig. 3B), a simple fabrication procedure was used such as evaporating source and drain electrodes through a shadow mask without patterning the CdSe active layer. In contrast, in the case of low-mobility devices with mobilities of ~100 cm^2 V^{-1} s^{-1} (fig. S16), we used a large-area and controlled device fabrication process to fabricate the CdSe TFTs. During the process, the devices are exposed to various device manufacturing processes such as photolithography, wet etch, and lift-off. Therefore, the CdSe active layer comes into contact with water, acid, and organic compounds originating from the photoresist and the

acetone. These fabrication processes may damage or influence the active layer and the insulating layer, leading to noticeable performance degradation. Therefore, we suspect that the main reason for the rather large mobility variations can be attributed to the fabrication processing accompanying physical damage or influence (Fig. 3B and fig. S16).

In addition, to investigate the charge transport behavior in present metal-chalcogenide semiconductors, we analyzed the temperature-dependent linear and saturation mobility variations in the TFTs. Figure 3D shows the evolution of linear and saturation field-effect mobility as a function of temperature. As shown in this figure, the decreasing mobility with increasing temperature in both linear and saturation regimes can be regarded as "band-like" charge transport, which is often observed in highly crystalline semiconductor materials (*43*). Overall, the small hysteresis, the steep subthreshold slope, and the tendency of the temperature-dependent linear and saturation mobilities in the metal-chalcogenide TFTs imply that well-ordered and less-defective semiconducting materials can be obtained via the present general synthetic route.

To take full advantage of the chalco-gel–processed metal-chalcogenide TFTs, large-area device fabrications were carried out on a 4-inch Si wafer and 2.5-inch borosilicate glass substrates (Fig. 4A). The scalability and device uniformity were verified by measuring a large number of devices distributed over the entire substrate area. Figure 4B shows that most of the TFTs exhibit identical transfer characteristics, showing good uniformity in device performance. However, the TFT in segment 1 shows a rather different electrical behavior and relatively large hysteresis. We speculate that this is due to the nonuniform thickness and the annealing environment at the outer region of the substrate. In each segment, the average areal saturation carrier mobility ranged from 103 to 144 $cm^2 V^{-1} s^{-1}$. For the more realistic application of the present TFT devices, more practical channel length (less than 10 μm) devices were fabricated, and their contact effects were examined. As shown in fig. S18, the saturation mobility was dropped slightly (from 119 to 87 $cm^2 V^{-1} s^{-1}$) along with decreasing channel length (from 50 to 5 μm). The extracted contact resistance and specific contact resistivity between source/drain electrodes and the semiconductor layer in the CdSe TFT devices were around 0.8 kilohm and ~10^{-4} ohm·cm^2, respectively, which are comparable with those of well-made vacuum-deposited metal-oxide TFTs (fig. S18) (*44*, *45*). On the basis of this discussion and experimental

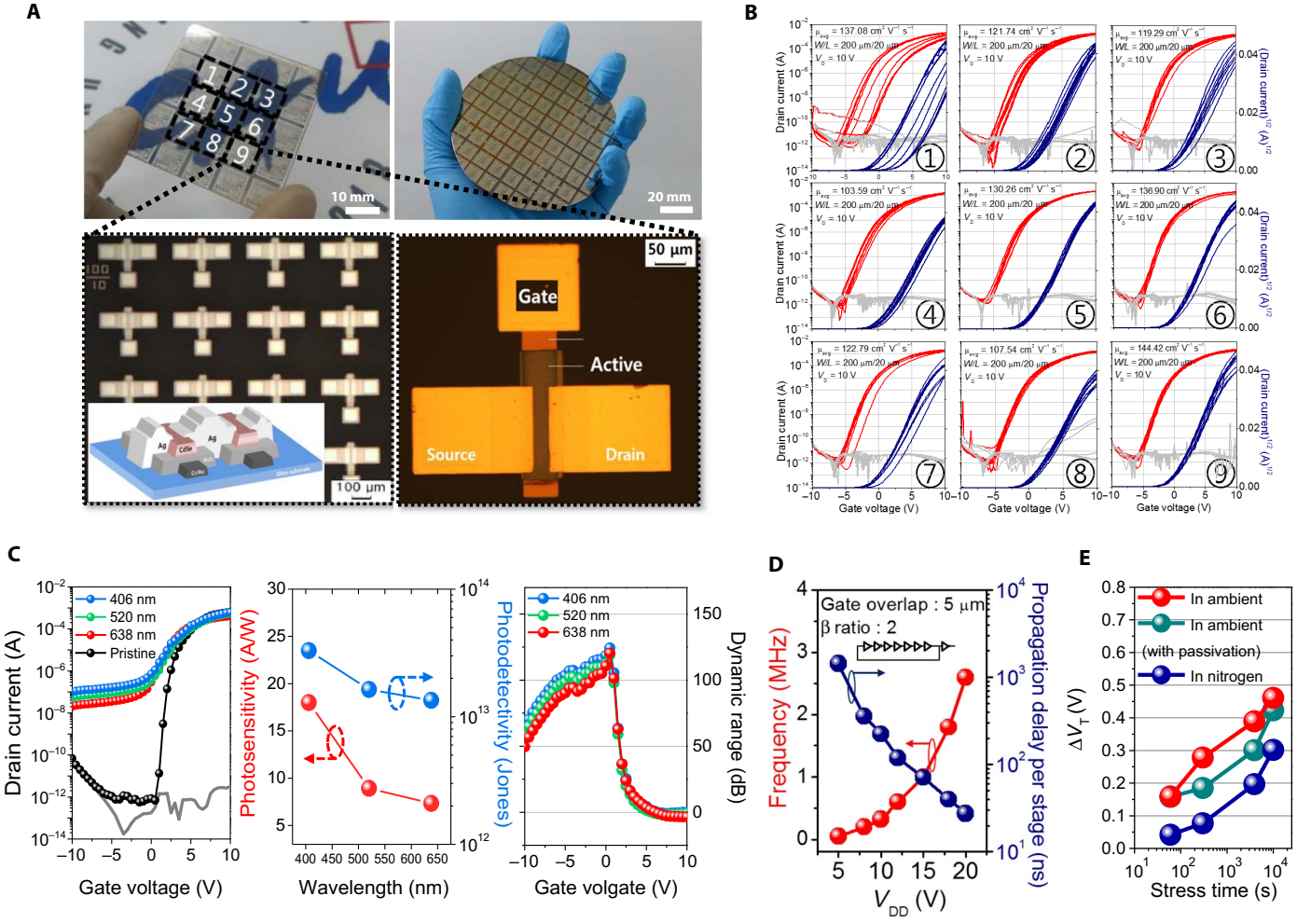


Fig. 4. Large-area solution-processed CdSe TFT arrays on a Si wafer and on glass substrates. (**A**) Photograph, optical microscope images, and schematics of CdSe TFTs fabricated on 2.5-inch glass substrates and a 4-inch Si wafer. (**B**) A series of TFT transfer characteristics on a glass substrate measured at each numbered segment (W/L = 200 μm/20 μm). (**C**) Transfer curves, photosensitivity, and dynamic ranges of CdSe phototransistors under pulsed-laser wavelengths of 406 nm (blue), 520 nm (green), and 638 nm (red). (**D**) Oscillation frequency and propagation delay per stage as a function of supply bias (V_{DD}) for a seven-stage CdSe ring oscillator circuit. (**E**) Threshold voltage shift (ΔV_T) of CdSe TFTs under positive gate bias stress measured in air and N_2 ambient.

findings, we argue that the chalco-gel–processed metal-chalcogenide TFTs can be applicable for more practical channel length devices, offering compatibility with standard CMOS processing and large-area device applications.

Demonstrations for the optoelectronics and integrated circuits

For a further practical demonstration of the synthesized structural design and its integrity in electronic systems, both broad spectral and dynamic range phototransistors and scalable integrated circuits were investigated (Fig. 4, C and D). As previously mentioned, the metal-chalcogenide semiconductors can be implemented in a wide range of optoelectronic applications owing to their inherent tunable band gaps and high light absorption over a broad range of the spectrum. As shown in Fig. 4C, the chalco-gel–processed highly crystalline CdSe phototransistors typically show exceptionally high electron mobilities, large on/off current ratios, and steep subthreshold slopes. The low optical band gap and extremely fast band-like electron transport ability (much faster than the rate of recombination time) (*46*–*48*) in CdSe semiconductors may facilitate the generation of large densities of electron-hole pairs and high photoconductive gain in a wide range of spectrum, enabling substantially increased photocurrents. Figure 4C shows the photocurrent, photodetectivity, and dynamic ranges of these devices as a function of input light wavelength (from a 1-mW laser source), which is consistent with the absorption spectra of the semiconductors (Fig. 2E). With a large gate bias–dependent current modulation (I_{light}/I_{dark}) in the wide spectral ranges, the CdSe phototransistor exhibits an extremely low off-current level (~10^{-13} A) and a steep subthreshold slope in the dark state. Overall, the phototransistor exhibits high photosensitivity (R) values of 7.33 A/W (red, 638 nm), 8.93 A/W (green, 520 nm), and 18.0 A/W (blue, 638 nm); a photodetectivity (D^*) of >10^{13} Jones; and a dynamic range [20 log (I_{light}/I_{dark})] of ~120 dB with minimal noise interference (fig. S19). Compared to conventional consumer-grade CMOS sensors (*49*) and covalent-bonded organic or amorphous oxide semiconductor devices (*50*, *51*), the chalco-gel–derived CdSe phototransistors exhibited an extremely high photodetectivity and a dynamic range over a broad band spectrum (400 to 640 nm) and fast switching properties, which can be translated into high-performance optoelectronic applications. To fully utilize the tunability of the optical properties, phototransistors using other metal-chalcogenide alloys, such as CdS, CdSeS, and CdZnS, were demonstrated, as shown in fig. S20. As expected, a clear wavelength-selective response is observed for CdZnSeS alloys, which confirms the tunability of optical properties of metal chalcogenides from the chalco-gel route. Moreover, to envision the viability of their integrity in high-speed and large-area electronic systems, seven-stage ring oscillator circuits featuring several cascading inverters with a buffer stage were fabricated and measured (fig. S21). With a supply voltage (V_{DD}) of 20 V, an oscillation frequency of >2.6 MHz (theoretically >15 MHz) and a corresponding propagation delay of <27 ns per stage were achieved in the seven-stage circuits (Fig. 4D).

For the present metal-chalcogenide films to emulate currently available high-performance and large-area electronics, long-term operational stability must also be considered. To examine the operational stability of the CdSe TFTs, positive gate bias stress (PBS) tests were performed under air and N_2 ambient conditions with or without an ALD Al_2O_3 passivation layer (Fig. 4E and fig. S22). Even without the passivation layer, the CdSe TFTs exhibit outstanding operational stability with a V_T shift (ΔV_T) of 0.46 V during the 10,000 s of PBS with an electric field of 1 MV cm^{-1}, whereas the passivated devices have only a slightly enhanced stability. Note that the outstanding stability of the devices in ambient air without passivation is nearly comparable to that in N_2 ambient (ΔV_T of 0.3 V). These exceptionally high operational stabilities can be attributed to the highly crystalline metal-chalcogenide structures and low interfacial states at the semiconductor/dielectric interface (*42*, *52*–*54*), which are expected from the CdSe film chemical and structural analysis showing high purity and structural integrity, and the electrical characteristics of the fabricated TFT devices showing low hysteresis and steep subthreshold slopes.

CONCLUSIONS

In summary, high-mobility and scalable metal-chalcogenide semiconductors have been successfully synthesized from solution and integrated in active electronic devices and circuits along with the presentation of a detailed understanding of the underlying mechanism. The present unique organic solvent–based chalco-gel systems offer an attractive option for current semiconductor technologies, enabling high-performance and scalable metal-chalcogenide semiconductors and devices via a simple fabrication process. With the preliminary investigations on nontoxic material–based TFTs, such as In_2Se_3, the chalco-gel route can be further expanded to high-performance large-area electronics with completely nontoxic processing methods and materials. Furthermore, this work establishes significant generality for the synthesis and applications of a variety of polycrystalline metal-chalcogenide thin films featuring a wide range of band gap tunability, high mobility, and outstanding operational stability. At this stage, we have successfully demonstrated high-performance metal-chalcogenide devices and their viability; however, for next-generation electronic applications, such as flexible and wearable electronics, low-temperature processing strategy remains as a challenge along with lower thermal budget chalco-gel precursor design.

MATERIALS AND METHODS

Solution preparation and characterization

To prepare the metal-chalcogenide solutions, commercially available reagents for metal, sulfur, and selenium sources were used without further purification. As a tellurium source, the *N*,*N*-dimethyl benzenecarbotelluroamide was synthesized using the reported procedure (*55*). For CdQ (Q = S, Se, Te) solutions, 0.4 M cadmium acetate dihydrate [$Cd(CH_3COO)_2{\cdot}2H_2O$, Aldrich] or cadmium chloride ($CdCl_2$, Aldrich) was dissolved in DMSO [$(CH_3)_2SO$, anhydrous, Aldrich]. After dissolving the metal precursor in the solvent, 0.8 M acetylacetone ($CH_3COCH_2COCH_3$, Aldrich) was added into the solution. After 15 min of stirring, 0.4 M thiourea (NH_2CSNH_2, Aldrich), selenourea (NH_2CSeNH_2, Alfa Aesar), or *N*,*N*-dimethyl benzenecarbotelluroamide ($C_9H_{11}NTe$, synthesized) was dissolved in the solution. For indium selenide (In_2Se_3), indium acetate [$In(C_2H_3O_2)_3$, Aldrich] was used as an indium source. After dissolving 0.2 M indium acetate in the solution, 0.3 M acetylacetone was added and stirred at 85°C for 15 min, and then 0.3 M selenourea was added. Other metal-chalcogenide systems are also fully illustrated in table S1. The "chalco-gel" precursor solutions with thiourea or selenourea were prepared under ambient air. Selenourea could be handled under ambient air with limited stability and should be stored under inert atmosphere for long-term storage. The telluroamide-based precursor solution should be prepared under inert nitrogen atmosphere.

For Zr-doped Al_2O_3 (ZAO) gate dielectrics, a precursor solution having 0.04 M zirconium(IV) acetylacetonate [$Zr(C_5H_7O_2)_4$, Aldrich] and 0.76 M aluminum nitrate nonahydrate [$Al(NO_3)_3{\cdot}9H_2O$, Aldrich] in 2-ME [($CH_3OCH_2CH_2OH$), Aldrich] was prepared. A mild stirring for 12 hours at 75°C was then carried out (*42*). For Al_2O_3 gate dielectrics, a precursor solution containing 0.8 M aluminum nitrate nonahydrate in 2-ME was prepared.

TGA was performed using the SCINCO TGA N-1000 system. The TGA was conducted in a flowing Ar atmosphere and at 10°C min^{-1}. To prepare the TGA sample, the metal-chalcogenide solution was dried under vacuum with mild heating (T_{drying} = 40°C). Approximately 15 to 20 mg of the vacuum-dried precursor solution was used for the measurements at temperatures ranging from room temperature to 400°C.

Film characterization

For the film characterization, the chalco-gel-route metal-chalcogenide precursor was spun-coated on substrates to grow films with thicknesses of 10 to 50 nm, and these were prebaked at 50°C for 1 min with subsequent annealing at 400°C (or 350°C) for 30 min in nitrogen or ambient air. HRTEM images were obtained by FEI Titan 80-300, and the samples were prepared by Ar^+ ion milling (Model 1010, Fischione Instruments) after mechanical polishing. Diffraction patterns were obtained by FFT of the DM program (Digital Micrograph, Gatan). AFM analysis was carried out using an XE-120 system with Al-coated noncontact tips. XRD was performed using the Dmax2500/PC x-ray diffractometer (Cu $K\alpha_1$, λ = 1.5406 Å). The reference data were retrieved from the inorganic crystal structure database. Thin-film transmittances were obtained by the LABMDA 35 UV/VIS spectrophotometer. SIMS analysis was carried out using the IMS 4FE7 (Cameca) with a Cs^+ ion gun of 5.5 kV. The RBS measurements were performed with He^+ particles delivered by a 450-keV vertical accelerator (HRBS V500, KOBELCO), and an XPS analysis was carried out using the K-Alpha + (Thermo Fisher Scientific), with an Al Kα source at 1486.6 eV and a base pressure of 7.83×10^{-9} mbar. FE-SEM images were obtained by using the SIGMA (Carl Zeiss).

TFT fabrication and electrical measurements

For a simple metal-chalcogenide TFT implementation, prime grade Si wafers (0.01 to 0.02 ohm·cm, QL Electronics Co. Ltd) were used as both the gate electrode and the substrate. Thermally grown SiO_2 with a thickness of 200 nm was used for the gate dielectric. The chalco-gel-route metal-chalcogenide solution was spun over the gate dielectric with a thickness of 14 to 18 nm and was prebaked at 50°C for 1 min with subsequent annealing at 400°C for 30 min in ambient air. Ag source/drain electrodes with a thickness of 100 nm were deposited through a shadow mask using the thermal evaporator, forming a channel width and a channel length of 1000 and 100 μm, respectively.

For the fabrication of scalable metal-chalcogenide TFTs on glass substrates, 0.7-mm-thick glass substrates (Eagle 2000, Samsung Corning Precision Glass) were used. For the gate electrode, a thermally evaporated Cr/Au (5 nm/45 nm) layer was patterned by standard photolithography processes and wet etching. On the gate electrode, a 160-nm-thick ZAO gate dielectric layer was formed by spin-coating at 3000 rpm for 20 s and subsequent annealing at 400°C for 1 hour. A 56-nm-thick ALD Al_2O_3 layer deposited at 250°C was also used as a gate dielectric. Before channel deposition, an oxygen plasma treatment (100 W, 5 min) was performed for the gate dielectric to achieve high surface energy and good wettability of the precursor solutions. For the channel layer, metal-chalcogenide films were formed by spin-coating the precursor solutions at 3000 rpm for 25 s. Subsequently, the films were prebaked at 50°C for 1 min and annealed at 400°C for 30 min in ambient air. After that, the channel layer and via holes were patterned using photolithography process. Finally, 100-nm-thick Ag source/drain electrodes were deposited by thermal evaporation and patterned by the lift-off process. For In_2Se_3 TFTs, 80-nm-thick Al source/drain electrodes were used. For a photolithography process, photoresist (AZ GXR-601, AZ Electronic Materials) was deposited onto the substrate by spin-coating at 3000 rpm for 20 s and subsequent baking at 90°C for 2 min. Then, the photoresist layer was covered with chrome mask and was exposed to 432-nm UV light irradiations for 1.5 s. The UV-exposed photoresist was removed by immersing it in a photoresist developer (DPD-200 developer) for 20 s and was subsequently rinsed by distilled water. Finally, the gate, the via holes, and the active layer were patterned by wet etching. In particular, a 20-nm CdSe layer was etched by immersing the substrate in a chrome etchant {$HClO_4/(NH_4)_2[Ce(NO_3)_6]/H_2O$ = 10.9%:4.25%:84.85%} for 25 s. The Cr layer was etched by immersing it in the same chrome etchant for a few minutes. The oxide dielectric layer was etched by immersing it in buffered hydrofluoric acid for 60 to 120 s. After the wet etch process, the remaining photoresist was removed by immersing and rinsing it with acetone. The gate leakage current analysis and the characterization of TFTs were conducted using a probe station and the Agilent 4156C precision semiconductor parameter analyzer. Further, the capacitance of the gate dielectric was measured using the Agilent 4284A precision LCR meter. The linear/saturation field-effect mobility (μ_{lin}/μ_{sat}) and subthreshold swing (SS) of TFTs were calculated using the following equations, respectively

$$\mu_{lin} = \frac{L}{WC_iV_{DS}}\left(\frac{\partial I_{DS}}{\partial V_G}\right) \quad (3)$$

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial \sqrt{I_{DS}}}{\partial V_G}\right)^2 \quad (4)$$

$$SS = \frac{\partial V_G}{\partial(\log I_{DS})} \quad (5)$$

For the operational stability tests, a constant positive gate bias (V_{GS} = +5 V) and a source/drain bias (V_{DS} = +0.1 V) were applied to the device for a preset time. During the bias stress tests, transfer characteristics were measured and recorded by sweeping the gate voltage from −10 to +10 V (0.2 V voltage step) while holding the V_{DS} at +10 V. As a passivation layer, an 80-nm-thick ALD Al_2O_3 was deposited at 150 layer deposition cycle steps.

Photoresponse and integrated circuit measurements

The photoresponse characteristics of CdSe TFT devices were carried out using the Agilent 4156C (Agilent Co.) in ambient air and at room temperature. For the light source, a laser source with a wavelength centered at 406 nm (blue), 520 nm (green), and 638 nm (red) (Thorlabs Inc.) was used (*51*). Samples were illuminated with a light intensity of 1 mW/cm^2. The noise power spectral densities (S_{ID}) were measured in the dark using the SR 570 low-noise current preamplifier (Stanford Research Systems) and the HP 89441A vector signal analyzer (Hewlett Packard Co.) with frequencies of 10 Hz to 1 kHz. (fig. S19). The photosensitivity

(R) and the photodetectivity (D^*) were calculated from the following equations

$$R = I_{ph}/P \quad (6)$$

$$D^* = (A\Delta f)^{1/2}/\mathrm{NEP} \quad (7)$$

where I_{ph} is the photocurrent ($I_{ph} = I_{light} - I_{dark}$), P is the incident optical power, A is the illuminated area [channel width (W) × channel length (L)], Δf is the spectral bandwidth (set to 1 in the measurement system for this work), and NEP is the noise equivalent power [NEP = $(\langle I_n^2 \rangle)^{1/2}/R$]. To evaluate D^*, a root mean square dark noise current of $(\langle I_n^2 \rangle)^{1/2}$ from the noise power spectral density was measured, and R is extracted from the photoresponse transfer characteristics of CdSe TFT devices. Here, we confirmed the relationship between R and the absorbance. R with the wavelength of the light is well matched with the absorbance spectrum of the CdSe film.

For the dynamic photoresponse characteristic measurements, the gate (Cr/Au) and source/drain (Ag) electrodes were biased using the Agilent 4156C with 0 and 10 V, respectively, and the pulsed-laser source illumination was controlled by the LabVIEW program. Initially, the phototransistor was placed in the dark and then the 406-nm, 520-nm, and 638-nm wavelengths of the laser source were turned on and off repeatedly at a frequency of 0.5 Hz. The light intensity of the laser source was 1 mW/cm^2. The active area (A) was defined with a width of 200 μm and a length of 20 μm.

For the ring oscillator fabrication, the inverter in the ring oscillator on a glass substrate includes a β ratio of 2 with a $(W/L)_{drive}$ of 100 μm/5 μm and a $(W/L)_{load}$ of 50 μm/5 μm, and a gate-to-source/drain electrode overlap distance of 5 μm, while demonstrating a fully logical operation (fig. S21). For the ring oscillators, a digital storage oscilloscope (TDS2012B, Tektronix) was used to measure the oscillation frequency. All of the measurements were carried out in the dark under ambient air. The AIMSPICE (www.aimspice.com) modeling parameters were extracted from the measured TFT characteristics in fig. S16B.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/4/4/eaap9104/DC1

fig. S1. ^{1}H NMR for coordination of acetylacetone on a cadmium precursor.
fig. S2. The photograph of vacuum-dried DMSO-based CdS and CdSe precursor solutions.
fig. S3. Metal-chalcogenide surface images were obtained by AFM.
fig. S4. Metal-chalcogenide surface images were obtained by FE-SEM.
fig. S5. Metal-chalcogenide surface images were obtained by an optical microscope.
fig. S6. Cross-sectional HRTEM image and diffraction pattern of the CdSe TFT.
fig. S7. RBS and XPS analysis of the CdSe films.
fig. S8. Transmittance of the metal-chalcogenide alloy films.
fig. S9. Characterization of the CdSe TFTs on the SiO_2 substrate.
fig. S10. Grazing incident XRD peaks of 20-nm-thick CdSe films made with different types of solvent.
fig. S11. XRD peaks of the CdSe layer with precursor concentrations.
fig. S12. SIMS data of the CdSe layer with precursor concentrations.
fig. S13. Electrical mobility properties of the CdSe TFTs with precursor concentrations.
fig. S14. FE-SEM image of the CdSe films.
fig. S15. Characterization of the gate dielectric layer.
fig. S16. Characterization of the CdSe TFTs on Al_2O_3 dielectric.
fig. S17. Temperature dependence of field-effect mobility for an n-channel CdSe TFTs.
fig. S18. Electrical characteristics of the CdSe TFTs with different channel lengths (5, 10, 20, and 50 μm).
fig. S19. Characterization of the CdSe phototransistor.
fig. S20. Characterization of the $Cd_{1-x}Zn_xSe_{1-y}S_y$ phototransistors.
fig. S21. Characterization of the CdSe circuits.
fig. S22. Positive bias stress test of the CdSe TFTs.
table S1. Solution stability relation of the metal-chalcogenide precursor with the complexing agent.
table S2. Synthetic information of the metal-chalcogenide solutions.
table S3. Diffraction pattern distance, d-spacing, and Miller indices of the CdSe thin film.
table S4. Average saturation mobility of CdSe TFTs with different types of solvent.
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