Capacitive pressure sensor with wafer-through silicon vias using SOI-Si direct wafer bonding and glass reflow technique

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Abstract: A micromachined capacitive pressure sensor with a single crystal silicon membrane and wafer-through silicon via electrodes embedded in the glass substrate is demonstrated. SOI (silicon-on-insulator)-Si direct wafer bonding and reflow technique of the bonded glass wafer are combined to fabricate the pressure sensor. The proposed process enables to access the sensing capacitor easily from the backside of the substrate without bondwires on the front, and helps to achieve uniform sensor performances thanks to the uniform thickness of the SOI device layer. The fabricated sensors show an initial capacitance of $7.68 \pm 0.39\,\mathrm{pF}$ with an averaged sensitivity of $1.29 \pm 0.06\,\mathrm{fF}$ from 0 to 360 Torr.

Keywords: capacitive pressure sensor, wafer-through silicon vias, direct wafer bonding, glass reflow technique
Classification: Micro- or nano-electromechanical systems

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1 Introduction

MEMS (Micro Electro Mechanical Systems) capacitive pressure sensors have been used for a variety of applications such as biotechnology, automotive or control systems thanks to their high sensitivity, low power, low noise, large dynamic range and especially little temperature dependence compared to the piezoresistive sensors [1, 2, 3, 4]. In most micromachined capacitive sensors, the sensing membrane and the bottom electrode constituting a sealed-cavity sensing capacitor are formed and led to the external circuitry usually on the front of the sensor by conventional wirebonding technology. However, in some special biomedical applications – for example, pressure sensors in oriental medicine for monitoring human pulse from the patients' wrist [5] – a specific sensor structure without bondwires on the front is required since the sensing membrane is directly in touch with human skin. Packaging of the whole sensor structure with soft resin could be one possible way to protect the bondwires, but it decreases the sensitivity of the sensor and cannot completely prevent physical damages on the bondwires during the repeated operations.

In this letter, a novel capacitive MEMS pressure sensor structure that does not require bondwires on the front of the sensor is demonstrated. Electrical access to the sensing capacitor is made from the backside of the substrate through the conductive wafer-through silicon via structures embedded in the glass substrate fabricated by glass reflow process [6, 7]. Pressure sensor with the doubly-doped p++ sensing diaphragm anodically bonded to a glass-in-silicon wafer fabricated by glass reflow process was reported [8]. In our approach, direct bonding technique of a SOI wafer to a silicon substrate wafer is used to form the single-crystal silicon sensing membrane capacitor. This process provides better performance uniformity thanks to the uniform thickness of the SOI device layer, and is free from the stress problem that might exist in the p++ diaphragm. Details of the sensor structure, fabrication process and performances of the fabricated sensors are described.

2 Pressure sensor structure

The schematic view of the proposed capacitive pressure sensor is shown in Fig. 1. The sensor structure is composed of the silicon circular sensing membrane, oxide insulating layer, and glass substrate with embedded wafer-through silicon vias.

The sealed cavity for a capacitance sensing gap is formed by direct bonding of a SOI wafer with a silicon wafer on which the separating oxide layer is patterned. The device layer of the SOI wafer is used to make the sensing membrane electrode which is deflected by the externally applied pressure. Wafer-through silicon vias are formed by reflowing of the glass wafer anodically bonded to the deep reactive ion etched silicon substrate. The larger via under the membrane is used for the bottom electrode as itself, and another via is electrically connected to the sensing membrane by a patterned metal layer.

The pressure sensor is designed to be operating at a full range from 0 to 360 Torr by the finite element software, COMSOL^{TM}. The dimensions of the designed sensor are shown in Table I. The initial capacitance gap is

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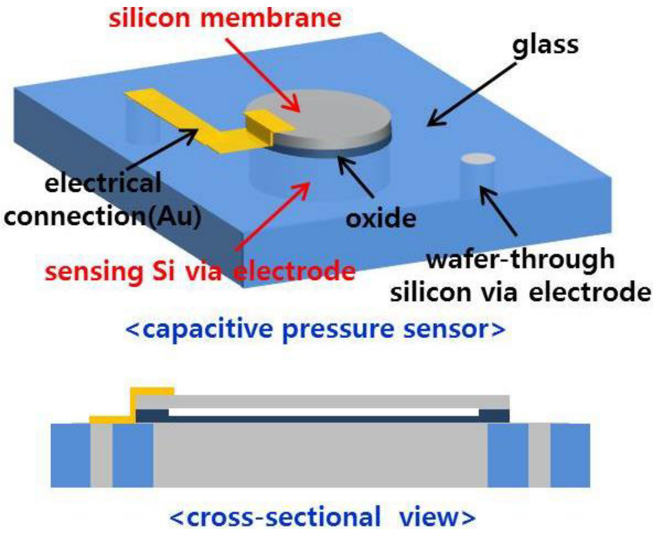

Fig. 1. Schematic view of the proposed capacitive pressure sensor

Table I. Dimensions of the designed pressure sensor

Parameters	Dimensions
Membrane thickness	14 µm
Membrane radius	626 µm
Sensing oxide gap	2 µm
Bottom sensing Si via radius	626 µm
Through-wafer Si via radius	175 µm
Si via height	380 µm

2 μm, and the membrane is designed to deflect by about 0.7 μm at a maximum applied pressure of 360 Torr.

3 Fabrication process

The overall fabrication process of the sensor is illustrated in Fig. 2. A 4-inch, 500-μm-thick (100) p-type low-resistive ($\rho = 0.01 \sim 0.02\,\Omega\cdot\mathrm{cm}$) silicon wafer is thermally oxidized to grow a 2-μm-thick oxide layer. The oxide layer is patterned by BOE (buffered oxide etch) solution to define the capacitance sensing gap. A 0.1-μm-thick oxide layer is deposited onto the etched surface to prevent possible electrical short of the membrane to the bottom electrode when deflected by the applied pressure. This wafer is then directly bonded to an SOI wafer which has a low-resistive, 14-μm-thick device layer. The two wafers are dipped in RCA1 solution for surface activation, washed by DI water and brought into contract manually at room temperature and atmospheric pressure for initial bonding. The wafer is then annealed in the tube furnace at a temperature of 1000℃ to improve the bonding strength.

Wafer-through silicon via structures are formed by deep reactive ion etching (DRIE) from the backside of the silicon substrate wafer using an aluminium layer as an etch mask. A 4-inch borosilicate glass wafer is then anodically bonded to the etched surface under the vacuum environment. After that, the whole wafer stack is heated up to 800℃ in the tube furnace and kept for 8 hours. During this procedure, the melted glass reflows and fills up the trench around the silicon vias due to the low vacuum pressure in

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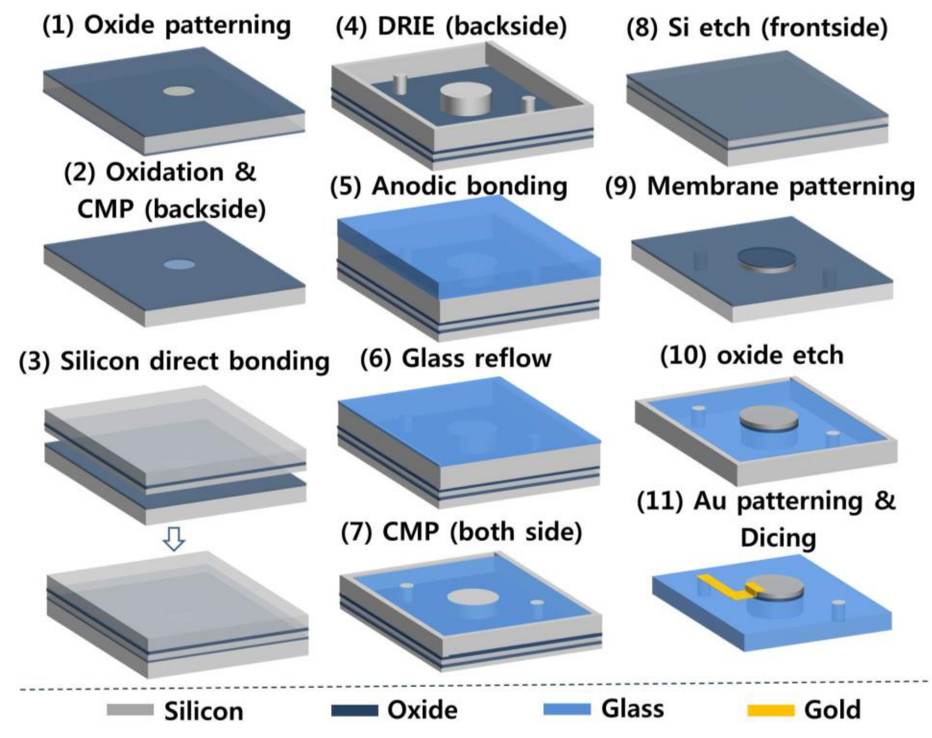

Fig. 2. Fabrication process of the pressure sensor

the sealed trench. The reflowed glass over the trench and silicon substrate are lapped and polished together down to the desired thickness of 380 μm. The wafer-through silicon via structures embedded in the glass part are exposed during this process.

The handling silicon substrate of the SOI wafer is removed by KOH etching, and the circular sensing membrane is defined by DRIE of the SOI device layer using the remaining BOX oxide layer as an etch mask. After removing the oxide etch mask, a Cr/Au layer is finally sputtered and patterned to electrically connect the sensing membrane with the wafer-through silicon via.

The photograph of the fabricated pressure sensor is shown in Fig. 3(a). The total device size is $4.0 \times 4.7\,\text{mm}^2$. The cross-sectional SEM image of the fabricated sensor is shown in Fig. 3(b). The silicon via is tapered by about 10° due to the non-ideal property of the DRIE machine we used. This effect

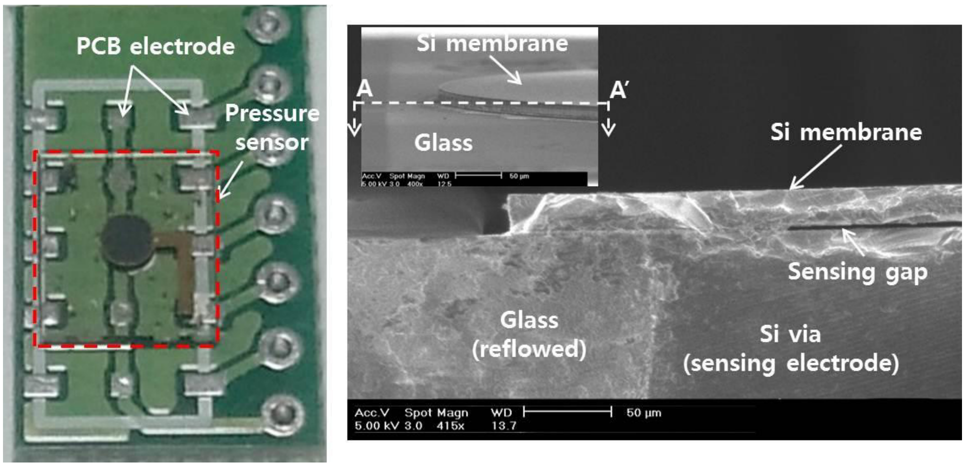

Fig. 3. (a) Photograph of the fabricated pressure sensor.
(b) Cross-sectional SEM image of the sensor

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is reconsidered in the simulation since it affects the initial capacitance value.

4 Experimental results

The fabricated pressure sensor is diced and mounted on the PCB board using a conductive silver epoxy as an adhesive, with the exposed backside silicon vias precisely aligned to the electrodes on the PCB, as shown in Fig. 3(a). The capacitance change of the sensor according to the applied pressure is measured with a capacitance-to-digital converter (CDC) chip (AD7147, Analog Devices) in the air-pressure chamber at room temperature. The real-time response of the sensor is monitored by the LABVIEW$^{\mathrm{TM}}$ program.

The measured capacitance changes of the fabricated sensors according to the applied pressure are shown in Fig. 4. The initial static capacitance of the sensors is measured to be 7.68 ± 0.39 pF, which is very close to the simulation result of 7.76 pF. The measured total capacitance change in the full range up to 360 Torr is 466 ± 21 fF, and the averaged sensitivity of the sensor is approximately 1.29 ± 0.06 fF/Torr. The fabricated five sensor samples that are chosen randomly show relatively uniform capacitance changes according to the applied pressure. The uniform device layer thickness of the commercially-available SOI wafer helps to improve the performance uniformity of the fabricated sensors.

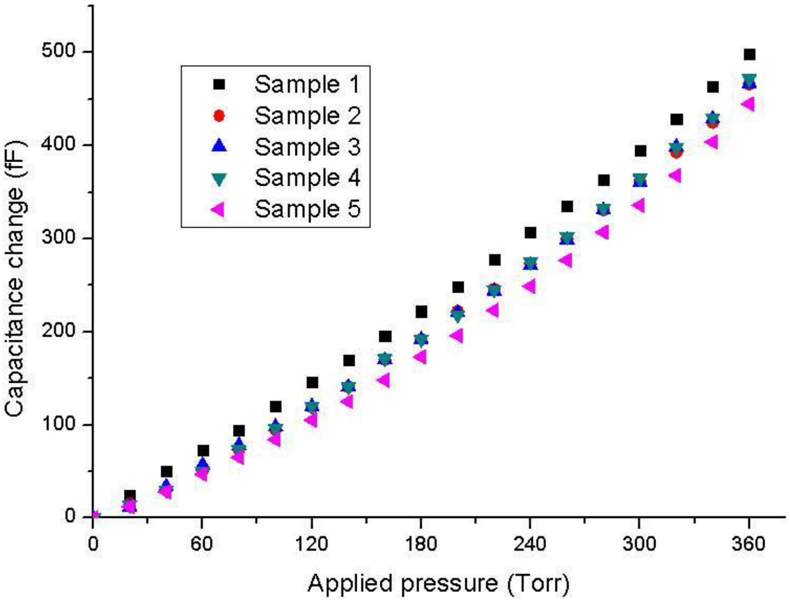

Fig. 4. Measured capacitance changes of the fabricated five pressure sensors according to the applied pressure

5 Conclusions

A capacitive pressure sensor with conductive through-wafer silicon vias is successfully demonstrated using the SOI-silicon direct wafer bonding and glass reflow process. Complete electrical access to the sensing capacitor is possible from the backside of the sensor through the silicon vias embedded

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in the glass substrate. Since the sensor structure does not require bondwires on the front, it will be a good platform for the specific biomedical application where the direct mechanical loading of the sensor membrane is difficult. For a practical usage of the sensor in the oriental medicine field, electrical shielding of the noise from a human body should be considered and it is currently being under way.

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