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A Highly Efficient Single-Phase Three-Level Neutral Point Clamped (NPC) Converter Based on Predictive Control with Reduced Number of Commutations

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Abstract: This paper proposes a highly efficient single-phase three-level neutral point clamped (NPC) converter operated by a model predictive control (MPC) method with reduced commutations of switches. The proposed method only allows switching states with none or a single commutation at the next step as candidates for future switching states for the MPC method. Because the proposed method preselects switching states with reduced commutations when selecting an optimal state at a future step, the proposed method can reduce the number of switchings and the corresponding switching losses. Although the proposed method slightly increases the peak-to-peak variations of the two dc capacitor voltages, the developed method does not deteriorate the input current quality and input power factor despite the reduced number of switching numbers and losses. Thus, the proposed method can reduce the number of switching losses and lead to high efficiency, in comparison with the conventional MPC method.

Keywords: model predictive control; single-phase three-level NPC converter; commutation

1. Introduction

Recently, multilevel converters have become popular in a variety of high-power systems owing to their low voltage stress, improved waveform qualities, and low electromagnetic interference (EMI) compared to two-level converters [1,2]. Among several kinds of multilevel converters, three-level neutral point clamped (NPC) converters with relatively simple configurations have been realized for many application areas. In addition to three-phase NPC converters, single-phase three-level NPC converters have been employed for high-speed traction systems as well. In order to control single-phase three-level NPC converters, traditional carrier-based pulse width modulation (CBPWM) methods combined with linear proportional and integral (PI) controllers have been investigated to synthesize ac sinusoidal current waveforms with three-level NPC converters. Aside from their adjustable ac voltage and current synthesis, the NPC converters require balancing of the two dc capacitor voltages because of their structure, which has two split dc capacitors in the dc link. As a result, CBPWM methods with offset voltage injection to remove imbalance of neutral point (NP) voltage in the NPC converters have been often used [3–7].

Recently, model predictive control (MPC) methods have been studied for numerous power converters including three-level NPC converters [8–10]. There have been several studies on MPC algorithms for single-phase NPC converters as well as three-phase NPC converters [11–13]. In the MPC methods for single-phase NPC converters, a cost function to determine an optimal switching state generally consists of two terms combined with a weighting factor not only to control both the ac sinusoidal currents but also to balance the two capacitor voltages. The ac sinusoidal current is

controlled by changing the converter voltage levels, whereas the NP voltage balance is adjusted by using redundant switching states that yield the same voltage level.

The conventional MPC method selects an optimal switching state among nine switching states allowed by the single-phase three-level NPC converter on the basis of a cost function considering the ac source current and the NP voltage balance. Consideration of all possible switching states in the conventional method can choose a switching state involved in many commutations as an optimal switching state for the next step, which can lead to an increased number of switchings and corresponding switching losses [14–18]. In addition, the conventional MPC method changes the optimal switching state by evaluating the capacitor voltage balance term using the redundant switching states to equal the two capacitor voltages [19,20] owing to a slight voltage difference even when the converter does not require a change in the voltage level. Thus, this operation can increase the number of switchings and switching losses as well [21,22]. Several trials to reduce switching losses based on the model predictive control methods have been addressed for a variety of power converters in literatures. In [23,24], approaches to reduce switching losses of matrix converters have been addressed. Ref. [23] proposed a switching loss reduction technique by adding an additional term related with a number of future commutations to a cost function used to control the matrix converter. In [24], a trial to decrease switching losses of the matrix converter has been presented, where a cost function includes an extra term directly representing switching losses at next step by calculating switch currents and switch voltages. In [25], a model predictive control method for modular multilevel converters (MMCs) has been developed with a cost function which is aimed at the elimination of the MMC circulating currents, regulating the arm voltages, and controlling the ac-side currents. In addition, this strategy tried to reduce power losses by decreasing the submodule switching frequency. In [26,27], reduction techniques of switching losses for two-level voltage source inverters have been presented. Ref. [26] proposed a switching strategy based on the model predictive control method to clamp one phase with the largest load current among the three legs in the voltage source inverter every sampling period, which can successfully reduce switching losses of the voltage source inverter. In addition, a model predictive control method for the voltage source inverter has been developed to reduce switching losses by injecting future zero-sequence voltage [27]. This approach decreased the switching losses by implementing optimal discontinuous pulse patterns to stop switching operations at vicinity of peak values of load currents. However, there has not been, to the authors' best knowledge, tried to reduce switching losses, using a trade-off between switching losses and capacitor voltage balancing in the three-level NPC converters, although several trials to reduce switching losses based on the model predictive control methods have been addressed for a variety of power converters.

In this paper, a highly efficient algorithm with a reduced number of switching and low switching losses for single-phase three-level neutral point clamped (NPC) converters is proposed based on a model predictive control (MPC) method with a decreased number of commutations of switches. The proposed method pre-excludes, from the candidates for possible future switching states, the switching states that yield more than two commutations in the next sampling period. As a result, the proposed technique can reduce the number of switchings and switching losses by utilizing switching states involving no commutation or only one commutation during every sampling instant for single-phase three-level NPC converters. In addition, the developed method does not deteriorate the input current quality or input power factor despite the reduced switching numbers and losses. Although the proposed method slightly increases the peak-to-peak variations of the two dc capacitor voltages at the expense of reduced commutation, the increased voltage variation is not high. Thus, the proposed method can obtain high efficiency and low switching losses at the expense of a slightly increased peak-to-peak variation of the NP voltage. The performance of the proposed method with a reduced number of switchings and higher efficiency is evaluated in terms of the total harmonic distortion (THD) and peak-to-peak variations of the capacitor voltages. Simulations and experimental results are presented to verify the effectiveness of the proposed method.

2. Single-Phase Three-Level NPC Converter and Model Predictive Control Method

Figure 1 shows a circuit diagram for the single-phase three-level NPC converter. As shown in Figure 1, the single-phase three-level NPC converter has an input inductor L_s and resistor R_s as an ac side filter, as well as two capacitors C_1 and C_2 at the dc side. In addition, v_{c1} and v_{c2} are the dc voltage of each capacitor, and R_L is a load resistor. Switches S_{aj} and S_{bj} (j = 1, 2, 3, 4) are Insulated Gate Bipolar Transistors (IGBTs) at the a-phase and b-phase, respectively. The switch states at each phase, produced by the converter, can be defined as a function of the switching status of the two upper devices as:

$$S_x = \begin{cases} 1 & (S_{x1}, S_{x2} : ON) \\ 0 & (S_{x2}, S_{x3} : ON) \\ -1 & (S_{x3}, S_{x4} : ON) \end{cases} \quad (x = a \text{ or } b) \tag{1}$$

The two switches S_{x1} and S_{x3} operate complementarily. Similarly, S_{x2} and S_{x4} work in a complementary manner. As a result, the switching status of the two lower devices is automatically determined by the upper switches. Owing to possible combinations of the switching states of (1) in the a and b phases, a total of nine operating states can be generated by the single-phase three-level NPC converter. On the basis of nine operating states, the phase switching state, upper device switching status, and converter input voltage v_{ab} are listed in Table 1. The nine operating states yield five voltage levels for the converter input voltage v_{ab}, which provides the single-phase NPC converter with redundancy.

As shown in Table 1, the two states (1, 0) and (0, −1) for (S_a, S_b) are redundant switching states that apply the same voltage level to the converter input terminal of the single-phase three-level NPC converter by assuming that the two capacitor voltages are well balanced. Likewise, the states (0, 1) and (−1, 0) for (S_a, S_b) are also redundant because they yield the equal converter input voltage v_{ab}. These redundancies can be utilized to balance the two capacitor voltages v_{c1} and v_{c2}. The currents i_u and i_l shown in Figure 1 can be expressed using the switching status and the source current i_s as in (2) and (3). Thus, they can be obtained without additional measurements [16]:

$$i_u = \frac{S_a(S_a+1) - S_b(S_b+1)}{2} i_s \tag{2}$$

$$i_l = -\frac{S_a(S_a-1) - S_b(S_b-1)}{2} i_s \tag{3}$$

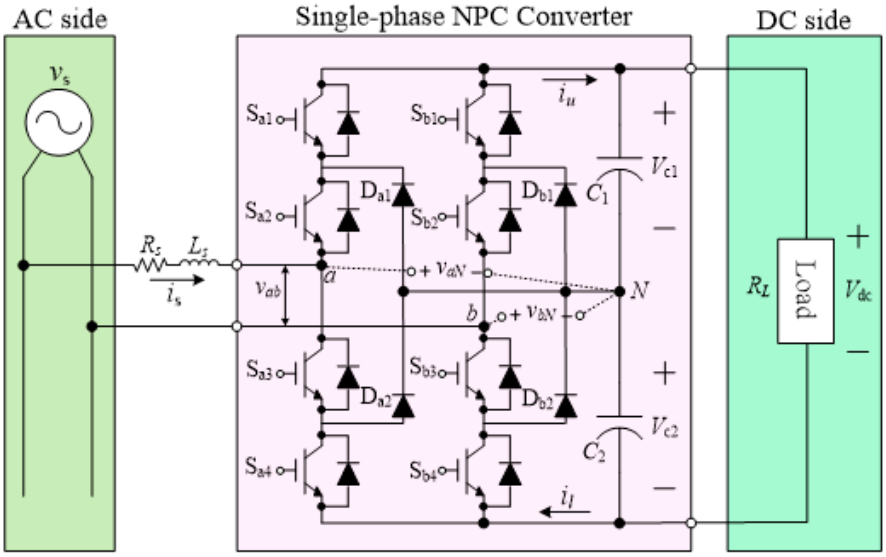


Figure 1. Single-phase three-level NPC converter.

Table 1. Nine operating states, phase switching state, upper device switching status, and converter input voltage of single-phase three-level NPC converter.

#	Operating Status		Phase Switching State				Converter input Voltage	Capacitor Voltage	
	S_a	S_b	S_{a1}	S_{a2}	S_{b1}	S_{b2}	v_{ab}	v_{c1}	v_{c2}
1	0	0	OFF	ON	OFF	ON	0	-	-
2	1	1	ON	ON	ON	ON	0	-	-
3	−1	−1	OFF	OFF	OFF	OFF	0	-	-
4	1	−1	ON	ON	OFF	OFF	V_{dc}	↑	↑
5	1	0	ON	ON	OFF	ON	$V_{dc}/2$	↑	↓
6	0	−1	OFF	ON	OFF	OFF	$V_{dc}/2$	↓	↑
7	0	1	OFF	ON	ON	ON	$-V_{dc}/2$	↑	↓
8	−1	0	OFF	OFF	OFF	ON	$-V_{dc}/2$	↓	↑
9	−1	1	OFF	OFF	ON	ON	$-V_{dc}$	↓	↓

The capacitor voltage dynamics of the dc link are calculated by using differential equations:

$$\frac{dv_{c1}}{dt} = \frac{1}{C_1} i_u \tag{4}$$

$$\frac{dv_{c2}}{dt} = \frac{1}{C_2} i_l \tag{5}$$

Using a constant sampling period T_s, the capacitor voltage dynamics in the discrete-time domain are described as:

$$\frac{dv_{cm}}{dt} \approx \frac{v_{cm}(k+1) - v_{cm}(k)}{T_s} \quad (m = 1,\ 2) \tag{6}$$

Using (6), Equations (4) and (5) can be expressed in the discrete time domain as:

$$v_{c1}(k+1) = v_{c1}(k) + \frac{T_s}{C_1}\left(\frac{S_a(S_a+1) - S_b(S_b+1)}{2}\right) i_s \tag{7}$$

$$v_{c2}(k+1) = v_{c2}(k) - \frac{T_s}{C_2}\left(\frac{S_a(S_a-1) - S_b(S_b-1)}{2}\right) i_s \tag{8}$$

The input current of the ac side shown in Figure 1 is expressed in the continuous time domain as:

$$v_s = R i_s + L\frac{di_s}{dt} + v_{ab} \tag{9}$$

Equation (9) is expressed in the discrete time domain as:

$$i_s(k+1) = \left(1 - \frac{RT_s}{L}\right) i_s(k) + \frac{T_s}{L}(v_s(k) - v_{ab}(k)) \tag{10}$$

The ac source current at the next step, $i_s(k+1)$, in (10) can have five possible movements owing to the five possible voltage levels for $v_{ab}(k)$. The single-phase three-level NPC converter needs to balance the two capacitor voltages by manipulating the phase switching states $S_a(k)$ and $S_b(k)$ shown in (7) and (8) as well as control the source current by changing the converter input voltage $v_{ab}(k)$ in (10). As a result, the cost function with two terms for the ac source current control part and the neutral point (NP) voltage control part of the two capacitor voltages is:

$$g = |i_s^*(k+1) - i_s(k+1)| + \lambda_c |v_{c1}(k+1) - v_{c2}(k+1)| \tag{11}$$

where λ_c represents the weighting factor of the capacitor voltage balancing term in the cost function. Moreover, the future ac reference current can be expressed with past and present currents from a Lagrange extrapolation as [28–31]:

$$i_s^*(k+1) = 3i_s^*(k) - 3i_s^*(k-1) + i_s^*(k-2) \quad (12)$$

where $i_s^*(k)$ is the present current, and $i_s^*(k-1)$ and $i_s^*(k-2)$ are the reference value of the one-step and two-step past ac source currents, respectively. The ac sinusoidal current is controlled by changing the converter voltage levels, whereas the NP voltage balance is adjusted by using redundant switching states that yield the same voltage level. As a result, the conventional MPC method changes the optimal switching state by evaluating the capacitor voltage balance term using the redundant switching states to equal the two capacitor voltages owing to a slight voltage difference even when the converter does not require a change in the voltage level. Thus, this operation can increase the number of switchings and the switching losses as well.

3. Proposed MPC Method Based on Voltage Tolerance Band

The conventional MPC method selects an optimal switching state among nine switching states allowed by the single-phase three-level NPC converter on the basis of a cost function considering the source current and the NP voltage balance. Consideration of all possible switching states in the conventional method can help to choose a switching state involved in many commutations as an optimal switching state for the next step. In addition, the conventional MPC method changes the optimal switching state by evaluating the capacitor voltage balance term using the redundant switching states to equal the two capacitor voltages owing to a slight voltage difference even when the converter does not require a change in the voltage level. Table 2 illustrates the number of commutations involved in switch transitions from the current step to the next step, which vary from zero to four.

Table 2. Number of commutations involved in switch transitions from current step to next step in conventional MPC method.

Current Operating Status		**Next Possible Operating Status**								
(S_a,S_b)	(0,0)	(0,0)	(0,1)	(1,0)	(−1,0)	(0,−1)	(1,−1)	(−1,1)	(1,1)	(−1,−1)
number of commutations		0	1	1	1	1	2	2	2	2
(S_a,S_b)	(1.1)	(1,1)	(1,0)	(0,1)	(−1,1)	(0,0)	(1,−1)	(0,−1)	(−1,0)	(−1,−1)
number of commutations		0	1	1	2	2	2	3	3	4
(S_a,S_b)	(−1.−1)	(−1,−1)	(−1,0)	(0,−1)	(−1,1)	(0,0)	(1,−1)	(0,1)	(1,0)	(1,1)
number of commutations		0	1	1	2	2	2	3	3	4
(S_a,S_b)	(1.−1)	(1,−1)	(0,−1)	(1,0)	(−1,−1)	(0,0)	(1,1)	(−1,0)	(0,1)	(−1,1)
number of commutations		0	1	1	2	2	2	3	3	4
(S_a,S_b)	(1.0)	(1,0)	(1,1)	(1,−1)	(0,0)	(0,1)	(0,−1)	(−1,0)	(−1,1)	(−1,−1)
number of commutations		0	1	1	1	2	2	2	3	3
(S_a,S_b)	(0.−1)	(0,−1)	(1,−1)	(−1,−1)	(0,0)	(0,1)	(1,0)	(−1,0)	(−1,1)	(1,1)
number of commutations		0	1	1	1	2	2	2	3	3
(S_a,S_b)	(0.1)	(0,1)	(1,1)	(−1,1)	(0,0)	(0,−1)	(1,0)	(−1,0)	(1,−1)	(−1,−1)
number of commutations		0	1	1	1	2	2	2	3	3
(S_a,S_b)	(−1.0)	(−1,0)	(−1,1)	(−1,−1)	(0,0)	(0,1)	(0,−1)	(1,0)	(1,−1)	(1,1)
number of commutations		0	1	1	1	2	2	2	3	3
(S_a,S_b)	(−1.1)	(−1,1)	(0,1)	(−1,0)	(−1,−1)	(0,0)	(1,1)	(1,0)	(0,−1)	(1,−1)
number of commutations		0	1	1	2	2	2	3	3	4

A switching operation with a number of commutations equal to that shown in Table 2, for example, implies that one switch turns off and another switch turns on at a switching instant. Likewise, two switches are off and two are on at a switching moment when the switching operation corresponds to a number of commutations equal to two in Table 2. The conventional method, which selects a next-step switching state depending on the cost function, does not consider the number of commutations.

Thus, the number of switchings can increases in a case where an optimal switching state with many commutations is chosen at the next step. Figure 2 shows simulation waveforms obtained by the conventional MPC method for a single-phase three-level NPC converter.

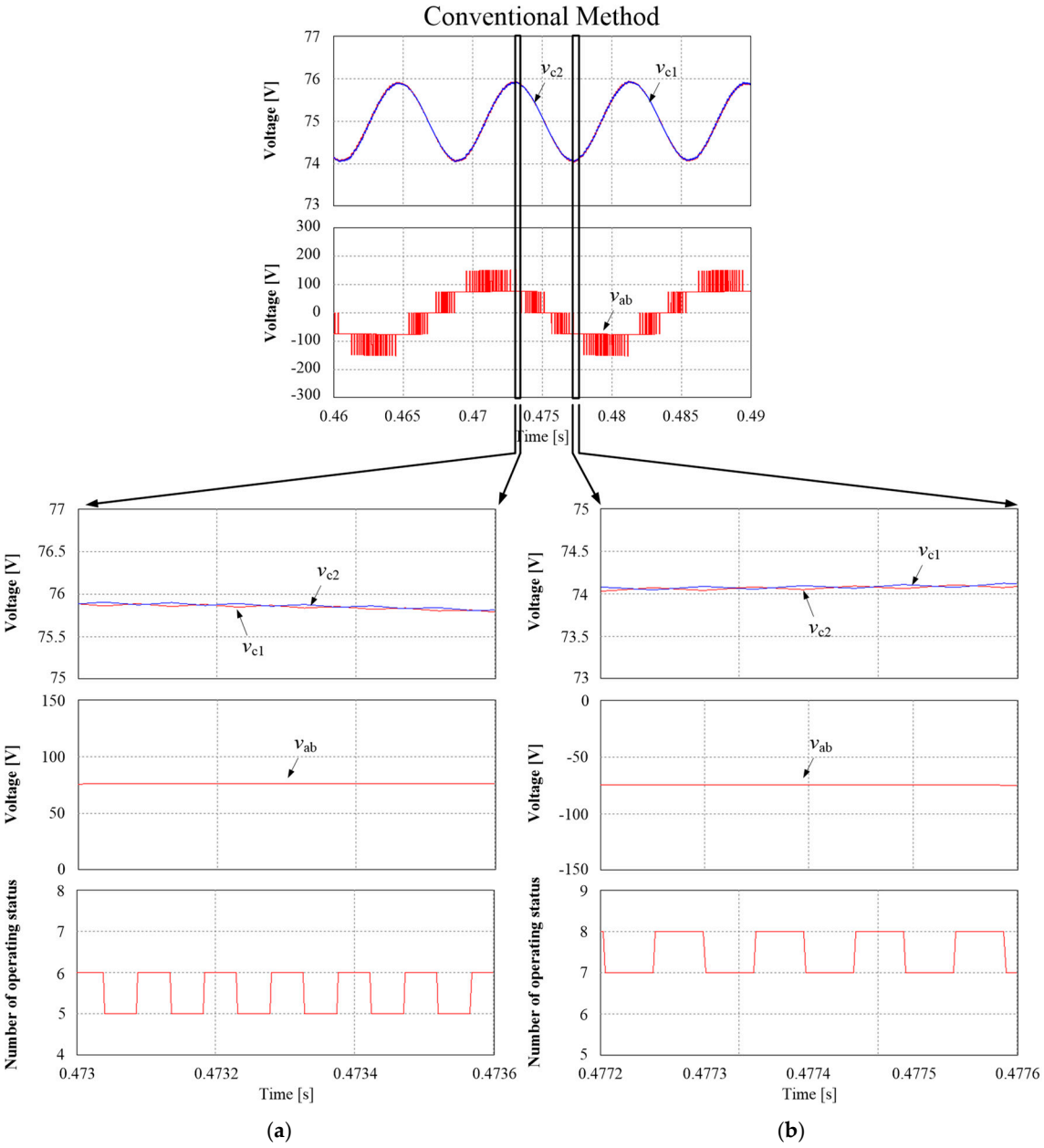


Figure 2. Simulation waveforms of conventional MPC method (**a**) during period with converter voltage v_{ab} fixed to $V_{dc}/2$ and (**b**) during period with converter input voltage v_{ab} fixed to $-V_{dc}/2$.

It is seen from Figure 2a that the conventional method, during the period with the converter voltage v_{ab} fixed to $V_{dc}/2$, repeatedly changes the switching states corresponding to an operating status between (1, 0) and (0, −1). This is the redundant state with respect to each other, although the switch transitions do not be required in terms of the ac source current control. These switching operations involve two commutations at every switching instant, as shown in Table 2. As a result, the number of switching operations substantially increases, whereas the two capacitor voltages perfectly match. Similarly, the simulation waveforms obtained by the conventional MPC method, especially during the period with the converter input voltage v_{ab} fixed to $-V_{dc}/2$, are depicted in Figure 2b. It is seen

that the switch transition repeatedly occurs between (0, 1) and (−1, 0) in terms of the operating status, which also involves two commutations at every switching instant, as shown in Table 2. Therefore, it is noted that the two capacitor voltages are tightly balanced by repeatedly using the redundant switching states, at the expense of an increased number of switchings in the conventional MPC method. The proposed method pre-excludes, from the candidates for possible future switching states, the switching states that yield more than two commutations in the next sampling period. As a result, the proposed technique can reduce the number of switchings and the switching losses by utilizing switching states involving no commutation or only one commutation at every sampling instant for single-phase three-level NPC converters. Table 3 shows the switching states allowed in the proposed method, which are states with the number of commutations restricted to zero or one

Table 3. Switching states allowed in proposed method.

Current Operating Status	Next Possible Operating Status
(0,0)	(0,0) (0,1) (1,0) (−1,0) (0,−1)
(1,1)	(1,1) (1,0) (0,1)
(−1,−1)	(−1,−1) (−1,0) (0,−1)
(1,−1)	(1,−1) (0,−1) (1,0)
(1,0)	(1,0) (1,1) (1,−1) (0,0)
(0,−1)	(0,−1) (1,−1) (−1,−1) (0,0)
(0,1)	(0,1) (1,1) (−1,1) (0,0)
(−1,0)	(−1,0) (−1,1) (−1,−1) (0,0)
(−1,1)	(−1,1) (0,1) (−1,0)

Figure 3 shows simulation waveforms obtained by the proposed MPC method for a single-phase three-level NPC converter. It is seen from Figure 3a that the proposed method, during the period with the converter voltage v_{ab} fixed to $V_{dc}/2$, does not change the switching states. This is because the operating status (0, −1) corresponding to the redundant status of (1, 0) is not a possible state for the next state when the current operating status is (0, −1). Similarly, simulation waveforms obtained by the proposed MPC method, especially during the period with the converter input voltage v_{ab} fixed to $-V_{dc}/2$, are depicted in Figure 3b. It is also seen that there is no switch transition because the operating status (−1, 0) corresponding to the redundant status of (0, 1) is not a possible state for the next state when the current operating status is (−1, 0). As a result, the proposed method can reduce the number of switchings and the corresponding switching losses, whereas an NP voltage imbalance between the two capacitor voltages occurs. The NP voltage imbalance that occurs when the periods of the converter voltage are fixed at $V_{dc}/2$ or $-V_{dc}/2$ is resolved by selecting switching states to eliminate the imbalance afterward. Figure 4 depicts simulation waveforms obtained by the proposed MPC method during the period when the converter voltage v_{ab} oscillates between $V_{dc}/2$ and V_{dc}. It is seen that the NP voltage imbalance is solved by the proposed algorithm, where the optimal states are 5, 4, 6, 4, 5, and so on, as shown in Figure 4. Figure 5 shows the capacitor voltage behavior in the switching states. Because switching states 4, 5, and 6 can increase or decrease the upper and lower capacitor voltages, the proposed method can successfully eliminate the NP voltage imbalance quickly.

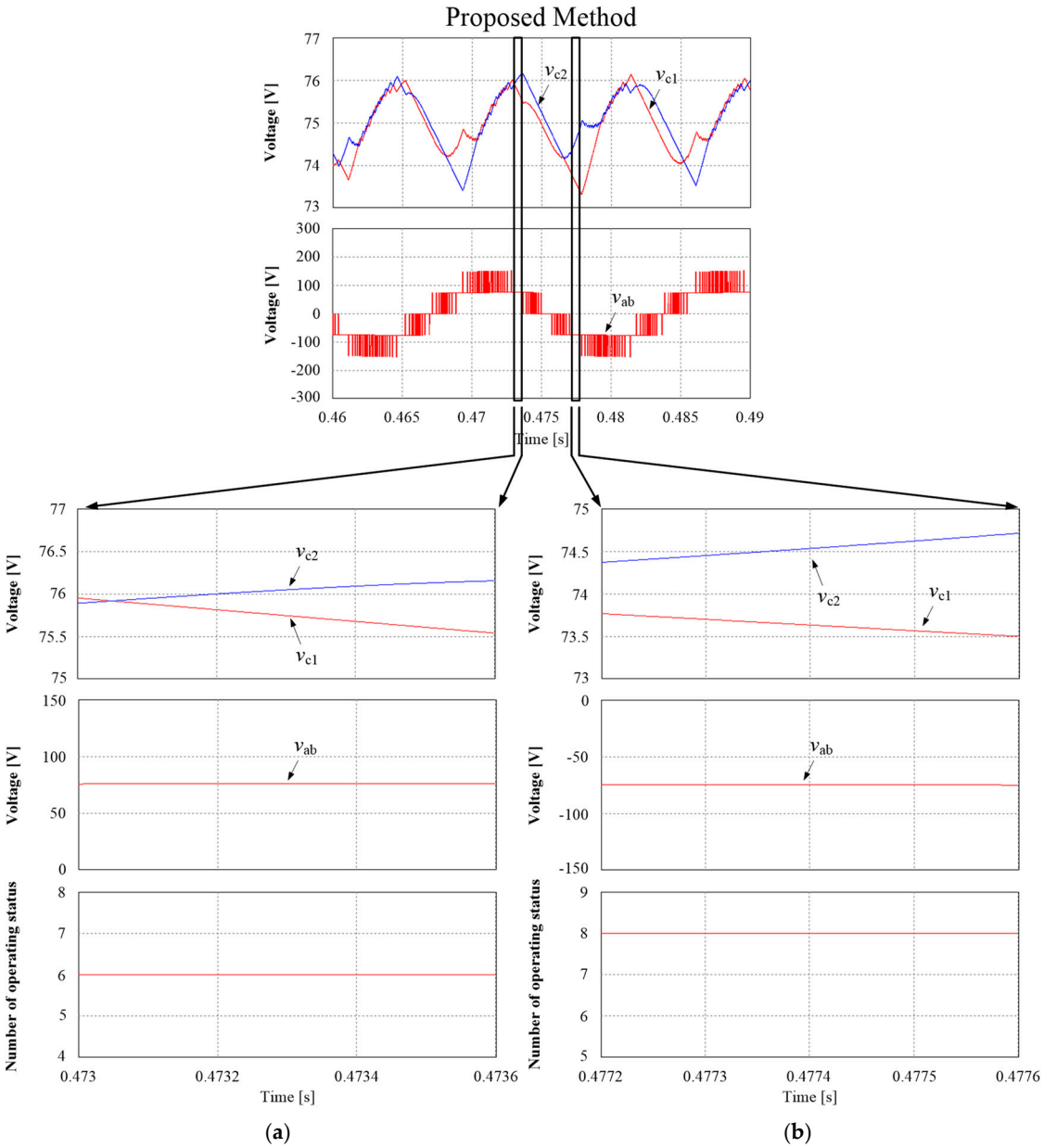


Figure 3. Simulation waveforms of proposed MPC method (**a**) during period with converter voltage v_{ab} fixed to $V_{dc}/2$ and (**b**) during period with converter input voltage v_{ab} fixed to $-V_{dc}/2$.

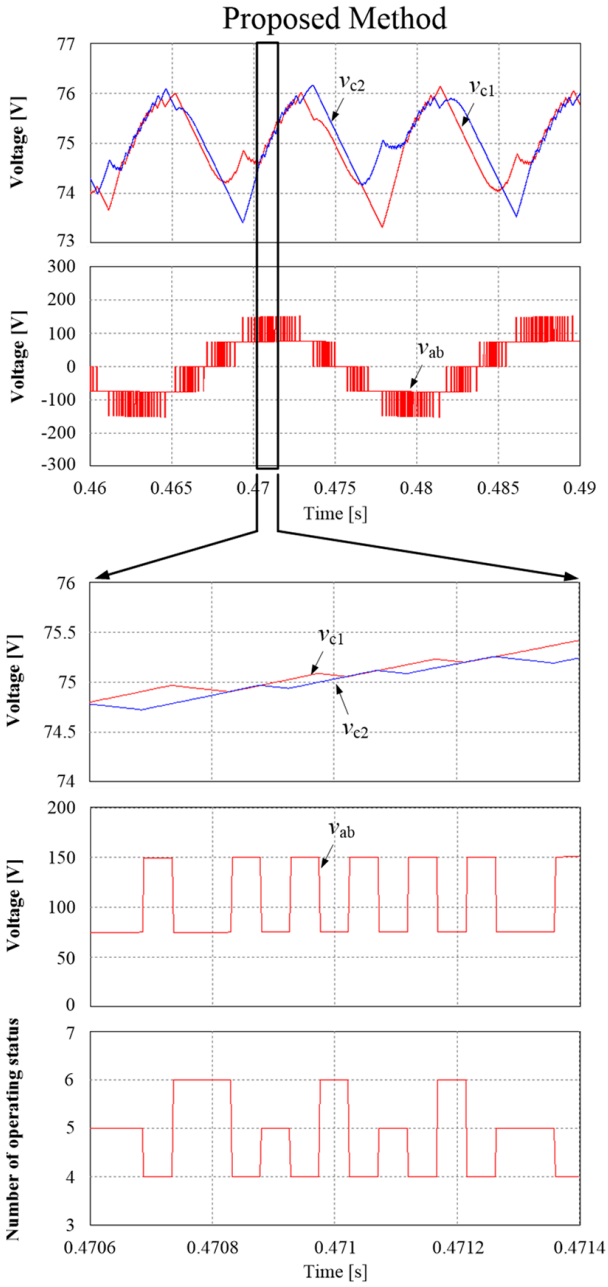


Figure 4. Simulation waveforms of proposed MPC method during period with converter voltage v_{ab} between $V_{dc}/2$ and V_{dc}.

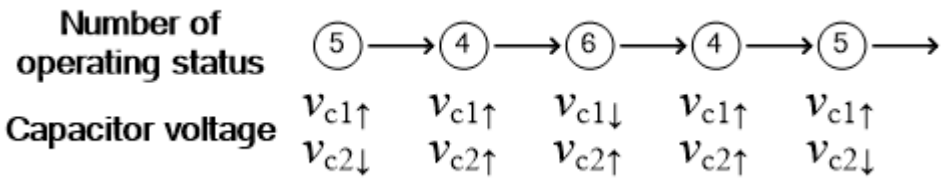


Figure 5. Number of operating status and capacitor voltage behavior of proposed MPC method during period with converter voltage v_{ab} between $V_{dc}/2$ and V_{dc}.

The performance of the MPC methods owing to its inherent operational principle is strongly influenced by the sampling frequency. The number of switchings by the conventional MPC and proposed methods as functions of the sampling periods are shown in Figure 6. It is seen that the

number of switchings of the proposed method is lower than that of the conventional MPC method for all considered sampling periods. Increasing the sampling frequency increases the number of switchings, leading to an increasing difference in the number of switchings obtained from the two methods. The conventional MPC and the proposed methods are compared in terms of the THDs of the source current and the peak-to-peak capacitor voltages vs. the sampling periods shown in Figure 6. It is observed that the proposed method results in almost the same THDs in the source current as those in the conventional MPC method. In addition, the peak-to-peak capacitor voltages of the proposed method are slightly higher than those of the conventional method, at the expense of a decreased number of switchings. Thus, it can be concluded that compared to the conventional MPC method, the proposed method can lead to a reduced number of switchings, which can lead to lower switching losses and a nearly equal THD of the source currents.

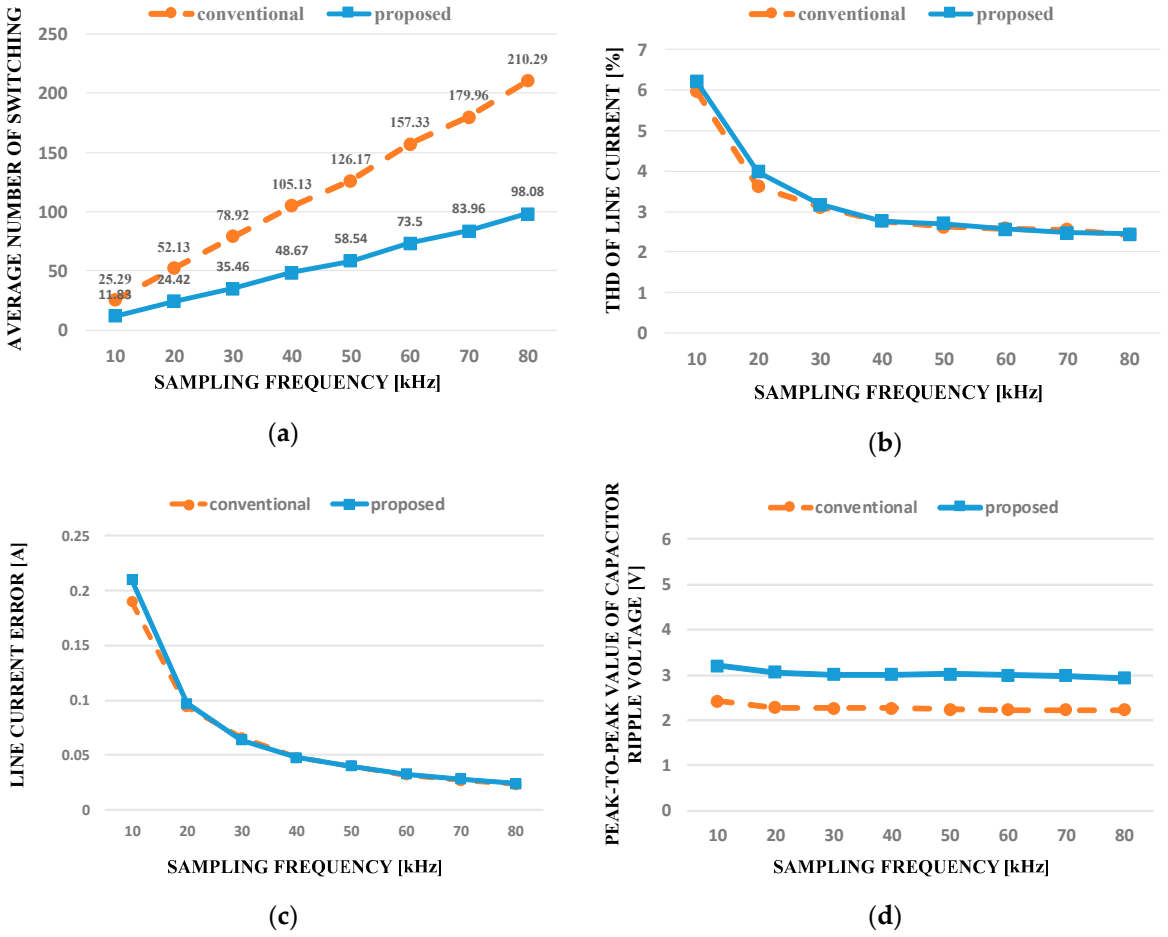


Figure 6. Comparison results obtained by conventional MPC method and proposed method vs. sampling frequency: (**a**) number of switchings; (**b**) THD values of source currents; (**c**) current errors; and (**d**) peak-to-peak values of capacitor ripple voltages.

Loss analysis and stress distribution among the switching devices were further conducted on conditions with v_s = 730 V, V_{dc} = 1000 V, and P_{in} = 10 kW. Losses resulted in each switching component by the conventional and the proposed methods are depicted in Figure 7. The proposed method yields reduced losses in all the switching component, including the IGBTs and the clamping diodes, in comparison with the conventional method. By comparing the conduction loss and the switching loss in Figure 7, the conduction losses generated by the two methods are almost the same. On the other hand, the switching losses of the proposed method are lower than those of the conventional method for all the components. Total efficiency of the conventional and the proposed method was 98% and

98. 7%, respectively. Regarding loss distribution shown in Figure 7, the two methods lead to more losses in the inner switches, S_{a2} and S_{b2}, than the outer switches, which is general in the three-level NPC converters. However, it is seen that the losses by the proposed method are less concentrated on the inner switches than the conventional method, as shown in Figure 7.

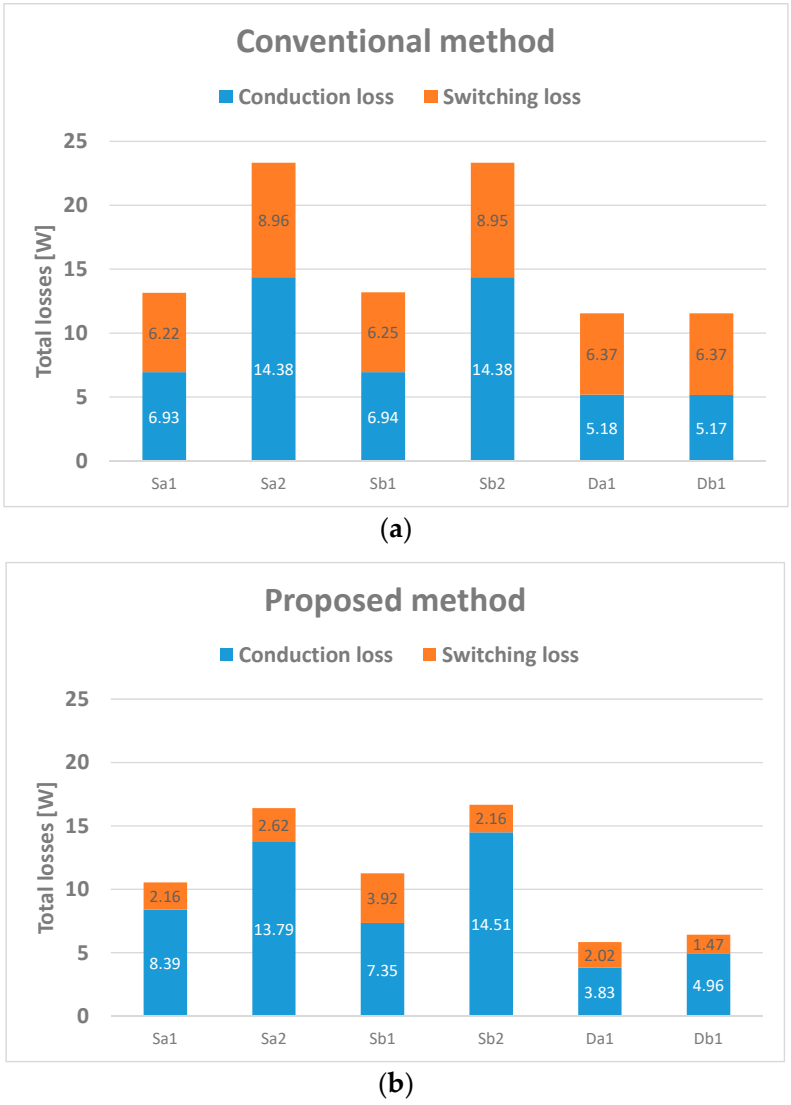


Figure 7. Loss comparison of (**a**) conventional method (**b**) proposed method.

4. Simulation and Experimental Results

In order to demonstrate the proposed method, a single-phase three-level NPC converter with the proposed method was operated at v_s = 110 V, V_{dc} = 150 V, T_s = 50 μs, R_L = 100 Ω, R_s = 1 Ω, and L_s = 10 mH. The weighting factor λ_c = 0.5 in (11) was used for both the conventional and the proposed methods. Figure 8 shows simulation waveforms of the source current (i_s), source voltage (v_s), line-to-line converter input voltage (v_{ab}), converter pole voltages (t), and frequency spectrum of the input current (i_s) obtained by the conventional and the proposed methods.

It is seen that the proposed method, operated with only a consideration of the reduced number of commutations, and the conventional method, using all possible switching states, make the source voltage and the source current in phase. This yields a unity power factor. It is noted that the source current and the ac line-to-line converter voltage generated by both methods are almost the same. On the other hand, the converter pole voltages of the proposed method are different from those of the

conventional method because of the reduced number of switchings. It is seen that the pole voltage of the proposed method has a lower number of commutations than the conventional method owing to the reduced switching operations of the proposed method. From the frequency spectrum waveforms, it can be shown that the two methods represent almost the same current THD values. Therefore, the proposed method can reduce the number of switchings and the switching losses without deteriorating the quality of the ac current waveform in comparison with the conventional method.

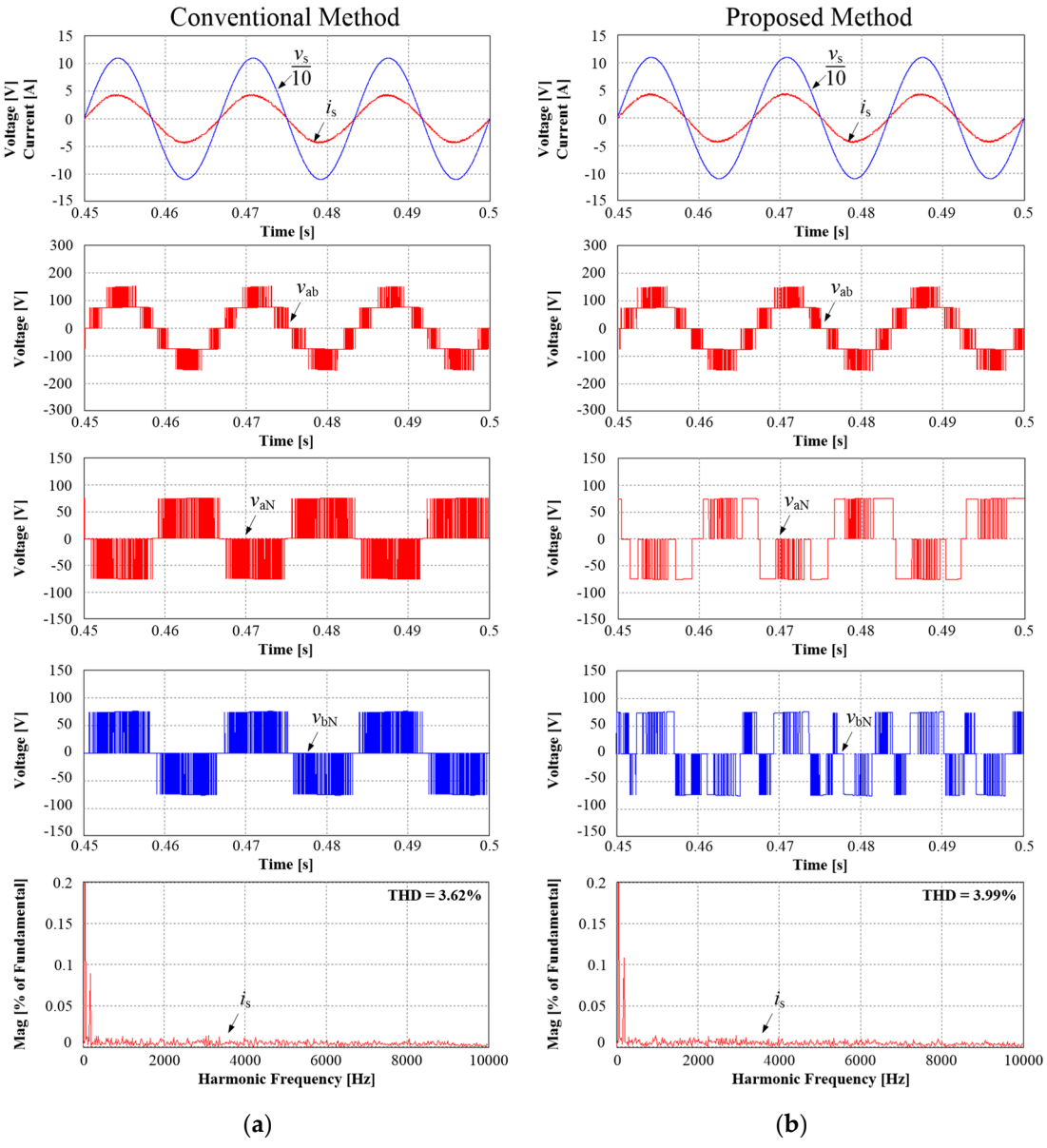


Figure 8. Simulation results of ac source current (i_s), source voltage (v_s), converter line-to-line voltage (v_{ab}), pole voltages (v_{aN}, v_{bN}), and frequency spectrum of input current (i_s) obtained by (**a**) conventional and (**b**) proposed methods.

Figure 9 shows simulation waveforms of the upper and the lower capacitor voltages (v_{c1} and v_{c2}) and switching patterns of the four upper switches (S_{a1}, S_{a2}, S_{b1}, and S_{b2}) during the steady state as obtained by the conventional and proposed methods. In Figure 9a, obtained by the conventional MPC method using all possible switching states, the two capacitor voltages with the NP voltage controlled by the redundant switching states are almost equal with an avoidable oscillation at a certain voltage boundary ΔV_C.

In the proposed method, as shown in Figure 9b, the converter is operated with only a consideration of the reduced number of commutations. It is clearly seen from the switching patterns that the proposed method yields a reduced number of switchings compared with the conventional method. This can lead to a decreased number of switching losses and higher efficiency. In addition, in the proposed method of Figure 9b, the NP voltage balance is well regulated without a continuous increase or decrease in the capacitor voltages, whereas the peak-to-peak ripple voltages of the two capacitors obtained by the proposed method are slightly increased compared with those of the conventional method. The number of switchings and switching losses of the proposed method were reduced by almost half in comparison with the conventional method.

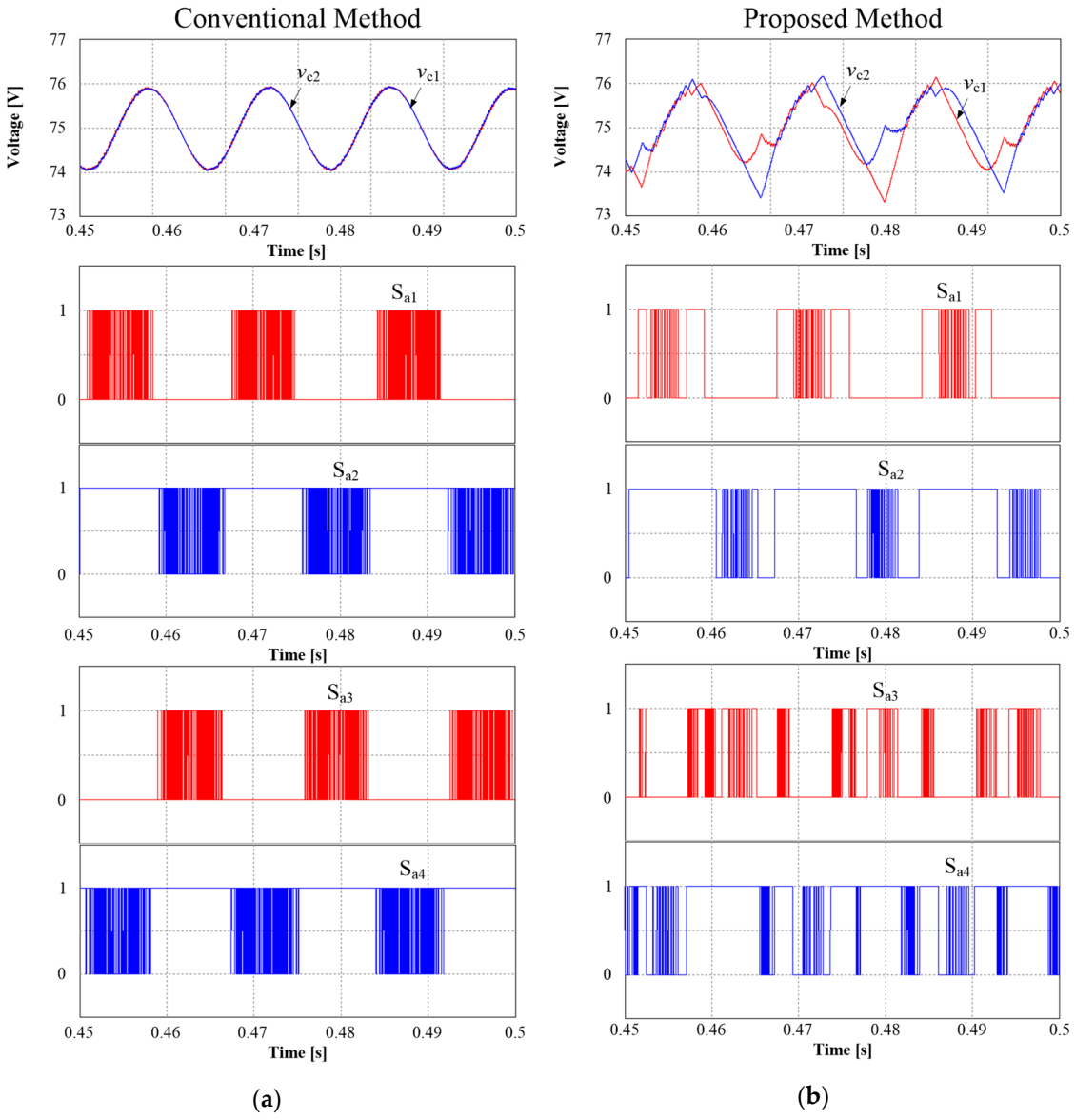
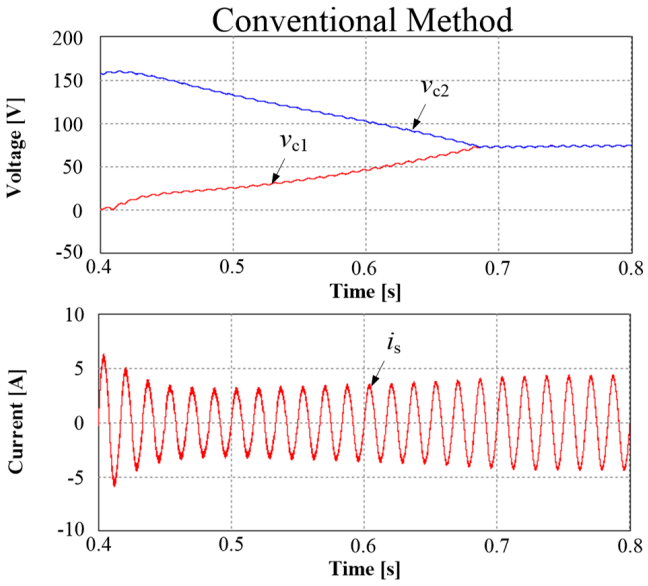
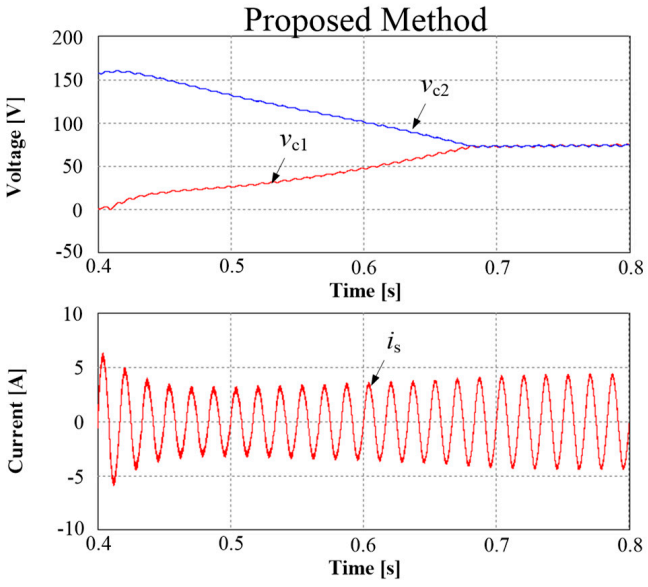


Figure 9. Simulation results of upper and lower capacitor voltages (v_{c1}, v_{c2}) and switching patterns of four upper switches (S_{a1}, S_{a2}, S_{b1}, S_{b2}) during steady state in (**a**) conventional MPC method and (**b**) proposed MPC method.

Figure 10 shows simulation waveforms of the two methods when imbalance conditions of the capacitor voltages, which were intentionally generated, occur. Both the conventional and proposed methods can balance the capacitor voltages, as shown in Figure 10. It is seen that the proposed method, using a reduced number of possible switching states for a reduced number of commutations, can yield an NP voltage balance at almost the same speed as the conventional method.



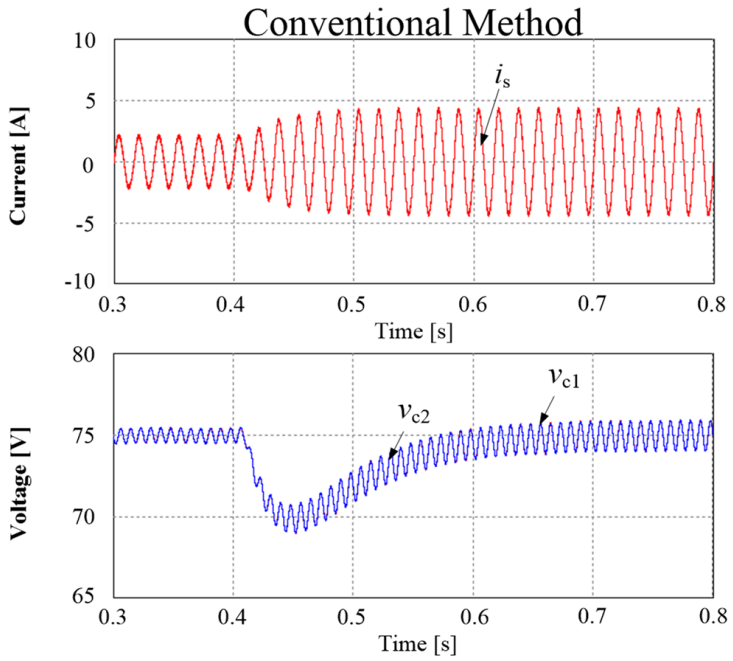
(**a**)



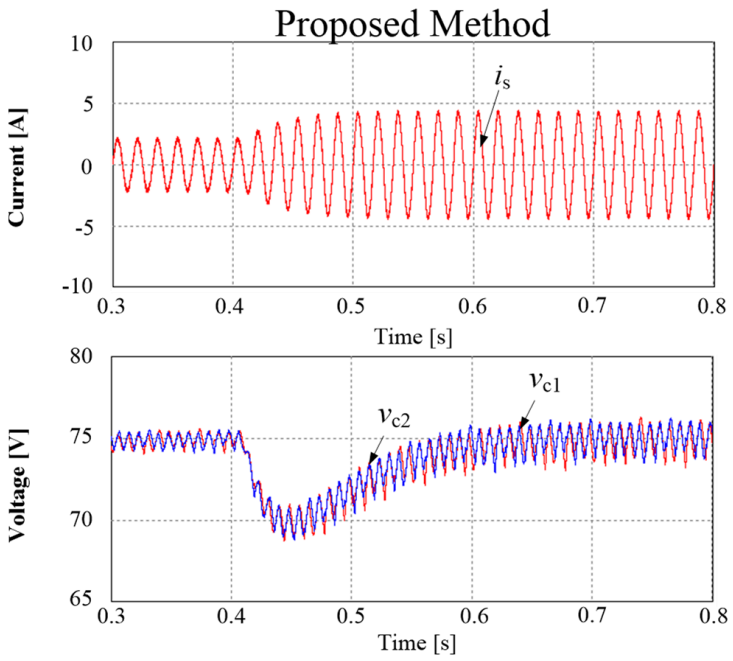
(**b**)

Figure 10. Simulation results of capacitor voltages (v_{c1}, v_{c2}) and source current during imbalanced NP voltage conditions obtained by (**a**) conventional method and (**b**) proposed method.

Figures 11 and 12 show simulation waveforms of step changes of the load resistance and the dc load voltage obtained by the two methods. It is seen that the proposed method achieves dynamic responses as quickly as the conventional method despite the reduced number of possible switching states to decrease the number of switching losses.



(**a**)



(**b**)

Figure 11. Simulation results of capacitor voltages (v_{c1}, v_{c2}) and source current with step change of load resistor from 200 Ω to 100 Ω obtained by (**a**) conventional method and (**b**) proposed method.

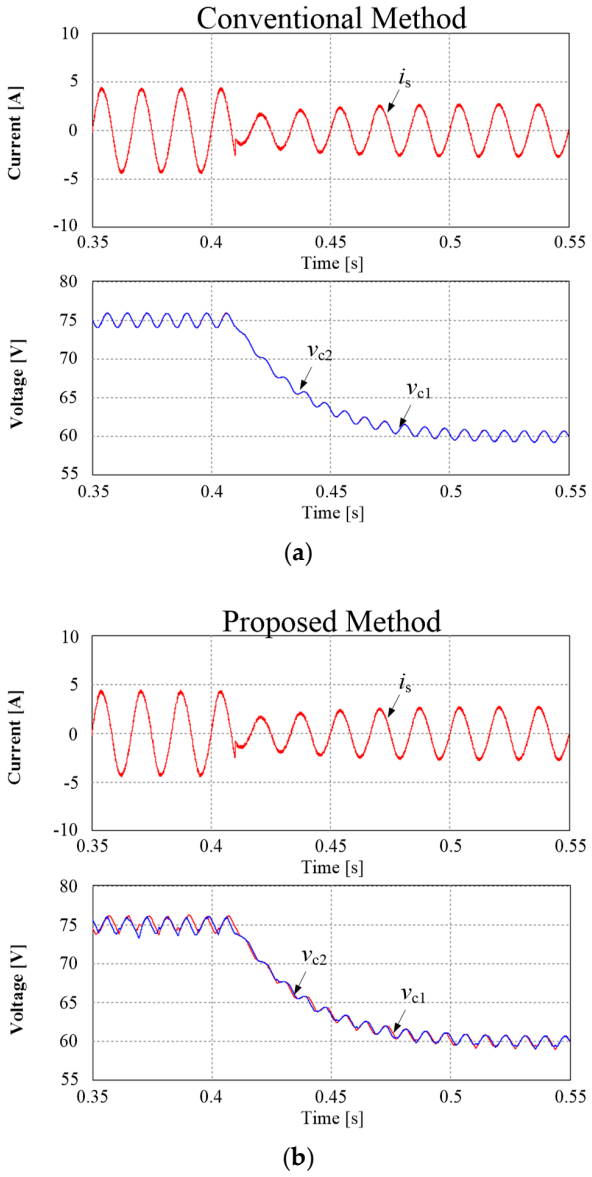


Figure 12. Simulation results of capacitor voltages (v_{c1}, v_{c2}) and source current with step change of dc voltage from 150 V to 120 V obtained by (**a**) conventional method and (**b**) proposed method.

Effects of the control parameter λ_c on performance were investigated, where Figure 13 shows the average number of switching, the THD values of line current, and the peak-to-peak values of capacitor ripple voltage of the conventional and the proposed methods, as a function of the weighting factor λ_c varying from 0.05 to 2. It is shown from Figure 13 that the proposed method results in much lower average number of switching and almost same THD values of the line currents in comparison with the conventional method, over the range of the varying weighting factor. Figure 14. depicts simulation results of ac source current, frequency spectrum of source current, and two capacitor voltages obtained by the conventional and the proposed methods with weighting factor $\lambda_c = 0.05$, $\lambda_c = 0.5$, and $\lambda_c = 2$, respectively. The peak-to-peak value of the two capacitor ripple voltages of the proposed method is slightly increased compared with that of the conventional method, with the trade-off with the reduced number of switching and the consequently decreased switching losses. It is seen that the proposed method with the three different weighting factors regulates the sinusoidal input current well and maintains the two capacitor voltage balancing, even with the lower switching operations than the conventional method.

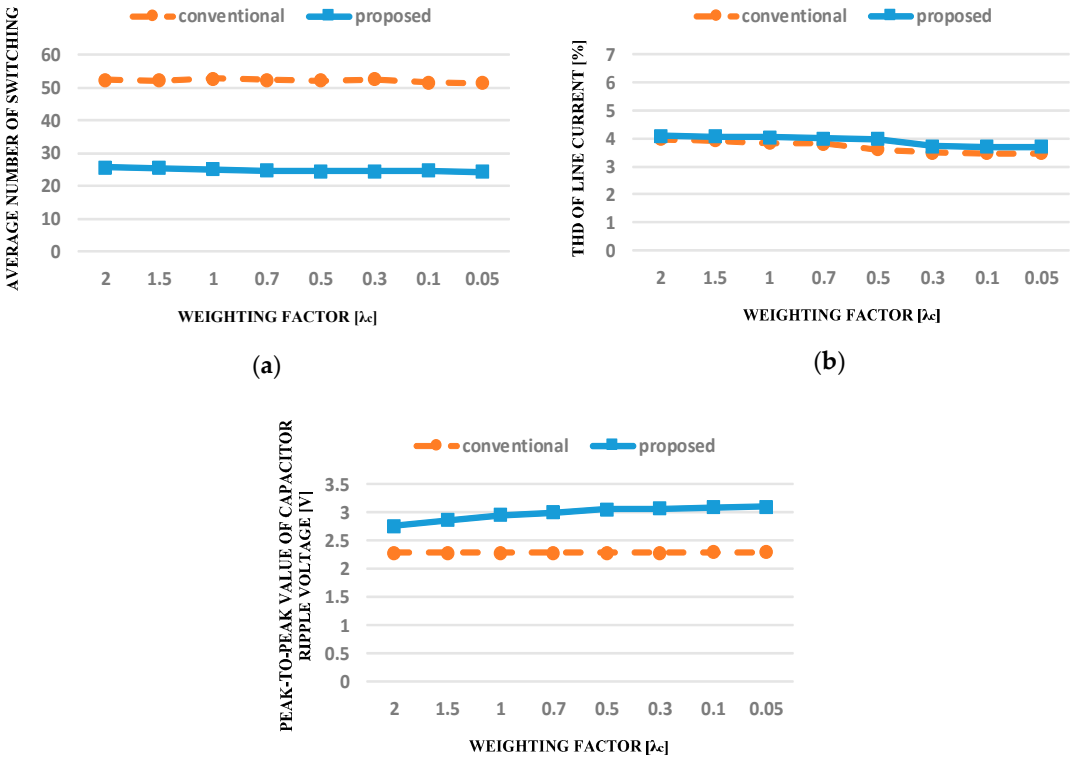
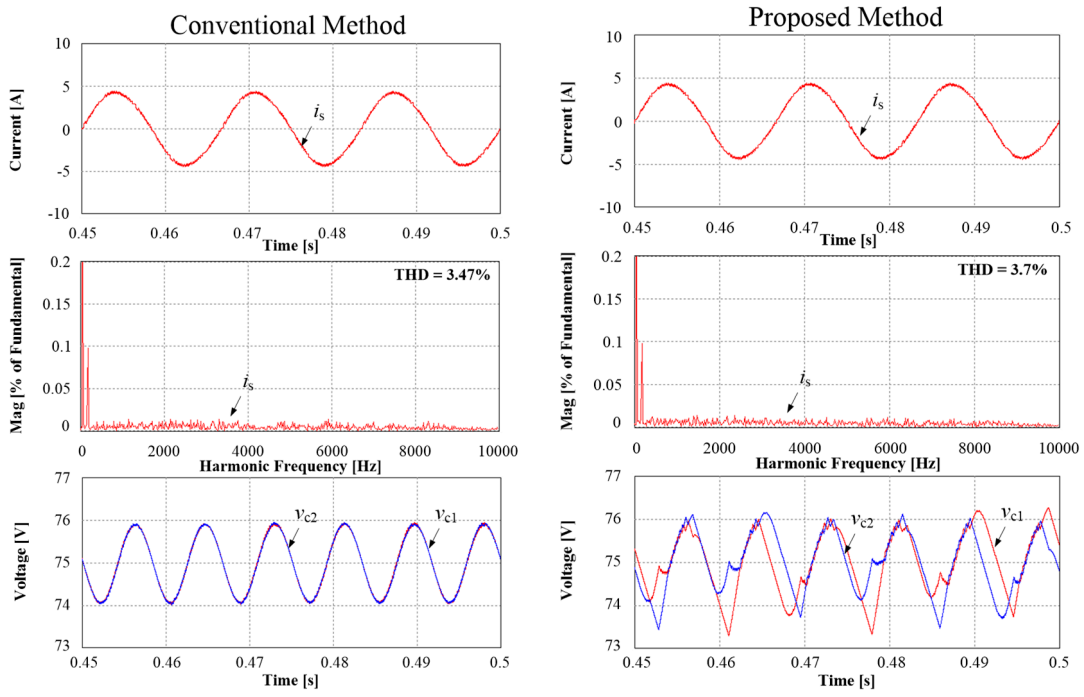
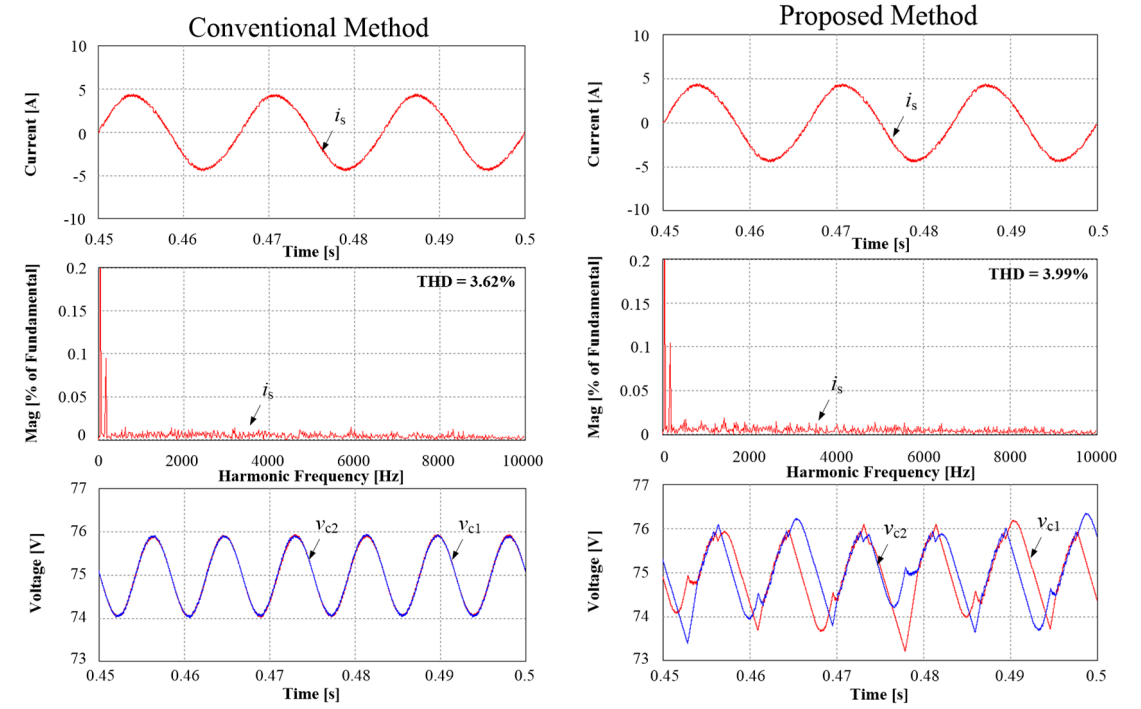


Figure 13. Effects of weighting factor λ_c varying from 0.05 to 2 on (**a**) average number of switching (**b**) THD of line current (**c**) peak-to-peak value of capacitor ripple voltage of the conventional and the proposed methods.

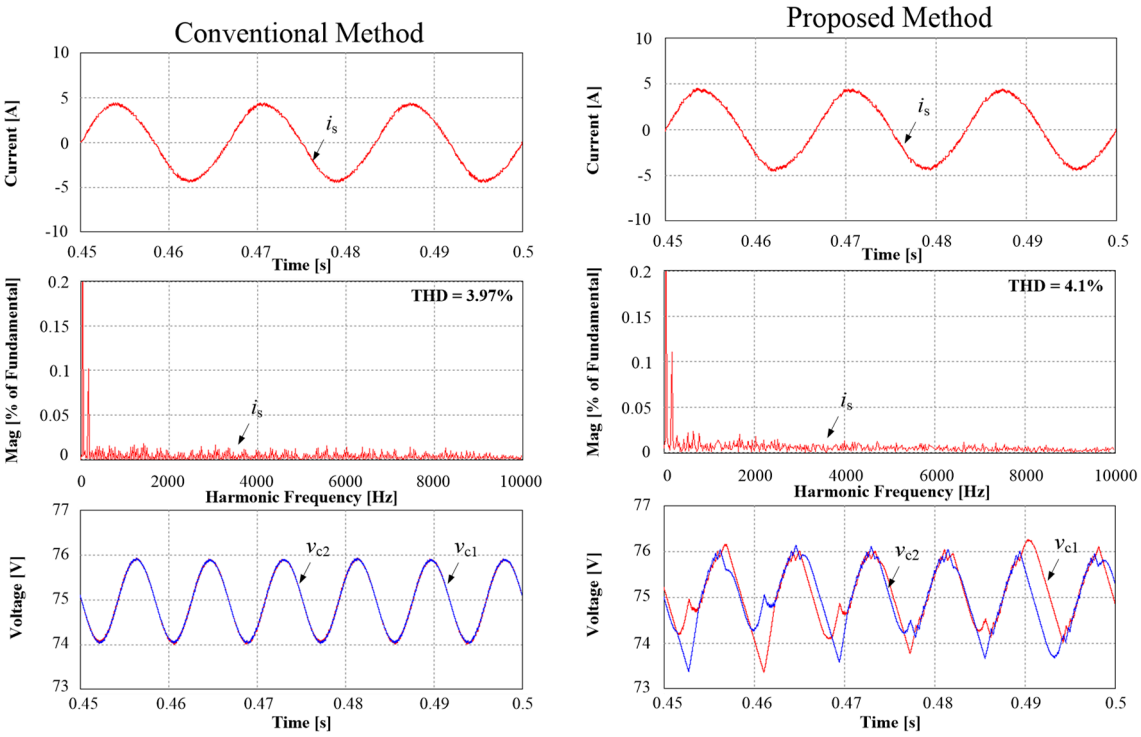


(**a**)

Figure 14. *Cont.*



(**b**)



(c)

Figure 14. Simulation results of ac source current (i_s), frequency spectrum of input current (i_s), and capacitor voltages (v_{aN}, v_{bN}) obtained by the conventional and the proposed methods with weighting factor (**a**) $\lambda_c = 0.05$, (**b**) $\lambda_c = 0.5$, and (**c**) $\lambda_c = 2$.

Performances with larger input resistance and input inductance were investigated. Figure 15 shows the average number of switching, the THD values of line current, and the peak-to-peak values of capacitor ripple voltage of the conventional and the proposed methods, for several values of the input resistance and the input inductance. It is shown from Figure 15 that the proposed method results

in much lower average number of switching and almost same THD values of the line currents in comparison with the conventional method, for the different input parameters. Figure 16. depicts simulation results of ac source current, frequency spectrum of source current, and two capacitor voltages obtained by the conventional and the proposed methods with the three different input resistances and input inductances. The peak-to-peak value of the two capacitor ripple voltages of the proposed method is slightly increased compared with that of the conventional method, with the trade-off with the reduced number of switching and the consequently decreased switching losses. It is seen that the proposed method with the three different input parameters regulates the sinusoidal input current well and maintains the two capacitor voltage balancing, even with the lower switching operations than the conventional method.

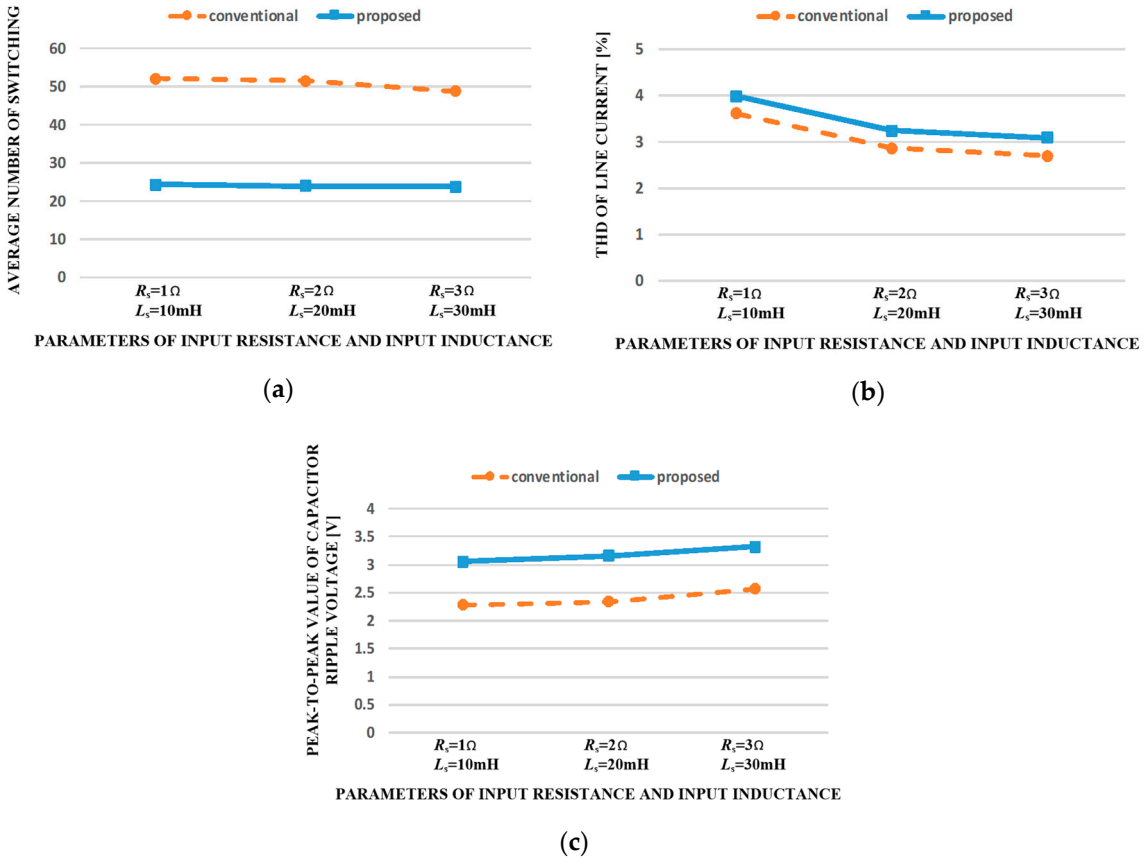
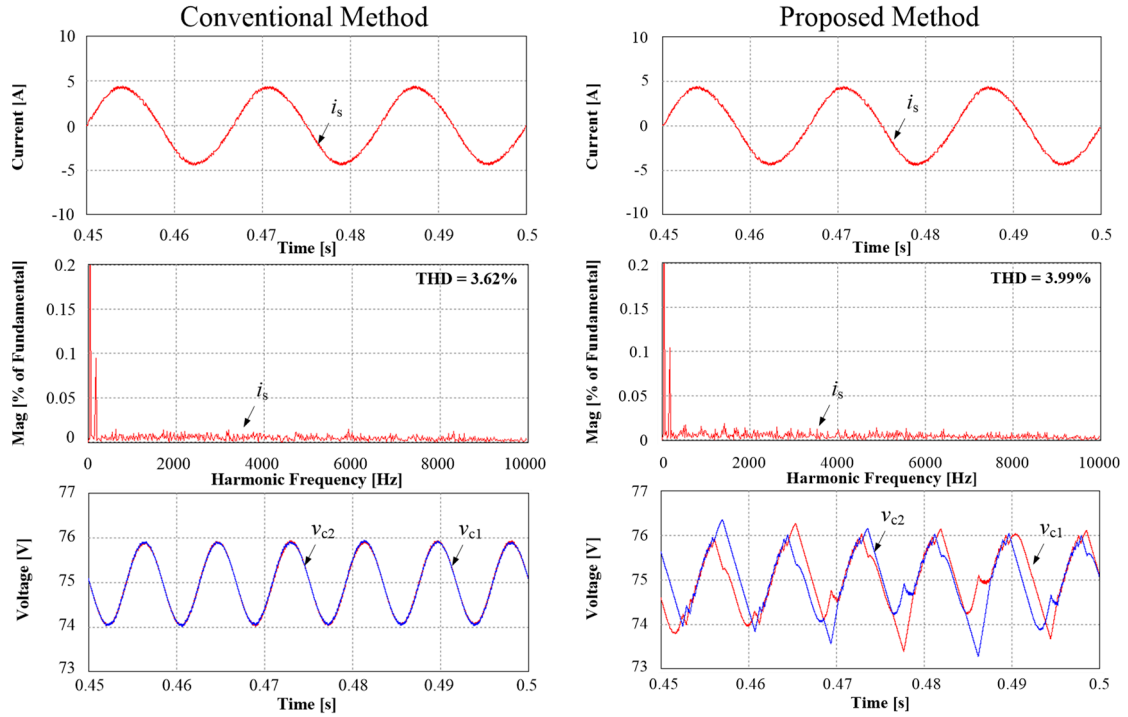
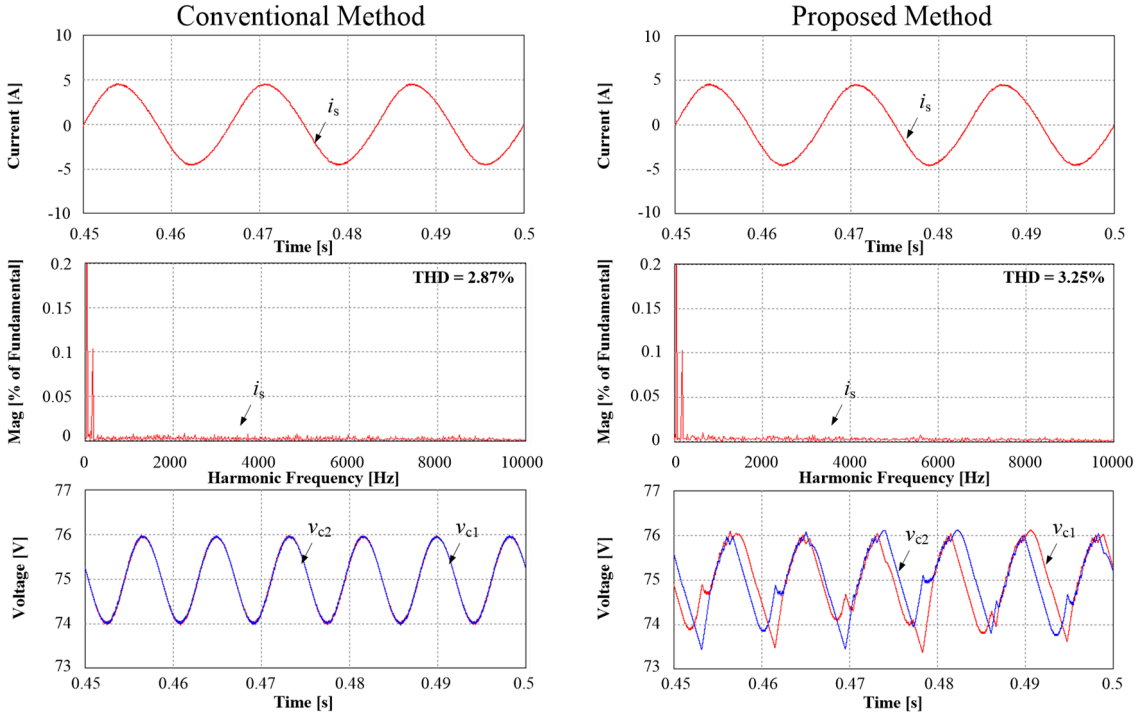


Figure 15. Effects of input resistance and input inductance on (**a**) average number of switching (**b**) THD of line current (**c**) peak-to-peak value of capacitor ripple voltage of the conventional and the proposed methods.

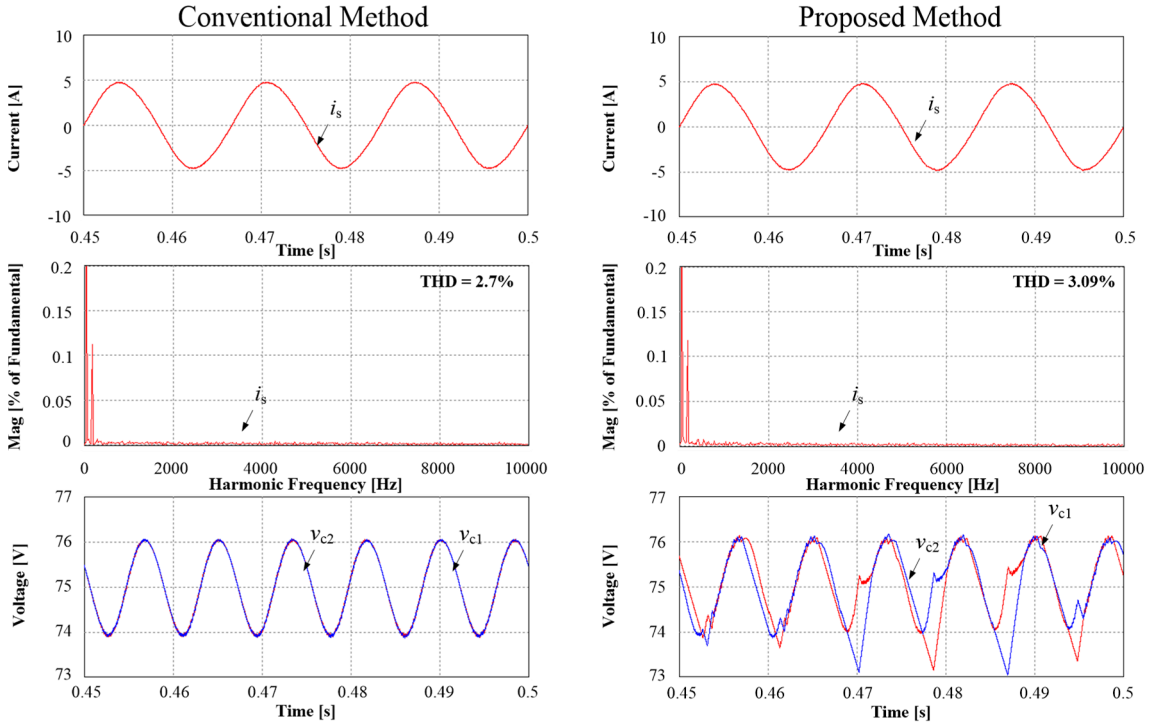


(**a**)



(**b**)

Figure 16. *Cont.*



(**c**)

Figure 16. Simulation results of ac source current (i_s), frequency spectrum of input current (i_s), and capacitor voltages (v_{aN}, v_{bN}) obtained by the conventional and the proposed methods with input parameters (**a**) R_s = 1 Ω and L_s = 10 mH (**b**) R_s = 2 Ω and L_s = 20 mH, and (**c**) R_s = 3 Ω and L_s = 30 mH.

The single-phase three-level NPC converter operated with the proposed method was tested with a nonlinear load, which is a three-phase voltage source inverter with a fundamental frequency of 80 Hz as shown in Figure 17. For the purpose of comparison, the simulation results obtained by the conventional method were also included. It is seen from Figure 18 that the single-phase three-level NPC converter with the proposed method well regulates the sinusoidal source current in phase with the source voltage with a low THD value, even with a nonlinear load. In addition, the two capacitor voltages of the proposed method are balanced in a case of the nonlinear load as the same as the linear load, as shown in Figure 18.

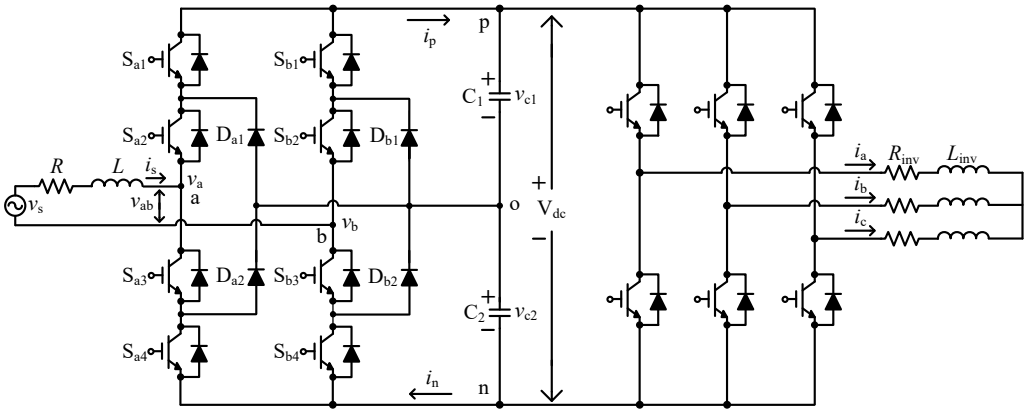


Figure 17. Schematic with a three-phase voltage source inverter as a nonlinear load.

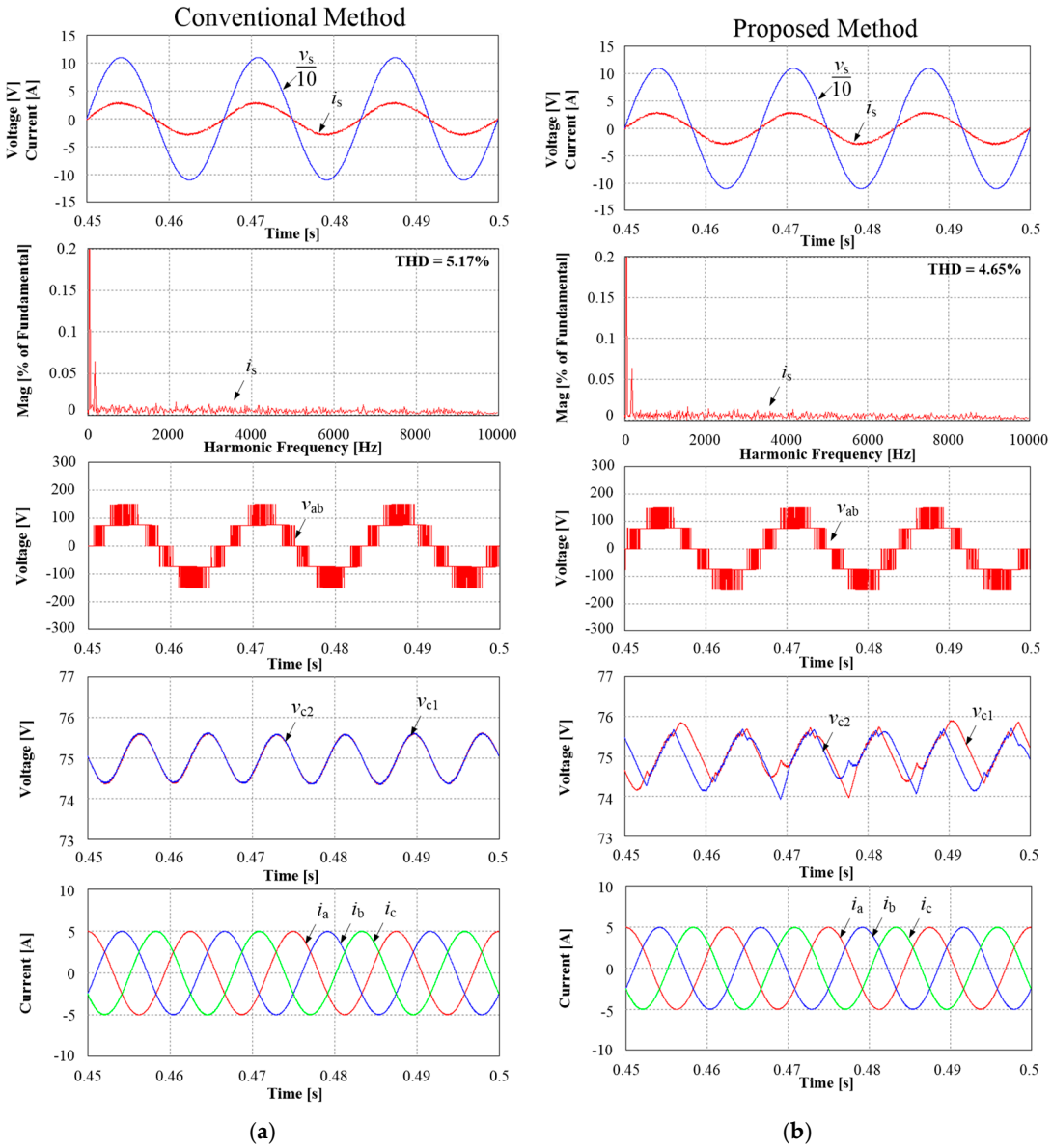


Figure 18. Simulation results with the three-phase voltage source inverter as a nonlinear load: ac source current (i_s), frequency spectrum of input current (i_s), line to line source voltages (v_{ab}), capacitor voltages (v_{c1}, v_{c2}), and three-phase load currents of the voltage source inverter (from top to bottom) obtained by (**a**) the conventional method (**b**) the proposed methods.

A prototype of a single-phase three-level NPC converter, shown in Figure 19, was fabricated in a laboratory to prove the proposed method. The conventional and proposed methods were implemented using a DSP board (TMS320F28335). To compare the performance of the two methods, experiments were conducted under the same conditions as the simulation. Figure 20 shows experimental waveforms of the source voltage/current, converter input voltage, each pole voltage, and an FFT analysis of the source current for the conventional method and the proposed method during steady-state conditions.

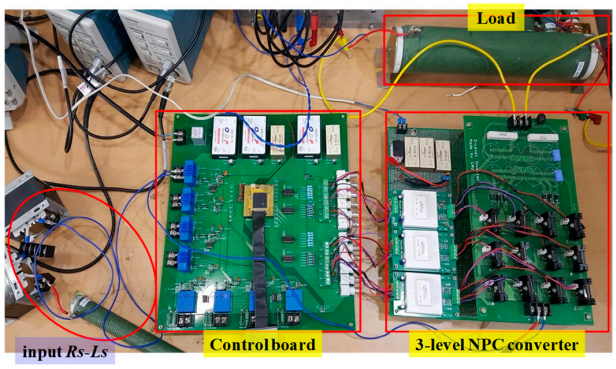


Figure 19. Photograph of prototype setup for single-phase three-level NPC converter.

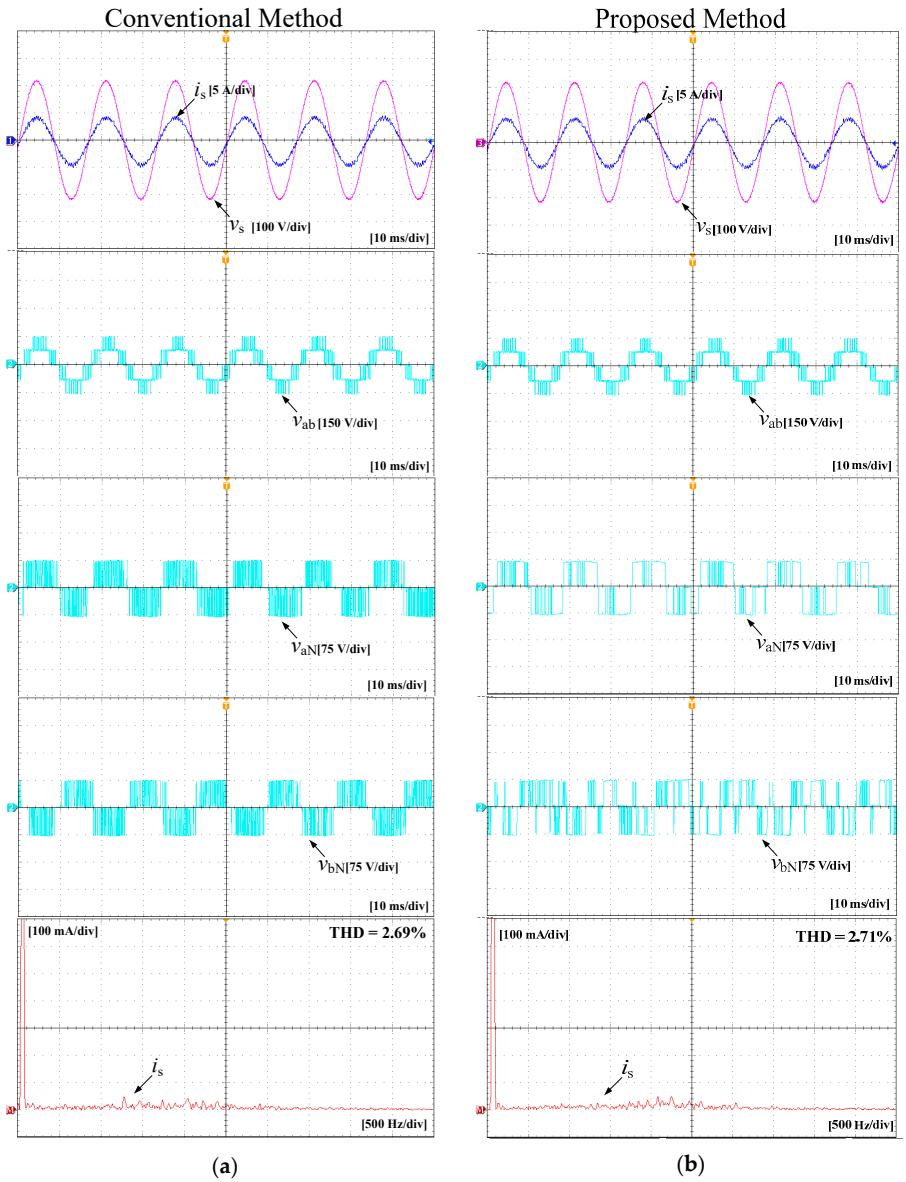


Figure 20. Experimental results of ac source current (i_s) and source voltage (v_s), converter input voltage (v_{ab}), pole voltage (v_{aN}, v_{bN}), and FFT analysis of source current (i_s) in (**a**) conventional and (**b**) proposed methods.

As in the simulation, the proposed method shows almost the same source current and converter input voltage waveforms as the conventional method. In addition, the proposed method through the FFT analysis shows performance that is very similar to that of the conventional method. On the other hand, as shown in Figure 20, the proposed method has a quite different pole voltage from the conventional method owing to the reduced number of switchings.

Figure 21 shows the upper and lower capacitor voltages, source current, and switching state in the steady state. As shown in Figure 21, the proposed method reduces the number of switchings in comparison with the conventional method. In addition, the NP voltage balance in the proposed method is well regulated without a continuous increase or decrease in the capacitor voltages, whereas the peak-to-peak ripple voltages of the two capacitors obtained by the proposed method is slightly increased compared with the conventional method.

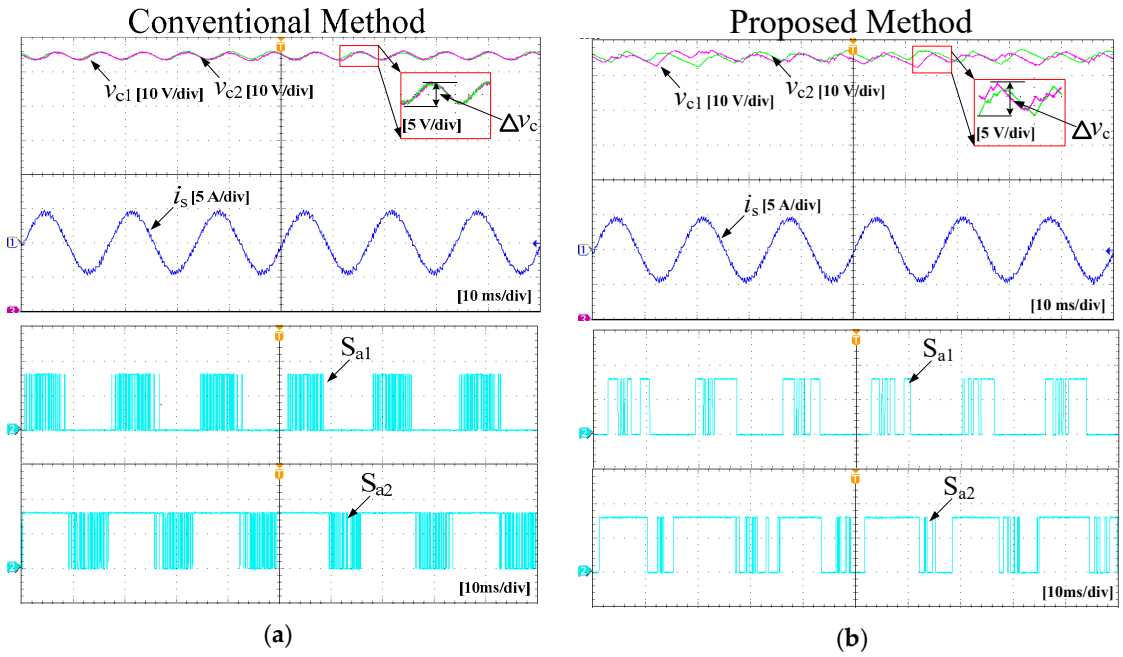


Figure 21. Experimental results of capacitor voltages (v_{c1}, v_{c2}), source current (i_s), and upper switch of a leg (S_{a1}, S_{a2}) during steady state in (**a**) conventional method and (**b**) proposed method.

In Figure 22, experimental waveforms of the two methods are shown when imbalanced NP voltage conditions of the capacitor voltages, which are intentionally generated, occur. Both the conventional and proposed methods can balance the capacitor voltages, as shown in Figure 22. This is the same as the simulation results of Figure 10. It is seen that the proposed method, using a reduced number of possible switching states for a reduced number of commutations, can yield an NP voltage balance at almost the same speed as the conventional method. Figures 23 and 24 show experimental waveforms of step changes of the load resistance and the dc load voltage obtained by the two methods. It is seen that the proposed method achieves dynamic responses as quickly as the conventional method despite the reduced number of possible switching states to decrease the number of switching losses.

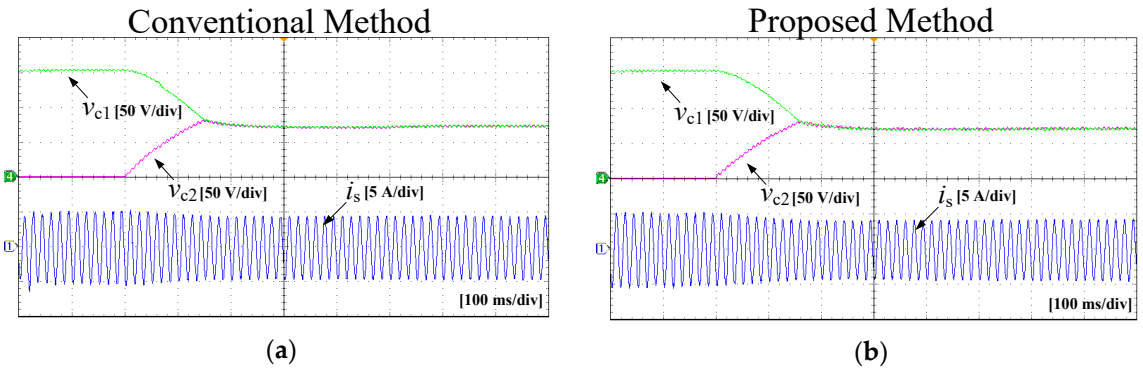


Figure 22. Experimental results of capacitor voltages (v_{c1}, v_{c2}) and source current during imbalanced NP voltage conditions obtained by (**a**) conventional method and (**b**) proposed method.

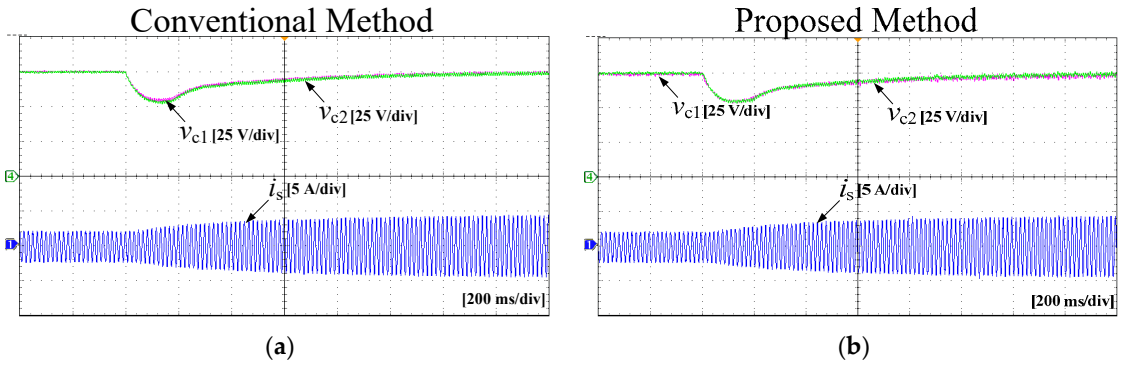


Figure 23. Experimental results of capacitor voltages (v_{c1}, v_{c2}) and source current with step change of load resistor from 200 Ω to 100 Ω obtained by (**a**) conventional method and (**b**) proposed method.

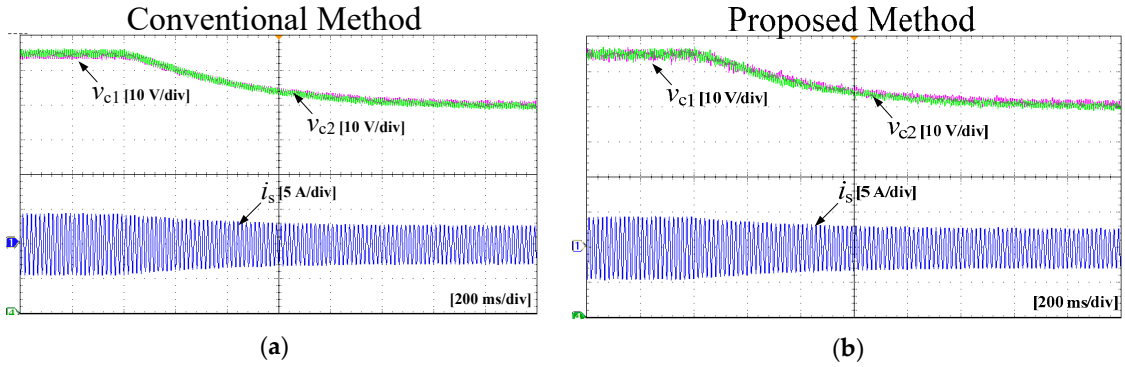


Figure 24. Experimental results of capacitor voltages (v_{c1}, v_{c2}) and source current with step change of dc voltage from 150 V to 120 V obtained by (**a**) conventional method and (**b**) proposed method.

5. Conclusions

This paper proposed a highly efficient algorithm with a reduced number of switchings and low switching losses for single-phase three-level NPC converters based on an MPC method with a decreased number of commutations of switches. The proposed method pre-excludes, from the candidates for possible future switching states, the switching states that yield more than two commutations in the next sampling period. As a result, the proposed technique can reduce the number of switchings and the switching losses by utilizing switching states involving no commutation or only one commutation at every sampling instant for single-phase three-level NPC converters. In addition, the developed method does not deteriorate the input current quality or input power

factor despite the reduced switching numbers and losses. Although the proposed method slightly increases the peak-to-peak variations of the two dc capacitor voltages at the expense of reduced commutation, the increased voltage variation is not high. Thus, the proposed method can obtain high efficiency and low switching losses at the expense of slightly increased peak-to-peak variations of the NP voltage. Simulations and experimental results were presented to verify the effectiveness of the proposed method.

Author Contributions: All authors contributed to this work by collaboration.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

Abbreviations

EMI	Electromagnetic interference
NPC	Neutral point clamped
CBPWM	Carrier-based pulse width modulation
PI	Proportional and integral
NP	Neutral point
MPC	Model predictive control
THD	Total harmonic distortion
IGBT	Insulated gate bipolar transistor

Variables

S_a	Operating status of *a*-phase
S_b	Operating status of *b*-phase
v_a	Source voltage
i_a	Source current
i_a^*	Reference source current
R_s	Input resistance
L_s	Input inductance
v_{ab}	Line-to-line source voltage
v_{aN}	Phase voltage of a-phase
v_{bN}	Phase voltage of b-phase
C_1	Output capacitance in upper capacitor
C_2	Output capacitance in lower capacitor
i_u	Current of upper dc-bus bar
i_l	Current of lower dc-bus bar
R_L	Output load resistance
V_{dc}	Output dc voltage
g	Cost function
λ_c	Weighting factor
T_s	Sampling period

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