Brief Papers

A Digitally Controlled Phase-Locked Loop With a Digital Phase-Frequency Detector for Fast Acquisition

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***Abstract*—A digitally controlled phase-locked loop (DCPLL) that achieves fast acquisition by employing a digital phase-frequency detector (DPFD) and a variable loop gain scheme was developed for an advanced clock synthesizer and was fabricated in a 3.3-V 0.6-μm CMOS process. The DPFD was developed to measure the frequency difference and to generate digital outputs corresponding to the difference. Using these features, the DCPLL achieves ideally one-cycle frequency acquisition when programmed with an appropriate gain. The experimental results show that the fabricated DCPLL exhibits three-cycle and one-cycle frequency acquisitions, when locking to 400 MHz (VCO at 800 MHz) and 200 MHz (VCO at 400 MHz), respectively.**

I. Introduction

AN INTEGRATED clock synthesizer that produces a high-frequency clock from an incoming lower frequency reference clock is widely used in clock generation and recovery applications [1]–[5]. It is usually difficult to feed a radio-frequency clock signal into a packaged chip due to signal reflection by the impedance mismatch at an interface between a pin and a printed circuit board (PCB) line. In order to circumvent this problem, a low-frequency clock is transmitted over the PCB line and a new desired high-frequency clock is generated by the integrated clock synthesizer in a chip. In most cases, the clock synthesizers are made up of charge-pump phase-locked loops (PLLs), primarily due to their simple structure compatible with CMOS processes.

However, the charge-pump PLL as a clock synthesizer poses several limitations for performance enhancement. First of all, acquisition time is rather limited since the PFD used in a conventional charge-pump PLL evaluates the frequency difference between the reference and the generated clocks by means of the phase difference. Fast acquisition time, thus achieving fast switching time between various on-chip clock frequencies is gaining importance as flexible frequency multiplication ratio following the hit ratio in the first level cache is desired in current microprocessors. In addition, various power management techniques require on-chip clocks to be suspended or scaled down in frequency. In both applications, the fast acquisition characteristic of PLL is crucial.

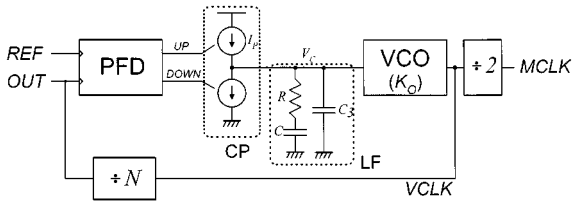

Fig. 1. Typical charge-pump PLL as a clock synthesizer.

As shown in Fig. 1, the PFD measures the phase difference between *REF* and *OUT* signals and generates either *UP* or *DOWN* pulse depending on the measured phase difference. This signal, in turn, produces a current pulse (I_P) with the corresponding duty ratio in a charge-pump (CP) block. At the loop filter (LF), this current is converted to voltage-controlled oscillator (VCO) control voltage, V_C. Since the acquisition process corresponds to either charging or discharging the loop filter until the alignment of the phases, the acquisition time $(T_{\rm acq})$ for the charge-pump PLL can be approximated by

$$T_{\rm acq} \approx \frac{R \cdot C}{\alpha \cdot N \cdot K_L} \cdot |\Delta f_{\rm init}| \tag{1}$$

where

- $\Delta f_{\rm init}$ initial difference between N times the frequency of *REF* and the frequency of *VCLK*;
- α average duty ratio of the current pulse stream during acquisition process;
- K_L loop bandwidth which is given by $I_p K_o R/2\pi N$ [6].

As can be seen in (1), the acquisition time is directly proportional to the initial frequency difference, $\Delta f_{\rm init}$, and inversely proportional to the loop bandwidth, K_L. Consequently, in order to reduce the acquisition time, small initial frequency difference and wide loop bandwidth are desirable. However, it is not always possible to achieve small $\Delta f_{\rm init}$ at the designing stage due to process, voltage, and temperature (PVT) variations. In addition, an enhancement of the acquisition time through wide loop bandwidth causes the increase of the input phase noise [7], [8]. Another limitation of charge-pump PLLs comes from resistors and capacitors used in the loop filter, which consume a large amount of precious silicon area, hampering the full adaptation

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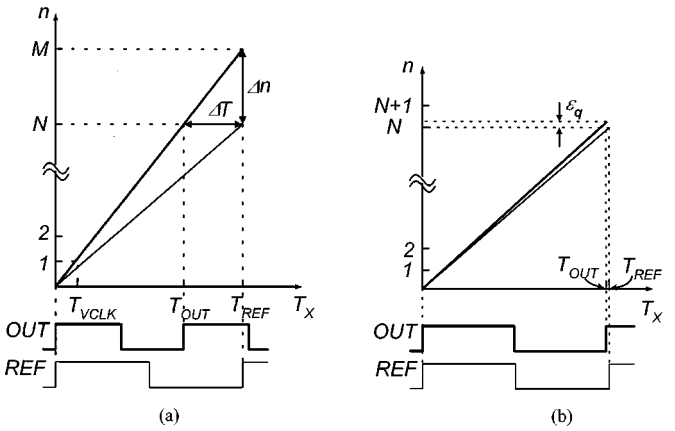

Fig. 2. Illustrations for the frequency difference measurement. (a) Measurement principle. (b) Quantization error.

of the clock synthesizer in digital systems [9]. The values of resistors and capacitors in the loop filters, once implemented, are unalterable, let alone the difficulty of fabricating with the exact values due to process variations.

In this paper, we present a new digital PLL that employs fast acquisition architecture. We propose and implement an advanced architecture for improving acquisition time using a digital PFD (DPFD) and adaptive loop control. The DPFD measures the frequency difference directly [10], unlike the conventional PFD that performs the task indirectly. The frequency difference measurement is achieved by measuring the period of the reference clock using a VCO clock with a smaller unit period. This measurement enables the digital PLL to reduce the acquisition time independent of the initial frequency difference Δf_{init}. Also, the DPFD renders a digital design of the loop filter possible, thus providing many benefits in terms of testability, flexibility, and portability to various processes [11].

The principle of frequency measurement used in DPFD design is presented in Section II, and the loop design for the digital PLL is described in Section III. The circuit implementations for the main blocks are described in Section IV. Finally, the experimental results for the prototype chip fabricated on a 0.6-μm CMOS process and the conclusion are described in Section V and Section VI, respectively.

II. Digital Phase-Frequency Detector (DPFD) Design

The proposed DPFD was designed to directly measure the frequency difference between *REF* and *OUT* using *VCLK*, where all signal notations are the same as those used in Fig. 1 for the ease of understanding. The basic operating principle for the frequency measurement is illustrated in Fig. 2, where x-axis represents time and y-axis represents the time normalized to T_{VCLK}, n. In a mathematical form, n can have an integer value and can be written as

$$n = \left\lfloor \frac{T_X}{T_{VCLK}} \right\rfloor \tag{2}$$

where T_X's represent the periods of signals designated by their subscripts, X's. At the completion of acquisition, T_{REF} is equal

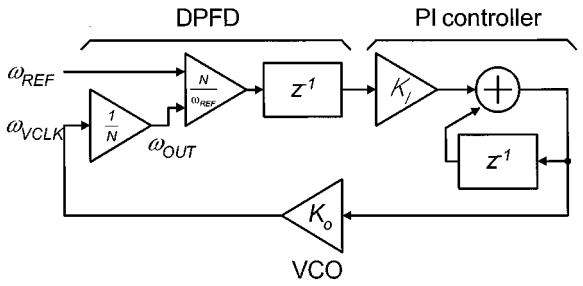

Fig. 3. Loop design for digital PLL using DPFD.

to N times T_{VCLK} and the *REF* signal can be represented by the thin line with the slope of N/T_{REF}, as shown in Fig. 2(a). Before the acquisition, however, the *OUT* signal may have a different period from that of the *REF* signal and can be represented by the bold line with the slope of M/T_{REF}. The deviation of the *OUT* signal line from the *REF* one reflects the period difference, originating from the frequency difference between them. If, as shown in Fig. 2(a), some mismatch between T_{OUT} and T_{REF} exists since *VCLK* is faster or slower than the desired clock, from the geometrical relationship between two lines we can calculate Δn, which is proportional to time difference ΔT.

$$\Delta n = \frac{1}{T_{\text{VCLK}}} \Delta T + \varepsilon_q \tag{3}$$

where ε_q is quantization error caused by the discrete nature of the y-axis. Since $\Delta T = T_{\text{OUT}} - T_{\text{REF}}$ and $\Delta n = N - M$, where M denotes the number of *VCLK* pulses enclosed in the duration of T_{REF}, (3) is arranged into

$$N - M = \frac{1}{T_{\text{VCLK}}} (T_{\text{OUT}} - T_{\text{REF}}) + \varepsilon_q. \tag{4}$$

As can be seen in (4), even though M is forced to have the value of N by the PLL, T_{OUT} does not become equal to T_{REF} because of ε_q. To demonstrate this effect in more detail, we show a condition that there remains quantization error while $N - M$ becomes zero in Fig. 2(b). This quantization error ε_q is placed in the range between -1 and 1, thus it cannot be resolved over the y-axis. Even at this condition, however, we can discriminate which signal is faster than the other; $N - M$ is equal to 0 when *OUT* leads *REF* in phase, while $N - M$ is equal to 1 when *OUT* lags *REF* in phase. These mutually exclusive values are used to correct the error ε_q in the loop design that will be presented in Section III. Also, the above equation can be converted into the form with respect to radian frequencies

$$N - M = \frac{N}{\omega_{\text{REF}}} (\omega_{\text{REF}} - \omega_{\text{OUT}}) + \varepsilon_q \tag{5}$$

where $\omega_{\text{REF}} = 2\pi/T_{\text{REF}}$ and $\omega_{\text{OUT}} = 2\pi/T_{\text{OUT}}$.

In the case that a reference clock is fixed to a constant frequency as in clock synthesis applications, (5) simply becomes the first-order function in terms of the frequency difference between the *REF* and the *OUT*. As a result, given the number of *VCLK* pulses enclosed in T_{REF}, we can deduce the frequency difference between the *REF* and the *OUT* within a constrained tolerance. Our DPFD is implemented based on this principle.

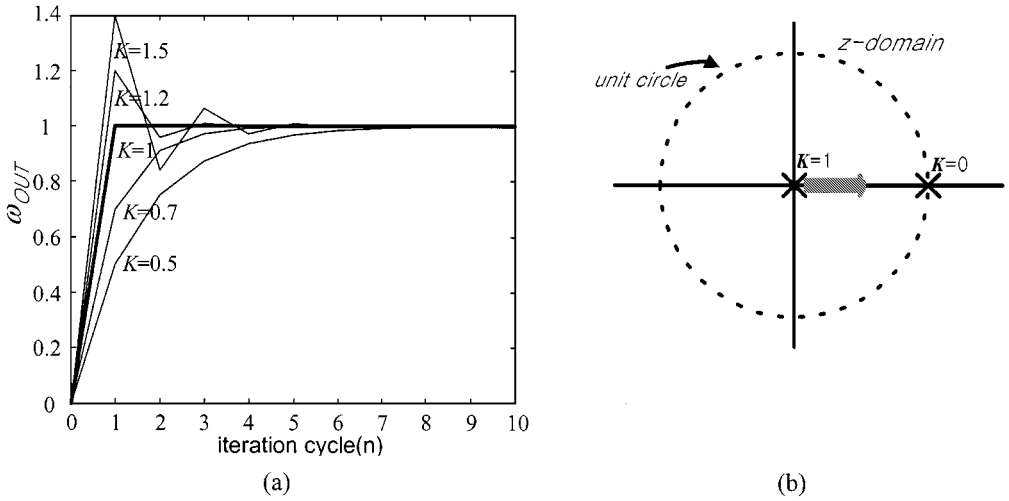

Fig. 4. Loop dynamics. (a) Unit step responses under various gain conditions. (b) Pole displacement by gain variation.

III. Loop Design

In the previous section, we showed how the DPFD issues the value of frequency difference with a constant gain. Using this property, the feedback system with a proportional-integral (PI) controller can be designed for a clock synthesizer, as in Fig. 3.

The purpose of the PI controller is to remove a dc offset at DPFD and to provide fast acquisition for the loop. In this configuration, therefore, the proportional gain K_I determines the performance metric of the loop. Also, this loop can be used to further correct the measurement quantization error left over from the DPFD. As mentioned above, the quantization error ε_q could cause a significant discrepancy between $\omega_{\rm REF}$ and $\omega_{\rm OUT}$, since the DPFD cannot measure this quantity smaller than 1. Therefore, we applied a successive approximation technique that fully scans the range based on binary searching to extend the measurable range of DPFD into a finer scale. For this purpose, two modifications are applied to the loop. First, when the output of DPFD is equal to 0, the value is encoded to -1. Thereby, the DPFD is modified to generate $+1$ when *OUT* lags *REF*, and -1 when *OUT* leads *REF*. Second, K_I is forced to decrease in the order of $K_I/2, K_I/4, K_I/8, \ldots$ per cycle of the reference. These combinations enable the DPFD to reduce the value of ε_q even smaller tolerances as cycle progresses. This sequence can be represented by

$$K_I \cdot \varepsilon_q \approx \sum_{i=1}^{n} \left(K_I \cdot 2^{-i}\right) \cdot X_i \tag{6}$$

where X_i, the output of DPFD, is equal to $+1$ or -1, and n represents the iteration number, which determines the accuracy of measurement. Since K_I is common in both sides of (6), ε_q can be obtained by

$$\varepsilon_q \approx \sum_{i=1}^{n} (2^{-i}) \cdot X_i. \tag{7}$$

Since this operation needs to be separated from the normal operation of the loop, two operational modes are defined in the loop: a frequency acquisition mode for the normal operation and a phase acquisition mode for the successive approximation.

The feedback loop shown in Fig. 3 can be characterized by analyzing its loop dynamics. For this purpose, the closed-loop transfer function $H(z)$ is given by

$$H(z) = \frac{\omega_{\rm OUT}}{\omega_{\rm REF}} = \frac{K \cdot z^{-1}}{1-(1-K)\cdot z^{-1}} \tag{8}$$

where $(K = K_I \cdot Ko/w_{\rm REF})$. From this equation, it should be noted that K has to be placed in the range from 0 to 2 for loop stability. Moreover, $H(z)$ simply becomes Kz^{-1} when K is equal to 1, and $\omega_{\rm OUT}$ can catch up with $\omega_{\rm REF}$ after one-cycle delay. In order to demonstrate this property in a time domain, unit step responses for various K's around 1 are plotted in Fig. 4. In this figure, it is shown that this loop attains the fastest acquisition, i.e., one-cycle frequency acquisition, when K is equal to 1 as previously mentioned. This fast frequency acquisition is achieved by the property that the DPFD directly measures the frequency difference in the frequency acquisition mode.

After the frequency acquisition, the loop enters into the phase acquisition mode. If K_I is initially set to $\omega_{\rm REF}/K_O$, it is reduced from that value by a factor of 2 per every cycle as the successive approximation progresses. The subsequent variation of K_I in the phase acquisition mode results in the displacement of pole in the transfer function. The pole movement from $K = 1$ to $K = 0$ caused by such variation of K_I is illustrated in z domain, as shown in Fig. 4(b).

IV. Circuit Implementation

A prototype chip was fabricated on a 0.6-μm 1-poly 3-metal CMOS process. Fig. 5 shows the functional block diagram of the chip. Notice that all the blocks except for the digital-to-analog converter (DAC) and the VCO are designed by using digital elements. Especially, the digital design of a loop filter, which determines the loop dynamics, provides many advantages to designers. First, loop design becomes so flexible that the designed PLL can be applied to applications with various specifications, while loop filters in a conventional charge-pump PLL cannot be easily replaced once they are integrated. Second, internal loop states such as filter coefficients and filter output can be monitored without any adverse effect on loop operation since their

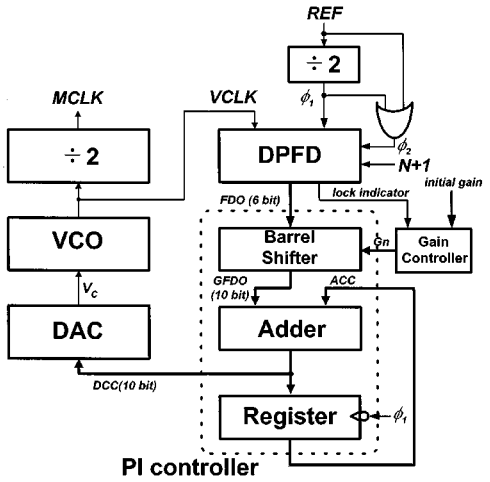

Fig. 5. Functional block diagram for digital PLL.

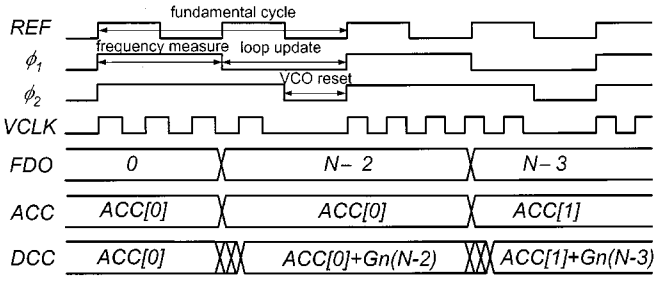

Fig. 6. Fundamental timing diagram.

values are in the form of digital codes. Besides these advantages, digital design provides more opportunities to enhance performance in current low-voltage low-power design environments.

In our design, the PI controller consists of a barrel shifter, an adder, and a register. Even though the employment of a barrel shifter instead of a multiplier causes maximum loop gain error of 33% since the barrel shifter just provides multiplication by a power of 2, we employed a barrel shifter that significantly simplifies the design, facilitates a divide-by-2 operation, and enhances speed, compared with using a multiplier.

The fundamental cycle of this PLL consists of two cycles of the reference clock, as shown in Fig. 6. During the first cycle of the reference clock, the DPFD measures the frequency difference and issues *FDO* values as a measurement result at the end of the cycle. An example of reaching a frequency acquisition in a PI controller is shown in Fig. 6. In the frequency measure cycle, M, the number of *VCLK* pluses enclosed in $T_{\rm REF}$, is measured to be 3. From this measurement, the *FDO* value of $N-2$ is generated at the start of the loop update cycle by subtracting the measured value, 3, from the initialization value $N+1$. The PI controller receives this *FDO* value, multiplies it by a predetermined gain *Gn*, and subsequently adds it to the value in a register. The output of the PI controller, the updated register value (*DCC*), is then fed to the DAC that produces the control voltage for the VCO as shown in Fig. 5. This operation repeats until it reaches the frequency acquisition $(M=N)$. The phase acquisition takes the same procedure as well, while the gain *Gn* is continuously halved every cycle. At this acquisition process,

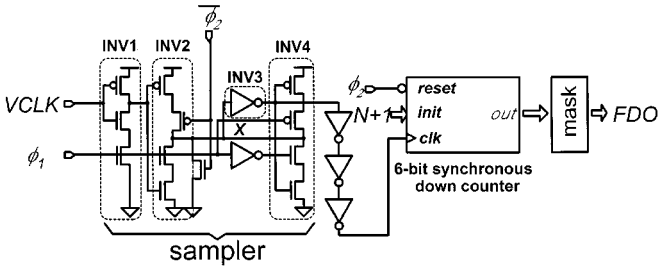

Fig. 7. DPFD implementation.

VCO needs to be reset for initial phase alignment with the reference clock at the start of every fundamental cycle, as is indicated by ϕ_2 in Fig. 6. After the full acquisition is complete, however, this reset step is not needed any more. In the following, we will go over the details of the critical functional blocks that compose our digital PLL.

A. DPFD

As explained in Section III, our DPFD measures the frequency difference by counting the number of the *VCLK* pulses during a period of *REF*. For this purpose, the DPFD is composed of a sampler and a 6-b synchronous downcounter as illustrated in Fig. 7. Basically, the sampler consists of two cascaded tristate inverters (INV1–INV2) to sample data with a single-phase clock and a switched latch (INV3–INV4) to prevent metastability caused by sampling asynchronous signal. Two cascaded tristate inverters (INV1–INV2) act as a simple noninverting buffer when ϕ_1 is high, but they cut off the path from the input *VCLK* to the node X when ϕ_1 is low. When ϕ_1 switches to low, a cross-coupled latch (INV3–INV4) is formed and drives the node X to either V_{DD} or *GND*, preventing the metastability. The input ϕ_2 in the sampler is used to set the initial condition of $X=0$.

When ϕ_2 is low, the downcounter is initialized to $N+1$ in order to cancel the effect of the first pulse edge, where N is a frequency multiplication factor, and then counts downward by the number of clock pulses transmitted from the sampler when ϕ_2 is high. This operation results in $N-M$ in case that the number of pulses enclosed in the *REF* period is M as mentioned above. The mask module in Fig. 7 forces the value of 0 to be the value of -1 on the phase acquisition mode, thereby two mutually exclusive values of -1 and 1 enable a successive approximation.

B. Gain Controller

Once the loop completes the frequency acquisition mode, it enters into the phase acquisition mode where the loop gain is halved every cycle in order to reduce the quantization error left over from the DPFD. To this end, a gain controller is designed to implement this successive approximation. The start of the phase acquisition mode is recognized by the time the output of the DPFD decreases to 1. The *lock indicator* signal in Fig. 5 also switches to 0 as the phase acquisition mode starts. The designed gain controller is a shift register, as shown in Fig. 8. Among the six output bits, $Gn\langle 5{:}0\rangle$, only a single bit is set to 1 and the index position of 1 from MSB tells us how many bits need

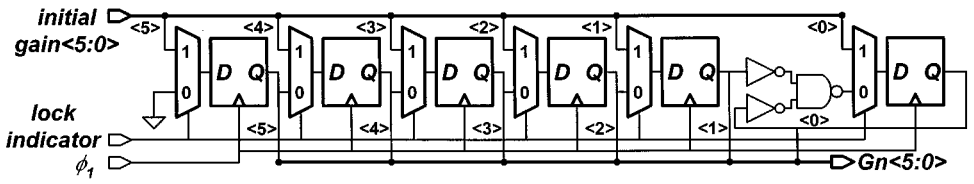

Fig. 8. Gain controller implementation.

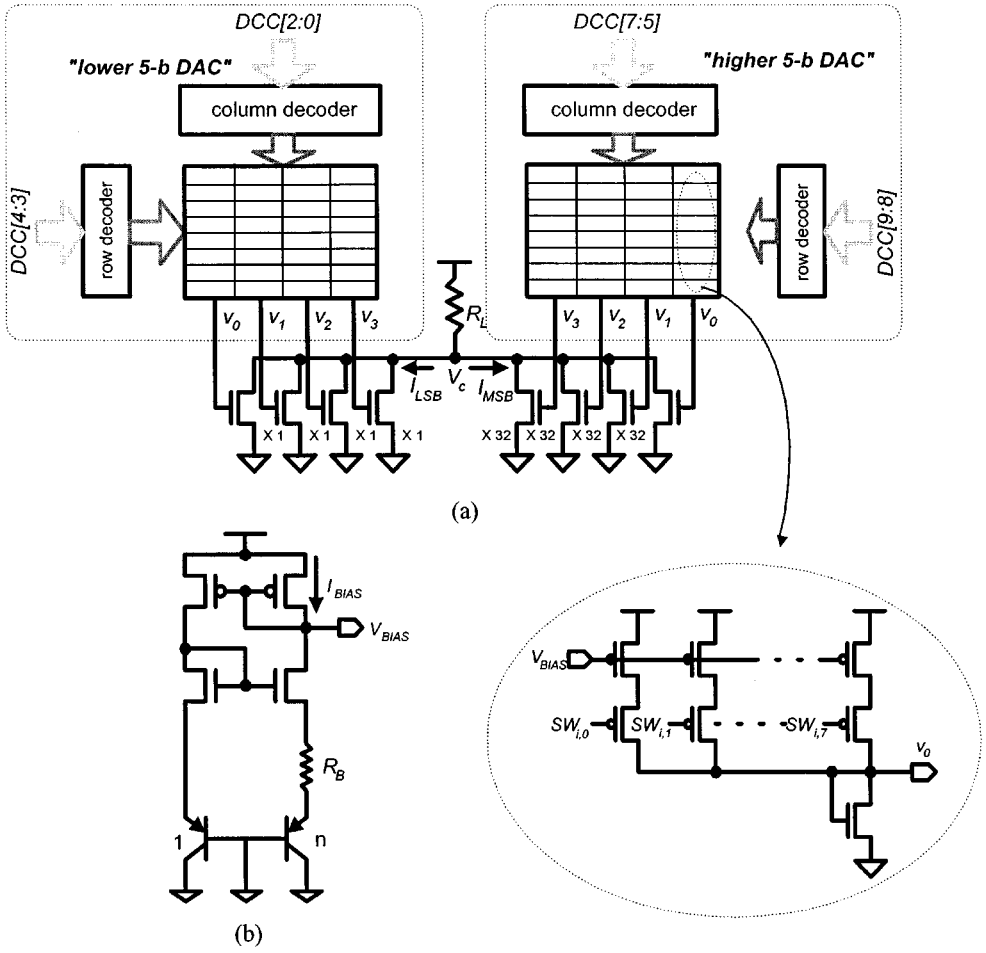

Fig. 9. DAC. (a) Overall block diagram. (b) Proportional to absolute temperature bias current generation circuit.

be shifted right in the barrel shifter. For example, if $Gn\langle 5{:}0\rangle$ is equal to 000100, the *FDO* value at the barrel shifter is totally shifted to the right by three bits, and thus executing an operation of divide by 2^3. When *lock indicator* is high (in the frequency acquisition mode), the gain controller passes *initial gain* $\langle 5{:}0\rangle$ to the output. When *lock indicator* goes to low (in the phase acquisition mode), it shifts the initial value to the right by one bit at the rising edge of ϕ_1. Once the bit with logic level 1 reaches the LSB position, it is circulated repeatedly from D to Q of the last flipflop. In this way, the PLL keeps the minimum loop gain after acquisition is completed.

C. Digital-to-Analog Converter

In digital design of PLL, a DAC is one of the crucial circuit blocks to determine the frequency resolution. In this design, linearity metrics such as integral nonlinearity (INL) and differential nonlinearity (DNL) are not important since nonlinearity is continuously corrected by the feedback loop, but high resolution and monotonicity are required for the fine frequency step in VCO and the wide lock range, respectively. The designed DAC incorporates two identical 5-b DACs in parallel to achieve 10-b resolution as in Fig. 9(a). Each 5-b DAC consists of 32 equally weighted current sources to maintain monotonicity, and eight current sources among these are grouped and connected to the nodes of v_0–v_3. The row and column decoders in each sub-DAC convert binary-coded words into the corresponding thermometer codes, $SW_{i,j}$.

Ten-bit resolution can be readily attainable since the current from the higher 5-b DAC, I_{MSB} is amplified 32 times that from the lower 5-b DAC, I_{LSB}. However, such an implementation to expand the dynamic range using the current amplification may give rise to problems such as discontinuities and code inversion,

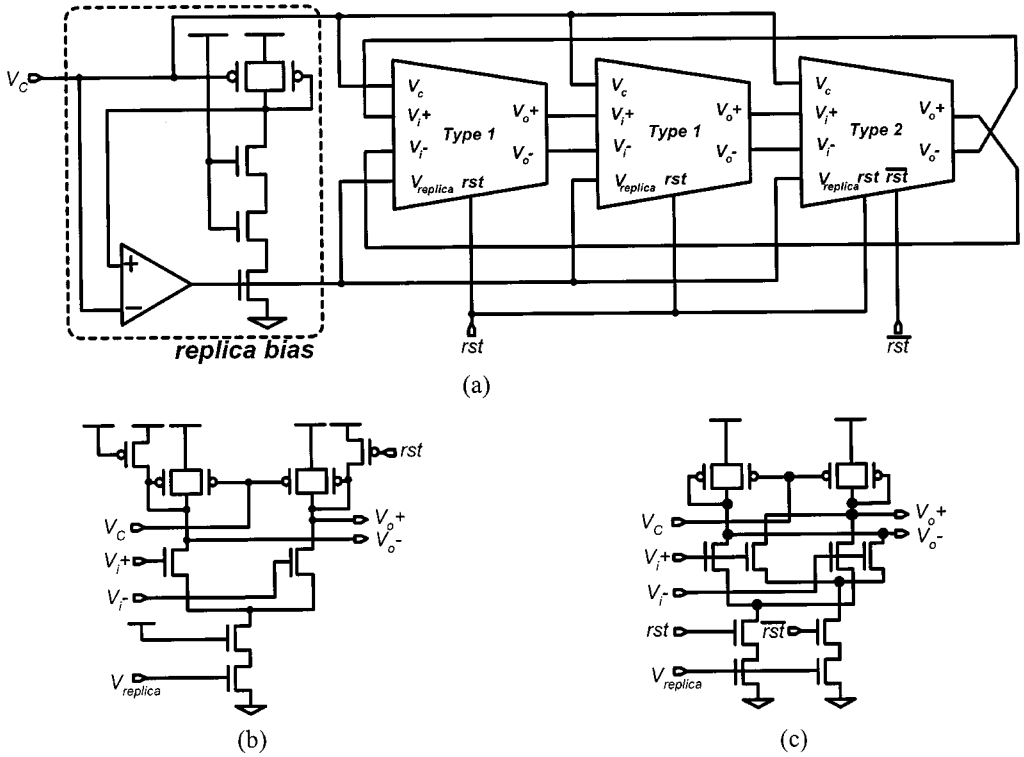

Fig. 10. Voltage-controlled oscillator. (a) Three-staged ring oscillator with a replica bias circuit. (b) Type-1 normal delay cell. (c) Type-2 delay cell with a phase-shifting function.

which result from the mismatch between the full range of the lower DAC and the 1-LSB range of the higher DAC. These problems, however, have little detrimental effect in this application since the input bits are determined sequentially from MSB to LSB.

The bias current I_{BIAS} used in each sub-DAC in common is generated from the bias circuit of Fig. 9(b). Although this current is determined as $V_T \ln(n)/R_B$ by an inaccurate passive resistor, the final output voltage of the DAC, V_C, is determined by the ratio, R_L/R_B, as in (9). Therefore, the variations that could occur on fabrication can be canceled out.

$$V_C \approx V_{DD} - V_T \cdot \ln(n) \cdot \frac{R_L}{R_B} \cdot \left(\sum_{i=0}^{9} DCC[i] \cdot 2^i \right). \quad (9)$$

D. Voltage-Controlled Oscillator

The VCO is a three-staged ring oscillator that consists of a couple of normal delay cells (Type-1) and one delay cell with a phase-shifting function (Type-2). For a resettable design, we employed the last delay cell of type-2. When *rst* is asserted to 0, the last cell is transformed from an inverting buffer to a noninverting buffer. Since the remaining first two delay cells are initialized with the same value, i.e., 1 at V_{o+} and 0 at V_{o-} and the total phase shift over the VCO becomes 360° at this condition, the VCO stops oscillating and keeps this status. Once *rst* returns to 1, the VCO resumes oscillating from this reset status. In this design, voltage swing of each delay cell is determined as $V_{DD} - V_C$ by the replica bias circuit. Every delay cell has a differential structure for an immunity to supply noises, as shown in Fig. 10(b) and (c).

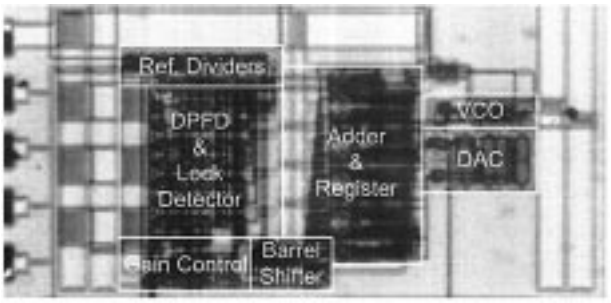

Fig. 11. Microphotograph of PLL.

V. Experimental Results

Fig. 11 shows the microphotograph of the chip, which occupies an active area of 0.83 mm^2. The measurements were taken while the chip was locked at 400 MHz (*VCLK* at 800 MHz) and 200 MHz (*VCLK* at 400 MHz) using 25 MHz *REF* clock with a 3.3-V supply voltage. In these experiments, the barrel shifter gain for unity loop gain was estimated to be 28.4 from the measured gain of VCO. Since the barrel shifter only provides gains with a power of 2, however, its initial gain was set to 32 which is the nearest power of two. Therefore, the resultant gain error is estimated to be 11.25%. In the case that a gain error exists as in this chip, the frequency acquisition time is affected by both the initial frequency difference and the magnitude of the gain error. The following criterion shows how the frequency acquisition time is determined.

$$\left| 1 - \frac{K_{\mathrm{real}}}{K_{\mathrm{ideal}}} \right|^n < \frac{f_{REF}}{\Delta f} \quad (10)$$

where n is the number of the iteration cycle, and Δf is the initial frequency difference. The number of iteration cycle n that

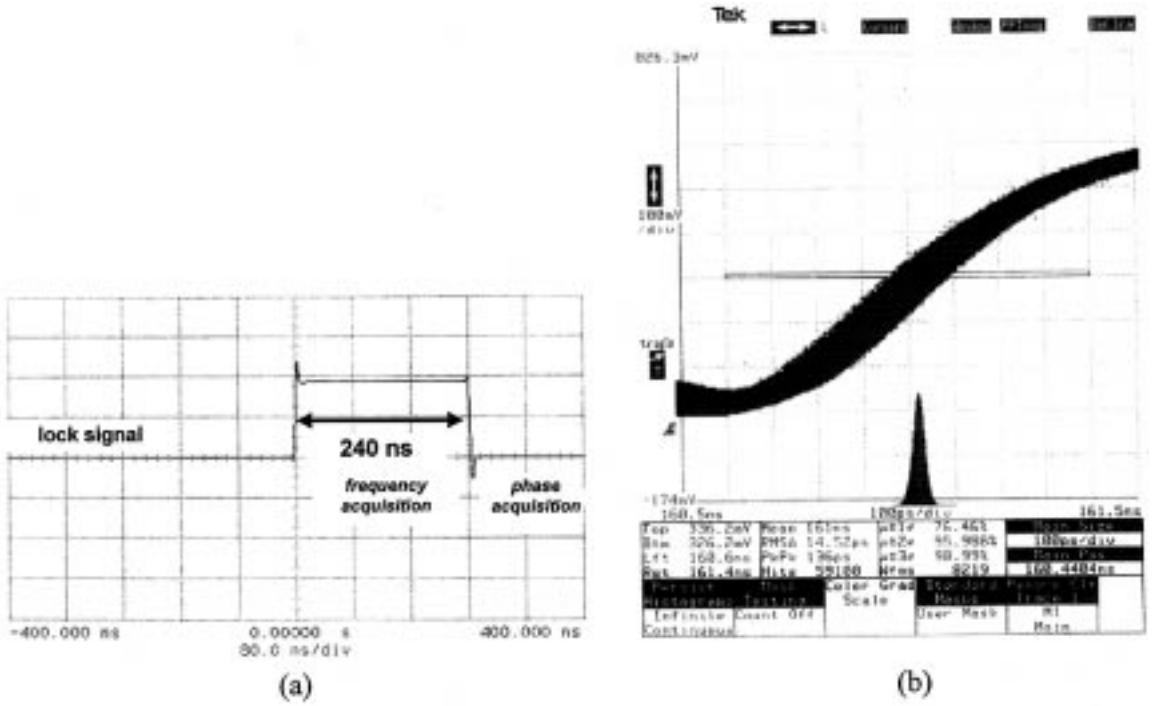

Fig. 12. Measurements at 400 MHz. (a) Frequency acquisition time. (b) Jitter histogram.

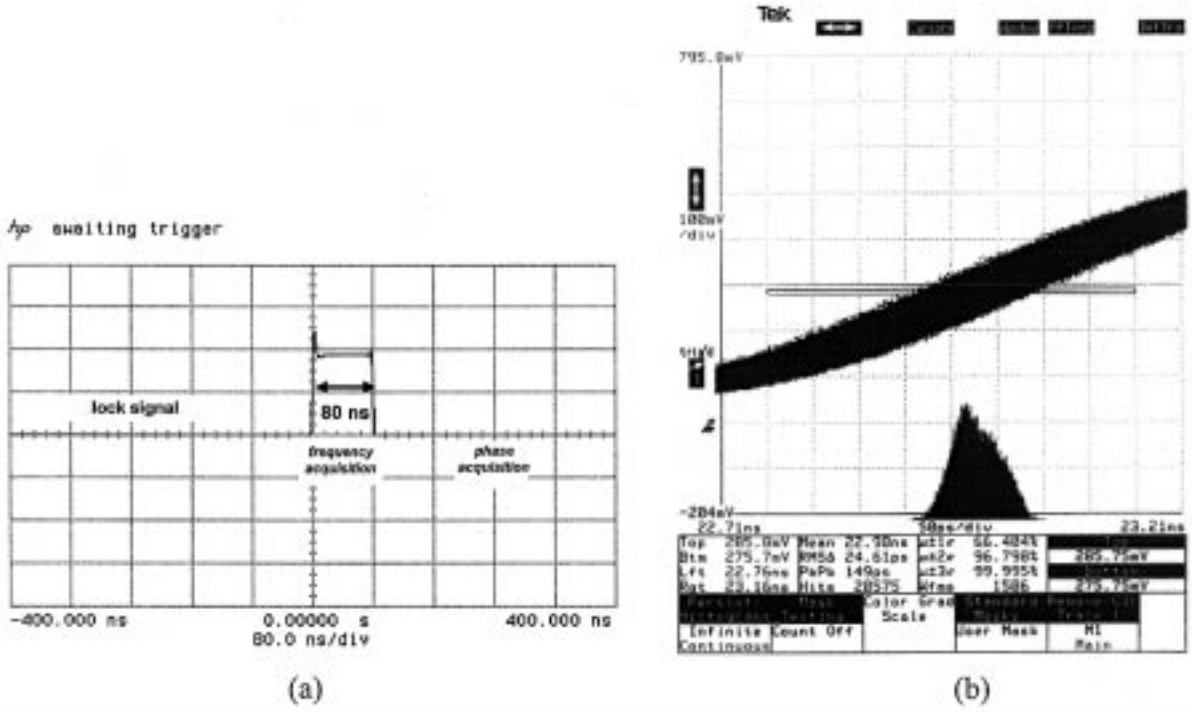

Fig. 13. Measurements at 200 MHz. (a) Frequency acquisition time. (b) Jitter histogram.

meets this criterion corresponds to the frequency acquisition time. Since the free-running frequency is about 302.4 MHz at this experiment, therefore, the frequency acquisition times are different from each other at these two locking conditions.

Fig. 12(a) shows the acquisition process at 400 MHz, which is represented as a encoded value (*lock*) that goes to "high" when the output of the DPFD is not equal to 1. From this plot, the frequency acquisition time is shown to be 240 ns, which corresponds to three cycles in terms of the fundamental clock cycle. The total acquisition time becomes eight cycles since the phase acquisition process additionally consumes five cycles starting from the initial barrel shifter gain of 32. Fig. 12(b) demonstrates jitter performance after acquisition. As can be seen here, this chip achieves a peak-to-peak jitter of 136 ps and a RMS jitter of 14.52 ps at 400 MHz. The power consumption is measured to be 105 mW.

Also, Fig. 13(a) shows the acquisition process at 200 MHz. In this figure, it can be seen that the frequency acquisition

TABLE I
PERFORMANCE SUMMARY FOR THE PROTOTYPE DCPLL

Process	1P3M 0.6 μm CMOS
Active area	0.83 mm^2
Supply Voltage	3.3 V
Power Dissipation	105 mW @ 400 MHz
VCO range	57.2 MHz – 934 MHz
Jitter	pk-pk : 136 ps @ 400 MHz
(cycle-to-cycle)	149 ps @ 200 MHz
	RMS : 14.52 ps @ 400 MHz
	24.61 ps @ 200 MHz
Acquisition time	16 reference cycles @ 400 MHz
	12 reference cycles @ 200 MHz

takes just one cycle since the initial frequency difference is so small compared to the case at 400 MHz. At this condition, the peak-to-peak jitter was measured to be 149 ps and the RMS jitter 24.61 ps, as shown in Fig. 13(b). Table I shows the summary of the performance of the chip.

VI. CONCLUSION

For an advanced clock synthesizer, a fast-locking digital phase-locked loop was designed and evaluated through the fabrication of a prototype chip in this work. For this purpose, the digital PFD that issues digital values corresponding to the frequency difference was developed. This DPFD was based on the principle that the frequency difference between the reference clock and the VCO clock can be measured by counting the number of the VCO pulses enclosed in one period of the reference clock. The DPFD enables the DCPLL to achieve fast acquisition independent of the free-running frequency of the VCO. Furthermore, our DCPLL inherits many benefits in the aspects of testability, flexibility, stability, and portability from the digital design.

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