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A Comprehensive Double-Vector Approach to Alleviate Common-Mode Voltage in Three-Phase Voltage-Source Inverters with a Predictive Control Algorithm

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Abstract: In this paper, a comprehensive double-vector approach is proposed to alleviate the common-mode voltage of voltage-source inverters based on a model predictive control scheme. Only six active vectors are selected to alleviate the common-mode voltage. Furthermore, one sampling period must be split to apply two non-zero vectors, which can generate currents with small current ripples and errors, despite not using zero vectors. The developed algorithm regards in full all 36 possible cases combined by two non-zero active vectors when selecting two vectors and splitting them into one sampling period. Thus, an optimal future set of two non-zero active vectors and optimal durations of two non-zero active vectors to produce the smallest current errors between the real currents and the reference in future load current trajectories were selected from 36 entire sets. This was done to minimize the cost function defined at the time when it varies from the first vector to the second vector and at the next sampling instant. Thus, the proposed algorithm can control the output currents with a fast transient response and reduce output-current ripples and errors, as well as alleviate the common-mode voltage to $\pm V_{dc}/6$.

Keywords: common-mode voltage; model predictive control; double vector; voltage-source inverter; current control

1. Introduction

Three-phase voltage-source inverters (VSIs) have been used commonly to generate three-phase line currents, while the frequencies and amplitude of the three-phase line currents are changeable [1,2]. In VSIs, the fast switching operation results in common-mode (CM) voltage, which has been considered the cause of over voltage stress to surrounding electronic systems [3–8]. To alleviate the amplitude of the CM voltage, multifarious studies have been conducted with a PWM algorithm that is designed by only selecting the non-zero active vectors, and this is because the zero vectors produce the highest CM voltage [3–8]. However, when the inverter is controlled by only using the non-zero active vectors without selecting the zero vectors, the Total Harmonic Distortion (THD) and error of the output currents of the inverter inevitably deteriorate. This is because zero vectors typically produce the smallest variation in the load dynamics. Therefore, methods for reducing the CM voltage without deteriorating the inverter performance have been studied extensively [9–16]. Recently, a model predictive control (MPC) method was studied for VSIs owing to its flexibility and simplicity of control [17–29]. Utilizing the basic principle that VSIs can apply two zero vectors and six different non-zero active voltage vectors to the load, seven different future current behaviors, which change according to the voltage vectors, can be predicted by the MPC method. The possible future currents of the VSI can be calculated using

the load dynamic model. Based on the cost function, which is predefined as the error between the reference currents and the predicted output currents, all predicted currents calculated by the seven different possible cases using the load dynamic model can be used to choose one voltage vector to minimize the predefined cost function. However, in the conventional MPC method which selects only one voltage vector during the sampling period, if only the active vector is used to reduce the CM voltage without using a zero vector which produces the highest CM voltage, the current error and current total harmonic distortion (THD) are inevitably higher than those of the method using PWM blocks. To overcome these problems, MPC methods using a double vector (DV) have been studied [8,17,18]. In this paper, there are two conventional DV-MPC algorithms, called DV-Conv1 and DV-Conv2. In the DV-Con1 method, two vectors closest to the reference are first selected, and then the sampling period is divided for minimizing the cost function [10]. In the DV-Con2 method, one vector closest to the reference vector is selected first, and the second vector is selected by dividing the sampling period to minimize the cost function [8,17,18]. However, such control methods have a disadvantage in that the calculation time is increased and if the conventional algorithm is operated with a half sampling period, selecting two vectors at one sampling period, for fair comparison, the current ripples and errors of the DV-Con1 and DV-Con2 methods are higher than those of the conventional method which selects one vector during one sampling period. Finally, the VSI using the MPC method applies the optimal voltage vector during each sampling period. Because of its simplicity, the MPC method has been used extensively to control the line current of many non-VSI converters, which are matrix converters, multiphase inverters, and multilevel inverters [19–30].

This paper proposes a comprehensive DV method to mitigate the CM voltage in VSIs based on the MPC scheme. Only six active vectors are utilized to control currents to alleviate the CM voltage in the proposed algorithm, because the zero vector makes the highest CM voltage. Therefore, the proposed algorithm can alleviate the CM voltage within $\pm V_{dc}/6$ except for the two zero vectors which make the CM voltage within $\pm V_{dc}/2$. Furthermore, the proposed algorithm uses two non-zero active vectors at one sampling period to compensate for the decreased number of candidates. The proposed algorithm selects two non-zero active vectors and divides them within one sampling period by considering all 36 possible combinations produced by the six non-zero active vectors to minimize the predefined cost function. This optimization process can minimize current ripples and errors. The proposed algorithm makes small current ripples and errors compared with the conventional algorithm despite not using zero vectors. The proposed algorithm also has a better control performance compared with the DV-Con1 method and DV-Con2 method because the proposed algorithm considers more cases than the two methods. Furthermore, as a solution to the computation time delay, the delay compensation technique was used in the proposed algorithm. In addition, the zero vectors are not selected in the normal transient condition, therefore the proposed algorithm does not adversely affect the fast transient response. To verify the proposed algorithm, simulation and experiment were performed.

2. Conventional Model Predictive Current Control Method for VSIs

Figure 1 shows the three-phase VSI, where the voltage vector applied to the load can be denoted as

$$v = \frac{2}{3}\left(v_{an} + v_{bn}e^{j\left(\frac{2\pi}{3}\right)} + v_{cn}e^{j\left(\frac{4\pi}{3}\right)}\right). \tag{1}$$

Figure 2 shows the eight voltage vectors that can be produced by VSIs. VSI can control the output currents by using voltage vectors [10,12]. The binary values of "0" and "1" in the switching functions indicate the open and closed states, respectively. Using the space-vector definition, the load current can be denoted as

$$i = \frac{2}{3}\left(i_a + i_b e^{j\left(\frac{2\pi}{3}\right)} + i_c e^{j\left(\frac{4\pi}{3}\right)}\right). \tag{2}$$
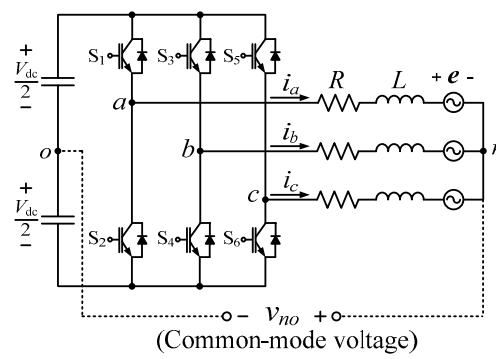
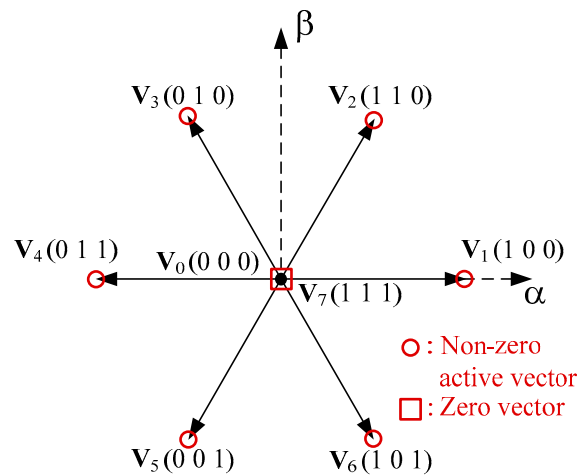**Figure 1.** Three-phase voltage-source inverter (VSI).

Figure 2. Vectors generated by the VSI.

In addition, as shown in Figure 1, the CM voltage of the VSI can be defined as the potential between the center of the dc bus and the neutral point n of the VSI. The CM voltage can be denoted as [10]

$$v_{no} = \frac{v_{a0} + v_{b0} + v_{c0}}{3}. \tag{3}$$

The CM voltages of the VSIs becomes $\pm V_{dc}/2$ for the zero vectors and $\pm V_{dc}/6$ for the non-zero active vectors, as listed in Table 1.

Table 1. All voltage vectors of the voltage-source inverter (VSI) and common-mode (CM) voltages according to voltage vectors.

Voltage Vector		CM Voltage (v_{no})
	V_1	$-V_{dc}/6$
	V_2	$V_{dc}/6$
	V_3	$-V_{dc}/6$
Non-zero active vectors	V_4	$V_{dc}/6$
	V_5	$-V_{dc}/6$
	V_6	$V_{dc}/6$
Zero vectors	V_0	$-V_{dc}/2$
	V_7	$V_{dc}/2$

In the VSIs, the output current dynamics can be obtained as

$$v = Ri + L\frac{di}{dt} + e, \tag{4}$$

where v, R, i, L, and e represent the voltage vector, output resistance, output current vector, output inductance, and back-emf vector, respectively. Using the forward Euler approximation, the differential of the output current vector in (2) can be described in the discrete-time domain with sampling period T_s as

$$\frac{di}{dt} \approx \frac{i((k+1)T_s) - i(kT_s)}{T_s}.$$ (5)

In the discrete-time domain, the load current can be described as

$$i((k+1)T_s) = i(kT_s) + \frac{T_s}{L}\left[v^k - Ri(kT_s) - e(kT_s)\right].$$ (6)

Seven possible voltage vectors of the VSI, v^k, generate seven possible output currents, and using (6), the future currents at the $(k+1)^{\text{th}}$ step can be obtained. Among seven possible output currents, one optimal future load current can be calculated and selected to minimize the cost function, which is predefined as the errors between the real output currents and the reference output currents at every sampling period.

Only six non-zero active vectors which generate the CM voltage within $\pm V_{dc}/6$ are considered in the proposed algorithm to alleviate the CM voltage, not using the zero vectors which generate CM voltage within $\pm V_{dc}/2$, as indicated in Table 1. However, applying the six non-zero active vectors may worsen the three-phase output current errors and ripples because the number of available voltage vectors is reduced. It is inevitable that the current ripple is increased when the proposed algorithm controls the load current, except when the zero vectors are used, as the zero vectors typically produce the smallest variation in the load dynamics. Therefore, in one sampling period, two non-zero active vectors are used to compensate for the decreased number of candidates. The selection of two non-zero active vectors and splitting two vectors at one sampling period are determined by the proposed optimization process and updated at every sampling period. Two non-zero active vectors are selected for application to the load at every sampling period. Therefore, one sampling period can be split into two parts as

$$T_1^k + T_2^k = T_s,$$ (7)

where T_1^k and T_2^k are the time intervals of applying non-zero active vectors v_1^k and v_2^k to the load, respectively, at the kth step. Time intervals, T_1^k and T_2^k, should be smaller than the sampling period T_s and larger than zero. Selecting two non-zero active vectors with changeable time intervals can lead to reduced output-current errors, output-current ripples, and CM voltage. Furthermore, optimal time intervals are determined at every sampling period. The load current at the $(k+1)^{\text{th}}$ step generated by utilizing two non-zero active vectors can be modified from (6) as

$$i((k+1)T_s) = i(kT_s) + \frac{T_s^k}{L}\left[v_1^k - Ri(kT_s) - e(kT_s)\right] + \frac{T_2^k}{L}\left[v_2^k - Ri\left(kT_s + T_1^k\right) - e\left(kT_s + T_1^k\right)\right].$$ (8)

Back-emf vectors vary at much lower frequencies than sampling frequencies; therefore, at one sampling period, the back-emf vector can be presumed as

$$e(kT_s) \approx e\left(kT_s + T_1^k\right).$$ (9)

Similar to (9), by shifting (9) one step backward, the past back-emf vector at the $(k-1)^{\text{th}}$ step can be obtained as

$$e(kT_s) \approx \hat{e}((k-1)T_s) =$$

$$\frac{T_1^{k-1}}{T_s}\left[v_1^{k-1} - Ri((k-1)T_s)\right] + T_2^{k-1}\left[v_2^{k-1} - Ri\left((k-1)T_s + T_1^{k-1}\right)\right] - \frac{L}{T_s}[i(kT_s) - ((k-1)T_s)].$$ (10)

As in the conventional method of selecting a single optimal vector, the two-step prediction is required for delay compensation technique for the calculation delay. Shifting (8) one step forward, the delay compensation technique can be attained [9] as

$$
\begin{aligned}
\boldsymbol{i}((k+2)T_s) = \boldsymbol{i}((k+1)T_s) + \frac{T_1^{k+1}}{L}\left[\boldsymbol{v}_1^{k+1} - R\boldsymbol{i}((k+1)T_s) - \boldsymbol{e}((k+1)T_s)\right] \\
+ \frac{T_2^{k+1}}{L}\left[\boldsymbol{v}_2^{k+1} - R\boldsymbol{i}\left((k+1)T_s + T_1^{k+1}\right) - \boldsymbol{e}\left((k+1)T_s + v_1^{k+1}\right)\right].
\end{aligned}
\tag{11}
$$

The future back-emf voltage vector at the $(k+1)^{\text{th}}$ step used in (11) can be obtained as

$$
\boldsymbol{e}((k+1)T_s) \approx \hat{\boldsymbol{e}}(kT_s) = \frac{T_1^k}{T_s}\left[\boldsymbol{v}_1^k - R\boldsymbol{i}(kT_s)\right] + \frac{T_2^k}{T_s}\left[\boldsymbol{v}_2^k - R\boldsymbol{i}\left(kT_s + T_1^{k-1}\right)\right] - \frac{L}{T_s}\left[\boldsymbol{i}((k+1)T_s - \boldsymbol{i}(kT_s)\right].
\tag{12}
$$

Future non-zero active vectors used in (11), $\boldsymbol{v}_1^{k+1}$ and $\boldsymbol{v}_2^{k+1}$, can assume six non-zero active vectors made by the VSI, respectively. Thus, 36 possible non-zero active vector sets can be made. Therefore, the proposed algorithm can completely achieve optimal current control considering the effectiveness of two non-zero active vectors used during one sampling period and their time intervals. As a result, the proposed algorithm can be regarded as a comprehensive DV approach to alleviate the CM voltage.

The proposed scheme estimates the reference output currents and real output currents not only at the next sampling period, but also at the changing time of two active vectors. The changing time of two active vectors changes depending on each non-zero active vector set. The proposed algorithm selects one optimal vector set among the 36 possible non-zero active vector sets to minimize the cost function, which is defined as the square errors between the reference output current and real output current at two intervals, of which one is fixed and and the other is changing, as

$$
\begin{aligned}
G = \{i_\alpha^* ((k+2)T_s - i_\alpha((k+2)T_s)\}^2 + \{i_\beta^*((k+2)T_s - i_\beta((k+2)T_s)\}^2 \\
+ \{i_\alpha^*\left((k+1)T_s + T_1^{k+1}\right) - i_\alpha\left((k+1)T_s + T_1^{k+1}\right)\}^2 + \left\{i_\beta^*\left((k+1)T_s + T_1^{k+1}\right) - i_\beta\left((k+1)T_s + T_1^{k+1}\right)\right\}^2.
\end{aligned}
\tag{13}
$$

For each non-zero active vector set, the duration of the two vectors, $\boldsymbol{v}_1^{k+1}$ and $\boldsymbol{v}_2^{k+1}$, applied at T_1^{k+1} and T_2^{k+1} is determined by optimizing each set. The optimal time intervals, T_1^{k+1} and T_2^{k+1}, are divided at the future sampling period for minimizing the square errors between the reference output current and the real output current. The optimal duration can be obtained as

$$
\frac{\partial G}{\partial T_1^{k+1}} = 0.
\tag{14}
$$

By reflecting on Equations (11), (13), (17), and (18) to (14), the future optimal time interval T_1^{k+1} can be obtained by using (15) as

$$
T_1^{k+1} = \frac{A_\alpha[LC_{2\alpha} + T_s(A_\alpha - B_\alpha)] + A_\beta[LC_{2\beta} + T_s(A_\beta - B_\beta)]}{(A_\alpha)^2 + (A_\beta)^2 + \left(\frac{L}{T_s}I_{d\alpha}^* - B_\alpha\right)^2 + \left(\frac{L}{T_s}I_{d\beta}^* - B_\beta\right)^2} - \frac{L\left\{C_{1\alpha}\left(\frac{L}{T_s}I_{d\alpha}^* - B_\alpha\right) + C_{1\beta}\left(\frac{L}{T_s}I_{d\beta}^* - B_\beta\right)\right\}}{(A_\alpha)^2 + (A_\beta)^2 + \left(\frac{L}{T_s}I_{d\alpha}^* - B_\alpha\right)^2 + \left(\frac{L}{T_s}I_{d\beta}^* - B_\beta\right)^2},
\tag{15}
$$

where $A_m = v_{1m}^{k+1} - v_{2m}^{k+1}$,
$\quad B_m = v_{1m}^{k+1} - Ri_m((k+1)T_s) - \hat{e}_m(kT_s)$,
$\quad C_{1m} = i_m^*((k+1)T_s) - i_m((k+1)T_s)$,
$\quad C_{2m} = i_m^*((k+2)T_s) - i_m((k+1)T_s)$,
$\quad I_{dm}^* = i_m^*((k+2)T_s) - i_m^*((k+1)T_s)$, and $m = \alpha,\ \beta$.
The remaining duration T_2^{k+1} for vector $\boldsymbol{v}_2^{k+1}$ can be calculated from (7) as

$$
T_2^{k+1} = T_s - T_1^{k+1}.
\tag{16}
$$

To compare the reference output currents and real load current at time, $t = (k+1)T_s + T_1^{k+1}$, of the transition from the first vector to the second, the references at time $t = (k+1)T_s + T_1^{k+1}$ are also required. Therefore, the reference load current at time $t = (k+1)T_s + T_1^{k+1}$ can be calculated as

$$i^*\Big((k+1)T_s + T_1^{k+1}\Big) = i^*((k+1)T_s) + \frac{T_1^{k+1}}{T_s}\{i^*((k+2)T_s) - i^*((k+1)T_s)\}. \tag{17}$$

Therefore, the reference output current $i^*\Big((k+1)T_s + T_1^{k+1}\Big)$ can be attained for each voltage vector set once the time interval of the former non-zero active vector in each set T_1^{k+1} is computed in (15). Similarly, the real output currents at turning time $t = (k+1)T_s + T_1^{k+1}$ can be expressed as

$$i\Big((k+1)T_s + T_1^{k+1}\Big) = i((k+1)T_s) + \frac{T_1^{k+1}}{L}[v_1^{k+1} - Ri((k+1)T_s - e((k+1)T_s)]. \tag{18}$$

After evaluating 36 possible voltage vector sets and the time distribution to minimize the cost function, one optimal future non-zero active set and their optimal durations can be selected. The two future active vectors, v_1^{k+1} and v_2^{k+1}, selected in the proposed scheme, are attained during the pre-selected durations T_1^{k+1} and T_2^{k+1} in the future sampling period. Examples of the output-current behaviors determined by voltage vectors generated by the proposed algorithm are shown in Figure 3. As shown in Figure 3, the final value of the output current depends on the voltage vector to be selected and the time intervals to be divided. The control block of the proposed algorithm is shown in Figure 4. The optimal control process for the proposed algorithm at the kth sampling period is attained with the following steps:
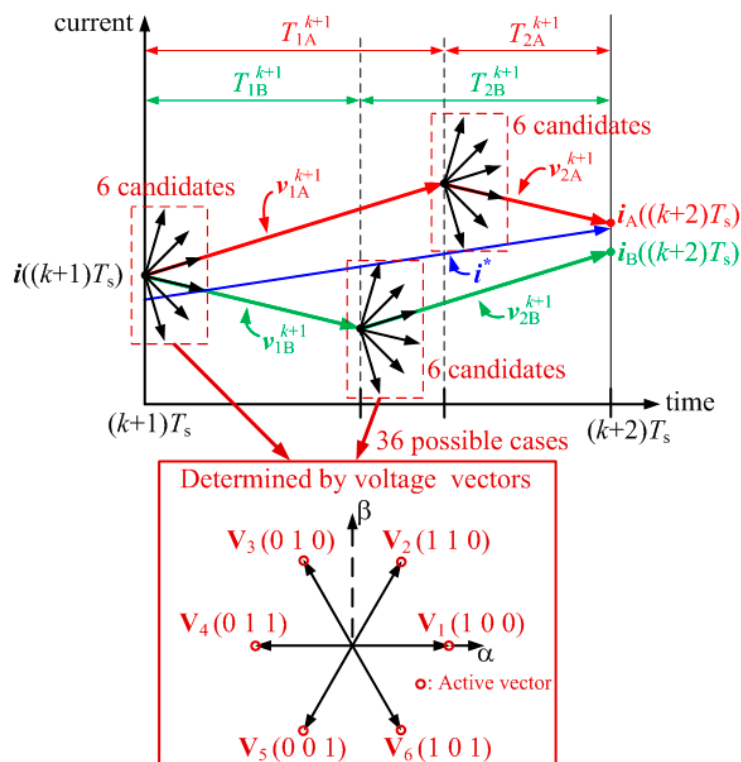

Figure 3. Examples of output-current behaviors determined by voltage vectors generated by the proposed algorithm.
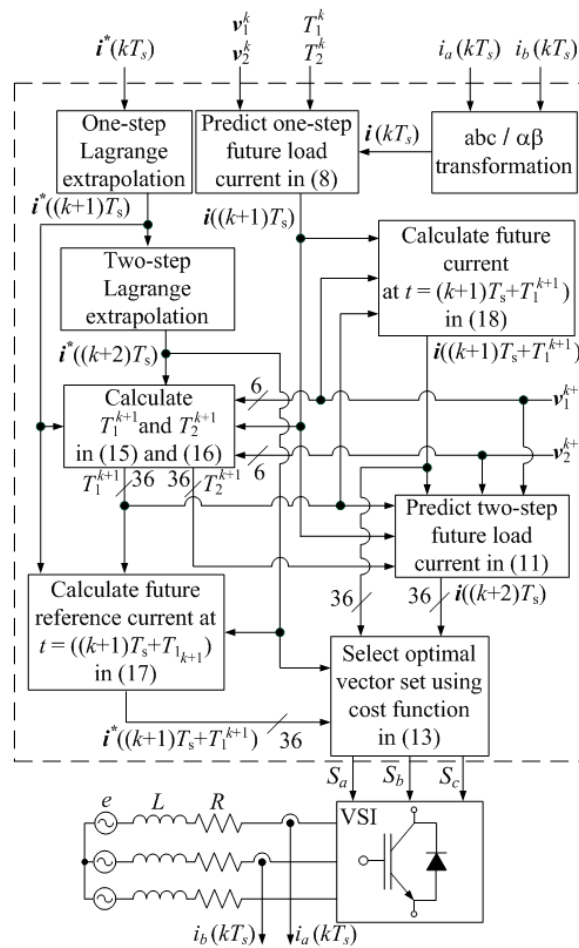
Figure 4. Control block of the proposed algorithm.

(1) Measuring output current $i(kT_s)$ at the kth step,

(2) Predicting the future output current $i((k+1)T_s)$ by applying the two nonzero active vectors v_1^k and v_2^k during T_1^k and T_2^k, respectively, which were fixed at the $(k-1)^{\text{th}}$ step by (8),

(3) Predicting the 36 possibilities for future currents $i((k+2)T_s)$ and $i\big((k+1)T_s + T_1^{k+1}\big)$ obtained by 36 possible voltage sets with non-zero vectors v_1^{k+1} and v_2^{k+1} along with their corresponding durations T_1^{k+1} and T_2^{k+1} obtained by (15) and (16),

(4) Calculating the future reference $i^*((k+2)T_s)$ and $i^*\big((k+1)T_s + T_1^{k+1}\big)$ using Lagrange extrapolation and (17), respectively,

(5) Evaluating 36 vector sets, v_1^{k+1} and v_2^{k+1}, and their corresponding durations, T_1^{k+1} and T_2^{k+1}, by utilizing the cost function in (13),

(6) Selecting one optimal set with v_1^{k+1} and v_2^{k+1} with their durations T_1^{k+1} and T_2^{k+1},

(7) Storing v_1^{k+1}, v_2^{k+1}, T_1^{k+1} and T_2^{k+1} for the $(k+1)^{\text{th}}$ step.

3. Simulation Results

To verify the proposed algorithm which only selects the non-zero active vectors, simulations were performed using the PSIM (power simulation) program. For comparing the performance between the proposed and conventional schemes, the simulations of the conventional method selecting one optimal voltage vector from seven different candidate vectors were also performed. The parameters are as follows: input voltage $V_{dc} = 100$ V, the amplitude of the reference $I^* = 6$ A, output inductance $L = 10$ mH, output resistance $R = 2.5$ Ω and back-emf voltage $e = 20$ V. In addition, the proposed

algorithm is operated with a sampling period T_s = 200 μs and the conventional algorithm is operated with a half sampling period, selecting two vectors at one sampling period, for fair comparison.

Figures 5 and 6 show the simulation results acquired from the proposed and conventional algorithm, respectively. The three-phase output currents of both control method are well controlled with the sinusoidal waveforms of the amplitude I^* = 6 A as shown in Figure 5a,b. Moreover, it is observed that the CM voltage of the proposed algorithm is limited to $\pm V_{dc}/6$, whereas that of the conventional method oscillates between $-V_{dc}/2$ and $V_{dc}/2$. Figures 5b and 6b show the fast Fourier transform (FFT) spectrum of a phase output current. As shown in the figures, the proposed algorithm shows much lower harmonic components than the conventional algorithm which is operated with a half sampling frequency despite no utilization of zero vectors. This is because the optimization algorithm selects two non-zero vectors and determines their durations. Therefore, the waveforms of the proposed scheme achieve improved quality compared with those of the conventional method that operates within a half sampling period.
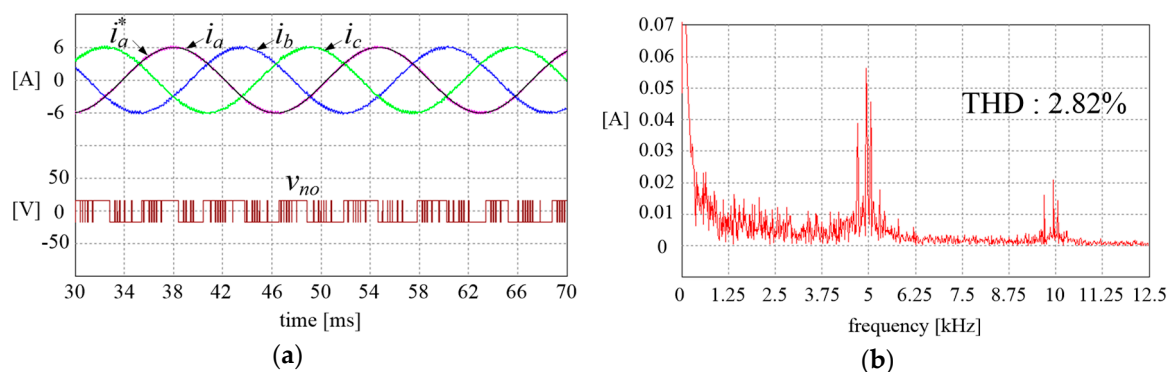

Figure 5. Simulation results acquired from the proposed algorithm with T_s = 200 μs: (**a**) the three-phase output currents (i_a, i_b, and i_c), a phase reference (i_a^*), and CM voltage (v_{no}) (**b**) Fourier transform (FFT) spectrum of the a aphase output current.
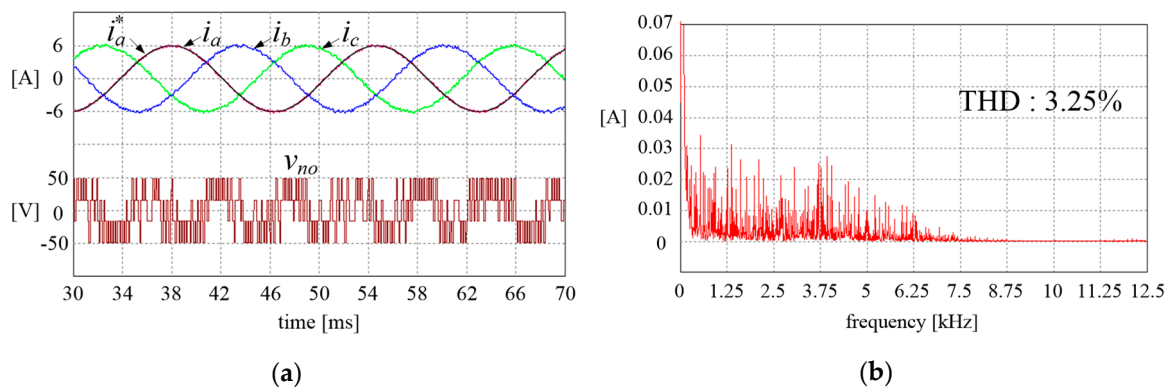

Figure 6. Simulation results acquired from the conventional algorithm with T_s = 100 μs: (**a**) the three-phase output currents (i_a, i_b, and i_c), a phase reference (i_a^*), and CM voltage (v_{no}) (**b**) FFT spectrum of the a phase output current.

Figure 7 shows the dynamic response of a fundamental frequency step change acquired from the conventional and proposed algorithm. The conventional and proposed algorithms are operated with the sampling period T_s = 100 μs and T_s = 200 μs, respectively. In Figure 7, the fundamental frequency varied from 60 Hz to 90 Hz. The proposed algorithm can change the fundamental frequency of the currents at the same speed as the conventional algorithm as shown in Figure 7.
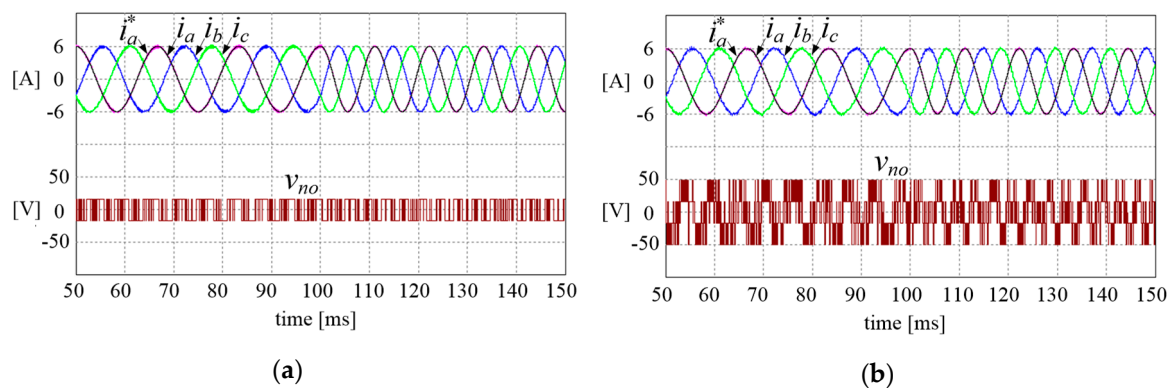
Figure 7. Three-phase output currents (i_a, i_b, and i_c), *a* phase reference output current (i_a^*), and CM voltage (v_{no}) for a fundamental frequency step change from 60 Hz to 90 Hz obtained from (**a**) the proposed algorithm with $T_s = 200$ μs (**b**) the conventional algorithm with $T_s = 100$ μs.

The dynamic response of an amplitude step change acquired from the conventional and proposed algorithm is shown in Figure 8. The conventional and proposed algorithms are operated with the sampling period $T_s = 100$ μs and $T_s = 200$ μs, respectively. In Figure 8, the amplitude of the reference varied from 9 A to 4.5 A. The three-phase output currents of the proposed scheme change as rapidly as the three-phase output currents of the conventional scheme as shown in Figure 8.
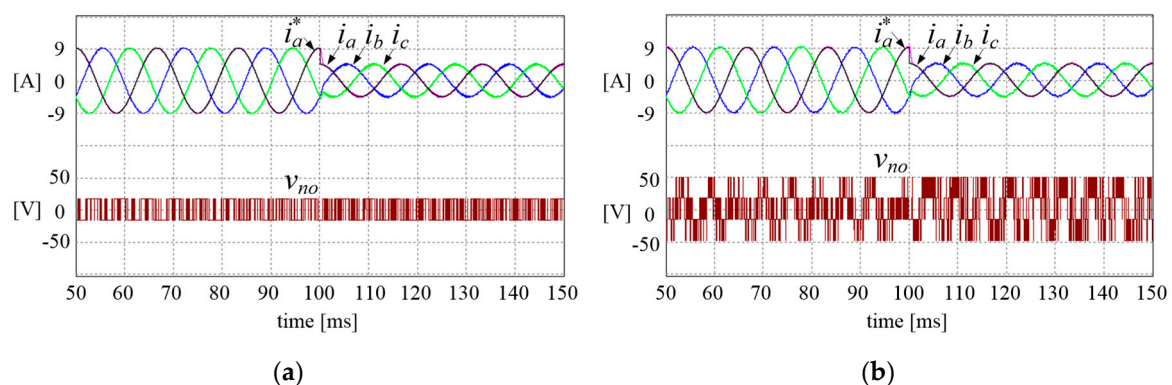

Figure 8. Three-phase output currents (i_a, i_b, and i_c), *a* phase reference output current (i_a^*), and CM voltage (v_{no}) for a amplitude step change obtained from 9 A to 4.5 A (**a**) the proposed algorithm with $T_s = 200$ μs (**b**) the conventional algorithm with $T_s = 100$ μs.

Because the performance of the MPC method is affected by the sampling period, the performance comparison of the four control methods which are the proposed, the conventional, DV-Con1, and DV-Con2 MPC methods from the perspective of the output-current ripples and errors versus sampling periods were added in this paper as shown in Figure 9. The DV-Con1 method and the DV-Con2 method only select non-zero active vectors like the proposed algorithm for reducing CM voltage. The output current errors attained by the conventional, DV-Con1, DV-Con2, and proposed schemes are shown in Figure 9a. The output current errors can be defined as

$$error(i_x) = \sum_{x=a,\,b,\,c} \frac{1}{N} \sum_{k=1}^{N} \left| i_x^*(k) - i_x(k) \right|, \tag{19}$$

where the value of N was 20,000. The proposed algorithm shows lower output current error than the conventional algorithm as shown in Figure 9a. Furthermore, the current error of the proposed algorithm also shows significantly lower than those of DV-Con1 and DV-Con2 methods. Figure 9b shows the average THD percentages of output currents attained by the proposed, conventional,

DV-Con1, and DV-Con2 methods. The average THD percentages of the three-phase currents can be defined as

$$\%\text{THD} = \frac{\sum_{x=a,\,b,\,c}\sqrt{i_{x2}^2 + i_{x3}^2 + \dots + i_{xn}^2}}{\sum_{x=a,\,b,c} i_{x1}} \times 100, \tag{20}$$

where i_{x1} is the fundamental component of the output currents and i_{xn} is the nth-harmonic component in the x phase. The value of n was set to 8335 in the PSIM. Figure 9b shows that the THD of the proposed algorithm is much lower than that of the conventional algorithm using a half sampling period. The proposed algorithm also shows lower THD than the DV-Con1 and DV-Con2 methods using the same sampling period.
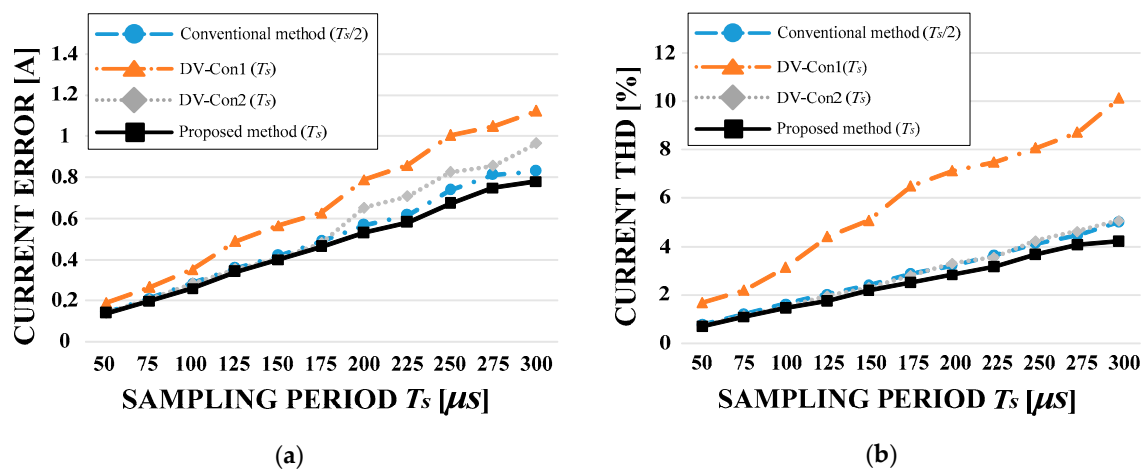
Figure 9. Comparative results of the conventional, the DV-Con1, the DV-Con2 and the proposed algorithms versus the sampling period: (**a**) output-current errors, (**b**) total harmonic distortion (THD) of the output currents.

4. Experimental Results

A prototype setup was used to test the proposed algorithm to operate with the comprehensive DV approach and implemented in a digital signal processing (DSP) board (TMS320F28335). The proposed algorithm was operated with the sampling period $T_s = 200$ μs, input dc voltage $V_{dc} = 100$ V and the amplitude of the reference $I^* = 6$ A. For performance comparison, the conventional algorithm was operated with the sampling period $T_s = 100$ μs which is a half sampling period of the proposed algorithm. The input dc voltage and the amplitude of the reference of the conventional algorithm are the same as those of the proposed algorithm.

Figures 10 and 11 show the experimental results acquired from two control methods. The waveforms acquired from the proposed algorithm, shown in Figure 10, are similar to those of the simulation results, shown in Figure 5. The three-phase output currents of the proposed algorithm are well controlled with a sinusoidal wave, and the CM voltage v_{no} is limited to $\pm V_{dc}/6$ because the proposed algorithm does not select the zero vectors. Otherwise, in the conventional method, the CM voltage oscillates from $-V_{dc}/2$ to $V_{dc}/2$, as shown in Figure 11a, because both the zero vectors $\mathbf{V}_0$ and $\mathbf{V}_7$ are used in the conventional algorithm. Figures 10b and 11b show the FFT spectrum of the a phase current acquired from the proposed and conventional algorithm, respectively. The harmonic components of the proposed scheme are much less than that of the conventional scheme with a half sampling period as shown in Figures 10 and 11. The THD and FFT spectrum of the output currents were measured from the MSO (mixed signal oscilloscope) 3054. The technical characteristics of the digital oscilloscope are shown in Table 2.
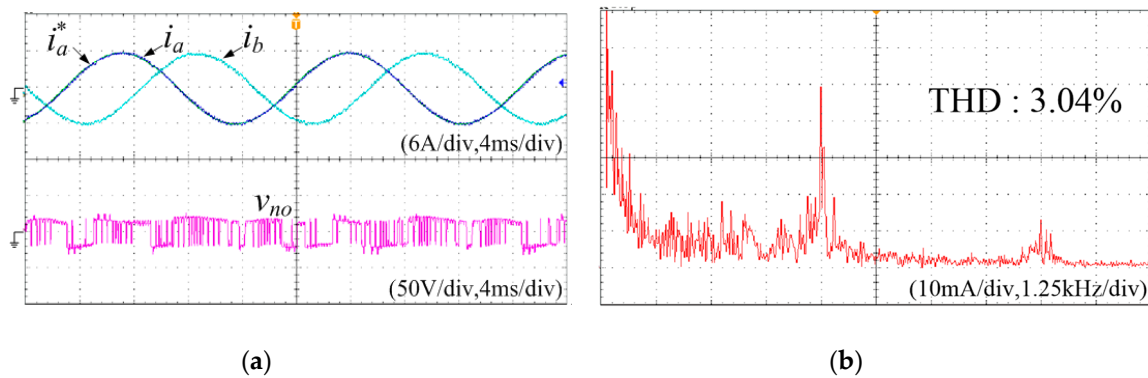
(a)

(b)

Figure 10. Experimental results of the proposed algorithm with $T_s = 200$ μs: (**a**) the output currents (i_a, i_b, and i_c), a phase reference (i_a^*), and CM voltage (v_{no}) (**b**) FFT spectrum of the a phase output current ($i^* = 6$ A and $V_{dc} = 100$ V).
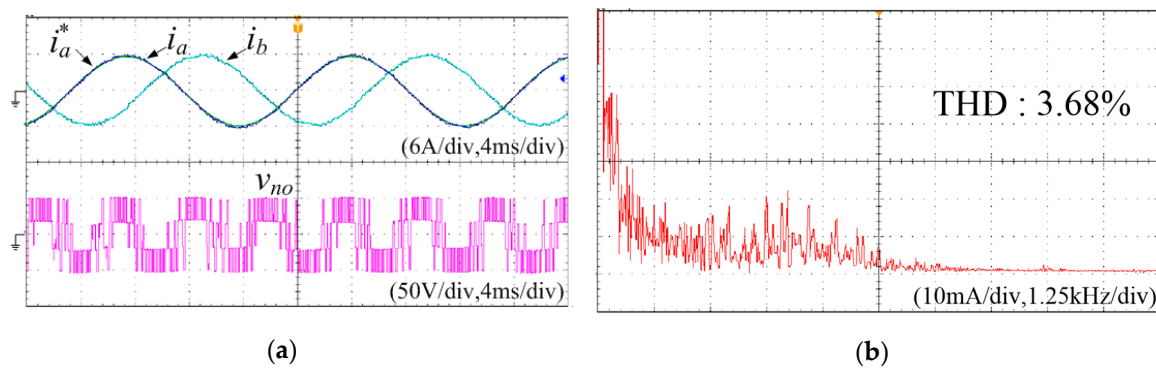

(a)

(b)

Figure 11. Experimental results of the conventional algorithm with a half sampling period ($T_s = 100$ μs): (**a**) the output currents (i_a, i_b, and i_c), a phase reference (i_a^*), and CM voltage (v_{no}), (**b**) FFT spectrum of the a phase output current ($i^* = 6$ A and $V_{dc} = 100$ V).

Table 2. The technical characteristics of the MSO (mixed signal oscilloscope) 3054.

Input Channels	4	Analog Bandwidth (-3 db)	500 MHz
Calculated rise time 5 mV/div (typical)	700 ps	Hardware bandwidth limits	20 MHz
Maximum sample rate (all channels)	2.5 GS/s	Maximum record length (all channels)	5 M points
Maximum input voltage, 1 MΩ	300 V$_{RMS}$ with peaks ≤ ± 450 V	Maximum input voltage, 75 Ω, 50 Ω	50 V$_{RMS}$ with peaks ≤ ± 20 V

Figure 12 shows the experimental waveforms of the dynamic responses of a fundamental frequency step change obtained from the conventional and proposed algorithm. The conventional and proposed algorithms are operated with the sampling period $T_s = 100$ μs and $T_s = 200$ μs, respectively. In Figure 12, the fundamental frequency of the reference varied from 60 Hz to 90 Hz. The proposed algorithm can change the fundamental frequency of the three-phase output currents at the same speed as the conventional algorithm as shown in Figure 12.
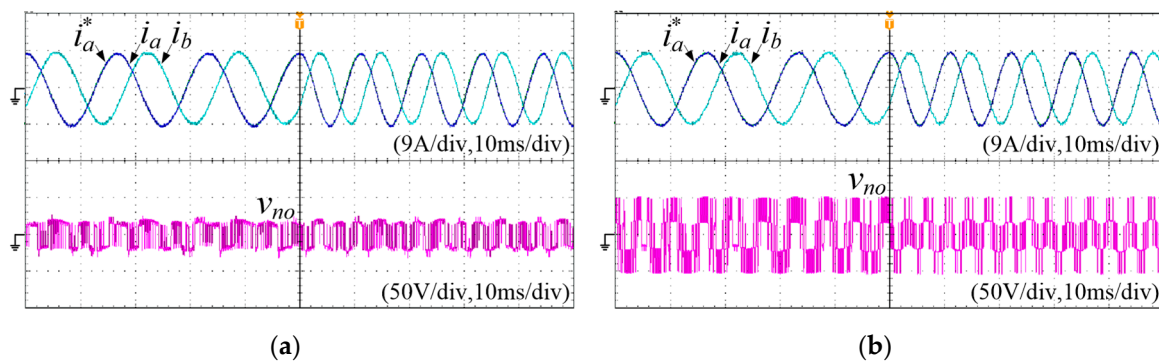
Figure 12. Experimental results of the output currents (i_a and i_b), a phase reference (i_a^*), and the CM voltage (v_{no}) for a fundamental frequency step change from 60 Hz to 90 Hz for (**a**) the proposed algorithm with T_s = 200 μs, (**b**) the conventional algorithm with T_s = 100 μs.

The experimental waveforms of the dynamic responses of an amplitude step change acquired from the conventional and the proposed algorithm are shown in Figure 13. The conventional and the proposed algorithms are operated with the sampling period T_s = 100 μs and T_s = 200 μs, respectively. In Figure 13, the magnitude of the reference varied from 9 A to 4.5 A. As shown in Figure 13, the proposed algorithm can change the amplitude of three-phase output currents at the same speed as the conventional algorithm.
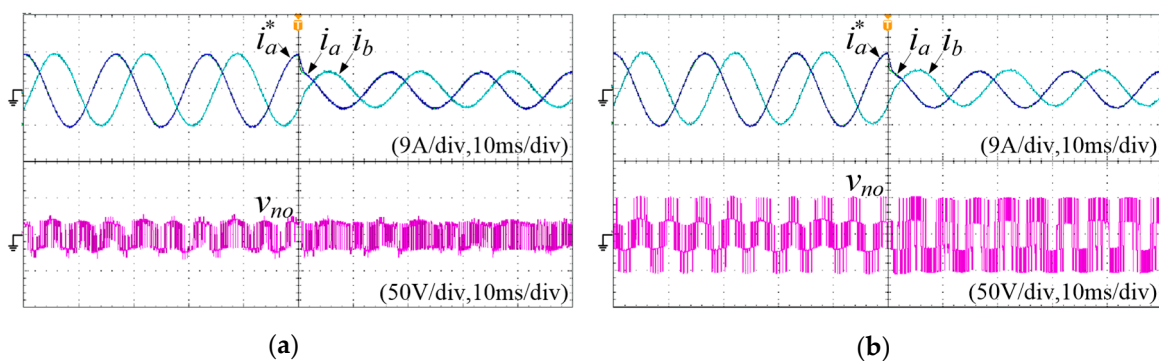

Figure 13. Experimental results of the output currents (i_a and i_b), a phase reference current (i_a^*), and the CM voltage (v_{no}) for a amplitude step change from 9 A to 4.5 A for (**a**) the proposed algorithm with T_s = 200 μs, (**b**) the conventional algorithm with T_s = 100 μs.

5. Conclusions

This paper proposed a comprehensive DV approach for VSI based on the MPC algorithm for reducing the CM voltage. Two non-zero active vectors were chosen and partitioned in one sampling period through the optimization process at every sampling instant, by considering all 36 possible combinations producible by two non-zero active vectors of the three-phase VSI in the proposed algorithm. The zero vectors produced the highest CM voltage; therefore the proposed algorithm only selected non-zero active vectors. Based on the optimal process for distributing and applying two active vectors during one sampling period, the proposed algorithm was able to decrease the output-current ripple, output-current error, and the CM voltage. The current ripples and errors of the proposed algorithm were also lower than those of the DV-Con1 and DV-Con2 methods that use a DV. The proposed algorithm can also control the output current with a rapid transient response. The proposed algorithm was validated by simulation and experimental results.

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