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Switching Loss Balancing Technique for Modular Multilevel Converters Operated by Model Predictive Control Method

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Abstract: The sorting algorithm is the most widely accepted capacitor voltage balancing strategy for a modular multilevel converter. This strategy offers to keep the balance among submodule capacitor voltages under all of the modular multilevel converter working conditions. However, this method generates unnecessary switching transitions in submodules, which results in high switching frequency and switching loss, and uneven distribution of switching transitions and switching loss among submodules (SMs). In this paper, a simplified switching loss balancing control strategy was proposed in order to handle these issues. The proposed approach adjusted the submodule selection process of the sorting algorithm by taking into consideration the number of switching transitions in addition to the capacitor voltages. Even distribution of switching transitions and switching loss was achieved, and the average switching loss was reduced at the cost of slightly increasing the capacitor voltage fluctuations. The effectiveness of the proposed approach was verified through both simulation and experimental results.

Keywords: modular multilevel converter; model predictive control; sorting algorithm; switching loss balancing

1. Introduction

Modular multilevel converter (MMC) has received a great deal of concern due to numerous advantages [1–3] such as a highly modular structure, easy scalability, and superior harmonic performance. Since it was first introduced in 2003 [4] by Lesnicar and Marquardt, MMC has become the most potential topology for medium- to high-power applications, specifically for the high-voltage direct current (HVDC) application.

In spite of the benefits of MMC, the control of this converter is quite challenging due to multiple control objectives. In order to guarantee proper operation of MMC, proper magnitude and frequency of output current, suppression of circulating current, and balance of submodule (SM) capacitor voltages must be satisfied. Various control methods have been studied extensively to address these requirements. Earlier, classical control method used proportional-integral (PI) [5] and proportional-resonant (PR) [6] controllers, combining a pulse-width modulator to control each objective. A typical control scheme, which was presented in [5,7], uses PI controllers and applies a pulse-width modulation (PWM) scheme to MMC with averaging and balancing control. Aside from this, different multicarrier PWM techniques have been reported [8–11] in evaluating their performance to MMC. The performance of classical control method is mostly influenced by the design and tuning of the PI controller's parameters, as well as the selected PWM type.

In recent years, model predictive control (MPC) [12–14] has been considerably involved in the control of MMC due to its capability of handling the drawbacks of the classical control method.

Owing to distinctive advantages such as the capability of controlling multiple objectives simultaneously with a single cost function, superior dynamic performance, and inclusion of system's nonlinearity, MPC has been extensively studied in recent years. The basic idea of MPC is to evaluate all possible switching states of a converter to obtain the optimal one through calculation of a predefined cost function. This MPC scheme refers to direct MPC [15,16], in which 2^{2N} (N is the number of SMs in one arm) possible switching states are evaluated in every sampling instant for MMC. The best switching state is selected from the minimum value for the cost function, which results in optimal value of the output current, circulating current, and SM capacitor voltages errors. In spite of straightforward implementation, the direct MPC suffers from computational burden due to the number of possible switching states increasing exponentially as the number of SMs increase. In order to handle this drawback, a standard method, which is widely applied to reduce the computational burden, is used to classify control objectives at different stages [17–20]. As in [17], this approach uses three independent cost functions corresponding to output current, circulating current, and capacitor voltages balancing to obtain optimal switching state. However, this method does not provide the flexibility of interaction among control objectives. A more popular scheme, which is referred as indirect MPC, is investigated in [20]. The indirect MPC decouples the capacitor voltage balancing task from the cost function using a voltage-sorting algorithm. In this case, the MPC is responsible for evaluating the optimal number of inserted SMs in the upper and lower arms, whereas the sorting algorithm could decide which SM should be inserted or bypassed in order to retain the balance of capacitor voltages among SMs.

Different from the conventional direct MPC, the voltage-sorting algorithm is implemented in the indirect MPC to carry out the SM capacitor voltage balancing task. This sorting method is the most widely accepted SM capacitor voltage balancing strategy [21,22], achieved by using the sorted capacitor voltages among SMs and direction of the arm current to determine which SM should be inserted or bypassed. In spite of the guarantee of SM capacitor voltage balancing under various MMC operating conditions, the sorting algorithm generates unnecessary switching transitions among SMs due to it needing to be implemented in every control period. This results in a case in which the number of inserted SMs within two adjacent control periods are precisely similar, wherein the inserted or bypassed actions of SM may occur. Thus, due to unnecessary switching transitions, the sorting algorithm leads to increased switching frequency and relatively high switching losses. Additionally, as for long-time MMC operation, it might result in a tremendous difference of switching transition number, switching frequency, and switching losses among SMs. Several methods, which aim at reducing the switching frequency, are proposed in [23–25]. In [23], a limited number of SMs are sorted within each control period to prevent unnecessary switching transitions. It means that if additional SMs in each arm need to be inserted (bypassed), the conventional sorting algorithm will only be applied to bypassed (inserted) SMs. Although this method significantly reduces the switching frequency, it may result in a higher capacitor voltage fluctuation due to the SM staying inserted or bypassed for a long time. Additionally, the previously reduced switching frequency methods do not balance the switching transitions and switching losses among SMs.

In this paper, a simplified switching loss balancing control strategy was proposed. The proposed approach allowed balancing the switching losses, reducing average switching transition and switching loss among SMs, and eliminating unnecessary switching transitions in conventional sorting algorithm. This simplified switching loss balancing adjusted the SM selection process of the sorting algorithm by taking into consideration the number of switching transitions in addition to the capacitor voltages. Moreover, the desired tolerance band of the capacitor voltage was set to avoid tremendous capacitor voltage fluctuation. Simulation results were provided to verify the effectiveness of the proposed approach in terms of balancing both the capacitor voltages and the switching loss. Additionally, a single-phase seven-level MMC laboratory prototype was also used to implement and validate the proposed approach.

This paper is organized as follows: Section 2 presents an introduction about the underlying structure and operation of MPC and the basic MPC schemes. Section 3 explains the conventional

sorting algorithm and the proposed approach in detail as for balancing both capacitor voltages and switching loss. Simulation and experimental results are discussed in Section 4, whereas Section 5 draws the conclusion.

2. Structure and Model Predictive Control of MMC

2.1. Standard Structure and Model of Single-Phase MMC

Figure 1 depicts a generalized configuration of a single-phase MMC. A converter phase consists of two arms, namely the upper arm and lower arm. The two identical arms were represented by a subscript "u" and "l" for upper arm and lower arm, respectively. In this, each arm was composed of N SMs, which connected in series with an inductor L_a that was in charge of limiting arm currents. As for SM, the MMC could be structured by various type of SMs, corresponding to the application, operating voltage, and power [26]. In this investigation, owing to its simplicity and low power-loss characteristics, a basic half-bridge SM topology was used. The half-bridge SM can only produce zero and positive output voltage, depending on the state of its two complementary switches S_j and S'_j ($j = 1 - N$).

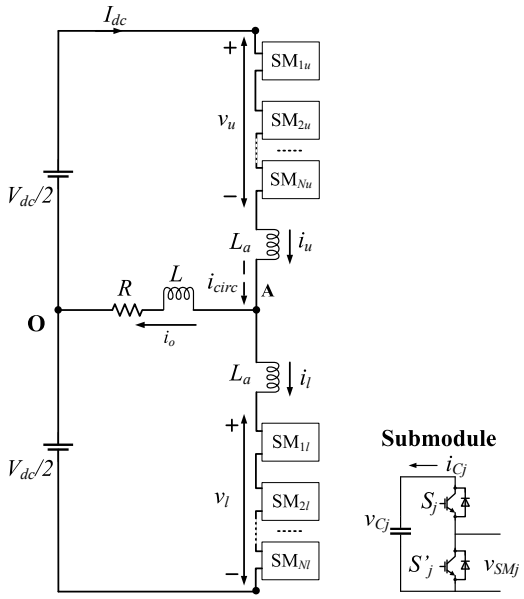


Figure 1. Generalized circuit diagram of a single-phase modular multilevel converter (MMC): (**a**) one phase of the MMC; (**b**) the half-bridge submodule (SM).

In Figure 1, the mathematical model of MMC can be generated by applying Kirchhoff's law. Output current i_o and circulating current i_{circ} equations can be derived by using Kirchhoff's current law as follows:

$$i_o = i_u - i_l, \tag{1}$$

$$i_{circ} = \frac{1}{2}(i_u + i_l), \tag{2}$$

where i_u and i_l are the upper and lower currents, respectively. Similarly, the voltage relationship of the MMC according to Kirchhoff's voltage law can be expressed as

$$\frac{V_{dc}}{2} - v_u - L_a\frac{di_u(k)}{dt} - Ri_o - L\frac{di_o(k)}{dt} = 0, \tag{3}$$

$$-\frac{V_{dc}}{2} + v_l + L_a\frac{di_u(k)}{dt} - Ri_o - L\frac{di_o(k)}{dt} = 0, \tag{4}$$

where V_{dc} is dc-link voltage, whereas v_u and v_l represent the upper and lower arm voltages, respectively. L and R represent load inductance and resistance, respectively.

Adding (3) and (4), and subtracting (3) from (4), mathematical dynamics of the output and circulating currents are deduced as

$$\frac{di_o(k)}{dt} = \left(\frac{1}{2L + L_a}\right)[v_l(k) - v_u(k) - 2Ri_o(k)], \tag{5}$$

$$\frac{di_{circ}(k)}{dt} = \left(\frac{1}{2L_a}\right)[V_{dc} - v_u(k) - v_l(k)]. \tag{6}$$

From (5) and (6), the output current only corresponded to the difference of the upper and lower arm voltages, whereas the circulating current related to the sum of the upper and lower arm voltages.

2.2. Model Predictive Control for MMC

Due to the challenging control of MMC, which involves various control objectives such as the proper magnitude and frequency of output current, circulating current suppression, and capacitor voltage balancing, the MMC requires a proper and robust control scheme to achieve these control objectives. In recent years, the MPC is known as an advantageous approach to control the MMC, owing to numerous advantages such as capability in controlling multiple objectives simultaneously with a single cost function and superior dynamic performance [27].

Although the direct MPC is straightforward to implement, it suffers from a substantial computational burden due to 2^{2N} possible switching states when evaluating every sampling instant. The indirect MPC proposed in [20] can help to reduce the computational burden. It can be observed from Figure 2 that the indirect MPC was different from the direct MPC in terms of decoupled SM capacitor voltage balancing. In this case, the capacitor voltage balancing term was not included in the cost function, whereas the MPC scheme evaluated the number of inserted SMs n_u and n_l in the upper and lower arms, respectively. Subsequently, a voltage sorting algorithm [21] can determine which SM should be inserted or bypassed in order to generate switching signal, as well as keeping capacitor voltages balancing. In this paper, the indirect MPC that was implemented in simulation and experimental studies is reviewed in detail for the single-phase MMC in Figure 1.

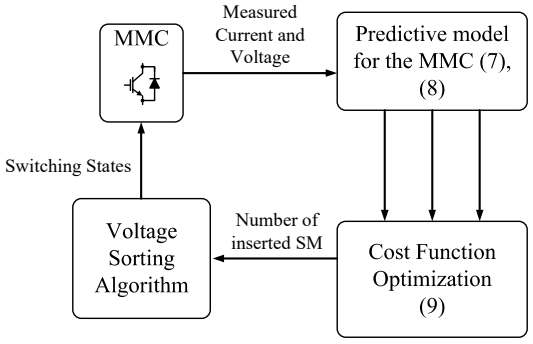


Figure 2. Indirect model predictive control scheme for MMC.

Due to the MPC operating in the discrete-time domain, it required the discrete-time domain mathematical model of control objectives. Applying the Euler approximation [12] to (5) and (6), the discrete-time model of the output and circulating current can be deduced as follows:

$$i_o(k+1) = \left(\frac{T_{sp}}{2L + L_a}\right)(v_l(k) - v_u(k)) + \left(1 - \frac{2RT_{sp}}{2L + L_a}\right)i_o(k), \tag{7}$$

$$i_{cir}(k+1) = \left(\frac{T_{sp}}{2L_a}\right)[V_{dc} - v_u(k) - v_l(k)] + i_{circ}(k). \tag{8}$$

A cost function g was designed to determine the optimal number of inserted SMs every sampling instant on the basis of the difference between the predicted output and circulating currents and the reference values ($i_o^*(k+1)$ and $i_{circ}^*(k+1)$), respectively. The cost function g can be expressed as

$$g = w_1\left|i_o^*(k+1) - i_o(k+1)\right| + w_2\left|i_{circ}^*(k+1) - i_{circ}(k+1)\right|, \quad (9)$$

where w_1 and w_2 are the corresponding weighting factors. It should be noted that the weighting factors used in the cost function had significant effects on the quality of control objectives. The selection of these weighting factors was based on [28], in order to guarantee the optimal quality of control objectives.

3. Conventional Sorting Algorithm and Proposed Switching Loss Balancing Control Strategy

3.1. Conventional Sorting Algorithm

The conventional sorting algorithm has received a great deal of attention in implementing the capacitor voltage balancing task. The basic idea of the sorting algorithm is based on the effect of arm currents on SM capacitor voltage. When the upper (lower) arm current is positive, if an SM is inserted, the corresponding SM capacitor voltage will increase because the SM capacitor is charged. On the other hand, if the upper (lower) arm current is negative, the SM capacitor will be discharged, which results in a decrease of corresponding capacitor voltage. As for bypassed SM, neither positive arm currents nor negative arm currents charge or discharge the corresponding SM capacitor. In this case, the capacitor voltage is unchanged.

In order to keep capacitor voltages balanced, the SM capacitor voltages from both arms are measured and sorted, whereas the upper and lower arm currents are considered to decide which SM should be inserted or bypassed. If the upper (lower) arm current is positive, n_u (n_l) SMs with the lowest voltages are determined and inserted, whereas the others are bypassed. Consequently, the corresponding SM capacitors are charged, and their voltages increase as well. If the upper (lower) arm current is negative, n_u (n_l) SMs with the highest voltages are inserted to discharge, and the others are bypassed. The corresponding capacitor voltages are decreased to retain the capacitor voltage balancing. A block diagram of the conventional sorting algorithm is presented in Figure 3.

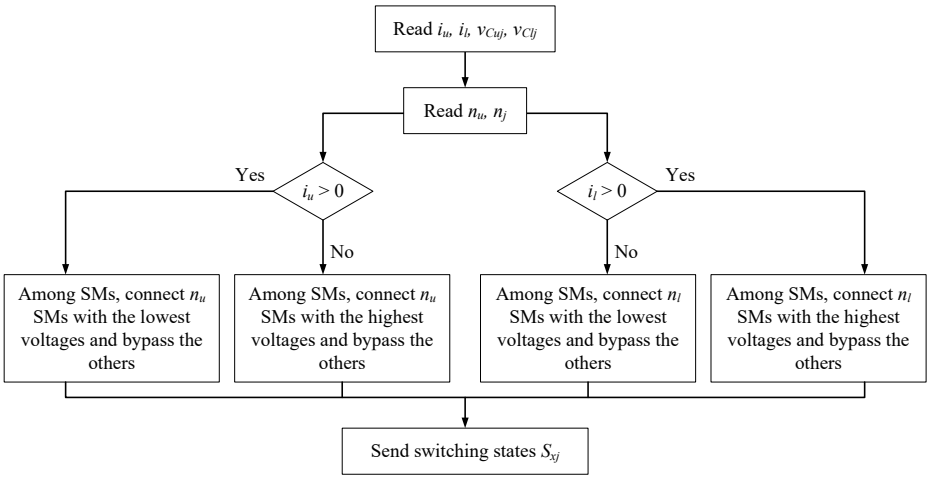


Figure 3. Conventional sorting algorithm.

Because the sorting algorithm inserts or bypasses the SMs according to their corresponding capacitor voltages, the conventional sorting algorithm can produce unnecessary switching transitions among the SMs, which results in the high switching frequency. Moreover, as the characteristic of each SM is different, this leads to uneven switching transitions and switching loss distribution among SMs under the conventional sorting algorithm.

3.2. Proposed Switching Loss Balancing Control

In order to solve the issues presented above, the simplified switching loss balancing control was proposed by combining the conventional sorting algorithm and switching loss balancing control term. Here, the number of the switching transitions of the switch S_j is used for balancing, as the switches S_j and S'_j are complementary. A flow chart of the proposed approach is shown in Figure 4.

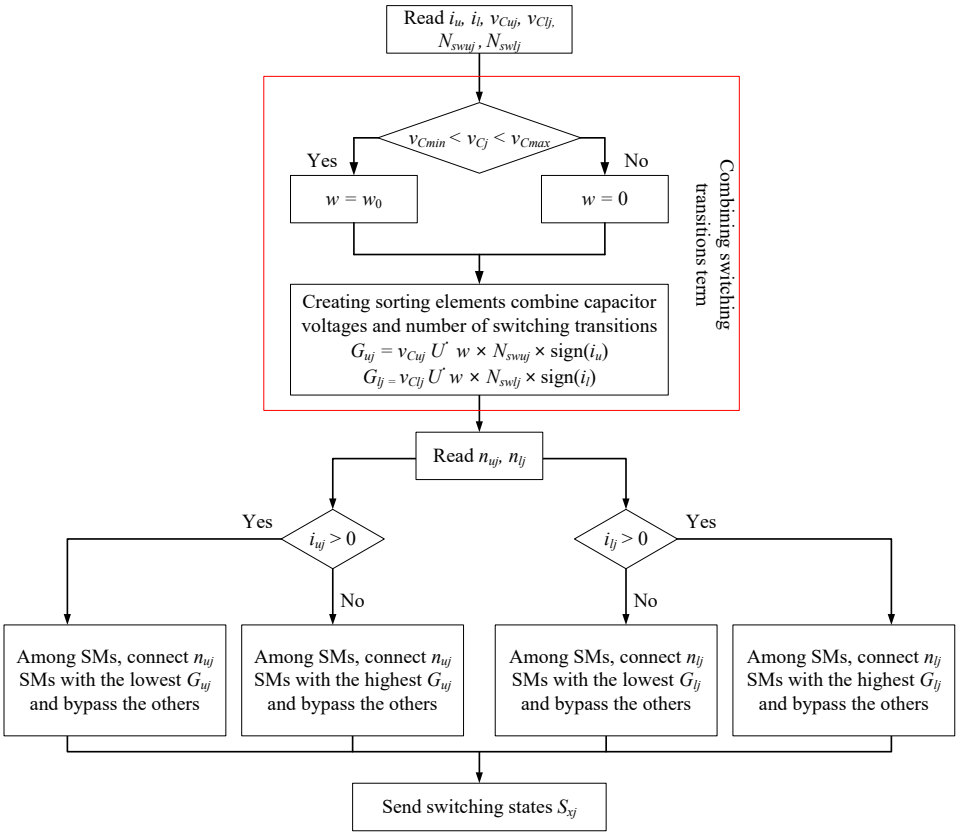


Figure 4. Proposed switching loss balancing control strategy-based capacitor voltage sorting algorithm.

The SM capacitor voltages and arm currents are first measured, and the number of switching transitions is counted. Subsequently, a cost function G_j corresponding to each SM is calculated as follows:

$$G_{uj} = v_{Cuj} - w \times N_{swuj} \times \text{sign}(i_u), \tag{10}$$

$$G_{lj} = v_{Clj} - w \times N_{swlj} \times \text{sign}(i_l), \tag{11}$$

where w is the weighting factor, N_{swuj} and N_{swlj} represent the number of switching transitions of each upper arm and lower arm SMs, respectively. The calculated cost functions G_{uj} and G_{lj} play the same role as SM capacitor voltages in the conventional sorting algorithm. This means that when the calculation of G_{uj} and G_{lj} for each SM is completed, they are sorted and the selection of SM is operated as in the conventional sorting algorithm. The number of switching transitions terms allow for the adjusting of the SM selection process to guarantee not only the capacitor voltage balancing but also switching loss balancing.

Due to the fact that the SM selection process is modified by adopting this method, it is possible that SMs are kept in an inserted or bypassed condition for a long time, which results in excessive capacitor voltage deviation. This exerts a negative impact on capacitor voltages balancing. In order to

handle this problem, the desired tolerance band is set with an acceptable peak-to-peak value of the SM capacitor voltage at 2% of the nominal value V_{dc}/N. This can be expressed as follows:

$$v_{Cmin} \leq v_{Cj} \leq v_{Cmax}, \tag{12}$$

where $v_{Cmin} = 0.98V_{dc}/N$, and $v_{Cmax} = 1.02V_{dc}/N$. If the SM capacitor voltage exceeds its voltage band, the proposed switching loss balancing control is disabled by assigning the weighting factor w as zero ($w = 0$). On the other hand, if the SM capacitor voltage is within its voltage band, the proposed approach is enabled and the weighting factor $w = w_0$ is assigned.

The selection of the weighting factor is carefully designed to balance both capacitor voltages and switching losses by using the method in [28]. Additionally, the direction of arm currents sign(i_u) and sign(i_l) are multiplied with the number of switching transitions terms, as the cost functions G_{uj} and G_{lj} are sorted in the opposite order when the arm current direction changes. With the use of the proposed approach, the balancing of both capacitor voltages and switching losses can be achieved.

The control structure of the MMC, including the proposed approach, is shown in Figure 5. The optimal number of inserted SMs in upper and lower arms (n_u(k) and n_l(k)) are obtained according to the cost function described in (9). Subsequently, the capacitor voltage sorting algorithm combines switching loss balancing control, generating the gate signals of the SMs.

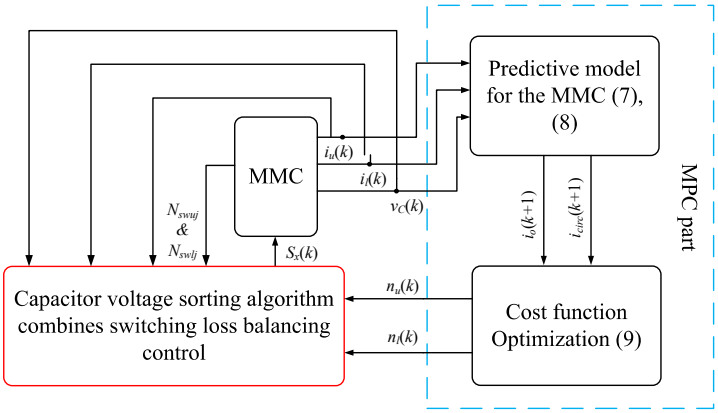


Figure 5. Control structure of proposed approach.

4. Results

4.1. Simulation Study

In order to verify the effectiveness of the proposed approach, the simulation of a single-phase MMC with $N = 3$ was carried out using PSIM software, the system's parameters for which are given in Table 1.

Table 1. Simulation parameters of the single-phase MMC.

DC-link voltage V_{dc} (V)	7000
SMs per arm N	3
SM capacitor voltage V_C (V)	2333.3
SM capacitance C (μF)	2200
Arm inductance L_a (mH)	4
Load inductance L (mH)	10
Load resistance R (Ω)	20
Output frequency f_o (Hz)	60
Rated MMC kVA S (kVA)	350
Sampling frequency f_{sp} (kHz)	10

The weighting factors, which are listed in Table 2, were used in both the simulation and experiment. The weighting factors selection procedure, based on [28], is shown in Appendix A.

Table 2. Weighting factor.

w_1	1
w_2	0.05
w_0	0.5

The phase output current, phase output voltage, SM capacitor voltages, and circulating current generated by the conventional indirect MPC without and with using switching loss balancing control during steady-state operation are shown in Figure 6a,b, respectively.

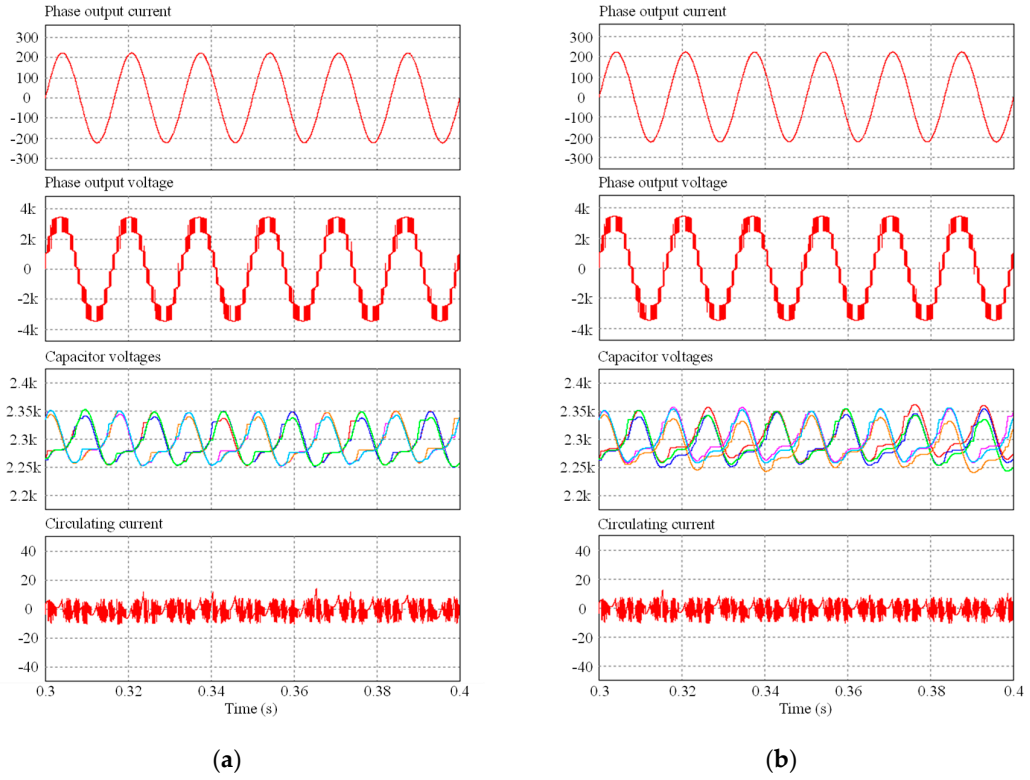


Figure 6. Simulation waveforms of phase output current, phase output voltage, SM capacitor voltages, and circulating current obtained from seven-level MMC (N = 3) during steady-state operation: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

The results of the steady-state operation depicted in Figure 6b showed excellent steady-state performance. The output current in Figure 6b had a correct sinusoidal form with total harmonic distortion THD = 1.27%, which slightly increased compared to the output current in Figure 6a with THD = 1.24%. The phase output voltage level from both of two figures contained sufficiently seven-levels that varied in the range $-V_{dc}/2$ to $V_{dc}/2$, whereas the circulating currents were well-suppressed. These results can be noticed from Figure 6b, wherein the deviation of capacitor voltages was higher than the results from Figure 6a. This was a trade-off when the switching loss balancing control strategy was adopted. From the magnification of SM capacitor voltages in Figure 7a, it was shown that the deviation of capacitor voltages from nominal value V_{dc}/N under which without applying switching loss balancing control was approximately 0.7%. This deviation from Figure 7b, when applying switching loss balancing control strategy, was about 1.2%, which was still acceptable with the desired tolerance band proposed in Section 3. This slight increase in terms of capacitor voltage deviation had a minor

effect on quality of MMC performance thanks to the optimal designed weighting factor and tolerance band. In Figure 7c, the SM capacitor voltage waveforms are presented under the application of the proposed method but without optimal weighting factor w_0 and tolerance band. It was apparent that without using optimal weighting factor and tolerance band, the balance of capacitor voltages among SMs was not guaranteed. The difference of MMC performance in terms of phase output current, phase output voltage, and circulating current between with and without applying the proposed method was not noticeable. This verified that the proposed method does not deteriorate the MMC performance.

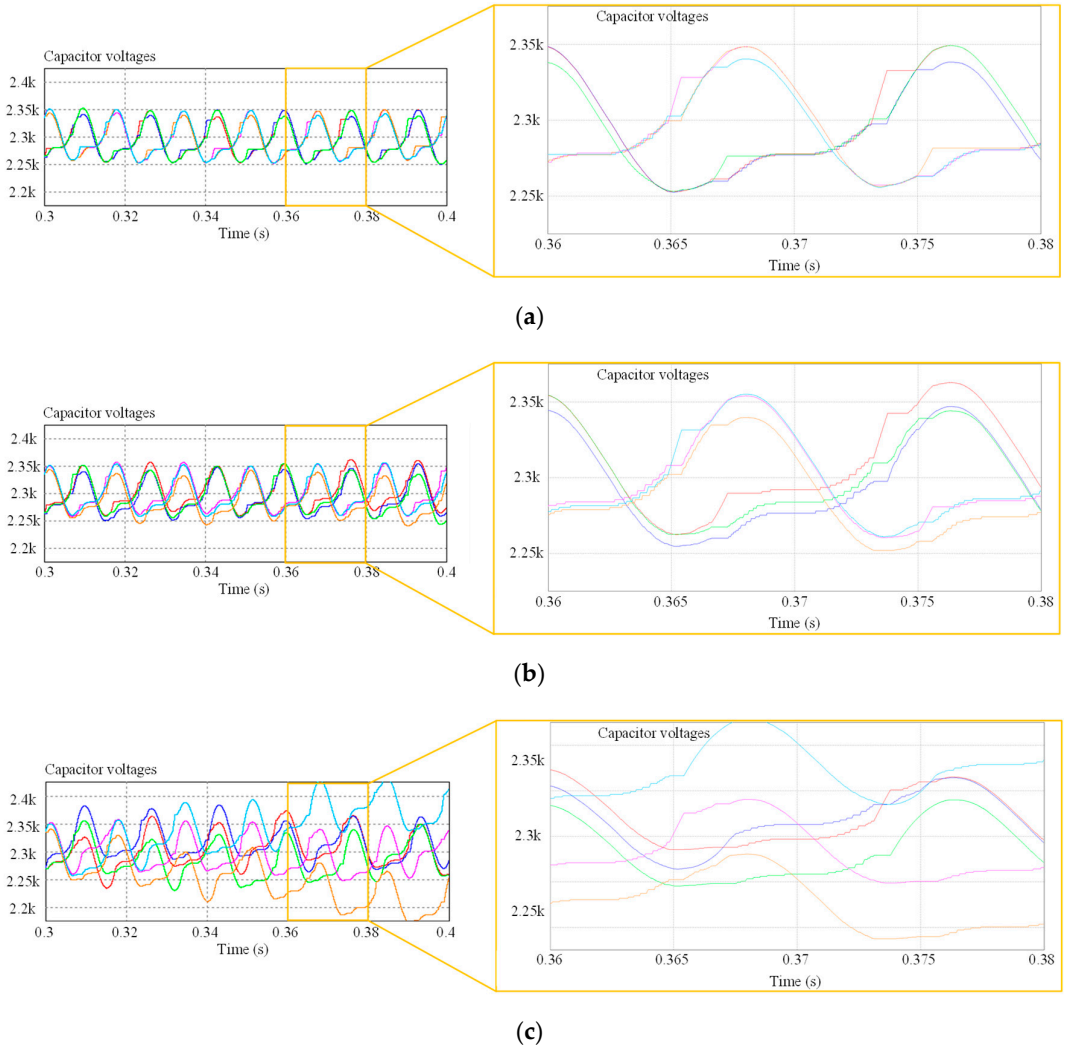


Figure 7. The magnification of SM capacitor voltages: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control; (**c**) without using optimal weighting factor w_0 and tolerance band.

Figure 8 shows the number of accumulated switching transitions within the time interval of 0.1 s of all SMs without applying switching loss balancing control and with applying switching loss balancing control. As observed in Figure 8a, the number of accumulated switching transitions among SMs was mainly divergent. This resulted in different switching frequencies, as well as switching loss distribution among SMs. It can be seen that the maximum switching transition number difference was 51 switching transitions. However, it significantly decreased to 13 switching transitions for SMs when applying the switching loss balancing control strategy, as in Figure 8b. Furthermore, the average number of switching transitions when applying the proposed switching loss balancing control strategy was smaller than without applying the switching loss balancing control.

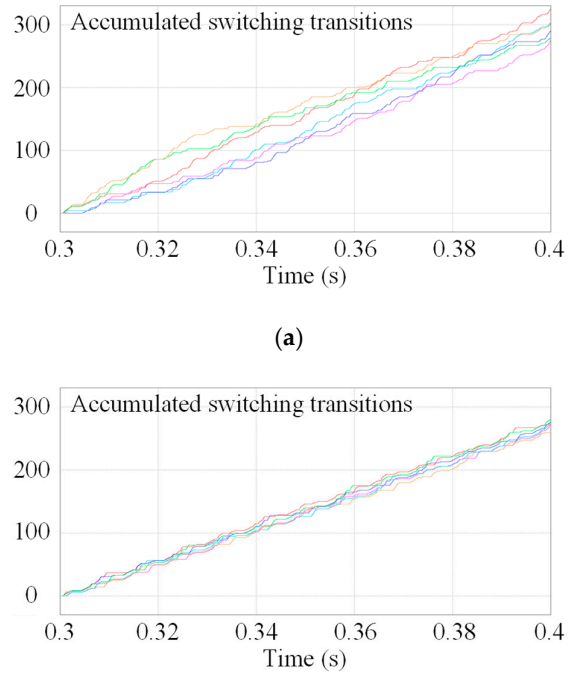


Figure 8. The number of accumulated switching transitions within 0.1 second among six SMs: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

The switching losses and conduction loss evaluation were investigated on the basis of the method used in [22]. The parameters of the insulated-gate bipolar transistor (IGBT) modules were derived from the datasheet of the BSM 50GB 60DLC from Infineon [29]. The junction temperature T_j was considered to be 125 °C for the loss performance calculation. The comparison between power losses of each SM is shown in Figure 9a,b.

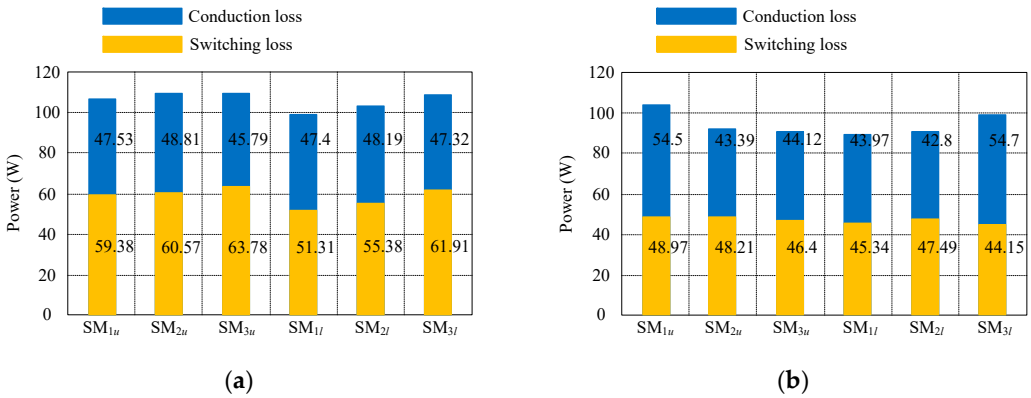


Figure 9. Switching losses and conduction losses among SMs of MMC: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

The deviation of number of accumulated switching transitions from the average value is shown in Figure 10a. It can be seen that by applying the proposed switching loss balancing control strategy, the difference between the deviation of number of accumulated transitions among SMs was negligible. It was apparent that the switching losses among SMs under applying the proposed switching loss balancing control strategy were more balanced than in the case of without applying the switching loss balancing control. Additionally, the average switching from Figure 8b was approximately 46.76 W,

which was apparently reduced compared to 58.72 W from Figure 8a; the reduction of average switching loss was about 20%. In Figure 10b, the deviation of switching loss among SMs from average value is illustrated. As observed, the difference of switching losses with applying the switching loss balancing control strategy was relatively narrowed. On the other hand, the maximum difference of switching loss without applying the switching loss balancing control was significantly high. Because the proposed approach aimed at balancing and reducing the switching losses among SMs, it can be seen from Figure 9 that the conduction losses among SMs were not balanced. However, the average total loss under applying the switching loss balancing control strategy was still lower than the case without applying the proposed scheme.

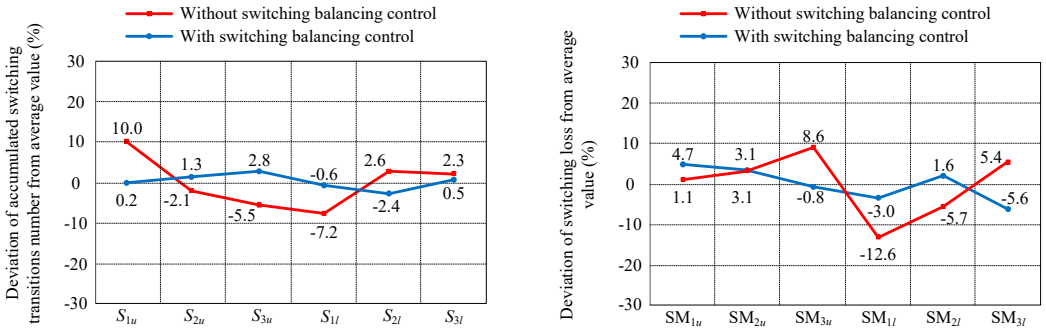


Figure 10. (**a**) Deviation of accumulated switching transition numbers from average value; (**b**) deviation of switching loss from average switching loss.

From the aforementioned simulation results, it was apparent that the balance of switching losses and the reduction of average switching loss could be achieved by applying the switching loss balancing control strategy. Additionally, the performance of output current, phase output voltage, and circulating current were not deteriorated, whereas the fluctuation of capacitor voltages was controlled in an acceptable range.

4.2. Experimental Study

The proposed switching loss balancing control strategy based on the indirect MPC was tested using a single-phase seven-level MMC laboratory prototype. The MMC laboratory prototype configuration and photographs are shown in Figure 11.

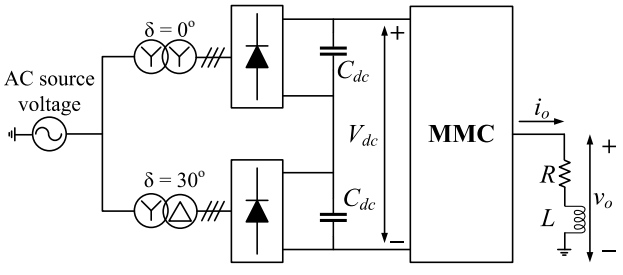
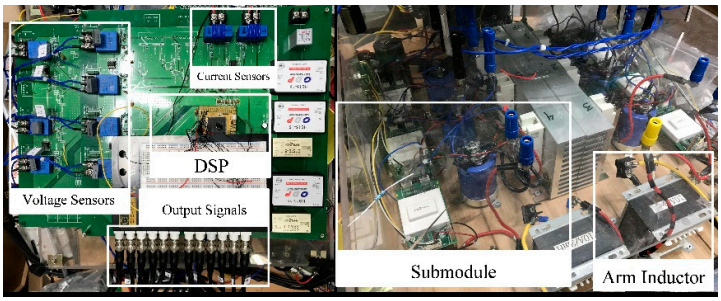


Figure 11. *Cont.*



(**b**)

Figure 11. Experimental setup of the single-phase seven-level MMC: (**a**) a circuit diagram; (**b**) single-phase seven-level prototype and control board.

The proposed switching loss balancing control strategy-based sorting algorithm and indirect MPC were carried out by using the digital signal processor (DSP) TMS320F28335 with a sampling frequency f_{sp} = 10kHz to operate MMC. The MMC laboratory prototype and control parameters are listed in Table 3.

Table 3. Experimental parameters of the single-phase MMC.

DC-link voltage V_{dc} (V)	100
SMs per arm N	3
SM capacitor voltage V_C (V)	33.3
SM capacitance C (μF)	2200
Arm inductance L_a (mH)	4
Load inductance L (mH)	10
Load resistance R (Ω)	20
Output frequency f_o (Hz)	60
Rated MMC kVA S (kVA)	0.1
Sampling frequency f_{sp} (kHz)	10

Figure 12a,b illustrates the experimental results of the output current, phase output voltage, SM capacitor voltages, and circulating current. It can be seen that quite the same output performance with and without applying the switching loss balancing control was achieved in terms of the experimental result, as expected. This validated the correction of the simulation results.

The frequency spectrums of the output current and circulating current are compared in Figures 13 and 14, respectively. The THD values of the output current were obtained by measuring the output current with and without applying the switching loss balancing control strategy and by computing them using the power analysis application module in the Tektronix digital oscilloscope. It can be seen that the difference in THD between the two results was negligible. The root mean square (RMS) value of circulating currents obtained from with and without applying the switching loss balancing control strategy were both close to zero. The negligible difference in terms of phase output current, phase output voltage, and circulating current between with and without applying the proposed switching balancing control approach was achieved thanks to the optimally designed weighting factor and the tolerance band.

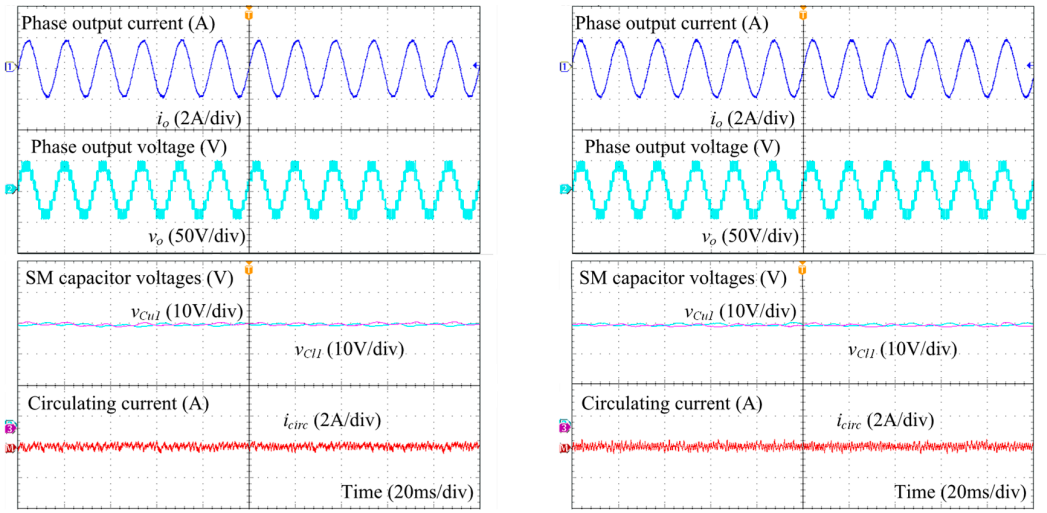


Figure 12. Experimental waveforms of phase output current, phase output voltage, SM capacitor voltages, and circulating current obtained from seven-level MMC (N = 3) during steady-state operation: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

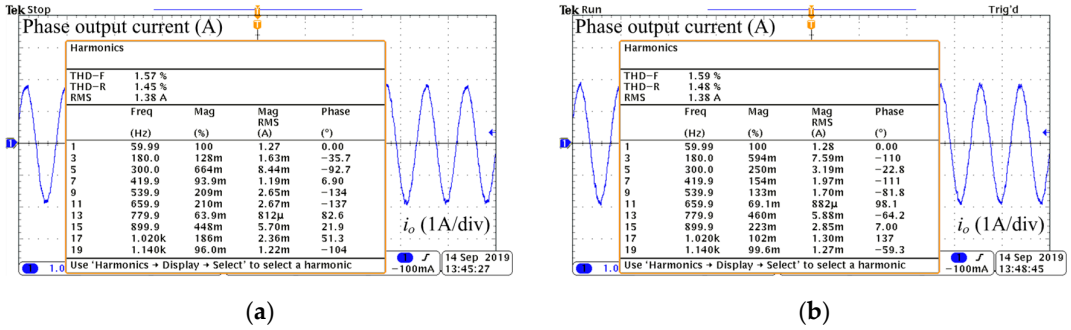


Figure 13. Frequency spectrum of phase output current: (**a**) without switching loss balancing control (THD = 1.57%, RMS = 1.38 A); (**b**) with switching loss balancing control (THD = 1.59%, RMS = 1.38A).

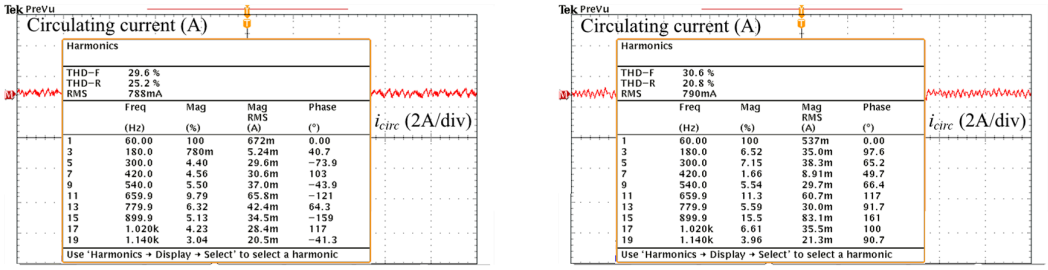
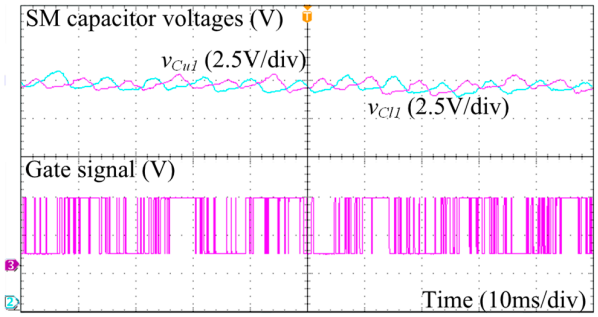


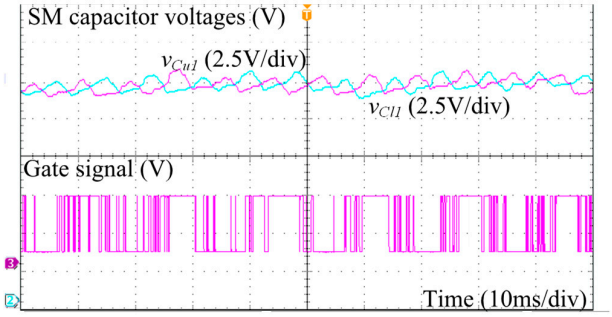
Figure 14. Frequency spectrum of circulating current: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

In Figure 15, the enlarged picture of the capacitor voltage of SM_{u1} and SM_{l1} are shown. As observed, the fluctuation of capacitor voltages in applying the switching loss balancing control strategy was slightly higher than without applying the proposed scheme. However, the balance of capacitor voltage was still guaranteed. Additionally, the experimental waveforms of the gate signal of the switch S_1 obtained with and without applying the switching loss balancing control strategy are also shown in Figure 15. The difference in the number of switching transition and conduction times between with

and without applying the switching loss balancing control strategy was noticeable. The switching loss balancing control strategy modified the SM selection process of the sorting algorithm; this resulted in increasing the conduction time and also reducing the number of switching transitions and switching loss. The experimental results verified the effectiveness of the proposed approach, validating the high quality of output performance with negligible deterioration under the application of the switching loss balancing control strategy.



(**a**)



(**b**)

Figure 15. SM capacitor voltages and gate signal of one power device: (**a**) without switching loss balancing control; (**b**) with switching loss balancing control.

5. Conclusions

In this paper, a simplified switching loss balancing control strategy was proposed for the operation of MMC, as the conventional sorting algorithm produces unnecessary switching transitions, which lead to high switching frequency and uneven switching loss distribution among SMs. The effectiveness of the proposed strategy was analyzed through both simulation and experimental results. It was shown that the balance of capacitor voltage and switching loss (the difference was only 3% compared to 10% without applying the proposed method) could be achieved with only a slight increase of capacitor voltage fluctuations and 20% reduction of the average switching loss compared to without applying the proposed method. Additionally, the output current, phase output voltage, and circulating current performances were kept the same as without applying the switching loss balancing control strategy. This apparently verified that the proposed approach does not deteriorate the performance of MMC.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

First, the selection of weighting factors w_1 and w_2 is discussed here. The cost function (9) included two terms, the phase output current and the circulating current. The weighting factor of the output current w_1 was set to 1. In addition, the weighting factor w_2 was determined by an iterative approach with a repeated process by updating values. The weighting factor w_2 was adjusted to identify an optimal value to minimize the THD values of the output current and the RMS values of the circulating current. A value of w_2 was selected, resulting in optimal performance in terms of the THD values of the output currents and the RMS values of the circulating currents.

Figure A1 illustrates the THD values of the output currents and the RMS values of the circulating currents versus varying w_2, and $w_1 = 1$. It can be concluded that the optimum performance in terms of the THD values of the output currents and the RMS values of the circulating currents occurred with $w_2 = 0.05$, which was selected in this paper.

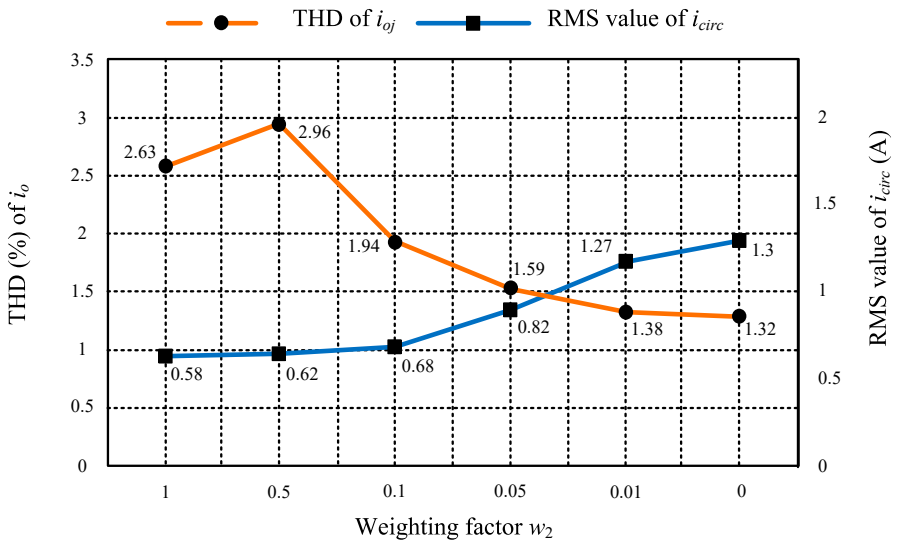

Figure A1. THD values of output currents and RMS values of circulating currents versus varying w_2 ($w_1 = 1$).

The selection of weighting factor w_0 was done following the same procedure as the selection of w_2. The weighting factor w_0 was adjusted to guarantee the balance of capacitor voltages and switching losses among SMs. Figure A2 depicts the deviation of average capacitor voltages and imbalance of switching losses among SMs versus varying w_0. From the results in Figure A2, $w_0 = 0.5$ was selected.

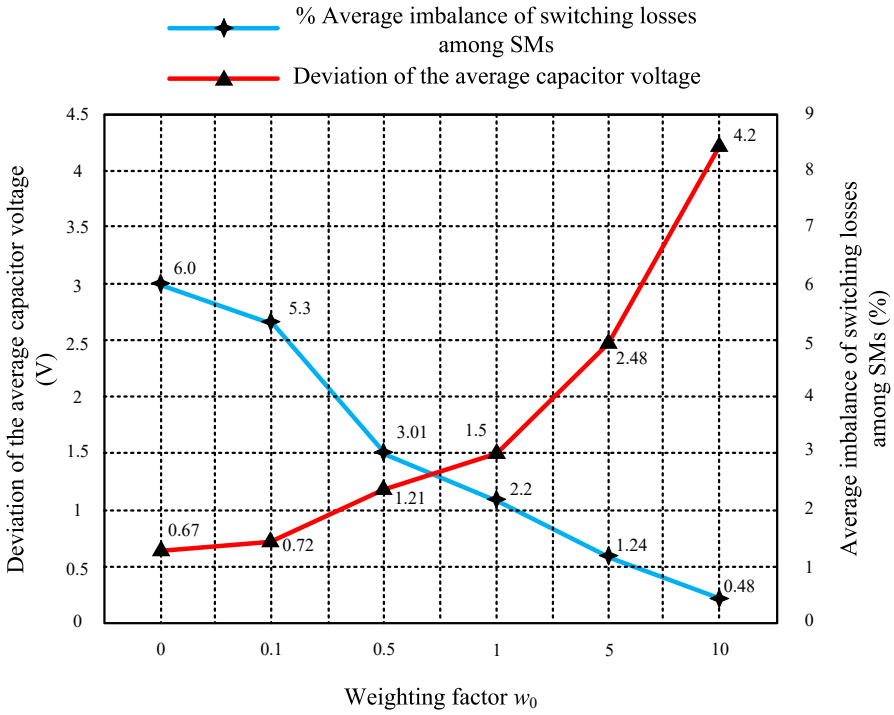

Figure A2. Deviation of the average capacitor voltages and average imbalance of switching losses among SMs versus varying w_0.

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