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Reduction of DC Current Ripples by Virtual Space Vector Modulation for Three-Phase AC–DC Matrix Converters

Hoang-Long Dang, Eun-Su Jun and Sangshin Kwak *

School of Electrical and Electronics Engineering, Chung-Ang University, Heukseok-dong, Dongjak-gu, Seoul 06974, Korea; danghoanglong2692@gmail.com (H.-L.D.); elizame3@naver.com (E.-S.J.)

* Correspondence: sskwak@cau.ac.kr; Tel.: +82-2-820-5346

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Abstract: In this paper, the virtual space vector modulation for the AC–DC (alternating current–direct current) matrix converters is proposed to reduce the DC current ripples in the whole modulation index range. In the proposed method, each virtual vector is synthesized by the two nearest original active vectors. To synthesize the current reference vector, two virtual vectors and one zero vector are used in every switching period. The main principle of the proposed method is to reduce the dwelling period of the largest active current vector in each sector. In addition, the optimized switching patterns are proposed to further reduce the DC current ripples at both high- and low-power operation. Finally, simulation and experimental results are illustrated to validate the effectiveness of the proposed strategy.

Keywords: AC-DC matrix converter; virtual space vector; DC ripple reduction

1. Introduction

In recent years, the AC–DC (alternating current–direct current) matrix converters (MC) have received significant attention in various fields. The AC–DC MC is derived from indirect MCs and inherited several advantages of the MCs, such as bidirectional power flow, sinusoidal input waveforms, controllable input power factor, high power density, and compact design [1–5]. There are various applications of the AC–DC MCs in various fields such as electric vehicles, photovoltaic generation systems, grid-connected converters, microgrids, fuel cell power systems, and battery chargers. [6–9]. Basically, it is a single-stage bidirectional current source AC–DC converter, which rectifies the sinusoidal AC signals to the pure DC signals. Different modulation strategies have been applied for the AC–DC MCs, such as the Alesina–Venturini [5], the pulse-width modulation (PWM) [10,11], the model predictive control (MPC) [12–14], and the space vector modulation (SVM) [15–21]. Predictive control strategies for the AC–DC MCs under unbalanced grid voltage were proposed in [12] and [13]. Literature [14] presented a unity power factor predictive control method for the AC–DC MC. The most wide modulation control strategy for the AC–DC MCs has been considered the SVM method. A unity power factor fuzzy battery charger using the ultra-sparse matrix rectifier was designed and implemented in [15] with only three switches; however, it is a unidirectional converter. The direct power factor control strategy for the three-phase AC–DC MCs was illustrated in [16] based on applying the reduced general direct SVM approach of the AC–AC MC theory. Modulation and control strategies of the AC–DC MC for the battery energy storage system applications were investigated in [17] and [18]. Literature [19] studied the optimal zero-vector configuration to reduce the output inductor current ripple for the space-vector-modulated AC–DC MCs. The optimized modulation strategy to deduce the charging current ripple for vehicle to grid (V2G) applications using the AC–DC MC was presented

in [20]. An input power factor control method was studied in [21] based on the concept of the virtual capacitor. A controlled rectifier was implemented in [22] using the AC–AC MC theory. Literature [23] presented a digitally controlled switch mode power supply based on the MC without any modulation block. Dynamic characteristics of the matrix rectifier researches were studied in [24]. One of the most important issues for the AC–DC MC operation is DC ripples. Generally, increasing the switching frequency or increasing the inductor size of output filter can reduce the DC ripples. However, higher switching frequency leads to higher switching losses and larger size of output inductor results in the increase of size and cost of the converter. There are several approaches based on the SVM algorithm to reduce DC ripples [19,20,25]. In [19], an optimal zero-vector configuration was proposed to reduce DC ripples, however, the effectiveness of this approach is mainly maintained at low modulation because a period of zero-vector at high-modulation operation is very short compared with periods of two active vectors. Thus, this optimal configuration does not effectively reduce the DC ripples in wide operation ranges. The approach [20] proposed a sectional optimized modulation strategy, which can reduce DC ripples within the whole operation range by dividing many different sectors, and different groups of vectors are selected to synthesize the current vector. However, the zero vector configuration is not optimized at low-modulation operations. A recent work in [25] reduced DC ripples by dividing 12 different sectors and using only active vectors to synthesize the current vector. Since only active vectors are used, the operation of this method is not guaranteed at low-modulation operation.

In this paper, the virtual space vector modulation (VSVM) for the AC–DC MC is proposed to reduce the DC current ripples within the whole modulation range. Previously, the VSVM concept was proposed to suppress the common-mode voltage of a two-level voltage source inverter (VSI) [26], and balance the neutral-point potential of a three-level neutral-point-clamped (NPC) inverter [27,28]. However, none of these approaches have been tried to reduce the DC current ripples using the VSVM, at the best knowledge of the authors. In this proposed VSVM method, each virtual vector is synthesized by two nearest active vectors, and each virtual sector is defined with the area between two virtual vectors. The current reference vector is synthesized by two virtual vectors and one zero vector in every switching period. The main principle of the proposed VSVM is reducing the dwelling period of the largest active current vector in each sector. In addition, the optimized switching patterns are proposed to further reduce the DC current ripples at both high- and low-power operations. Simulation and experimental results are demonstrated to verify validity and effectiveness of the proposed VSVM for reducing the DC current ripples of the AC–DC MCs.

2. Topology and Modulations of AC–DC Matrix Converter

2.1. The Topology of AC–DC Matrix Converter

The topology of the AC–DC MC is shown in Figure 1. It is made up of an array of six bidirectional power semiconductor switches, with the ability to conduct current in both directions. Each bidirectional switch is generally constructed by two insulated-gate bipolar transistors (IGBTs) connected in series with a common emitter. An input filter is used to suppress the high-frequency harmonic generated by the operation of converter and the grid. At the output terminal, the LC filter is used to smooth the output current. The AC–DC MC is powered by the AC voltage sources; thus the AC voltages are not allowed to be shorted. In addition, because of the inductive nature of the load, the load terminal must never be opened. Therefore, the AC–DC MC operates by connecting only one bidirectional switch in the upper-arm and only one bidirectional switch in the lower-arm at any instant. This leads to there being nine switching current vectors for the operation of the AC–DC MC.

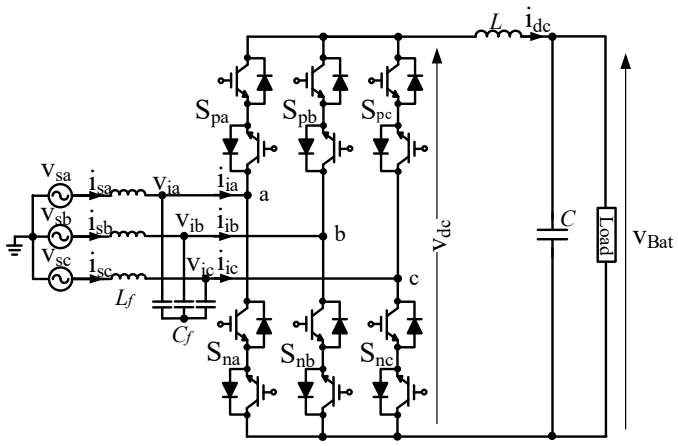

Figure 1. Topology of AC–DC (alternating current–direct current) matrix converter.

2.2. *Modulations of AC–DC Matrix Converter*

2.2.1. Conventional Space Vector Modulation

The current space vector diagram of conventional space vector modulation (C-SVM) for the AC–DC MC is illustrated in Figure 2. In order to synthesize the desired input current reference vector $\vec{I}_{ref}$, C-SVM uses the two nearest active vectors and one zero vector among six active vectors $\vec{I}_1 \sim \vec{I}_6$ and three zero vectors $\vec{I}_7 \sim \vec{I}_9$, according to the sector location of the input current reference vector. Each sector is denoted as the area between two active vectors, for example, the area between two active vectors $\vec{I}_1$ and $\vec{I}_2$ is sector I, the area between two active vectors $\vec{I}_2$ and $\vec{I}_3$ is sector II, and so on. As it can be seen from Figure 2, the input current reference vector locates in sector I, thus two active vectors $\vec{I}_1$, $\vec{I}_2$ and one zero vector are used to synthesize the desired current reference vector. The selection of zero vector is based on the constraint to minimize the switching frequency of bidirectional switches so that the commutation between two switching states involves only two switches in two phase-legs of the converter, one switch is turned on, and one switch is turned off at the same time. Among three zero vectors, only zero vector $\vec{I}_7$ satisfies the requirements for switching devices. Therefore, zero vector $\vec{I}_7$ and two active vectors $\vec{I}_1$, $\vec{I}_2$ are selected.

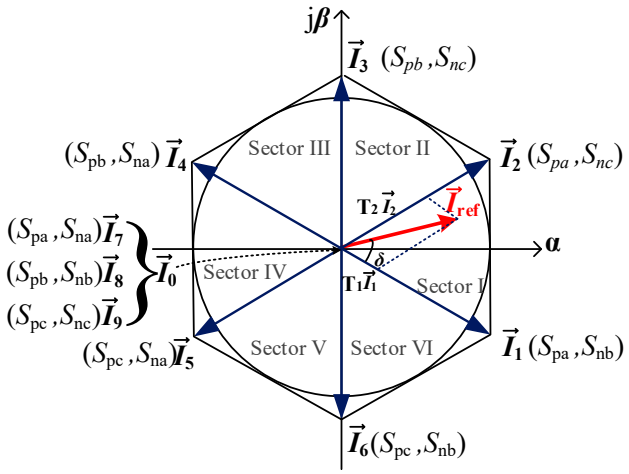

Figure 2. Space vector diagram of conventional space vector modulation (C-SVM) for AC–DC matrix converter.

The duty cycles d_1, d_2, and d_0 of the active and zero vectors, when the input current reference vector is in the sector I, are given by:

$$d_1 = m_i \sin\left(\frac{\pi}{3} - \delta\right) \tag{1}$$

$$d_2 = m_i \sin(\delta) \tag{2}$$

$$d_0 = 1 - d_1 - d_2 \tag{3}$$

where m_i: modulation index; $m_i = i_{i1}/i_{dc}$ $m_i \in [0,1]$; i_{i1}: the peak value of the fundamental-frequency component in i_i; δ : input current reference vector angle, $\delta \in \left[0, \frac{\pi}{3}\right]$.

The durations T_1, T_2, and T_0 of the active vectors $\vec{I}_1$, $\vec{I}_2$, and zero vector $\vec{I}_0$ are respectively expressed as:

$$T_1 = d_1 T_s \tag{4}$$

$$T_2 = d_2 T_s \tag{5}$$

$$T_0 = T_s - T_1 - T_2 \tag{6}$$

where T_s: switching period: $T_s = \frac{1}{f_s}$; f_s: switching frequency.

The calculation of the duty cycles and durations, when the input current reference vector passes through other sectors one by one, is obtained in a similar algorithm as sector I.

2.2.2. Proposed Virtual Space Vector Modulation

(a) Sector division and duty cycles.

In the proposed VSVM, each virtual vector is synthesized by the two nearest active vectors, and each virtual sector is denoted as the area between two virtual vectors. There are totally six virtual vectors $\vec{I}_a \sim \vec{I}_f$ and six virtual sectors. The concept of virtual vector in this paper is similar to the virtual vector concept in [26]. Figure 3 presents the virtual sector divisions according to the virtual vectors and the synthesis of input current reference vector in the virtual sector I of the proposed method. As it can be seen from Figure 3b, when the input current reference vector $\vec{I}_{ref}$ is in virtual sector I, two virtual vectors $\vec{I}_a$, $\vec{I}_b$ and one zero vector are used to synthesize the reference vector depending on the magnitude of modulation index m_i. The selection of zero vector in the proposed VSVM is similar to zero vector selection of the C-SVM method.

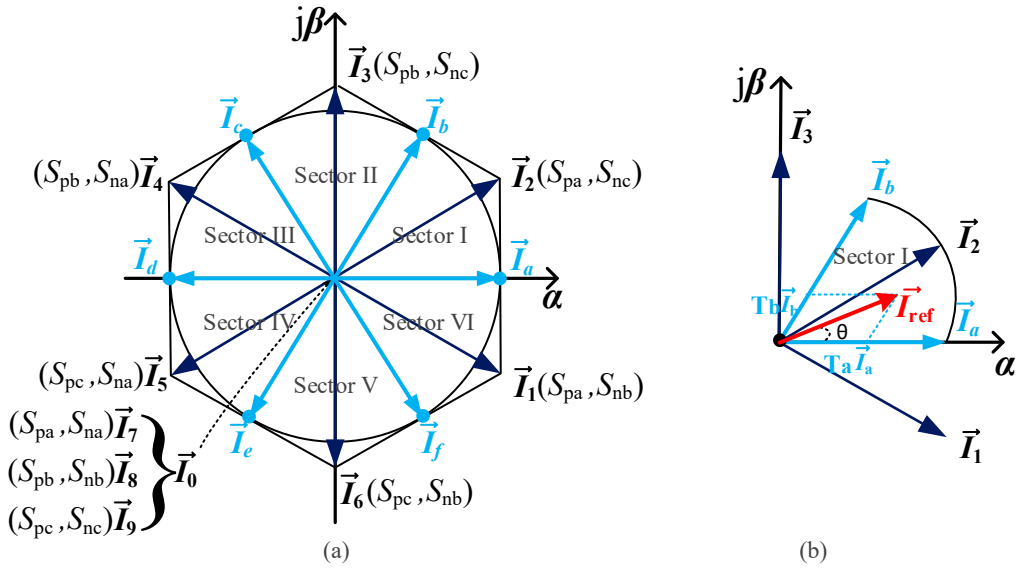

Figure 3. Space vector diagram of proposed virtual space vector modulation (VSVM) for AC–DC matrix converter. (**a**) Sector division; (**b**) Input current reference vector synthesis.

The duty cycles d_a, d_b, d_0 of virtual vectors $\vec{I}_a$, $\vec{I}_b$ and zero vector $\vec{I}_0$, when the input current reference vector is in the virtual sector I, are expressed as:

$$d_a = m_i \sin\left(\frac{\pi}{3} - \theta\right) \tag{7}$$

$$d_b = m_i \sin(\theta) \tag{8}$$

$$d_0 = 1 - d_a - d_b. \tag{9}$$

where m_i: modulation index; $m_i = i_{i1}/i_{dc}$; $m_i \in [0,1]$; i_{i1}: the peak value of the fundamental-frequency component in i_i; θ: input current reference vector angle $\theta \in \left[0, \frac{\pi}{3}\right]$.

The durations T_a, T_b, T_0 of virtual vectors $\vec{I}_a$, $\vec{I}_b$ and zero vector are determined as:

$$T_a = d_a T_s \tag{10}$$

$$T_b = d_b T_s \tag{11}$$

$$T_0 = T_s - T_a - T_b. \tag{12}$$

The virtual vectors $\vec{I}_a$, $\vec{I}_b$ are synthesized by three original active vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_3$. The dwell times T_1, T_2, T_3 of three original active vectors can be derived by:

$$T_1 = \frac{T_a}{2} \tag{13}$$

$$T_2 = \frac{T_a}{2} + \frac{T_b}{2} \tag{14}$$

$$T_3 = \frac{T_b}{2}. \tag{15}$$

The dwell times of other virtual and original active vectors in remaining sectors are determined in the similar manner of the sector I.

(b) Switching patterns.

The effectiveness of the proposed VSVM not only depends on the modulation of virtual vectors, but also on the switching patterns.

Figure 4 presents the switching patterns of conventional VSVM (C-VSVM) in [26]. This switching pattern, which is a seven-segment pattern, is not optimized for reducing the DC current ripple. In this paper, the optimized switching patterns are proposed to further reduce the DC current ripple at both high- and low-modulation operation. The proposed switching patterns of the VSVM strategy for AC–DC MC under different modulation index ranges in sector I are illustrated in Figure 5. At low modulation index operation, the switching period of the zero vector is the longest switching period compared with other switching periods of the remaining active vectors. The longer the switching period of the zero vector, the higher the current ripple due to the longer period of decreasing output DC current. Most of the approaches for DC ripple reduction are not optimized for the zero vector at low-modulation operation. Thus, the optimized switching patterns for the zero vector are proposed in this paper to further reduce the DC current ripple of AC–DC MC.

(c) Controller system.

The control block diagram of the proposed control strategy is illustrated in Figure 6. The battery voltage is sensed and compared with the reference voltage, then passed through the proportional-integral (PI) controller and compared with the DC current or using direct DC current reference depending on the selection of constant voltage (CV) control mode or constant current (CC) control mode. After that, the signal is passed through the PI controller to obtain the modulation index. At the input terminal, three-phase source voltages, three-phase source currents are sensed and passed through the $\alpha\beta$-transformation, then

combined with the PLL block for the calculation of input current. Finally, the VSVM algorithm is applied to compute the duty cycles for AC–DC MC.

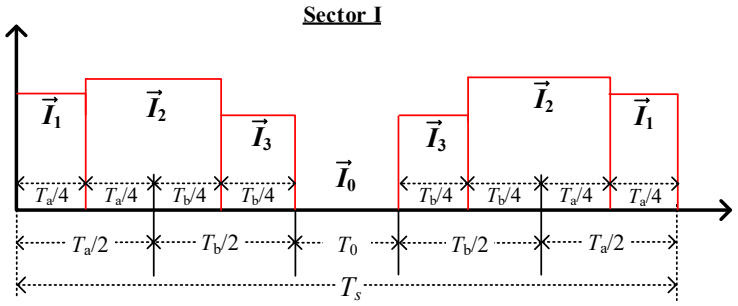

Figure 4. Switching patterns of C-VSVM (conventional VSVM) for AC–DC matrix converter.

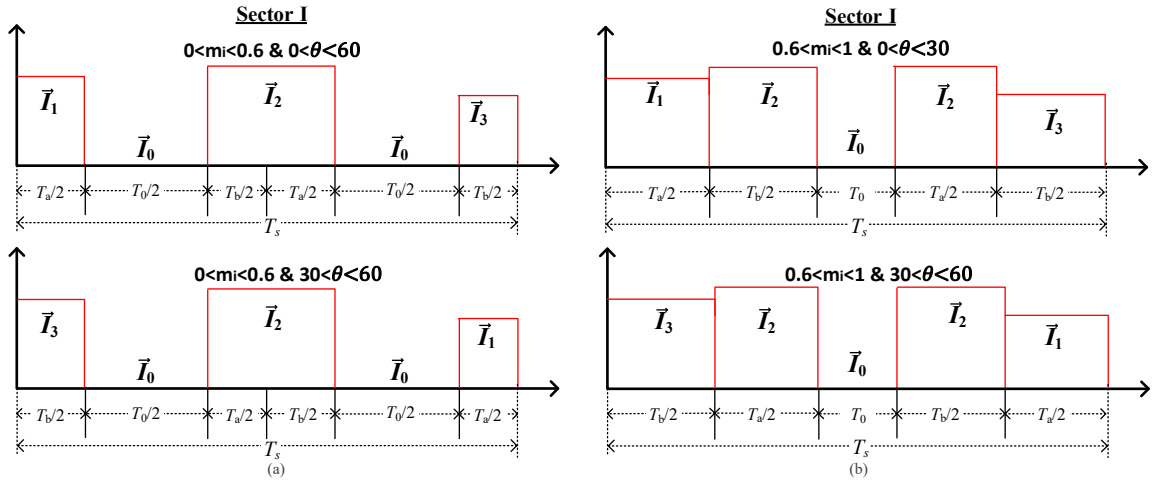

Figure 5. Switching patterns of proposed VSVM for AC–DC matrix converter under different modulation index and input current reference angle. (**a**) Low modulation index; (**b**) High modulation index.

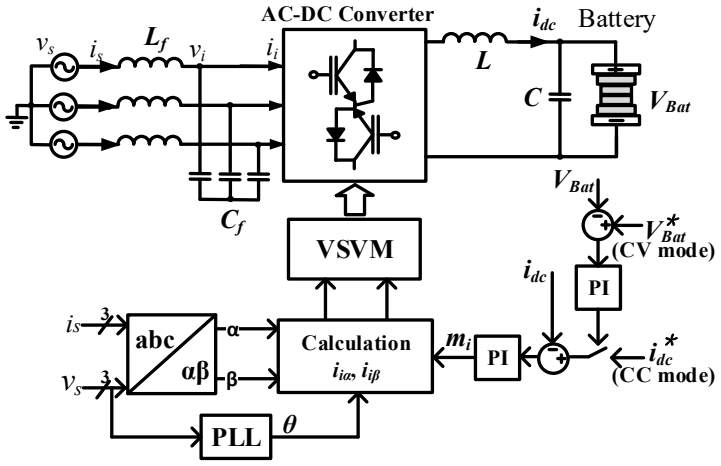

Figure 6. Control block diagram of proposed VSVM for AC–DC matrix converter.

3. DC Current Ripple Analysis

3.1. DC Current Ripple Analysis of C-SVM

In this analysis, the voltage drops by the power devices are neglected and the battery voltage is assumed constant. The load side model of the converter is given by:

$$v_{dc} = V_{Bat} + L\frac{di_{dc}}{dt}. \tag{16}$$

Hence, the DC current ripple in one switching period can be obtained from (16) as follows:

$$\Delta i_{dc} = \frac{v_{dc} - V_{Bat}}{L} T_s. \tag{17}$$

From (17), it is clear that the DC current ripple depends on the instantaneous output voltage v_{dc} of converter, switching period T_s, and output inductor L. Increasing the size of output inductor or switching frequency ($T_s = 1/f_s$) can reduce DC current ripple, however, the size, cost, and switching losses of converter are increased. These solutions are not preferred in this paper.

In one switching period of C-SVM, two active vectors and one zero vector are used to synthesize the input current reference vector. DC current ripples of each vector in the sector I are derived by:

$$\Delta i_{dc1} = \frac{v_{ab} - V_{Bat}}{L} T_1 \tag{18}$$

$$\Delta i_{dc2} = \frac{v_{ac} - V_{Bat}}{L} T_2 \tag{19}$$

$$\Delta i_{dc0} = \frac{v_0 - V_{Bat}}{L} T_0. \tag{20}$$

According to the location of input current reference vector in Figure 2 and the bilateral symmetric switching pattern, the peak-to-peak DC current ripple in one switching period is Δi_{dc0}, as shown in Figures 7a and 8a.

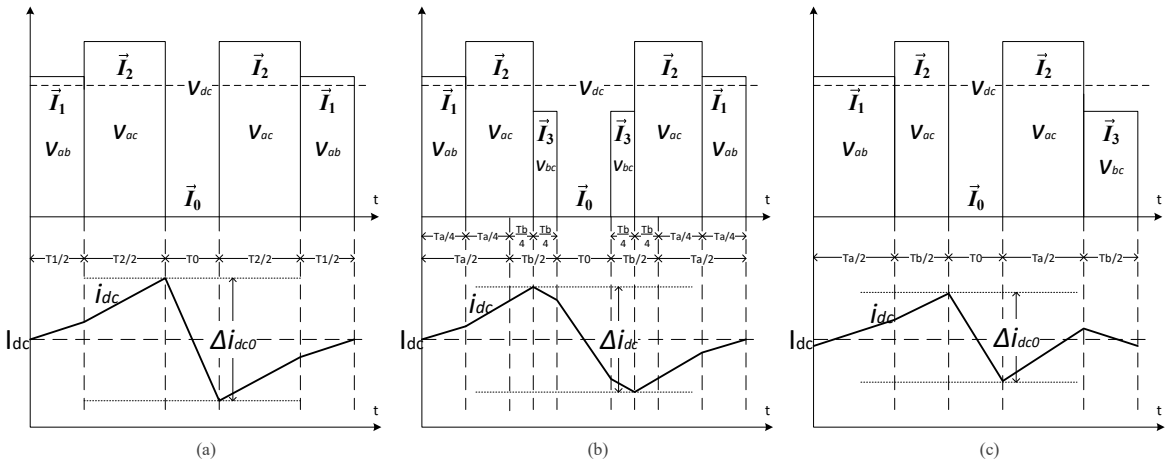

Figure 7. DC current ripple waveforms under different modulation strategies for AC–DC matrix converter at high modulation index. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

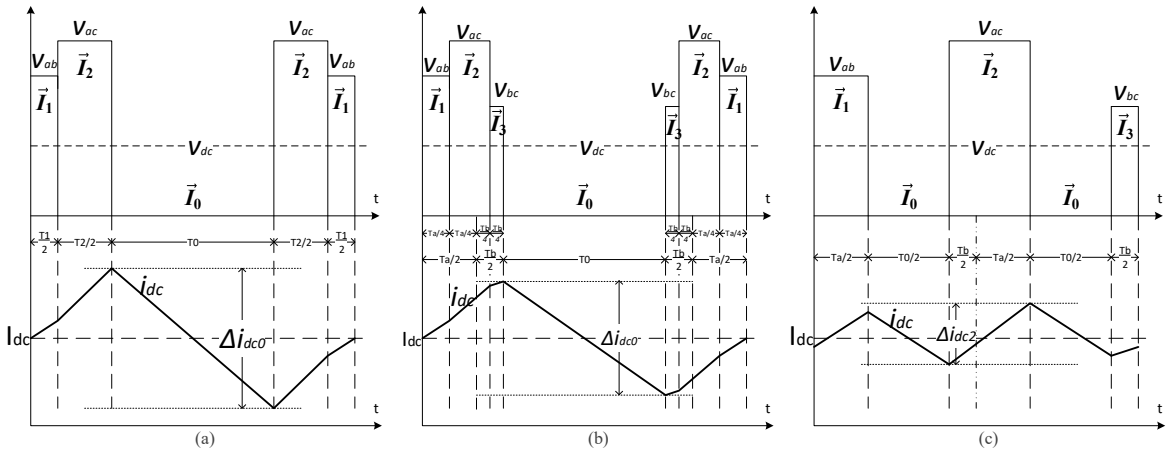

Figure 8. DC current ripple waveforms under different modulation strategies for AC–DC matrix converter at low modulation index. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

3.2. DC Current Ripple Analysis of Proposed VSVM

In one switching period of the proposed VSVM, two active vectors and one or two zero vectors are used to synthesize the input current reference vector.

DC current ripples of each vector in the virtual sector I are derived by:

$$\Delta i_{dc1} = \frac{v_{ab} - V_{Bat}}{L}\left(\frac{T_a}{2}\right) \tag{21}$$

$$\Delta i_{dc2} = \frac{v_{ac} - V_{Bat}}{L}\left(\frac{T_a}{2} + \frac{T_b}{2}\right) \tag{22}$$

$$\Delta i_{dc3} = \frac{v_{bc} - V_{Bat}}{L}\left(\frac{T_b}{2}\right) \tag{23}$$

$$\Delta i_{dc0} = \frac{v_0 - V_{Bat}}{L} T_0. \tag{24}$$

According to the location of the input current reference vector in Figure 3 and the switching pattern, the peak-to-peak DC current ripples in one switching period are Δi_{dc0} at high-modulation operation, as shown in Figure 7c, and Δi_{dc2} at low-modulation operation, as shown in Figure 8c.

The goal of VSVM is reducing the switching period of the switching vector, which has the longest switching period, according the amplitude of input current reference vector in one switching period. In C-SVM, it can be seen from Figure 2 that the switching period of active vector $\vec{I}_2$ is longest and greater than the switching period of active vector $\vec{I}_1$, expressed as:

$$T_2 > T_1 \tag{25}$$

hence

$$T_2 > \frac{T_1 + T_2}{2} \tag{26}$$

then

$$T_2 > \frac{T_s - T_0}{2}. \tag{27}$$

In the proposed VSVM, applying a similar manner as in C-SVM and using (13–15), the switching period of active vector $\vec{I}_2$ is expressed as:

$$T_2 = T_1 + T_3 \tag{28}$$

hence

$$T_2 = \frac{T_1 + T_2 + T_3}{2} \tag{29}$$

then

$$T_2 = \frac{T_s - T_0}{2}. \tag{30}$$

As it can be seen from Figure 7, the switching period of zero vector of C-SVM, C-VSVM, and proposed VSVM is almost the same, however, the longest switching period is active vector $\vec{I}_2$ and reduced by VSVM. Thus, the increasing of DC current ripple is lower than in the conventional strategy, resulting in a reduction in the DC current ripple of VSVM at high-modulation operation. The proposed switching patterns further reduce the DC current ripple compared with the conventional switching pattern of VSVM. In addition, the switching period of zero vector is the longest period at low-modulation operation, thus the optimized switching patterns for zero vector are proposed in this paper to further reduce the DC current ripple of AC–DC MC. Figure 8 presents the DC current ripples under different modulation control strategies at low-modulation operation. As it can be seen from Figure 8, the switching period of zero vector is divided into two intervals by the proposed switching pattern. Hence, the continuous reduction of DC current is avoided compared with the switching patterns of C-SVM and C-VSVM, resulting in the reduction in DC current ripple.

4. Simulation and Experimental Results

4.1. Simulation

In order to verify the validity and effectiveness of the proposed control strategy, simulations were carried out with the parameters in Table 1 using PSIM software. Figure 9 shows the comparison of three-phase currents, A-phase voltage, DC current, and DC current reference at 6 A. It can be seen that the proposed VSVM control strategy effectively reduces the DC current ripple of AC–DC MC compared with C-SVM and C-VSVM strategies in the range of high-modulation operation. Figure 10 presents the zoom-in on DC current and DC output voltage in one switching period of the sector I under different modulation control strategies. The switching period of the largest line-to-line voltage vector was significantly reduced by the proposed VSVM compared with C-SVM. Therefore, the increasing of DC current is reduced before decreasing when zero vector is applied to the converter. Both switching patterns of the VSVM methods effectively reduce the DC current ripple. The proposed optimized switching patterns were applied, and the DC current ripple of AC–DC MC was successfully further reduced while accurately tracking its reference, which is in agreement with the current ripple analysis in Figure 7. The peak-to-peak values of the DC current ripples of the C-SVM, the C-VSVM, and the proposed VSVM operating at a high modulation index are 2.9 A, 2.4 A, and 1.65A, as shown in Figure 10, respectively. As a result, comparing with the C-SVM and the C-VSVM, the proposed VSVM can reduce the DC current ripples by 43.1% and 31.25%, respectively.

Table 1. Parameters for AC–DC matrix converter.

Parameters	Value
Source phase voltage (v_s)	100 V
Source frequency (f_i)	60 Hz
Input filter inductance (L_f)	2.5 mH
Input filter capacitance (C_f)	60 μF
Output filter inductance (L)	1 mH
Output filter capacitance (C)	40 μF
Load resistance (R)	20 Ω
Sampling frequency (f_s)	10 kHz

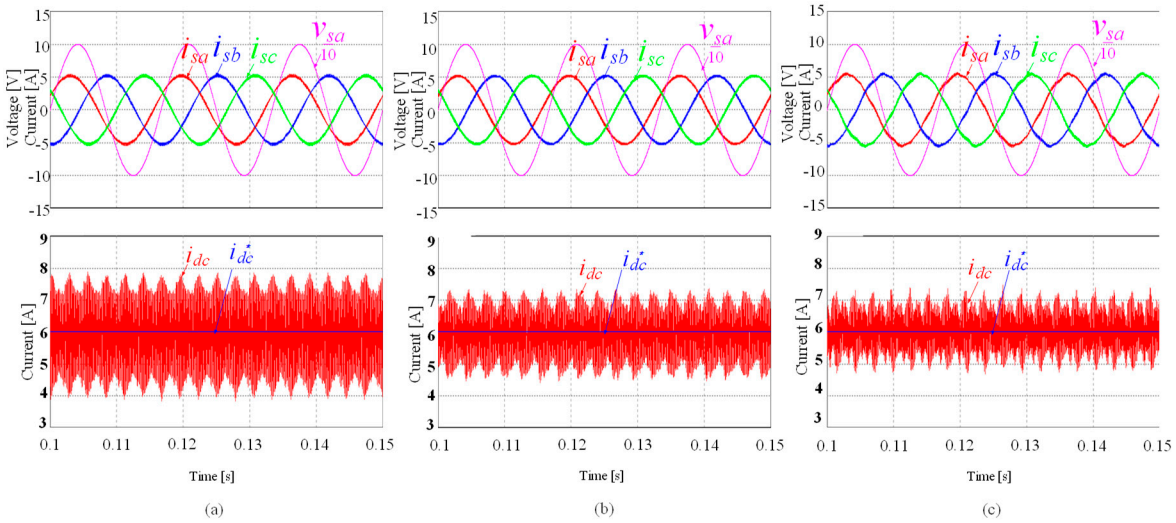

Figure 9. Three-phase currents, A-phase voltage, DC current, and DC current reference under different modulation strategies for AC–DC matrix converter at high-modulation operation. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

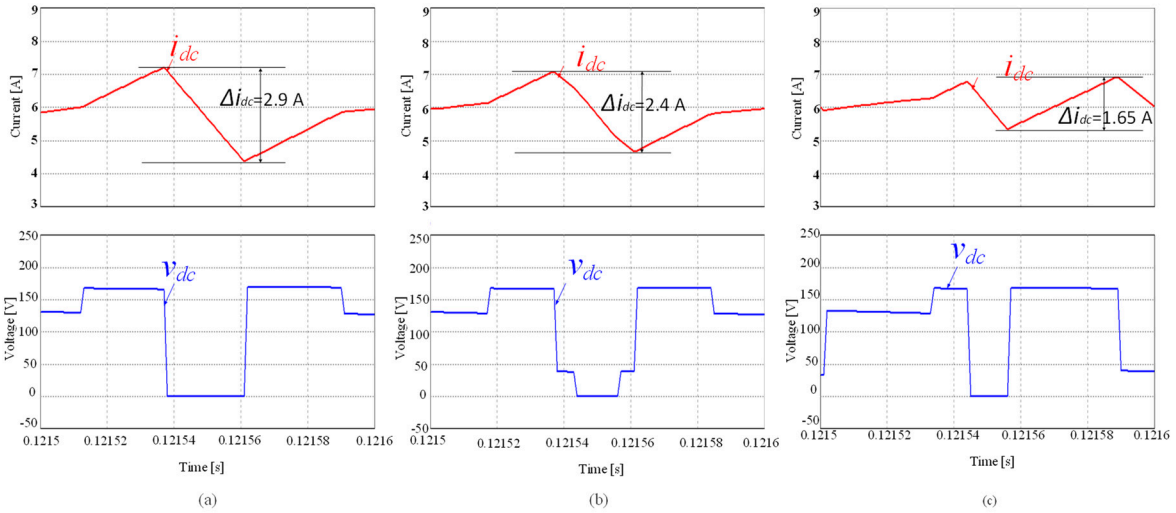

Figure 10. The zoom-in of DC current and DC output voltage under different modulation strategies for AC–DC matrix converter at high-modulation operation. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

The total distortion harmonics (THD) of A-phase source current of C-SVM and VSVM methods are shown in Figure 11. The THD value of the proposed VSVM method is slightly higher than that of the C-SVM method because the four vectors are used to synthesize the input current reference vector in the proposed VSVM to decrease the dc current ripples, including three active vectors and one zero vector, compared with two optimal active vectors and one zero vector of the C-SVM. The distance between the reference current vector and one additional stationary vector used for generating a virtual vector in the proposed VSVM is larger than that of the C-SVM. Besides, the symmetrical switching pattern is applied to guarantee low input current distortion in the C-SVM, whereas the proposed VSVM utilizes unsymmetrical switching patterns to further reduce the dc current ripples. Based on the above factors, the THD of three-phase currents of the proposed VSVM becomes slightly higher than that of the conventional methods, at costs of the reduction of the dc current ripples, although the envelope waveforms of the three-phase input currents are still sinusoidal. The simulation waveforms of three-phase source currents, A-phase source voltage, DC current, and DC current reference at 2 A of AC–DC MC under the C-SVM strategy, the C-VSVM strategy, and the proposed VSVM strategy are illustrated in Figure 12. It can be seen that the effectiveness of the proposed VSVM method in

the reduction of DC current ripple correctly operates within the whole range of modulation while maintaining the high performance of AC–DC MC compared with the C-SVM and the C-VSVM methods. Without the proposed optimized switching pattern at low-power mode, the C-VSVM slightly reduces ripple compared with the C-SVM. The zoom-in of DC currents, DC output voltages in one switching period under the proposed VSVM and the C-SVM are presented in Figure 13. The optimized switching patterns for zero vector are applied when the converter operates at low modulation range. The switching period of zero vector is rearranged to avoid the continuous decreasing of DC current. Therefore, the DC current ripple is further reduced by the proposed VSVM strategy, which agrees with the theoretical analysis in Figure 8. In addition, the peak-to-peak values of the DC current ripples of the C-SVM, the C-VSVM, and the proposed VSVM at a low modulation index are 3.15 A, 2.88 A, and 2.04 A, respectively. Thus, it can be known that comparing with the C-SVM and the C-VSVM, the reduction of the DC current ripples by the proposed VSVM can be obtained by 35.23% and 29.17%, respectively. The transient state performances of AC–DC MC under the C-SVM, the C-VSVM, and the proposed VSVM methods are illustrated in Figure 14. The proposed method successfully reduces the DC current ripple in both high- and low-power operation compared with the C-SVM and the C-VSVM methods. The simulation results show the effectiveness of the proposed method in the reduction of DC current ripple compared with the conventional methods.

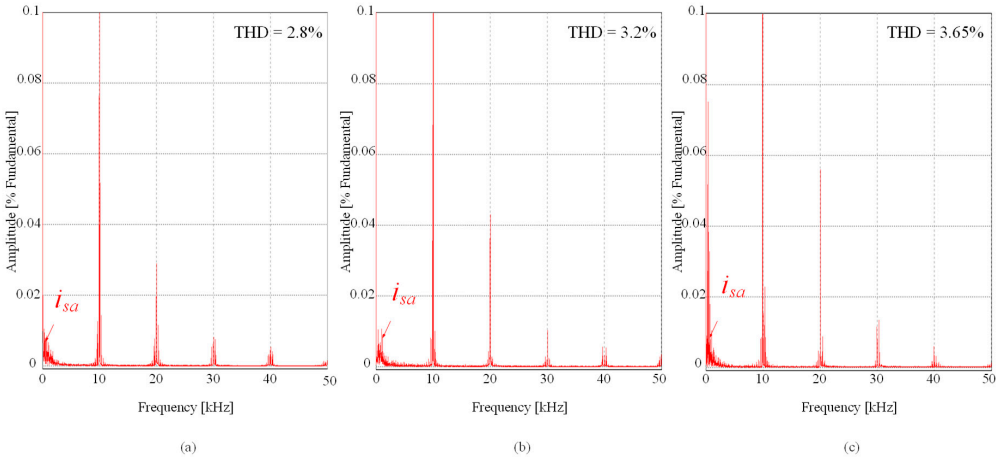

Figure 11. THD (total distortion harmonics) of A-phase source current under different modulation strategies for AC–DC matrix converter at high-modulation operation. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

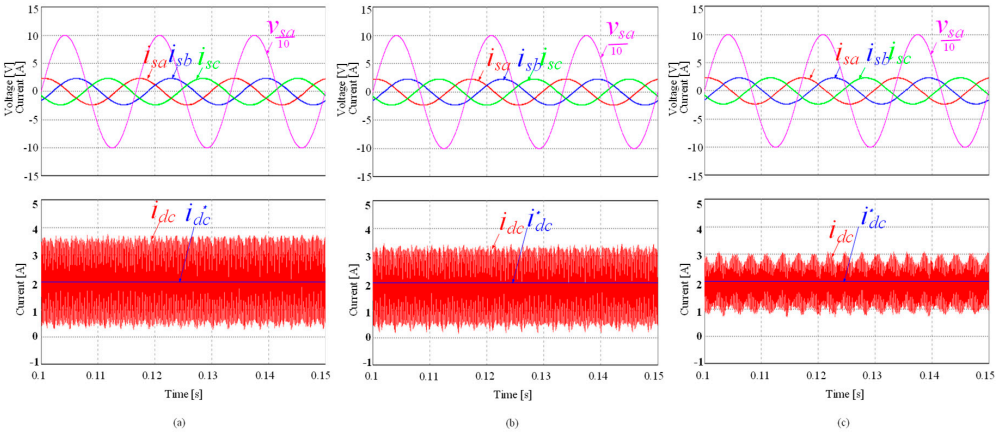

Figure 12. Three-phase currents, A-phase voltage, DC current, and DC current reference under different modulation strategies for AC–DC matrix converter at low-modulation operation. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

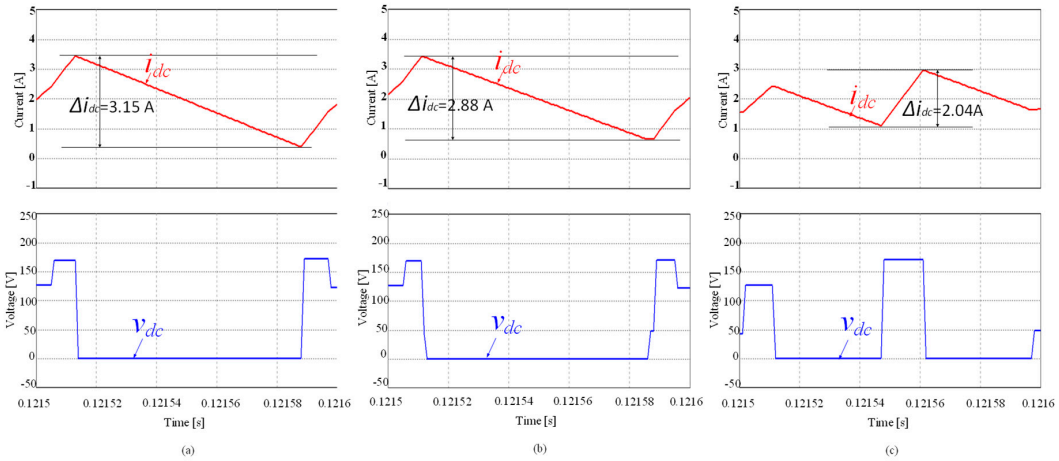

Figure 13. The zoom-in of DC current and DC output voltage under different modulation strategies for AC–DC matrix converter at low-modulation operation. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

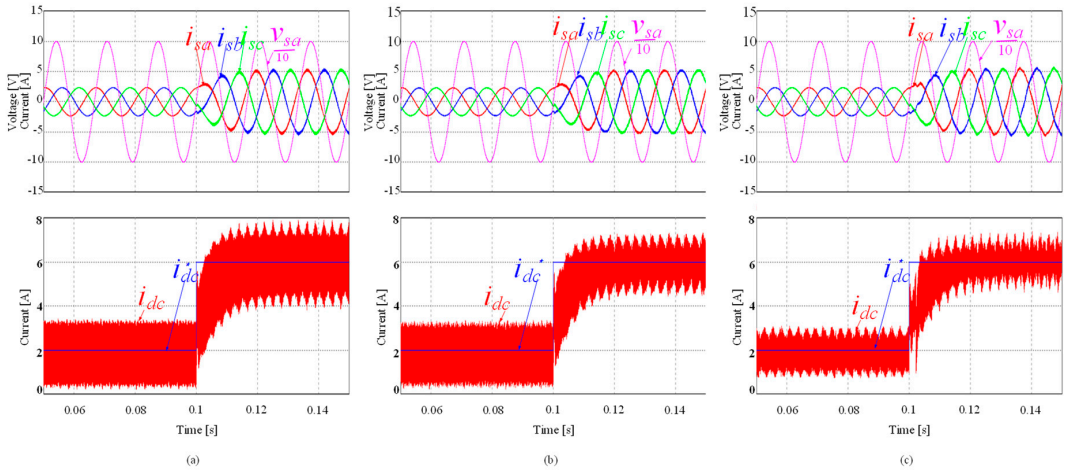

Figure 14. Three-phase currents, A-phase voltage, DC current, and DC current reference under different modulation strategies for AC–DC matrix converter at transient state. (**a**) C-SVM; (**b**) C-VSVM; (**c**) Proposed VSVM.

4.2. Experiment

In order to validate the effectiveness of the proposed control strategy in a real system, an AC–DC MC prototype was constructed with six bidirectional switches, which are built by two insulated-gate bipolar transistors (IGBTs) modules (IXA37IF1200HJ), connected in series with a common emitter to validate the effectiveness of the proposed VSVM. The proposed strategy is performed by a Texas Instrument digital signal processor board (TI TMS320F28335). The parameters of the experiment are the same as in Table 1. Figure 15 shows the comparison of A-phase current, A-phase voltage, battery voltage, and DC current at 5 A. It can be seen that the proposed VSVM control strategy effectively reduces the DC current ripple of AC–DC MC compared with the C-SVM strategy in the range of high-modulation operation. The THDs of A-phase source current of both the C-SVM and the proposed VSVM methods are shown in Figure 16. The THD of the proposed VSVM method is slightly higher than the THD of the C-SVM method, this is a trade-off between ripple reduction and increasing current distortion.

The experimental waveforms of A-phase source current, A-phase source voltage, battery voltage, and DC current reference at 2 A of AC–DC MC under the C-SVM strategy and the proposed VSVM strategy are illustrated in Figure 17. Applying the optimized switching patterns for zero vector at low-modulation operation, the DC current ripple of the proposed VSVM is further reduced

while maintaining the performance of AC–DC MC compared with the C-SVM. The transient state performances of AC–DC MC under the C-SVM and the proposed VSVM methods are illustrated in Figure 18. The proposed method successfully reduces the DC current ripple at both high and low power range compared with the C-SVM method. The experimental results show the effectiveness of the proposed method in the reduction of DC current ripple compared with the conventional methods in the whole range of operation. The assessment of the proposed VSVM method compared with the conventional methods in terms of the reduction of DC current ripples and the increase in the THD values of the input currents is shown in Table 2.

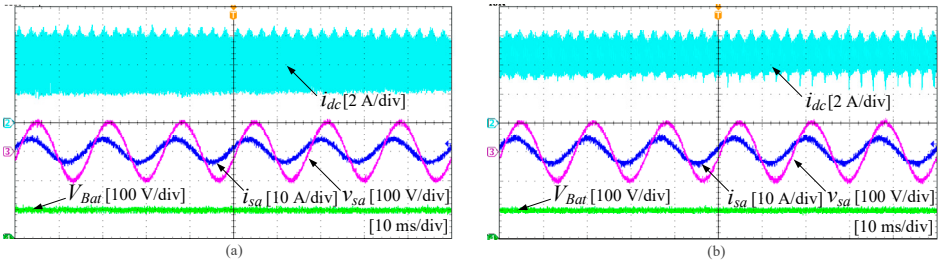

Figure 15. A-phase current, A-phase voltage, battery voltage, and DC current under different modulation strategies for AC–DC matrix converter at high-modulation operation. (**a**) C-SVM; (**b**) Proposed VSVM.

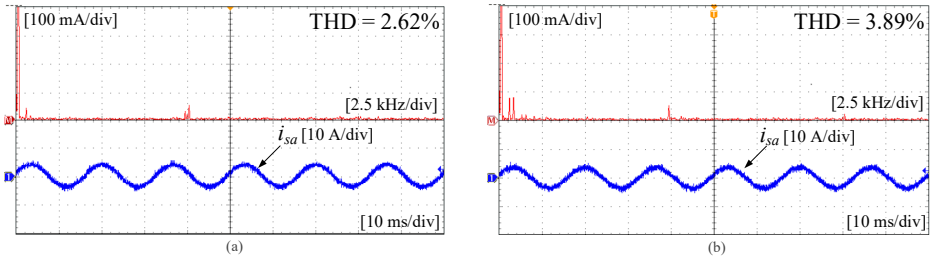

Figure 16. THD of A-phase source current under different modulation strategies for AC–DC matrix converter at high-modulation operation. (**a**) C-SVM; (**b**) Proposed VSVM.

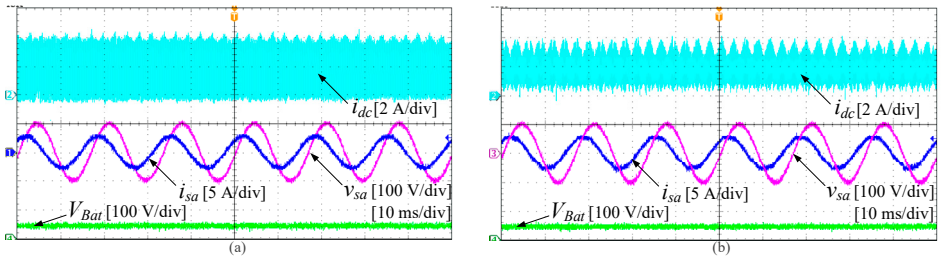

Figure 17. A-phase currents, A-phase voltage, battery voltage, and DC current under different modulation strategies for AC–DC matrix converter at low-modulation operation. (**a**) C-SVM; (**b**) Proposed VSVM.

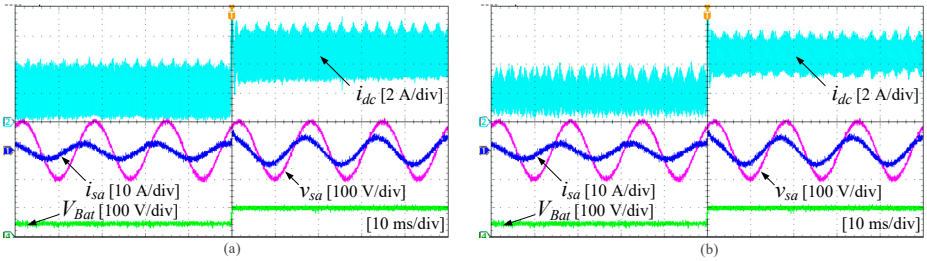

Figure 18. A-phase currents, A-phase voltage, battery voltage, and DC current under different modulation strategies for AC–DC matrix converter at transient state operation. (**a**) C-SVM; (**b**) Proposed VSVM.

Table 2. Percentage comparison of reducing DC current ripple and increasing THD value of the proposed method compared with the conventional methods.

Compared by	Proposed VSVM Method	
	Percentage of Reducing DC Current Ripple	**Percentage of Increasing THD**
C-SVM	43.1%	30.36%
C-VSVM	31.25%	14.06%

5. Conclusions

In this paper, the virtual space vector modulation control strategy is proposed for the AC–DC matrix converter to reduce the DC current ripple in the whole range of modulation. The proposed strategy successfully reduces the DC current ripples by reducing the longest switching period of the largest active vector and dividing one entire switching period with the five-segment optimized switching patterns. In addition, the optimized switching patterns for the zero vector are proposed to further reduce the DC current ripple at low-modulation operations. The THD value of the proposed VSVM method is slightly higher than that of the C-SVM method, this is a trade-off between the reduced DC current ripples and the increased input current distortion. The effectiveness of the proposed strategy was validated by the simulations and the experimental results.

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References

1. Casadei, D.; Serra, G.; Tani, A.; Zari, L. Matrix converter modulation strategies: A new general approach based on space-vector representation of the switching state. *IEEE Trans. Ind. Electron.* **2002**, *49*, 370–381. [CrossRef]
2. Nguyen, T.D.; Lee, H. Modulation Strategies to reduce common-mode voltage for indirect matrix converters. *IEEE Trans. Ind. Electron.* **2012**, *59*, 129–140. [CrossRef]
3. Rivera, M.; Wilson, A.; Rojas, C.A.; Rodrigez, J.; Espinoza, J.R.; Wheeler, P.W.; Empringham, L. A comparative assessment of model predictive current control and space vector modulation in a direct matrix converter. *IEEE Trans. Ind. Electron.* **2013**, *60*, 578–588. [CrossRef]
4. Rodriguez, J.; Rivera, M.; Kolar, J.W.; Wheeler, P.W. A review of control and modulation methods for matrix converters. *IEEE Trans. Ind. Electron.* **2012**, *59*, 58–70. [CrossRef]
5. Alesina, A.; Venturini, M.G.B. Analysis and design of optimim-amplitude nine-switch direct AC-AC converter. *IEEE Trans. Power. Electron.* **1989**, *4*, 101–112. [CrossRef]
6. Vazquez, S.; Lukic, S.M.; Galvan, E.; Franquelo, L.G.; Carrasco, J.M. Energy storage systems for transport and grid applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 3881–3895. [CrossRef]
7. Yilmaz, M.; Krein, P. Review of battery charger topologies, charging power levels and infrastructure for plug-in electric and hybrid vehicles. *IEEE Trans. Power Electron.* **2013**, *28*, 2151–2169. [CrossRef]
8. Bhuiyan, F.A.; Yazdani, A. Energy storage technologies for grid connected and off-grid power system applications. In Proceedings of the 2012 IEEE Electrical Power and Energy Conference (EPEC), London, ON, Canada, 10–12 October 2012; pp. 303–310.
9. Roberts, B.P.; Sandberg, C. The role of energy storage in development of smart grids. *Proc. IEEE* **2011**, *99*, 1139–1144. [CrossRef]
10. Loh, P.C.; Rong, R.; Blaabjerg, F.; Wang, P. Digital carrier modulation and sampling issues of matrix converters. *IEEE Trans. Power Electron.* **2009**, *24*, 1690–1700. [CrossRef]

11. Yan, Z.; Jia, M.; Zhang, C.; Wu, W. An integration SPWM strategy for high-frequency link matrix converter with adaptive commutation in one step based on De-Re-coupling idea. *IEEE Trans. Power Electron.* **2012**, *59*, 116–128. [CrossRef]
12. Nguyen, T.; Lee, H. An enhanced control strategy for ac/dc matrix converters under unbalanced grid voltage. *IEEE Trans. Ind. Electron.* **2019**, 1718–1727. [CrossRef]
13. Nguyen, T.; Lee, H. Simplified model predictive control for ac/dc matrix converters with active damping function under unbalanced grid voltage. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**. [CrossRef]
14. Gokdag, M.; Gulbudak, O. Model predictive control of ac-dc matrix converter with unity input power factor. In Proceedings of the IEEE 12th International Conference on Compatibility Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, Qatar, 10–12 April 2018.
15. Metidji, R.; Metidji, B.; Mendil, B. Design and implementation of unity power factor fuzzy battery charger using ultrasparse matrix rectifier. *IEEE Trans. Power Electron.* **2013**, *28*, 2269–2276. [CrossRef]
16. You, K.; Xiao, D.; Rahman, M.F.; Uddin, M.N. Applying reduced general direct space vector modulation approach of AC-AC matrix converter theory to achieve direct power factor controlled three-phase AC-DC matrix rectifier. *IEEE Trans. Ind. Electron.* **2014**, *50*, 2243–2257. [CrossRef]
17. Feng, B.; Lin, H.; Wang, X. Modulation and control of ac/dc matrix converter for battery energy storage application. *IET Power Electron.* **2015**, *8*, 1583–1594. [CrossRef]
18. Feng, B.; Lin, H.; Hu, S.; An, X.; Wang, X. Control strategy of AC-DC matrix converter in battery energy storage system. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 2128–2134.
19. Feng, B.; Lin, H.; Wang, X.; An, X.; Liu, B. Optimal zero-vector configuration for space vector modulated AC-DC matrix converter. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 291–297.
20. Su, M.; Wang, H.; Sun, Y.; Yang, J.; Xiong, W.; Liu, Y. AC/DC matrix converter with an optimized modulation strategy for V2G applications. *IEEE Trans. Power Electron.* **2013**, *28*, 5736–5745. [CrossRef]
21. Kim, J.; Kwak, S.; Kim, T. Power factor control method based on virtual capacitor for three-phase matrix rectifiers. *IEEE Access* **2019**, *7*, 12484–12494. [CrossRef]
22. Holmes, D.G.; Lipo, T.A. Implementation of a controlled rectifier using AC–AC matrix converter theory. *IEEE Trans. Power Electron.* **1992**, *7*, 240–250. [CrossRef]
23. Ratanapanachote, S.; Cha, H.J.; Enjeti, P.N. A digitally controlled switch mode power supply based on matrix converter. *IEEE Trans. Power Electron.* **2006**, *21*, 124–130. [CrossRef]
24. Yang, X.J.; Cai, W.; Ye, P.S.; Gong, Y.M. Research on dynamic characteristics of matrix rectifier. In Proceedings of the IEEE Conference on Industrial Electronics and Applications, Singapore, 24–26 May 2006; pp. 1–6.
25. Guo, X.; Yang, Y.; Wang, X. Optimal space vector modulation of current source converter for DC link current ripple reduction. *IEEE Trans. Ind. Electron.* **2019**, *66*, 1671–1680. [CrossRef]
26. Tian, K.; Wang, J.; Wu, B.; Xu, D.; Cheng, Z.; Zargari, N.R. A virtual space vector modulation technique for the reduction of common-mode voltage in both magnitude and third-order component. *IEEE Trans. Power Electron.* **2016**, *31*, 839–848. [CrossRef]
27. Hu, C.; Yu, X.; Holmes, D.G.; Shen, W.; Wang, Q.; Luo, F.; Liu, N. An improved virtual space vector modulation scheme for three-level active neutral-point-clamped inverter. *IEEE Trans. Power Electron.* **2017**, *32*, 7419–7434. [CrossRef]
28. Gang, L.; Dafang, W.; Miaoran, W.; Cheng, Z.; Mingyu, W. Neutral-point-voltage balancing in three-level inverters using an optimized virtual space vector PWM with reduced commutations. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6959–6969.