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Design of a DC–DC Converter Customized for Ultra-Low Voltage Operating IoT Platforms

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Abstract: With remarkable advances in IoT, big data, and AI, the fourth industrial revolution is upon us. Low power design methodologies and techniques have been greatly contributing to these advancements by addressing the critical issue of how to increase the device service life under a fixed and limited energy source. In particular, ultra-low power (ULP) technology, which exploits ultra-low voltage (ULV) operating circuit, has recently emerged as a cutting-edge technology for realizing ULP devices. Although a number of studies on ULV circuits have been made so far, and the results have been very successful, research on DC–DC converters optimized for the ULV operation must be carried out in order to use them ultimately in ULP devices. In this paper, a DC–DC converter with low power, small area, and high-resolution digital pulse width modulator (DPWM) for ultra-low voltage (ULV) operating IoT platforms is presented. The proposed DPWM design uses a much smaller number of D flip-flops than conventional ones, achieving significant power saving and area reduction while showing excellent resolution of power conversion. In addition, by utilizing the proposed DPWM, the DC–DC converters can take full advantage of the dynamic switch width modulation technology without overhead, greatly improving the power conversion efficiency under ultra light load conditions. A prototype DC–DC converter with the proposed DPWM is fabricated in Samsung 65nm technology, and the experimental work with this converter and a target ULV operating platform demonstrates that this converter is best suited for the target platform.

Keywords: power conversion, DC–DC converter; low power inductive DC–DC converter; high efficient conversion; lost-cost converter, IoT platform

1. Introduction

Ultra-low power (ULP) IoT platforms are drawing attention from academia [1,2] and industry [3,4] by offering the most practical solution on how to extend the service life of IoT devices under limited small energy sources such as thin film batteries, photovoltaic cells, and thermoelectric generators. These ULP IoT platforms rely on ultra-low voltage (ULV) operation with near-/sub-threshold voltage operating circuits, in which power consumption can be up to several hundred times lower than the nominal voltage operating circuits. Furthermore, recent studies on the ULV operation-specialized low power methods such as applying voltage scaling [2,5], body biasing [6,7], and power gating and frequency scaling (PGFS) [8] techniques to the ULV operating platforms have achieved significant power savings, driving the evolution of IoT platforms.

However, to get the most out of the ULV operation and to take full advantage of the special low power methods, there is a critical device that should not be overlooked: a DC–DC converter. This DC–DC converter must be able to operate not only at nominal voltage (e.g., 1.2 V) and but also in the ULV (e.g., 0.6 V) range, support low output voltage conversion, have a very high voltage control resolution, and be designed to show high power conversion efficiency (η) over a wide range of load

conditions. For example, if a small PV cell with a 0.7 V output voltage powers our prototype ULV operating platform [2] that operates at 20 MHz to 100 MHz clock speed from 0.4 V to 0.6 V supply, the DC–DC converter must work at 0.7 V supply and support up to 0.4 V voltage conversion. Plus, to achieve full power savings from the voltage and/or frequency scaling technique as a result of [2], the DC–DC converter should support at least 10 mV level of voltage controllability and have a high η range in load power from tens of μW to several mW.

As such, considering that DC–DC converters for ULV operating platforms have special requirements over existing DC–DC converter designs, the designs of DC–DC converters have been intensively studied, but only a few (e.g., [9–11]) can work with the ULV operating platforms. Moreover, each previous work has the disadvantage that η under ultra lightweight load conditions [9] or heavy load conditions [10] are not sufficient, or requires additional complex circuitry [11]. Meanwhile, there have been several previous works that focus on the extremely low voltage operating circuits (e.g., less than 0.4 V) [12,13], whereby the DC–DC converters are designed to supply extremely low voltage, and accordingly, their maximum efficiency occurs only at certain very low voltages and rapidly decreases at other output voltages. These converters are not suitable for the IoT platforms that operate at least at tens of MHz frequency. In reality, there is no IoT platform that can operate at tens of MHz with a power supply below 0.4 V. In this paper, focusing on the digital pulse width modulator (DPWM) in a DC–DC converter that can ensure the reliable operation of the converter for the target IoT platforms, we first propose a high resolution and low-power DPWM architecture. We then utilize the proposed DPWM to control the multiple parallel-connected switches in the DC–DC converter to improve η under wide load power conditions. The details of the proposed converter design are elucidated in the following sections.

2. Issues on Conventional PWM Designs

Inductive DC–DC converters typically use PWM to control two power switches in a converter to adjust the converter's output voltage V_{OUT}. The PWM can be classified into analog and digital types, namely APWM and DPWM. Looking at APWM first, the operation of the conventional APWM is as described in Figure 1. In the figure, the ramp generator generates a ramp signal V_{ramp} at specific intervals. Separately, the output voltage V_{OUT} is compared to the reference voltage V_{REF} through the error amplifier (EA), and the difference is expressed as the error voltage V_{err}. Then the V_{ramp} and V_{err} are compared to generate the PWM signal that is used to turn on and off the two power switches, M_p and M_n as seen in the figure.

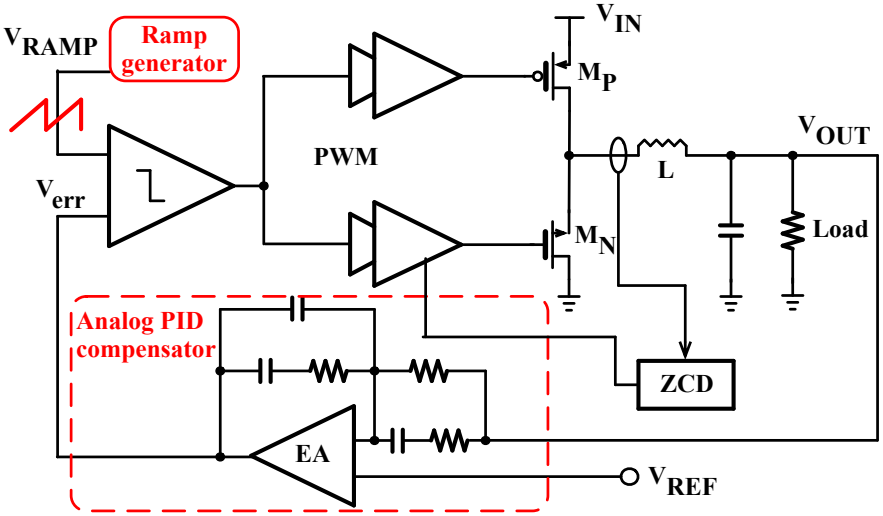

Figure 1. Structure of a DC–DC converter with the analog pulse width modulator (APWM).

Figure 2 shows a detailed analysis of the APWM. In the figure, the duty of the PWM signal is determined by the magnitude of V_{err}. Higher V_{err} increases the time required for V_{ramp} to produce the same voltage as V_{err}, and vice versa. The APWM signal is generated at the intersection of V_{err} and V_{ramp}. Then, the generated PWM signal controls the two power switches. To reduce the supply voltage to the load, the PWM signal is controlled to be large so as to shorten the on-time of the M_p. Similarly, the controlling PWM signal small results in increase the supply voltage to the load.

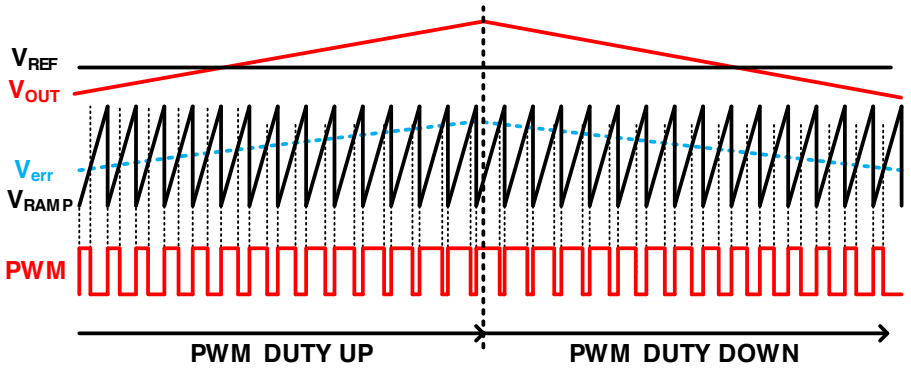

Figure 2. Structure of a DC–DC converter with the APWM.

The APWM exposes serious weakness at low supply voltage, in that the ramp generator and EA in the APWM tend to malfunction. More precisely, these analog circuits are designed to have multiple MOS stacks due to performance and stability issues, which is problematic because the voltage headroom that MOS stacks require for normal operation is not guaranteed at low supply voltages. The DPWM, on the other hand, is advantageous for low supply voltage operation by designing analog circuits as digital circuits that are problematic in low supply voltage operation. More in detail, the DPWM consists of up/down counter, pulse selector, and pulse generator, as shown in Figure 3, all of which are designed as digital circuits. The pulse generator generates delay pulse lines created by delaying the set signal set *Set* by *clk*1. At this time, each generated line has information about the time-delayed by *clk*1. Note that the resolution of the DPWM is determined by the number of delay pulse lines. For example, the pulse generator used for the DPWM with 6-bit resolution produces pulses delayed by one clock each in a total of 2^6 lines. The up/down counter stores and updates the digital code. After comparing V_{REF} and V_{OUT}, this counter increments the digital code to increase the width of the PWM signal when $V_{REF} < V_{OUT}$, and vice versa. Finally, the pulse selector uses the generated code to select one of the pulse lines to generate the PWM signal.

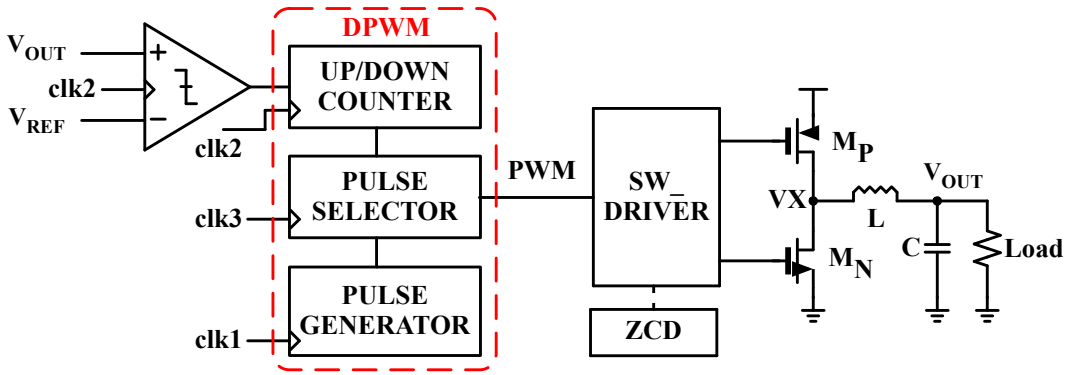

Figure 3. Structure of a DC–DC converter with the digital pulse width modulator (DPWM).

The conventional DPWM designs have significant limitations with the exponential increase in power and area overhead as the resolution of the DPWM increases. The conventional DPWM architecture with n-bit resolution must have the 2^n number of D flip-flops (DFFs) in the pulse generator.

For instance, as shown in Figure 4, the conventional DPWM with 6-bit resolution [9] includes 64 DFFs. Considering the high resolution required for the aforementioned special low power methods [2,5–8], the power and area overhead due to the large number of DFFs can be considerable. In addition, as the number of DFFs increases, the fan-out of each signal increases, which gives rise to power and area overhead increase. For example, the conventional DPWM in Figure 4 utilizing a clock driver that generates *clk*1, *clk*2 (64 times slower than *clk*1), and clk3 (128 times slower than *clk*1) already needs a lot of buffers to meet the timing constraints. Increasing the resolution greatly increases the buffer insertion required, further increasing the power and area of the clock driver. Similar issues arise with the up/down counter, which are generally designed by thermometer codes that are is exponentially proportional to the resolution of the DPWM.

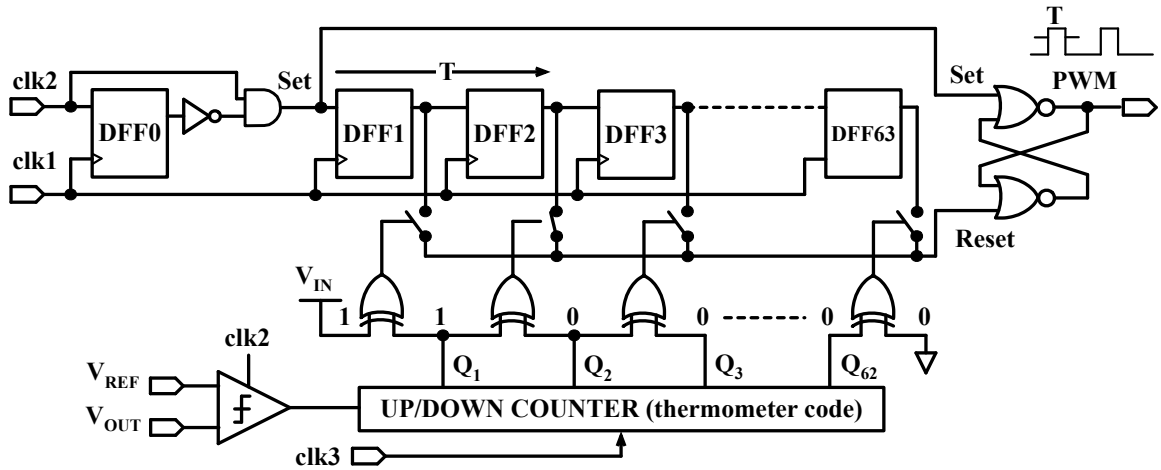

Figure 4. Block diagram of the conventional DPWM.

3. Proposed DPWM Designs

In order to minimize the power and area overhead of the DPWM, we propose an idea of designing a pulse generator that has a small number of DFFs, but each DFF is repeatedly used to generate multiple delay pulses. The proposed DPWM structure is described in Figure 5, which supports 7-bit (higher than the conventional 6-bit) resolution. As seen in the figure, the *Set* pulse is generated by using *clk*1 and *clk*2. The pulse generator with 16 DFFs uses *Set* pulse and *clk*1 to make 16 delay pulses. Then, by exploiting the feedback mechanism, the output pulse from the 16th DFF enters the 1st DFF to generate the next 16 delay pulses, which are repeated for 8 times so as to have a total 2^7 delay pulses. The feedback mechanism is implemented by using *clk*2, *clk*2 $\times$ 4, *clk*2 $\times$ 8 and AND gate. Note that, this additional clock generation can increase the power consumption of the clock driver, but as the resolution of the DPWM increases, the difference in the number of nodes connected per clock within conventional and proposed DPWMs can overwhelm this overhead. In other words, as the resolution increases, the clock driver uses a much smaller number of buffers in the proposed design, so that the reduced power consumption can be greater than the power consumption increase due to the additional clocks. In fact, the power consumption of the clock driver in the proposed 7-bit DPWM is slightly less than that of the 6-bit conventional DPWM, and if the number of bits goes up, the difference will be even greater.

To select a pulse from the generated pulses, the up/down counter uses both the thermometer and binary codes, unlike the conventional thermometer only. The 16-bit thermometer code (thus 4-bit resolution) taking the LSB side is used to select a pulse line from one of the DFFs. The 3-bit binary code using the MSB side is used to select a pulse from the selected pulse line. In other words, as shown in Figure 4, one on and 15 off switches are determined by the thermometer code to select a pulse line among the DFFs with eight pulses each, resulting in the *Re*_8 signal generation. Then one of the eight pulses is selected by the binary code, which contains delay information about how many clocks (*clk*1)

the pulse is relatively delayed to the *Set* signal. When defining $\tau_{i,j}$ by the delay information of the pulse selected from the i-th DFF and j-th pulse among the eight pulses by the up/down counter, the $\tau_{i,j}$ can be derived as followings:

$$\tau_{i,j} = i + j \times 16. \tag{1}$$

For example, the pulse with $\tau_{1,2}$ has a 33 clock delay signal. Meanwhile, as seen in the figure, each code is designed separately. Therefore, when a carry occurs in the thermometer code, there should be a way to update it in the binary code. To do so, we make a carry high if all thermometer codes are 1 and the input is 1, and carry low, if all thermometer codes are 0 and the input is 0.

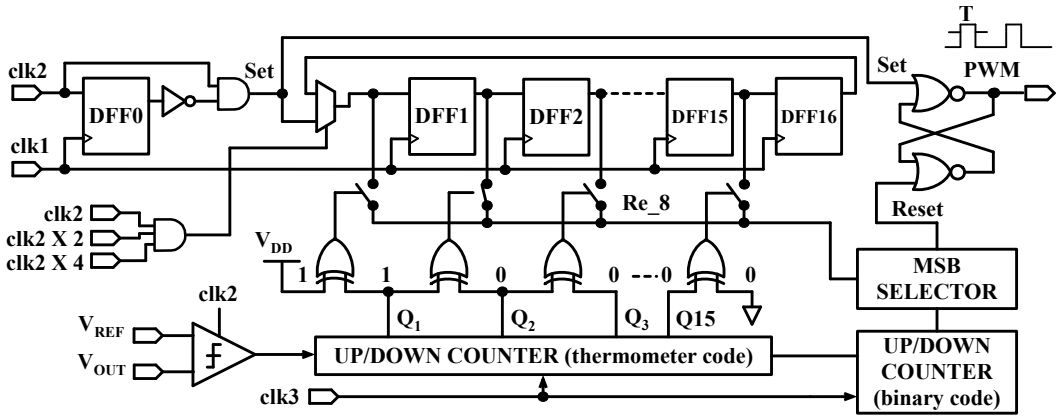

Figure 5. Block diagram of the proposed DPWM.

Figure 6 illustrates a detailed timing diagram of the proposed DPWM design. In this diagram, a pulse with $\tau_{1,2} = 33$ is selected as an example to show how to generate the PWM signal with $\frac{33 \times 100}{128}$% duty cycle. For the 2^7 resolution and 100 kHz switching frequency, *clk*1 and *clk*2 are set to 12.8 MHz and 100 kHz, respectively. When the pulse is selected from the binary code, the 3-bit MSB selector (cf. Figure 4) makes the MSB = 010 part HIGH to pass the selected pulse. Starting with *Set*, the PWM signal holds the on state until the pulse with $\tau_{1,2} = 33$ resets it to the off state.

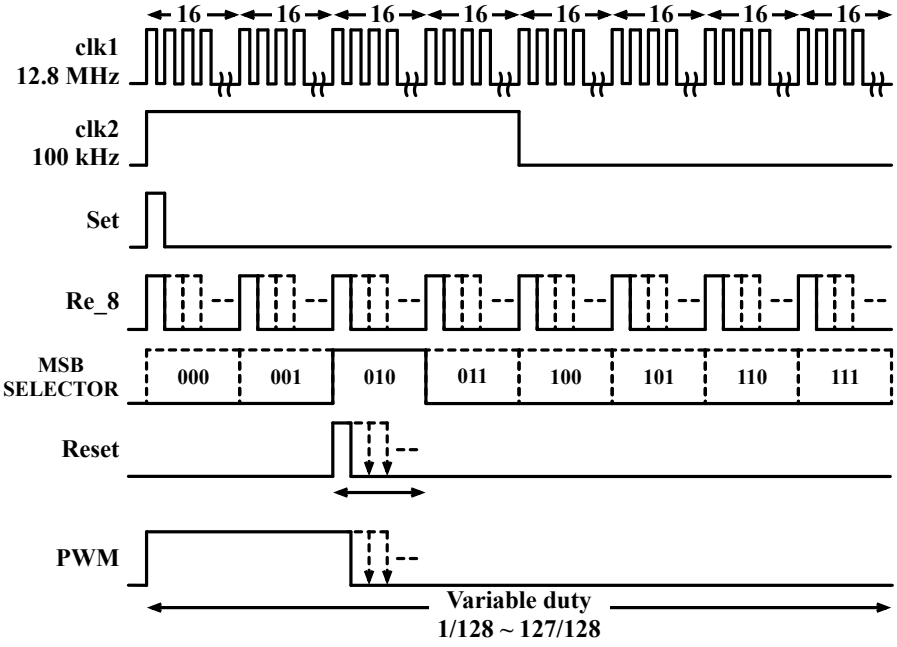

Figure 6. Timing diagram of the proposed DPWM.

Finally, the proposed DPWM and the conventional DPWM are both fabricated in Samsung 65 nm CMOS technology. For the ULV operation, we use the width sizing technique [14,15], so that all the digital circuits including DFFs, comparator, etc. in the proposed DPWM use the six times larger width transistors than the minimum sized transistor in the technology. In case for the conventional DPWM design, the width of the transistor is sized 24 to 30 times larger than the minimum sized transistor of the technology, in order to support a large number of fan-outs. In addition, we adopt the stacking limiting technique [16,17], so that the number of the stacked transistors is limited to four. The measured results of the fabricated chip demonstrates that the proposed one achieves significant area reduction and power savings (thereby power conversion efficiency enhancement), compared to the conventional one. The details will be presented in Experimental work.

4. Leverage the Proposed DPWM for Low Power Dynamic Switch Modulation

Dynamic switch width modulation (DSM, or power switch splitting method) is a special technique for increasing η under various load power conditions. This technique adaptively turns on or off some of the multiple parallel-connected switches in a DC–DC converter in response to dynamically changing load conditions, maximizing η at a given load power P_{load} [18–20]. Unfortunately, inevitable area/control overhead caused by the additional logics to detect the load conditions and control the switch selections has limited the efficacy of this technique. Furthermore, this overhead becomes even more severe when the DC–DC converter powers the ULP platform.

To tackle the overhead problem of the DSM and utilize it to improve η in full load power region of the ULP platforms, we propose a method that exploits the proposed DPWM design to control the power switch selection, instead of using additional detecting logics of the load condition in the conventional DSM. In other words, the proposed DC–DC converter design measures the load condition using a digital code originally designed for use in determining the duty cycle of the PWM signal in the proposed DPWM, which allows the selection of the appropriate switch among several switches. This eliminates the need for load condition detection circuitry for conventional DSMs. For example, the fabricated DC–DC converter targets the ULP platform in [2] is designed to have two different sizes of the power switches (i.e., the width of the big switch and that of the small switch are set to 4:1), and if the PWM duty cycle is less than 3/8, the small switch is selected, otherwise, the large switch is selected. In other words, the digital code $0110000_{[2]}$ is used as a condition to determine the size of the switches. As a result, the minimum conversion efficiency η_{min} is higher than 27% @ $P_{load} = 20\,\mu W$, and the conversion efficiency becomes higher than 60% when $P_{load} \geq 100\,\mu W$, and reaches up to the maximum efficiency $\eta_{max} = 92.77\%$ @ $P_{load} = 10$ mW. Detailed experimental results will be provided in the following section.

5. Experimental Work

Prototype chips of two DC–DC converters each using the proposed DPWM and the conventional DPWM design were fabricated in Samsung 65 nm technology, shown in Figure 7a, the test board of which is shown in Figure 7b. These DC–DC converters are designed specifically for powering the ULP IoT platform in [2]. The layout of the conventional DPWM and the proposed DPWM are shown left and right in Figure 7c, respectively. We used 220 µH inductor. As seen in this layout figure, the proposed DPWM is much smaller than the conventional DPWM, in that its area is 8500 μm^2 while the conventional one occupies 42,075 μm^2.

Figure 8 shows the measured power conversion efficiency of the two DC–DC converters, when the input voltage V_{input} and the output voltage V_{output} are 0.7 V and 0.48 V, respectively. In the figure, the black line with diamond marks indicates the efficiency of the converter with conventional DPWM and one big switch, which shows that η_{min} and η_{max} are 8.7% and 91.4%, respectively. The efficiency of the converter using the same big switches but with the proposed DPWM is indicated by the orange line with square marks, showing that η_{min} and η_{max} are 15.2% and 92.8%, respectively. The η's of the

proposed design were taken into account all the power consumption of the proposed DPWM including the increased power consumption due to the additional clock signal.

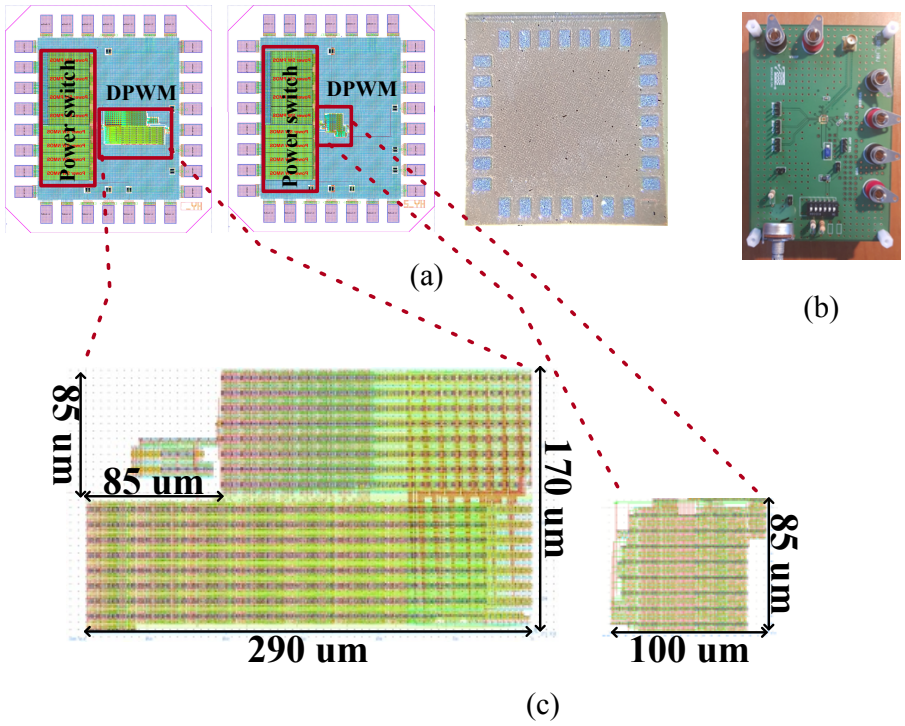

Figure 7. (**a**) Chip layouts and die photo, (**b**) test board, and (**c**) layout of (**left**) the proposed DPWM and (**right**) the conventional DPWM.

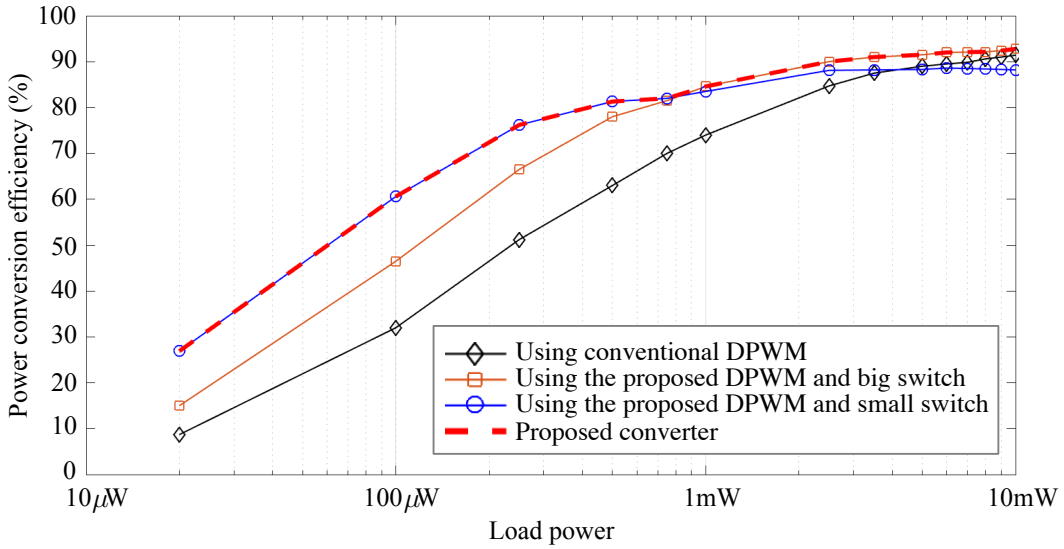

Figure 8. Measured η of the conventional and proposed converters.

In particular, the efficiency of the orange line in Figure 8 is higher than that of the black line under full load conditions, thanks to the power savings of the proposed DPWM. In addition, when adopting a DSM with multiple switches in the converter, that is, adding a small switch to a converter with a large switch, the efficiency of the converter will be greatly improved, which also can be seen in the figure. More precisely, the blue line with circle marks indicates the efficiency of the converter with the proposed DPWM and the small switch only. This line clearly shows that, when $P_{load} \leq 750\,\mu W$, the efficiency is much higher than the black line (e.g., the minimum efficiency at $P_{load} = 20\,\mu W$ increases to 26.9%,

which can be translated to the 18.2% efficiency improvement.) Finally, without additional circuitry, the DC–DC converter utilizes only digital code (e.g., $0110000_{[2]}$) in the proposed DPWM to selectively combine orange and blue lines to maximize efficiency under all load conditions. This combined line is shown by the red dotted line in the figure.

The comparison results between the proposed DC–DC converter and the converter with the conventional DPWM, plus the converter with the conventional APWM for reference are summarized in Table 1. When deriving the efficiencies of the converters, V_{input} of the converter with the conventional APWM is set to 1.2 V (i.e., this is because the APWM cannot operate in the ULV regime, due to the ramp generator and EA that are malfunctioned at the ULV), while those of the others are set to 0.7 V. All the V_{output} are set to 0.48 V. For the output current of the converter, I_{output} ranging from 20 µA to 20 mA, the efficiency of the converter with the conventional APWM is simulated and those of the converters with the DPWMs are measured with the fabricated chip. Because of the area/power overhead and design complexity due to the additional load condition detection logic, it is rare to apply DSM to existing DPWM-based DC–DC converters, so we do not apply DSM to the convention converters in the table. As expected, thanks to the proposed low power and small area DPWM, the control current I_{ctrl} is much smaller than the others, and the proposed converter shows excellent power conversion efficiency over the full range of P_{load}.

Table 1. Performance comparison of the conventional and proposed DC–DC converters.

Specification	Converter w/The Conventional APWM (Simulation)	Converter w/The Conventional DPWM (Measured)	The Proposed Converter (Measured)
ULV operation?	no	yes	yes
V_{input}	≥1.2 V	0.6 V∼1.2 V	0.6 V∼1.2 V
V_{output}	0.2 V∼0.6 V	0.2 V∼0.6 V	0.2 V∼0.6 V
I_{output}	20 µA∼20 mA	20 µA∼20 mA	20 µA∼20 mA
η_{max}	90.19%	91.46%	92.77%
η_{min}	11.59%	8.73%	26.99%
I_{ctrl}	203 µA	294 µA	36 µA
f_{sw}	100 KHz	100 KHz	100 KHz
Area	–	42,075 µm^2	8500 µm^2

6. Conclusions

We have presented a low power, small area, and high-resolution DPWM design that equips to the DC–DC converter to power the ULV operating IoT platforms. Through the experimental work with the fabricated DC–DC converters using the conventional DPWM and the proposed DPWM each, we have verified that the proposed converter achieves the higher power conversion efficiency under the full range of the load conditions while occupying a much smaller area. For targeting our prototype of the ULV operating IoT platform, the proposed converter have shown the most suitable specifications, especially in that it supports the high resolution (7-bit) of the voltage level control and its power conversion efficiency is higher than 27% under the lowest load power condition (20 µW) and reaches up to 92.7% at the highest load power condition (10 mW).

Author Contributions: W.H., W.L. and K.-H.B. were the main researchers who initiated and organized research reported in the paper, and all authors including K.Y. and D.V.T. were responsible for analyzing the simulation results and writing the paper. All authors have read and agreed to the published version of the manuscript.

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