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Switch Ladder Modified H-Bridge Multilevel Inverter With Novel Pulse Width Modulation Technique

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ABSTRACT It is difficult to make a structure of multilevel inverter for the efficient conversion of dc to ac having a smaller number of power electronic components, less switching losses, less voltage stress on switches, and a greater number of output voltage levels. To breakthrough this problem, a modification is performed in the existing H-bridge multilevel inverter to form a switch ladder modified H-bridge multilevel inverter (SLMHB-MLI). Moreover, for the minimization of maximum voltage rating on the switches and optimization of switching sequence of the multilevel inverter, a novel pulse width modulation (PWM) technique is proposed in this research. Furthermore, in SLMHB-MLI, the novel PWM technique is integrated with an ANDed PWM technique for the variation of output voltage magnitude. The usefulness of the proposed topology and PWM technique are confirmed via comparison with previous topologies simulation and experimentation, respectively.

INDEX TERMS ANDed and novel PWM techniques, switch ladder multilevel inverter, total harmonic distortion.

I. INTRODUCTION

Over the past few years, multilevel inverters (MLI) play a vital role for the conversion of DC to AC in industrial and renewable energy applications [1]. MLIs are able to produce output voltage in the form of stairs, which overlaps and close to sinusoidal waveform. Therefore, MLIs are considered to be better as compared to two level inverters in terms of applications [2], [3]. High efficiency and small amount of total harmonic distortion (THD) are the essential parameters for the applications of MLI [4]. Various topologies of MLIs have been discovered in the past few years and researchers are trying to make an efficient topology of MLI comprises of a smaller number of power electronics components and a greater number of output voltage levels, which increases its reliability, efficiency and ultimately the size of output filter reduces drastically. Generally, MLIs are divided into three fundamental types such as flying capacitors, diode clamped, and cascaded H-bridge MLIs. However, all these conventional topologies have some drawbacks such as a greater number of power electronic components, DC sources and capacitors, which make these conventional topologies impractical for industrial application. By observing the magnitude of DC voltage sources of MLI, it is further divided into symmetric and asymmetric configurations [5]–[10]. Moreover, the MLIs comprising of equal magnitude of DC voltage sources categorized as symmetric, while MLIs with different DC voltage magnitudes are termed as asymmetric MLIs. The staircase (SC) MLI is classified as low-frequency inverters [11]–[13]. In SC-MLIs, all the switches accompanied in the configuration are controlled by low-frequency signals [14], [15]. However, SC-MLI comprises of a large number of power electronic components, which ultimately increases losses. The most recent topology of the inverters described in [22]–[24] have a smaller number of levels and more switching losses due to many switches.

Besides the conventional topologies of MLIs, the topologies comprise of cascaded H-bridge (CHB) have

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simple structure. However, these topologies have an issue of isolated DC sources [25]. MLI is used in various applications such as electric machine drives [26] and grid connectivity [27]. On the other hand, the use of MLIs are advancing in the field of photovoltaic (PV) system [28], [29], optimized topologies [30]–[32] and control techniques [33], [34]. However, all these MLIs have some drawbacks regarding complexity, applications, number of components and control strategy. By increasing the number of components in a structure of MLI make it more complex and costly. Due to which, an evolution of making the new efficient topology is under evolution. A new topology of hybrid MLI is presented in [35], comprises of a smaller number of components and their DC sources are symmetrical in nature. However, this topology lags behind, when compared with asymmetric MLIs. To mitigate the problem of symmetric and asymmetric complexities of DC sources, a new structure is developed in [36]. However, it comprises of a large number of components and DC sources when compared with the new topology of modified H-bridge MLI as presented in this paper. To reduce the cost, voltage stress on switches and switching losses, a new symmetric topology of MLI is developed in [37]. This topology uses two types of switches such as low frequency and high voltage switch and high frequency and low voltage switch. However, this topology has unequal voltage distribution across its switches, which restricts it for high voltage applications. Another new topology of symmetric MLI is presented in [38] which has optimized structure regarding number of components. However, this topology has serious issue in its control technique because of the loss of modularity. In [39], a new structure is developed based on the concept of hybrid MLI to boost the magnitude of the output voltage. Contrarily, this topology has a large number of power electronic components which makes it more complex and impractical due to more switching losses. The problem of isolated DC sources is resolved in Packed U-Cell (PUC) topology [40]. It uses a smaller number of components and a small amount of isolated DC sources. However, most of the topologies presented in published papers are focusing on the greater number of output voltage levels by ignoring the number of unidirectional and bidirectional switches, reliability and efficiency.

The switching technique of PWM plays a vital role in the performance of MLI. Various switching techniques have been developed. Furthermore, MLIs incorporating low switching frequency techniques provide good performance as compared to MLIs with high switching frequency techniques [41]. However, transient response of the MLI is improved, while it is operating on high switching frequency technique. Various high switching frequency technique includes sinusoidal PWM (SPWM), space vector PWM (SVPWM), level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) [42] [43]. In SPWM, it is easy to implement and it does not need any optimization algorithm for optimized switching [44]–[47]. Furthermore, due to high switching frequency, SPWM causes large amount of switching losses [48] [49]. In SVPWM, the amount of THD is less [18], [42], [43]. Moreover, the switching sequences can be controlled and optimized [50]. On the other hand, due to the space vectors the switching scheme become more complex and clarke transformation is used for a single-phase application [51]–[53]. LSPWM technique is considered to be the useful for the minimization of THD [54]. Furthermore, this technique does not have complex structure [55]. Moreover, if the capacitors are present in the topology, the control of switching sequence becomes more complex and it is not suitable for the topologies of flying capacitor (FC) and cascaded H-bridge (CHB) [56]–[58].

To mitigate the existing problems of LSPWM, another technique was introduced termed as PSPWM [59]–[65]. This technique is suitable for FC and CHB topology and it is easy to control the topologies comprising of capacitors [62]. Furthermore, it produces a large amount of THD and due to phase shifting technique, synchronization with the grid became challenging issue [64], [65].

Switching losses play a vital role in the performance of MLI. The researchers have developed the techniques having low or fundamental switching frequency such as selective harmonic elimination (SHE), nearest level control (NLC) and space vector control (SVC). Although all these techniques have less amount of THD. However, these techniques became complex and impractical, if used on a large scale [66]–[74].

In this paper, to address the problems of maximum voltage rating on the switches, number of components, amount of THD, and number of output voltage levels, a modified H-bridge MLI is proposed in this paper. Moreover, the switches used in the proposed topology are all unidirectional. Furthermore, a novel PWM technique is developed, which is used to optimize the switching sequence of the MLI to decrease the switching losses and maximum voltage stress on the switches. On the other hand, for the variation of the output voltage magnitude, the ANDed PWM technique is integrated with a novel PWM technique. The induction motor (IM) is fed on SLMHB-MLI operating on novel PWM technique and compared with another IM operating on an ideal AC supply. To validate the proposed topology, it is compared with conventional and recently developed topologies.

The remaining paper is classified as: Section II proposed a modified H-bridge MLI. The novel and ANDed PWM techniques are proposed in Section III. The comparison of the proposed topology is performed in Section IV. Section V is the simulation and discussion of SLMHB-MLI. Section VI shows the experimental results gathered through the hardware followed by the conclusion in Section VII.

II. PROPOSED SWITCH LADDER MODIFIED H-BRIDGE MULTILEVEL INVERTER (SLMHB-MLI)

Fig. 1 shows a circuit diagram of the proposed topology comprising of 2 DC sources (V_1, V_2), 4 capacitors (2 of C_1, 2 of C_2), 8 unidirectional switches (S_1, $S_2 \ldots$, S_8) and 14 freewheeling diodes connected across each switch. Moreover, Fig. 1 shows the conversion of bidirectional

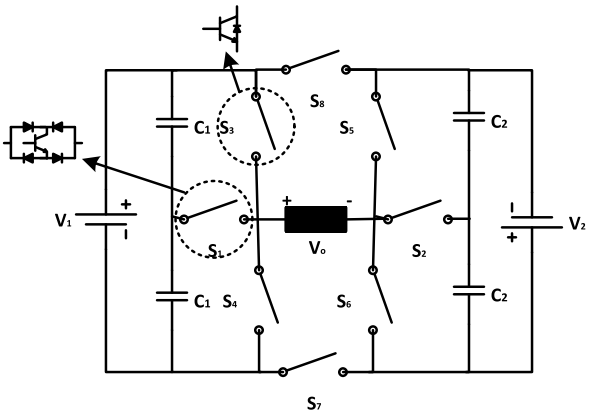

FIGURE 1. Schematic of the SLMHB-MLI.

switches (S_1, S_2) to unidirectional switches termed as "converted unidirectional switches" of the proposed topology. Due to the closed loop structure at every switching sequence, all the switches of the SLMHB-MLI should not be turned on at the same time, otherwise random voltage occurs across the connected load. The 2 capacitors on the left side (C_1) and 2 capacitors on the right side (C_2) are identical with each other and used for the voltage divider. The necessary conditions for the efficient capacitive voltage division includes: both the pair of capacitors (C_1, C_2) should be of the same value and belong to the same manufacturer; the voltage rating of the capacitors should meet the minimum requirements of the DC voltage source with which it is connected. Moreover, for the efficient capacitive voltage division, a large value of resistors (Mega Ohms) are connected in parallel with each capacitor, to have equal voltage across these resistors. These capacitors play a vital role for the generation of a large number of voltage levels at the output.

A. ALGORITHMS FOR THE SELECTION OF DC VOLTAGE MAGNITUDES

The magnitude of DC voltage sources attached with the MLI plays a vital role in the generation of output voltage levels. For the appropriate selection of the DC voltage magnitude, the number "n" of converted bidirectional switches (S_1, S_2) are considered. For this purpose, two algorithms are defined.

In the first algorithm, the DC sources of the SLMHB-MLI are identical and of same value as presented below:

$$V_1 = V_2 = V_{DC} \tag{1}$$

The maximum voltage generated at the output of the proposed topology is:

$$V_{o(max)} = (n)(V_{DC}/2 + V_{DC}/2) \tag{2}$$

In the second algorithm, the values of DC sources have a different magnitude as shown below:

$$V_1 = V_{DC};\ V_2 = 3V_1 = 3V_{DC} \tag{3}$$

TABLE 1. Classification of voltage magnitude at the output.

Switching Sequence								V_o
S1	S2	S3	S4	S5	S6	S7	S8	
0	0	1	0	1	0	1	0	V_1+V_2
1	0	0	0	1	0	1	0	$V_1/2 + V_2$
0	1	1	0	0	0	1	0	$V_1 + V_2/2$
1	1	0	0	0	0	1	0	$V_1/2 + V_2/2$
0	0	0	1	1	0	1	0	V_2
0	0	1	0	0	1	1	0	V_1
0	1	0	1	0	0	1	0	$V_2/2$
1	0	0	0	0	1	1	0	$V_1/2$
0	0	1	0	1	0	0	1	0
1	0	0	0	1	0	0	1	$-V_1/2$
0	1	1	0	0	0	0	1	$-V_2/2$
0	0	0	1	1	0	0	1	$-V_1$
0	0	1	0	0	1	0	1	$-V_2$
1	1	0	0	0	0	0	1	$-V_1/2 - V_2/2$
0	1	0	1	0	0	0	1	$-V_1 - V_2/2$
1	0	0	0	0	1	0	1	$-V_1/2 - V_2$
0	0	0	1	0	1	0	1	$-V_1 - V_2$

The maximum voltage generated at the output by using distinct values of DC sources is:

$$V_{o(max)} = (n)(V_{DC}/2 + 3V_{DC}/2) \tag{4}$$

In conclusion, by selecting the appropriate magnitude of the DC voltage sources, the number of output voltage levels are adjusted. For example, by selecting $V_1 = V_2 = V_{DC}$, the output voltage comprising of 9 levels having the voltage levels of $0V_{DC}$, $\pm V_{DC}/2$, $\pm V_{DC}$, $\pm 3V_{DC}/2$ and $\pm 2V_{DC}$ are obtained. While, by selecting $V_1 = 1V_{DC}$ and $V_2 = 2V_{DC}$, 13 levels at the output voltage are generated. To obtain 17 levels at the output the voltage magnitudes are adjusted in such a way that $V_1 = 1V_{DC}$ and $V_2 = 3V_{DC}$.

The general formulas for calculating the number of components for the SLMHB-MLI are:

Number of switches $= N_{Switches} = (N - 1)/2$

Number of DC sources $= N_{DC\_Sources} = (N + 3)/10$

Number of gate drivers $= N_{Drivers} = (N - 1)/2$

Number of distinct voltage sources $= N_{Variety} = (N + 3)/10$

The output of 17 level MLI based on their magnitude is shown in Table 1.

By applying gate pulses according to the configuration given in Table 1, output voltage levels are obtained accordingly. The schematics of different switching states of the SLMHB-MLI are shown in Fig. 2. As shown in Fig. 2, all the switches operate to make a close path, so that none of the switch overlaps with other one to prevent from short-circuiting.

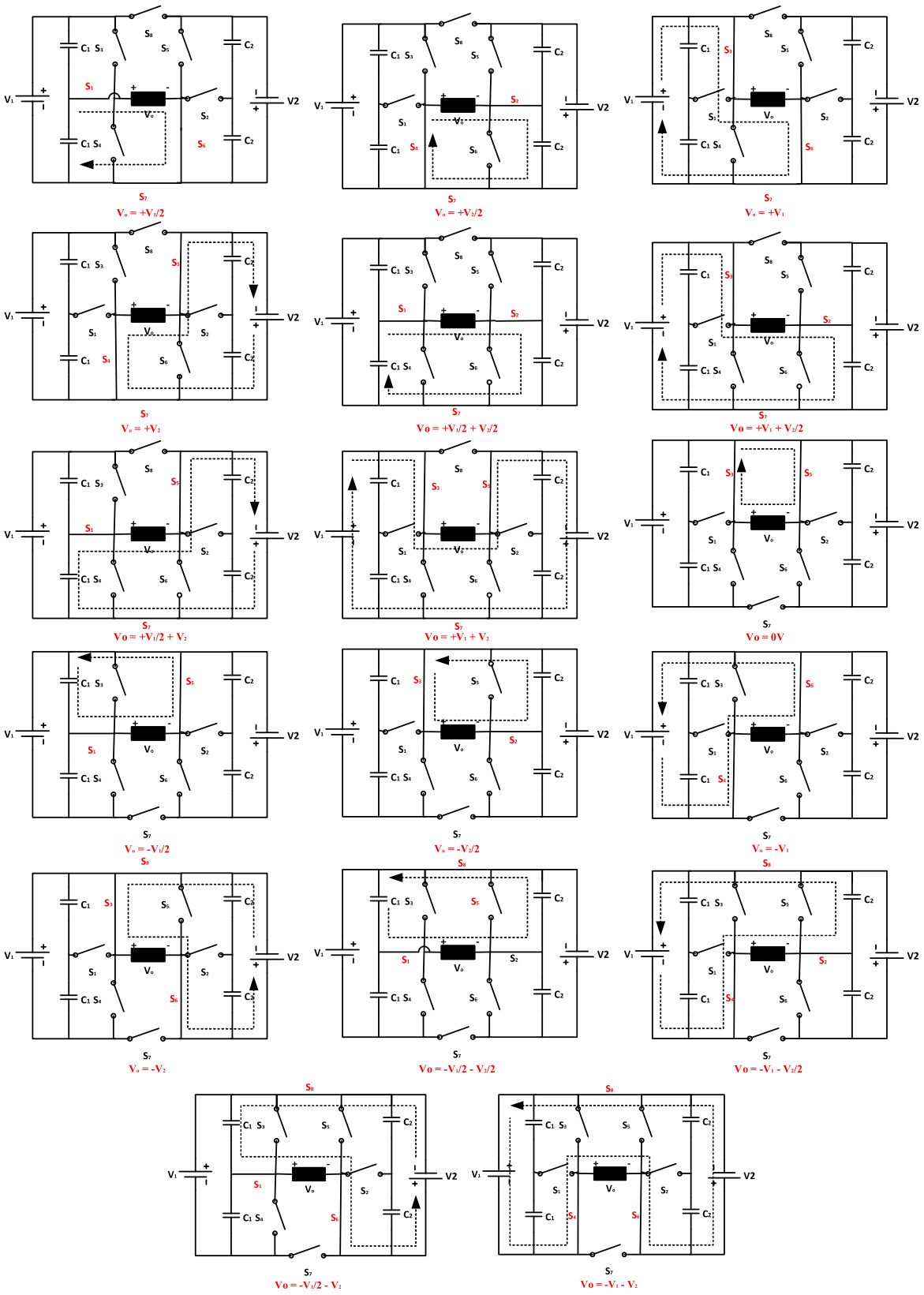

FIGURE 2. Schematic of different switching states of the proposed topology (SLMHB-MLI).

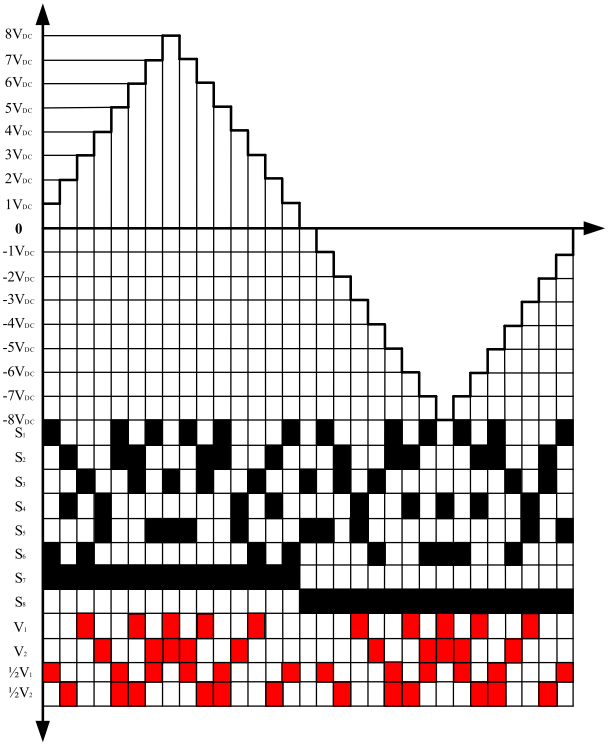

FIGURE 3. Switching pattern of the SLMHB-MLI of one cycle.

Fig. 3 shows the switching pattern of the proposed topology for the duration of one cycle. As shown in Fig. 3, only 3 switches conduct for the generation of each voltage level. Hence, switching frequency decreases. Moreover, S_3, S_5 and S_8 conducts for the generation of zero voltage. The conduction path of all the respective voltage levels is shown in Fig. 2. The DC sources employed for the generation of respective voltage level is also shown in Fig. 3.

B. TOTAL MAXIMUM VOLTAGE RATING (TMVR) ON ALL THE SWITCHES

The maximum voltage rating of the unidirectional ($MVR_{U.Sw}$) and bidirectional switches ($MVR_{B.Sw}$) are:

$$MVR_{U.Sw} = \sum_{i=3}^{8} V_{Si} \tag{5}$$

$$MVR_{B.Sw} = \sum_{i=1}^{2} V_{Si} \tag{6}$$

where V_{Si} represents the maximum voltage on the respective switches $S_1, S_2 \ldots, S_8$.

$$V_{S1} = V_{S2} = V_1 + V_2 \tag{7}$$

$$V_{S3} = V_{S4} = V_1 \tag{8}$$

$$V_{S5} = V_{S6} = V_2 \tag{9}$$

$$V_{S7} = V_{S8} = V_1 + V_2 \tag{10}$$

The total maximum voltage rating ($TMVR$) on all the switches of SLMHB-MLI is:

$$TMVR = MVR_{U.Sw} + MVR_{B.Sw} \tag{11}$$

By using (3) and (5-10) $TMVR$ comes out to be:

$$TMVR = 6V_1 + 6V_2 \tag{12}$$

$$TMVR = 24V_1 = 24V_{DC} \tag{13}$$

From (13) it is concluded that, the $TMVR$ of all the switches depends on the magnitude of V_{DC}

C. CALCULATION OF LOSSES

The losses of the MLI comprised of conduction and switching losses. The conduction losses ($P_{loss,c}$) occur while the MLI is in operation. These losses are due to the switches (IGBTs/MOSFETs) and diodes present in a conduction path. The losses occur in switch ($P_{switch}(t)$) and diode ($P_{diode}(t)$) while the operation of the MLI are described as:

$$P_{switch}(t) = \left[V_{switch} + R_{switch} i^{\beta}(t)\right] i(t) \tag{14}$$

$$P_{diode}(t) = \left[V_{diode} + R_{diode} i(t)\right] i(t) \tag{15}$$

In this, V_{switch} and V_{diode} are the voltage drop across switch and diode respectively, while they are conducting. Similarly, R_{switch} and R_{diode} are the resistances of the switch and diode respectively. Moreover, β represents the switch constant.

The switching losses ($P_{switching}$) occur during the turn-on and turn-off time of the switches (IGBTs). $P_{loss,turn-on}$ and $P_{loss,turn-off}$ are the powers, which are lost during the turn-on and turn-off operation of the switches respectively, as described below:

$$P_{loss,turn-on} = \int_0^{t_{on}} v(t)\, i(t)\, d(t) \tag{16}$$

$$P_{loss,turn-on} = \frac{1}{6} v_{sw} I_{on} t_{on} \tag{17}$$

$$P_{loss,turn-off} = \int_0^{t_{off}} v(t)\, i(t)\, d(t) \tag{18}$$

$$P_{loss,turn-off} = \frac{1}{6} v_{sw} I_{off}\, t_{off} \tag{19}$$

where v_{sw} represents the voltage on the switch, while it is not conducting. However, I_{on} and I_{off} represents the current on the switch during and before its conduction respectively.

The total loss (P_{loss}) of the SLMHB-MLI will be:

$$P_{loss} = P_{loss,c} + P_{switching} \tag{20}$$

$$P_{loss} = (P_{switch}(t) + P_{diode}(t)) + (P_{loss,turn-on} + P_{loss,turn-off}) \tag{21}$$

To show the competency of the proposed SLMHB-MLI practically, $R_{switch} = 0.15\Omega$, $R_{diode} = 0.1\ \Omega$, $V_{switch} = 2.5$V, $V_{diode} = 1.5$V, $\beta = 1$, and $t_{on} = t_{off} = 1us$ are selected respectively.

The losses of the SLMHB-MLI are examined for the duration of two cycles. Moreover, the efficiency of the proposed topology is 99.71% because of novel PWM technique having less switching losses. By considering all the above-mentioned parameters for the implication of SLMHB-MLI practically, input power, output power, P_{loss} and efficiency are presented in Fig. 4 (a), (b) and (c) respectively.

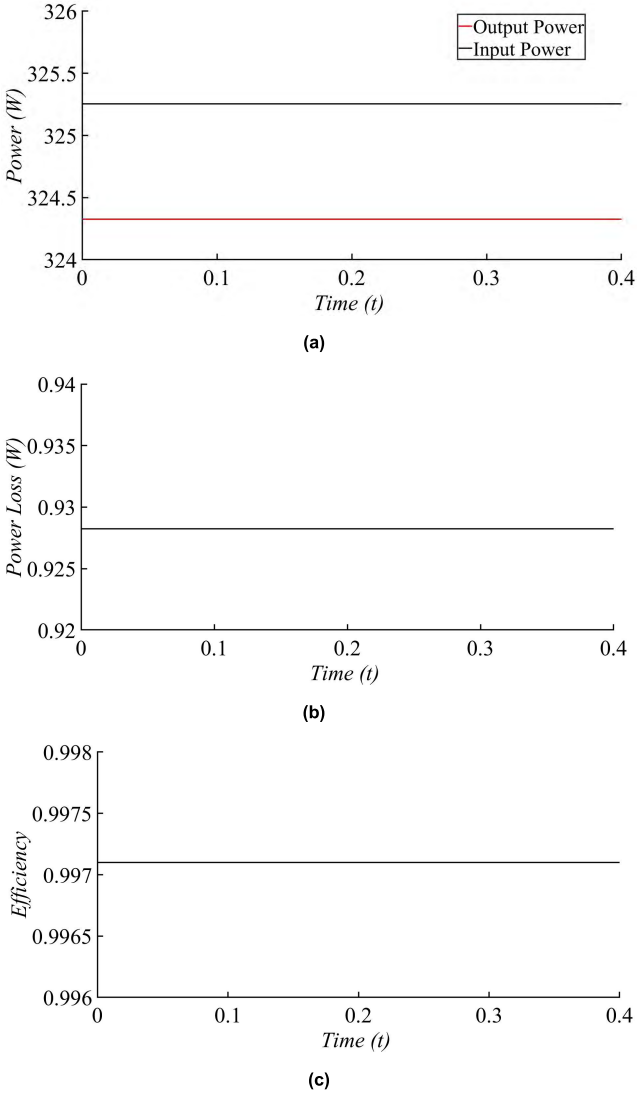

FIGURE 4. (a) Input and output power; (b) P_{loss}; (c) efficiency; of the SLMHB-MLI.

III. IMPLEMENTATION OF NOVEL AND ANDed PWM TECHNIQUES

In novel PWM technique, the reference sine wave of a particular frequency (50Hz) is selected. Moreover, after the selection, the sampling of the one cycle of a reference sine wave (V_R) is performed and the aforementioned samples are stored in an array with respect to their voltage magnitudes. On the other hand, the switching sequence (S_I) and voltage magnitudes (V_I) of the SLMHB-MLI are stored in the separate arrays. The optimized switching sequence in novel PWM technique is selected by the process of comparison between V_R and V_I to make the output of the MLI overlapping the ideal sine wave incorporating the minimum switching losses.

If the V_R is less than or equal to V_I, then the switching sequence of the SLMHB-MLI (S_I) generating the respective voltage level (V_I) is selected. Moreover, the V_I is maintained and V_R is moved towards the next sample. However, if the V_R is greater than V_I, then both the switching sequence (S_I) and the voltage magnitude of reference sine wave (V_R) move towards the next sample respectively, and again the process of comparison is performed for the optimized switching sequence. Fig. 5 shows the block diagram of novel PWM technique.

In ANDed PWM technique, the gate pulses or optimized switching sequence, generated from the novel PWM technique are logically ANDed with the pulse train of 5kHz through the AND gate in order to obtain the required ANDed PWM sequence. These output sequences are provided to the gate signals of switches of the SLMHB-MLI. The pulse train signal of 5kHz is generated by the microcontroller through which the duty cycle of the pulse train signal can also be changed. In ANDed PWM technique, the voltage magnitude of the output voltage is varied by changing the duty cycle of the pulse train signal. Hence, it can be used for the speed control of an induction motor. Fig. 6 shows the block diagram of ANDed PWM technique.

In ANDed and novel PWM techniques, zero voltage level is generated through the semiconductor switches (MOSFETs). All the inner switches are responsible for the zero-voltage level generation. This topology does not need the injection of any external voltage for the generation of zero voltage level at the output. The switching sequence of zero voltage level in both PWM techniques remains same.

The switching frequency of the proposed topology working on the novel PWM technique is 2kHz and only 3 switches conduct for each output voltage level. Henceforth, the switching losses are very small.

A. DESIGNING OF FILTER

Although the proposed topology is able to produce 17 levels at the output voltage, but still small number of harmonics exist at the output voltage, reduces the efficiency of the SLMHB-MLI. To remove such harmonics, filters are used before the output voltage. Amongst L, LC, and LCL filters, LC filter is used for the removal of harmonics and improving THD. Because, L and LCL filters give bad performance and increase the complexity and cost of the filter. L and C refers to the inductor and capacitor, respectively.

To find the value of L and C, the equation is used as written below:

$$10F_o \leq F_r \leq \frac{F_{sw}}{2} \tag{22}$$

where, F_o, F_r and F_{sw} represents the frequency of the output voltage, resonance frequency and switching frequency of SLMHB-MLI, respectively. Furthermore, the F_r is calculated by using the equation below:

$$F_r = \frac{1}{2\pi\sqrt{LC}} \tag{23}$$

To calculate the suitable values of L and C, the resonance frequency of between 500Hz to 1kHz is tested and value of THD is calculated. By doing this process, the THD of SLMHB-MLI is improved to some extent. Table 2 shows the parameters of filter at different switching frequencies.

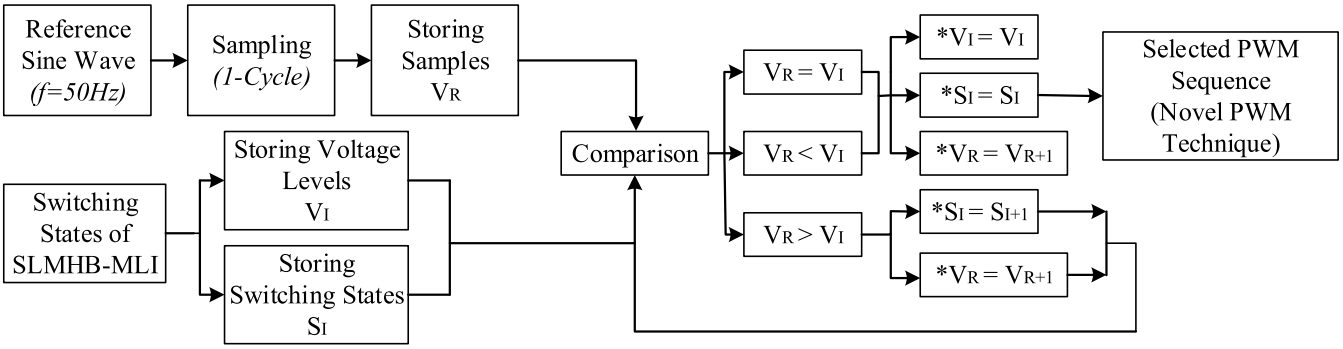

FIGURE 5. Novel PWM technique.

TABLE 2. Parameters of filter.

F_r	C(F)	L(H)
500	4.7μ	21.56E-03
550	4.7μ	17.82E-03
600	4.7μ	14.97E-03
650	4.7μ	12.75E-03
700	4.7μ	10.99E-03
750	4.7μ	9.58E-03
800	4.7μ	8.42E-03
850	4.7μ	7.46E-03
900	4.7μ	6.65E-03
950	4.7μ	5.97E-03
1000	4.7μ	5.39E-03

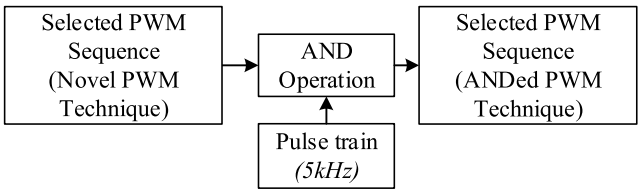

FIGURE 6. ANDed PWM technique.

The THD of 17 level SLMHB-MLI without using any filter is 6.19%. Furthermore, by incorporating filter at the output of the proposed topology reduces the THD to the amount of 5.463%. Moreover, almost 11.74% of THD improves as compared to unfiltered output of SLMHB-MLI. To improve the THD, filter is operated at F_r of 625Hz having L=13.8mH and C=4.7μF. Fig. 7 shows the amount of THD at different values of F_r.

Fig. 8 shows the complete circuit diagram of SLMHB-MLI connected with the load and grid side connection. If the amount of power is more than the connected load then the grid-tied MLI is used for the supply of power to the utility grid. As shown in Fig. 8, any kind of renewable energy source can be used for the generation of DC voltage. These DC voltages are attached with the SLMHB-MLI, operating on the novel and ANDed PWM technique, according to the load demand and category. The low pass filter LC in novel PWM technique, used at the output for minimizing the THD is optional because the amount of THD is about 6.19% without

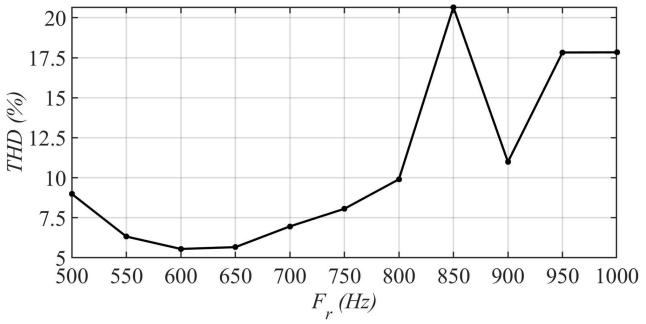

FIGURE 7. THD of SLMHB-MLI at different values of F_r.

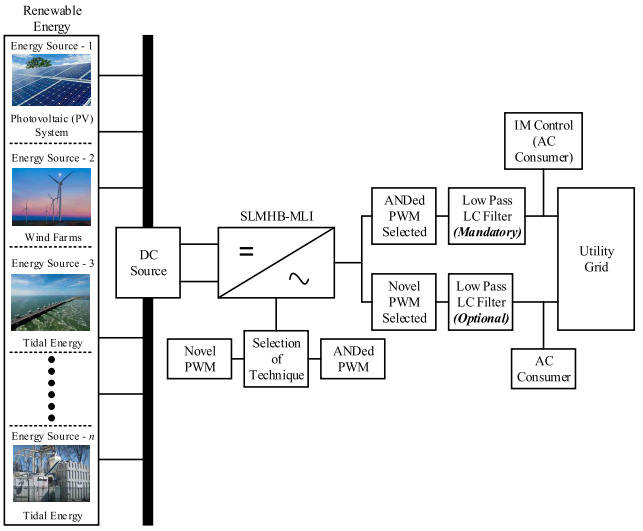

FIGURE 8. Complete circuit diagram of SLMHB-MLI.

using any filter. Contrarily, filter is necessary in ANDed PWM technique. Thus, the proposed SLMHB-MLI can also be used without using any filter.

IV. COMPARISON WITH THE PREVIOUS TOPOLOGIES

To justify the efficiency of proposed topology, it is compared with the previous topologies on the basis of number of switches ($N_{Switches}$), DC sources ($N_{DC\_Sources}$), gate drivers ($N_{Drivers}$), distinct voltage sources ($N_{Variety}$) and total

TABLE 3. Comparison of proposed topology with other fundamental topologies.

Inverter Type	Flying Capacitor	Neutral Point Clamped (NPC)	Reverse Voltage Topology	Cascaded	Proposed Topology
MOSFETs	6(N-1)	6(N-1)	3((N-1) +4)	6(N-1)	(N-1)/2
Diodes across MOSFETs	6(N-1)	6(N-1)	3((N-1) +4)	6(N-1)	(N+11)/2
Clamping Diodes	0	3(N-1) (N-2)	0	0	0
Isolated DC Sources	(N-1)	(N-1)	(N-1)/2	3(N-1)/2	(N+3)/10
Flying Capacitors	3/2 (N-1) (N-2)	0	0	0	0
Total Number of Components	½(N-1) (3N+20)	(N-1) (3N+7)	(13N+35)/2	27/2 (N-1)	11(N+53/11)/10

TABLE 4. Comparison of SLMHB-MLI with recent developed topologies.

Components	[74] & [75]	[76]	[77]	[78]	[79]	[80]	[81]	[82]	[83]	[84]	[85]	[86]	Proposed SLMHB-MLI
Unidirectional Switches	6	6	6	12	16	20	16	15	8	6	8	13	8
Bidirectional Switches	2	7	3	0	0	0	0	0	1	1	0	0	0
DC Sources	4	2	4	2	4	8	1	1	3	3	3	1	2
Diodes	10	22	12	12	28	32	16	16	10	8	8	14	14
Gate drivers	8	13	9	12	16	20	16	15	9	7	8	13	6
Levels	17	17	17	17	17	17	17	17	15	11	13	17	17

maximum voltage rating (*TMVR*). Fig. 9 (a) shows the SLMHB-MLI has a smaller number of switches compared to [10], [22], [23], modular multilevel converter (MMC), and [12]–[20]. The proposed topology requires 2 DC sources than the MMC and other topologies presented in [11]–[23], as shown in Fig. 9 (b). The cost of MLI depends on the *TMVR* on all the switches involved in the topology. Therefore, the proposed configuration is premeditated in such a way that it has less value of *TMVR* across all the switches. Fig. 9 (c) shows the SLMHB-MLI has a lower voltage rating as compared to [10], [12] and [15]–[23]. Fig 9 (d) represents the number of gate drivers required for the MLI, which is less in number as compared to configurations presented in MMC, [10]–[18] and [21], [23]. The distinct values of DC sources play a vital role in the levels of MLI as shown in Fig. 9 (e). The magnitudes of DC sources are adjusted in such a way that it gives 17-levels at the output by using minimum number of distinct DC sources compared to [14]–[17] and [19]–[22].

The SLMHB topology is also compared with the fundamental topologies to prove the merits of the SLMHB-MLI as shown in Table 3. While, in Table 3, "N" represents the number of levels generated at the output. Table 3 concludes that, the proposed SLMHB-MLI has a smaller number of power electronic components as compared to other topologies.

The quantitative comparison of the proposed SLMHB-MLI is performed with the recently discovered topologies developed in 2018 and 2019 as shown in Table 4. The Table 4 portrays that the proposed topology uses a smaller number of switches (unidirectional and bidirectional switches) as compared to the topologies presented in [74]–[86]. However, the number of switches in the topology of [84] are less than the proposed topology.

Moreover, the number of DC voltage sources in SLMHB-MLI is also less than or equal to the topologies of [74]–[80], [83]–[85]. However, the structure of MLI presented in [81], [82], [86] uses a smaller number of DC voltage sources, but due to single DC voltage source, a large number of capacitors are installed in the structure, which causes serious issue of voltage balancing. The number of diodes in the proposed topology are less than the structures of [76], [79]–[82] as compared to other topologies listed in the Table 4. The greater number of gate drivers, increases the complexity of the structure. Hence, the SLMHB-MLI has a smaller number of gate drivers as compared to other recently developed topologies presented in the Table 4.

V. SIMULATION AND DISCUSSIONS

To validate the effectiveness of a proposed topology, the experimental and simulation results of 9-levels and 17-levels are presented. Moreover, the IM is fed to the SLMHB-MLI operating on Novel PWM technique.

A. SIMULATION OF 9-LEVELS AND 17-LEVELS SLMHB-MLI ON NOVEL PWM TECHNIQUE

By selecting the identical values of DC sources ($V_1 = V_2 = 100$V), 9-levels are generated at the output. Because of same magnitudes of DC voltage sources, it is termed as symmetric MLI. The RL (resistive-inductive) load is connected to the inverter so that R=260Ω and L=100mH. As shown in Fig. 10, 9 distinct voltage levels are generated at the output with a positive and negative peak at 200V and −200V, respectively. Similarly, Fig. 11 represents the THD of 9 level MLI having the value of 20.15%.

For 17 level MLI, the magnitude of DC voltage sources are adjusted in such a way that: $V_1 = 25$V and $V_2 = 75$V.

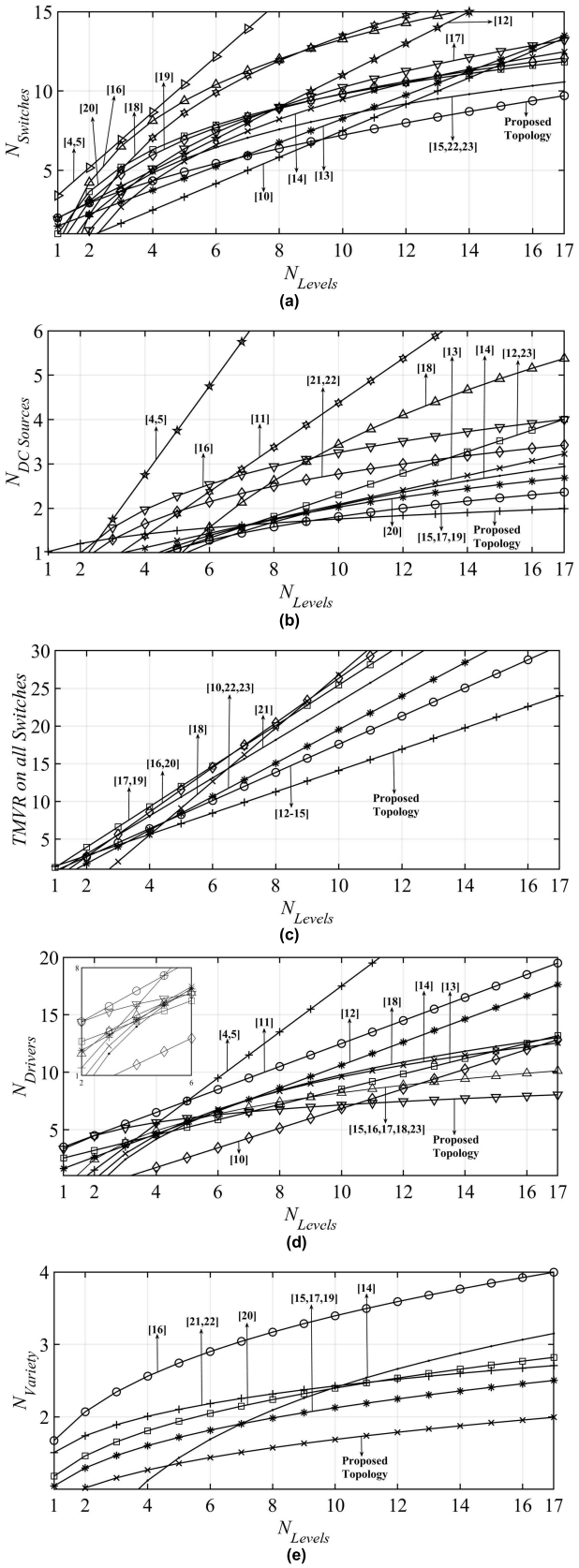

FIGURE 9. Comparison of (a) $N_{Switches}$ (b) $N_{DC\_Sources}$ (c) *TMVR* (d) $N_{Drivers}$ (e) $N_{Variety}$; with respect to other topologies.

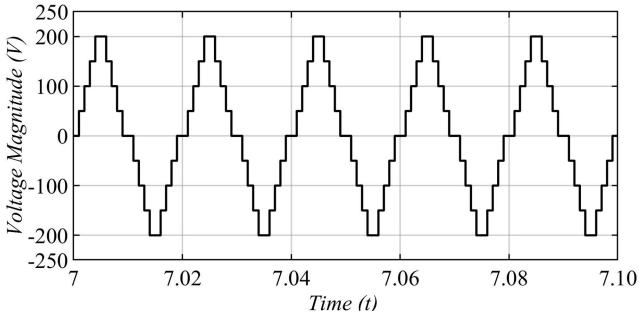

FIGURE 10. Output waveform of 9-level MLI operating on novel PWM. technique.

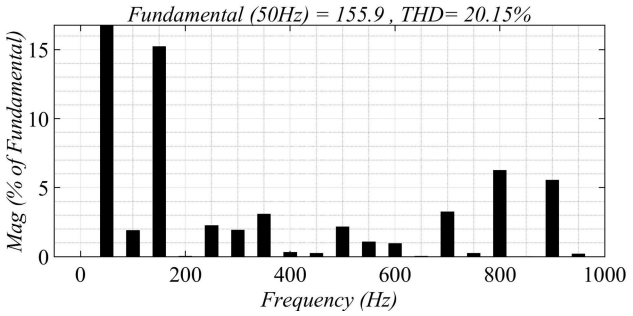

FIGURE 11. THD of 9-level MLI operating on novel PWM technique.

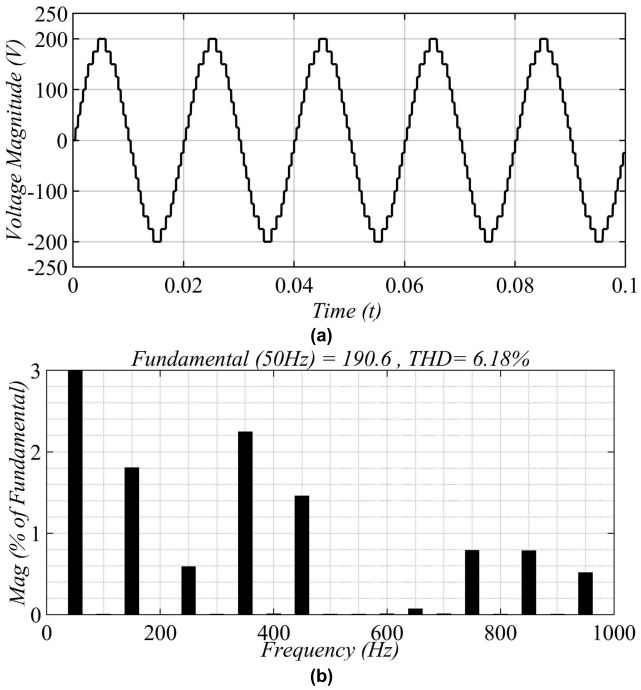

FIGURE 12. (a) Output waveform of 17 level SLMHB-MLI (b) THD of the proposed topology; operating on novel PWM technique.

RL load which is connected across the MLI comprises of: R=30Ω and L=110mH. As shown in Fig. 12 (a), it is concluded that by selecting the appropriate magnitude of DC voltage sources, a greater number of output voltage

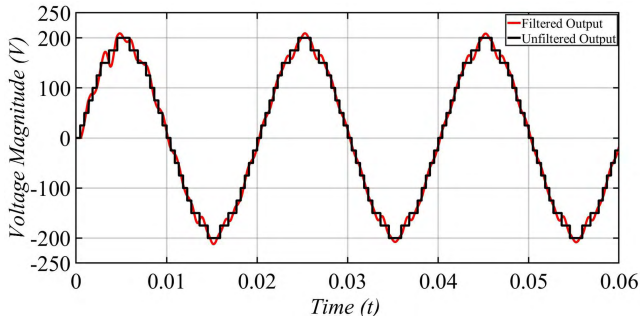

FIGURE 13. Filtered and unfiltered output waveform of SLMHB-MLI operating on novel PWM technique.

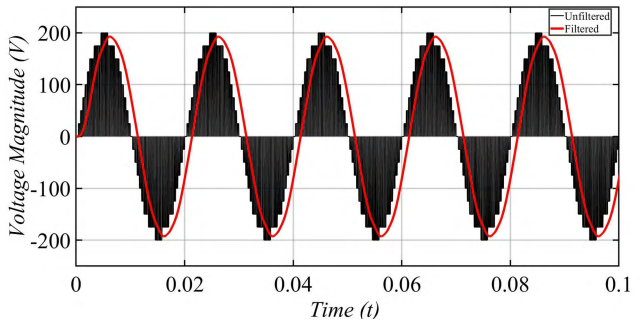

FIGURE 14. Filtered and unfiltered output waveform of SLMHB-MLI operating on ANDed PWM technique.

levels are attained. Furthermore, it shows that the 200V is the peak output voltage of the proposed topology. The THD associated with the proposed topology is 6.18% as shown in Fig. 12 (b). Although the THD of 17 level MLI is not large in amount. However, LC filter is designed which reduces the THD of 17 level inverter to about 11.74%. F_r of the designed filter is 625Hz having L=13.8mH and C=4.7μF. The output of the SLMHB-MLI after passing through the filter is shown in Fig. 13.

B. SIMULATION OF 17-LEVELS SLMHB-MLI ON ANDed PWM TECHNIQUE

In ANDed PWM technique, after the AND operation the THD of the output voltage increases to about 100%. A low pass LC filter is designed to reduce the amount of THD. Fig. 14 indicates the filtered and an unfiltered output of MLI. In this technique, the values of DC sources are: $V_1 = 25V$ and $V_2 = 75V$. The load connected across this technique is classified as: R = 30 Ω and L=110mH.

Fig. 14 proves that after passing through the filter, the magnitude of output voltage decreases slightly from 138.1V (RMS) to 137V (RMS). Furthermore, due to filter the filtered output voltage produces a delay of about 1.350ms.

The unfiltered three-phase output of a proposed topology with ANDed PWM technique having the duty cycle of 99% is shown in Fig. 15.

On the other hand, after passing through the low pass filter, the THD is reduced and the output of the filtered three-phase SLMHB-MLI at 99%, 70% and 50% duty cycle is presented in Fig. 16 (a), (b) and (c), respectively. Fig. 15 and

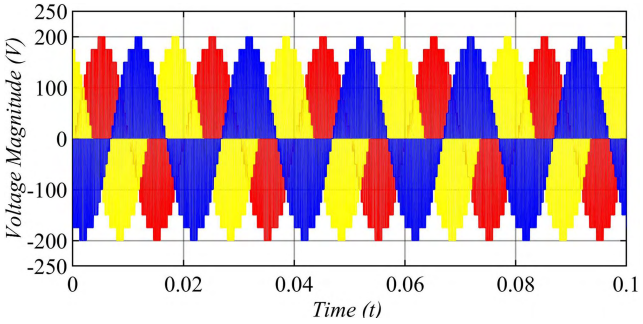

FIGURE 15. Unfiltered three phase output waveform of SLMHB-MLI operating on ANDed PWM technique.

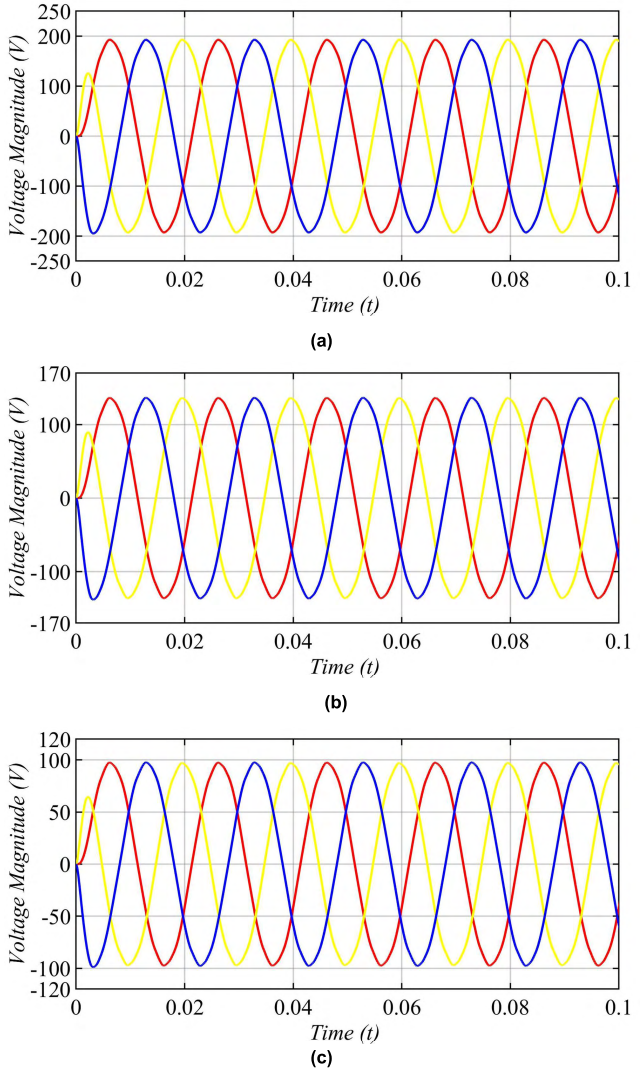

FIGURE 16. Filtered output of three phase SLMHB-MLI on (a) 99% (b) 70% (c) 50% duty cycle; operating on ANDed PWM technique.

Fig. 16 verifies that, although this technique has more THD and switching losses but by changing the duty cycle of the pulse train signal, the RMS of the output voltage is changed and can be used in the speed control of an induction motor.

Table 5 shows the variations in voltage magnitude of the output voltage by changing duty cycle in ANDed

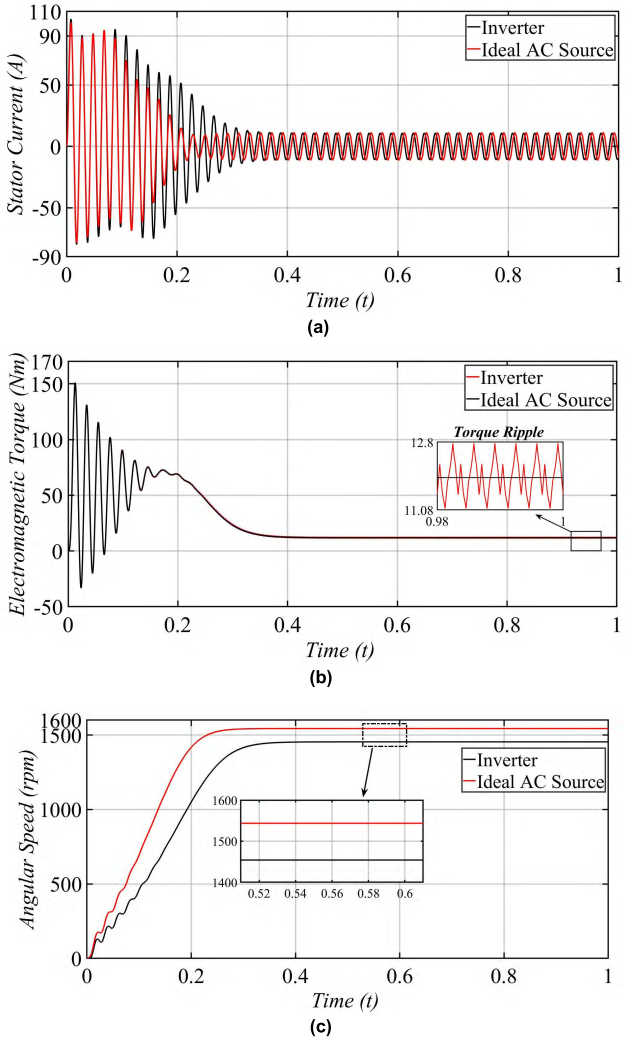

FIGURE 17. Comparison of (a) Stator current (b) electromagnetic torque (c) angular speed; of IM fed to SLMHB-MLI and an ideal AC source.

PWM technique. By using this technique, about 30% of the voltage magnitude is changed by varying duty cycle from 99% to 50%.

C. IM OPERATING ON 17-LEVELS SLMHB-MLI WITH NOVEL PWM TECHNIQUE

Fig. 17 verifies that the stator current, electromagnetic torque and angular speed of an IM operating on SLMHB-MLI with novel PWM technique are identical with the IM operating on an ideal AC source. Furthermore, the angular speed of IM fed to SLMHB-MLI is greater than the IM fed to ideal AC source. However, IM on SLMHB-MLI has ripple torque of 14.23% as shown in Fig. 17 (b).

VI. EXPERIMENTAL RESULTS

After all the simulations, the proposed SLMHB-MLI (operating on the novel PWM technique) is tested and verified on the hardware. The RL load is used at the output classified as: R=70Ω and L=150mH. At the very first, the SLMHB-MLI is tested on the resistive load having power factor (PF) of unity. By selecting $V_1 = 25V$ and $V_2 = 75V$,

TABLE 5. Variations in the magnitude of output voltage by changing duty cycle.

Duty Cycle	Output Voltage	Voltage Magnitude (RMS)
99%	Filtered	137V
	Unfiltered	138.1V
70%	Filtered	97.18V
	Unfiltered	116.2V
50%	Filtered	69.13V
	Unfiltered	98.14V

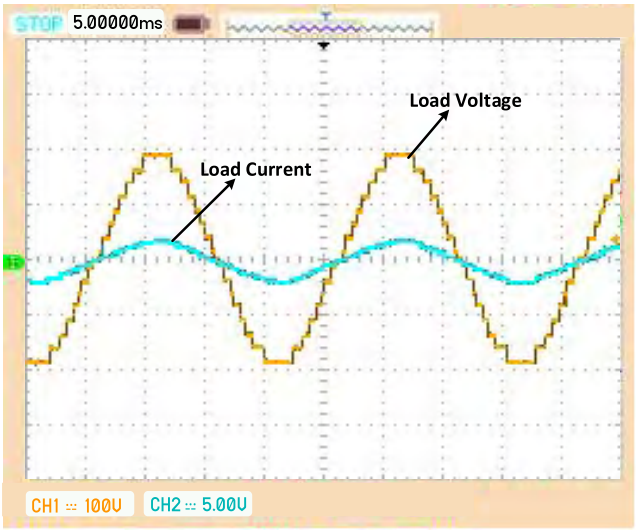

FIGURE 18. Experimental Result of the load voltage and load current at unity PF.

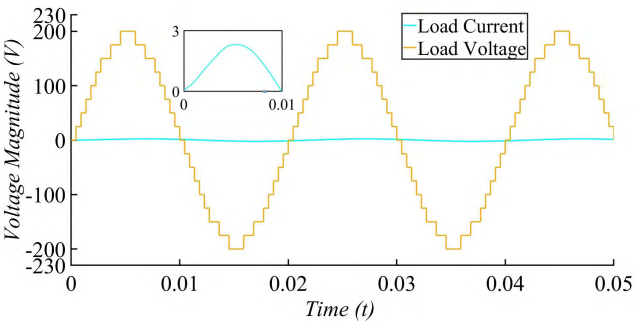

FIGURE 19. Simulated Result of the load voltage and load current at unity PF.

the output voltage has the magnitude of 138.1V (RMS) and the peak voltage of 200V. Fig. 18 and Fig. 19 shows the experimental and simulated result of the load voltage and load current respectively, which are in phase with each other satisfies the unity power factor and resistive load.

The SLMHB-MLI is verified by applying RL load at the output having PF of 0.8. Fig. 20 and Fig. 21 shows that the experimental and simulated waveform of load current is leading the waveform of the load voltage respectively, satisfies the PF of 0.8.

The Fig. 18 to Fig. 21 shows that the simulated results of the proposed topology are exactly overlapping the

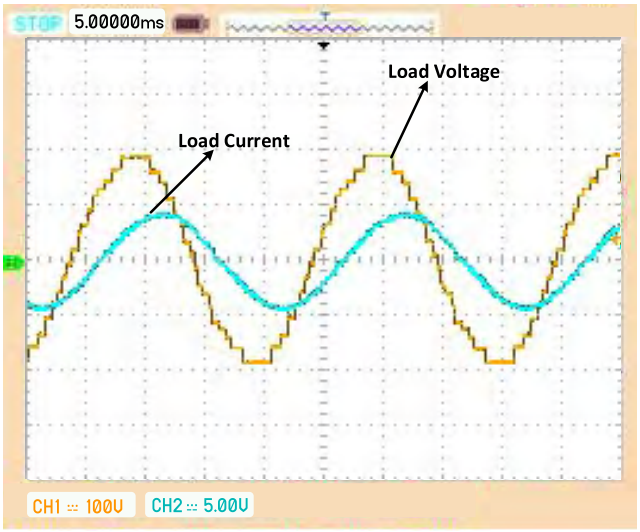

FIGURE 20. Experimental result of the load voltage and load current at 0.8 PF.

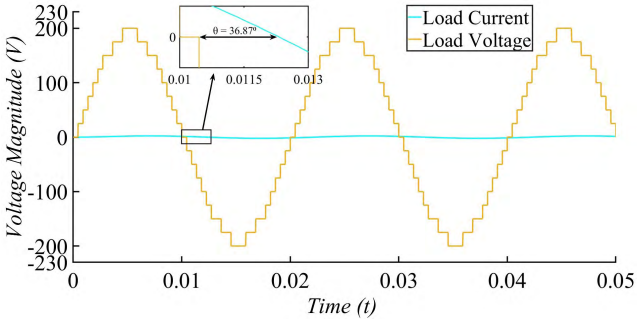

FIGURE 21. Simulated result of the load voltage and load current at 0.8 PF.

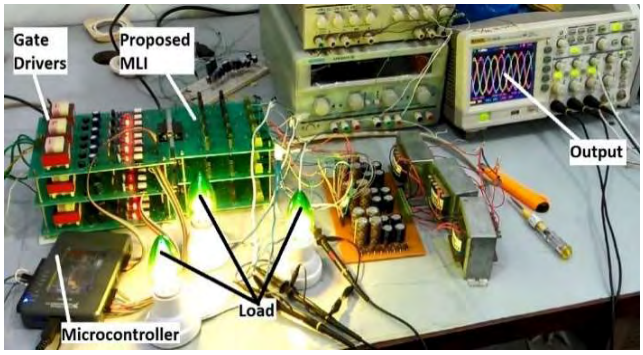

FIGURE 22. Hardware of the proposed topology.

experimental result. Moreover, the number of output voltage levels in the simulation are equal to the output voltage levels in experimental waveform. Hence, it proves the competency of the proposed topology.

The hardware of a proposed topology showing the gate drivers, microcontroller, output voltage, and the load is presented in Fig. 22. The three-phase SHMHB-MLI is shown in Fig. 22. For gate drivers, each phase comprises of 3-center tapped transformers, each transformer steps down the voltage from 220V to 12V. This 12V (AC) is rectified using rectifier and passed through the regulator to make 12V DC

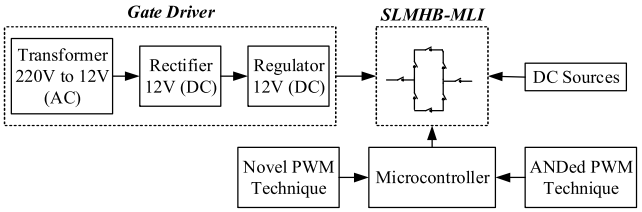

FIGURE 23. Hardware Configuration of the SLMHB-MLI.

without ripple. The complete hardware configuration is shown in Figure 23.

VII. CONCLUSION

This paper presents a new switch-ladder modified H-bridge multilevel inverter (SLMHB-MLI). The main aim of the proposed topology is to generate the maximum number of output voltage levels with the minimum voltage rating on the switches, THD and power electronic components. The SLMHB-MLI is compared with the recommended architecture of MMC and [10]–[23] based on the number of gate drivers, DC sources, switches, distinct DC sources and maximum voltage rating. In novel PWM technique, the switching frequency of the proposed MLI is less, ultimately decreases the switching losses. Furthermore, the SLMHB-MLI is operated on an ANDed PWM technique to vary the RMS of the output voltage by changing the duty cycle of the pulse train signal associated with it. The comparison results indicate that the proposed topology overcome the drawbacks of other structures. These benefits arise indirectly from the hard research took place. Theoretical approaches to the ideas presented in this paper are confirmed by laboratory experiments.

REFERENCES

[1] C. Xia, Z. Wang, T. Shi, and X. He, "An improved control strategy of triple line-voltage cascaded voltage source converter based on proportional—Resonant controller," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2894–2908, Jul. 2013.
[2] J. Wen and K. M. Smedley, "Hexagram inverter for medium-voltage six-phase variable-speed drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2473–2481, Jun. 2008.
[3] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.
[4] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. TarafdarHaque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electr. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.
[5] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
[6] A. Rufer, M. Veenstra, and K. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 1999, pp. 1–10.
[7] H. Ertl, J. W. Kolar, and F. C. Zach, "A novel multicell DC-AC converter for applications in renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1048–1057, Oct. 2002.
[8] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC-DC multilevel boost converter," *IET Power Electron.*, vol. 3, no. 1, pp. 129–137, Jan. 2010.
[9] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical method for pattern generation in five-level cascaded h-bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, Nov. 2014.
[10] J. Schmid and R. Schatzle, "Inverter for converting a direct voltage into an alternating voltage," U.S. Patent 4 775 923, Oct. 4, 1988.

[11] M. R. Banaei, E. Salary, and H. Khounjahan, "A ladder multilevel inverter topology with reduction of on-state voltage drop," *Gazi Univ. J. Sci. Part A, Eng. Innov.*, vol. 1, no. 1, pp. 1–9, Mar. 2013.

[12] E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in *Proc. Int. Conf. Elect. Mach. Syst. (ICEMS)*, Oct. 2007, pp. 74–79.

[13] S. Laali, K. Abbaszadeh, and H. Lesani, "A new algorithm to determine the magnitudes of DC voltage sources in asymmetric cascaded multilevel converters capable of using charge balance control methods," in *Proc. Int. Conf. Elect. Mach. Syst.*, Oct. 2010, pp. 56–61.

[14] M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive applications," in *Proc. APEC*, Feb. 1998, pp. 523–529.

[15] Y. S. Lai and F. S. Shyu, "Topology for hybrid multilevel inverter," *IEE Proc.-Electr. Power Appl.*, vol. 149, no. 6, pp. 449–458, Nov. 2002.

[16] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[17] K. K. Gupta and S. Jain, "A multilevel Voltage Source Inverter (VSI) to maximize the number of levels in output waveform," *Int. J. Elect. Power Energy Syst.*, vol. 44, no. 1, pp. 25–36, Jan. 2013.

[18] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014.

[19] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Electr. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[20] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109–3118, Nov. 2011.

[21] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, Feb. 2012.

[22] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 256–269, Jan. 2015.

[23] S. P. Gautam, S. Gupta, and L. K. Sahu, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," *IET Power Electron.*, vol. 9, no. 4, pp. 698–709, Mar. 2016.

[24] N. Sandeep and U. R. Yaragatti, "A switched-capacitor-based multilevel inverter topology with reduced components," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5538–5542, Jul. 2018.

[25] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[26] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[27] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1504–1511, Oct. 2006.

[28] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, Jul. 2004.

[29] A. Ristow, M. Begovic, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2581–2592, Jul. 2008.

[30] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[31] K. K. Gupta and S. Jain, "Multilevel inverter topology based on series connected switched sources," *IET Power Electron.*, vol. 6, no. 1, pp. 164–174, Jan. 2013.

[32] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, May/Jun. 2000.

[33] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May 1996.

[34] K. K. Gupta and S. Jain, "Comprehensive review of a recently proposed multilevel inverter," *IET Power Electron.*, vol. 7, no. 3, pp. 467–479, Mar. 2014.

[35] D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S. A. Mussa, and M. L. Heldwein, "Symmetrical hybrid multilevel DC—AC converters with reduced number of insulated DC supplies," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2307–2314, Jul. 2010.

[36] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[37] E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.

[38] K. K. Gupta S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014.

[39] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "A new general multilevel converter topology based on cascaded connection of submultilevel units with reduced switching components, DC sources, and blocked voltage by switches," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7157–7164, Nov. 2016.

[40] H. Vahedi, P.-A. Labbé, and K. Al-Haddad, "Sensor-less five-level packed U-cell (PUC5) inverter operating in stand-alone and grid-connected modes," *IEEE Trans. Ind. Informat.*, vol. 12, no. 1, pp. 361–370, Feb. 2016.

[41] N. V. Nho and M. J. Youn, "Comprehensive study on space-vector-PWM and carrier-based-PWM correlation in multilevel invertors," *IEE Proc.-Electr. Power Appl.*, vol. 153, no. 1, pp. 149–158, Jan. 2006.

[42] M. Hasan, S. Mekhilef, and M. Ahmed, "Three-phase hybrid multilevel inverter with less power electronic components using space vector modulation," *IET Power Electron.*, vol. 7, no. 5, pp. 1256–1265, 2014.

[43] K. P. Panda and G. Panda, "Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, Jul. 2018.

[44] J. Liu, K. W. E. Cheng, and Y. Ye, "A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4219–4230, Aug. 2014.

[45] A. Kumar and V. Verma, "Performance enhancement of single-phase grid-connected PV system under partial shading using cascaded multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2665–2676, Jun. 2018.

[46] C. D. Fuentes, C. A. Rojas, H. Renaudineau, S. Kouro, M. A. Perez, and M. Thierry, "Experimental validation of a single DC bus cascaded H-bridge multilevel inverter for multistring photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 930–934, Feb. 2017.

[47] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156–1169, Feb. 2017.

[48] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and DC-link capacitor voltage balancing using only the switching-state redundancy—Part I," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2600–2608, Oct. 2007.

[49] A. Kshirsagar, R. S. Kaarthik, K. Gopakumar, L. Umanand, and K. Rajashekara, "Low switch count nine-level inverter topology for open-end induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1009–1017, Feb. 2017.

[50] T. Boller, J. Holtz, and A. K. Rathore, "Neutral-point potential balancing using synchronous optimal pulsewidth modulation of multilevel inverters in medium-voltage high-power AC drives," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 549–557, Feb. 2014.

[51] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, Mar. 2005.

[52] S. Jain and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2865–2875, Apr. 2017.

[53] Z.-G. Lu, L.-L. Zhao, W.-P. Zhu, C.-J. Wu, and Y.-S. Qin, "Research on cascaded three-phase-bridge multilevel converter based on CPS-PWM," *IET Power Electron.*, vol. 6, no. 6, pp. 1088–1099, Jul. 2013.

[54] A. Chitra and S. Himavathi, "Reduced switch multilevel inverter for performance enhancement of induction motor drive with intelligent rotor resistance estimator," *IET Power Electron.*, vol. 8, no. 12, pp. 2444–2453, Dec. 2015.

[55] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power. Electron.*, vol. 29, no. 12, pp. 6712–6724, Dec. 2014.
[56] L. A. Solomon, A. Permuy, N. D. Benavides, D. F. Opila, C. J. Lee, and G. F. Reed, "A transformerless PCB-based medium-voltage multilevel power converter with a DC capacitor balancing circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3052–3067, Apr. 2016.
[57] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308–5322, Oct. 2014.
[58] R. Rabinovici, D. Baimel, J. Tomasik, and A. Zuckerberger, "Thirteen-level cascaded H-bridge inverter operated by Generic phase shifted pulse-width modulation," *IET Power Electron.*, vol. 6, no. 8, pp. 1516–1529, Sep. 2013.
[59] S. K. Sahoo and T. Bhattacharya, "Phase-shifted carrier-based synchronized sinusoidal PWM techniques for a cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 513–524, Jan. 2018.
[60] M. T. Khosroshahi, "Crisscross cascade multilevel inverter with reduction in number of components," *IET Power Electron.*, vol. 7, no. 12, pp. 2914–2924, 2014.
[61] E. Villanueva, P. Correa, J. Rodríguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
[62] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.
[63] J. C. Kartick, B. K. Sujit, and K. Suparna, "Dual reference phase shifted pulse width modulation technique for a N-level inverter based grid connected solar photovoltaic system," *IET Renew. Power Gener.*, vol. 10, no. 7, pp. 928–935, Jul. 2016.
[64] L. Liu, H. Li, Y. Xue, and W. Liu, "Decoupled active and reactive power control for large-scale grid-connected photovoltaic systems using cascaded modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 176–187, Jan. 2015.
[65] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
[66] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
[67] S. S. Lee, M. Sidorov, C. S. Lim, N. R. N. Idris, and Y. E. Heng, "Hybrid cascaded multilevel inverter (HCMLI) with improved symmetrical 4-level submodule," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 932–935, Feb. 2018.
[68] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.
[69] G. S. Konstantinou, M. S. A. Dahidah, and V. G. Agelidis, "Solution trajectories for selective harmonic elimination pulse-width modulation for seven-level waveforms: Analysis and implementation," *IET Power Electron.*, vol. 5, no. 1, pp. 22–30, Jan. 2012.
[70] M. A. Memon, S. Mekhilef, M. Mubin, and M. Aamir, "Selective harmonic elimination in inverters using bio-inspired intelligent algorithms for renewable energy conversion applications: A review," *Renew. Sustain. Energy Rev.*, vol. 82, pp. 2235–2253, Feb. 2018.
[71] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg, and S. Farhangi, "Optimal selective harmonic mitigation technique on variable DC link cascaded H-bridge converter to meet power quality standards," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1107–1116, Sep. 2016.
[72] C. Qi, P. Tu, P. Wang, and M. A. Zagrodnik, "Random nearest level modulation strategy of multilevel cascaded H-bridge inverters," *IET Power Electron.*, vol. 9, no. 14, pp. 2706–2713, Nov. 2016.
[73] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and H. M. Suryawanshi, "Hybrid control technique-based three-phase cascaded multilevel Inverter topology," *IEEE Access*, vol. 5, pp. 26912–26921, 2017.
[74] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2072–2080, Mar. 2017.
[75] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4530–4538, Jun. 2017.
[76] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. M. Kojabadi, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6738–6754, Aug. 2018.
[77] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-Type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.
[78] A. Kshirsagar, R. S. Kaarthik, A. Rahul, K. Gopakumar, L. Umanand, S. K. Biswas, and C. Cecati, "17-level inverter with low component count for open-end induction motor drives," *IET Power Electron.*, vol. 11, no. 5, pp. 922–929, May 2018.
[79] S. P. Gautam, L. Kumar, and S. Gupta, "Single-phase multilevel inverter topologies with self-voltage balancing capabilities," *IET Power Electron.*, vol. 11, no. 5, pp. 844–855, 2018.
[80] C. Dhanamjayulu and S. Meikandasivam, "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads," *IEEE Access*, vol. 6, pp. 738–746, 2017.
[81] R. V. Nair, K. Gopakumar, and L. G. Franquelo, "A very high resolution stacked multilevel inverter topology for adjustable speed drives," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2049–2056, Mar. 2018.
[82] B.-B. Ngo, M.-K. Nguyen, J.-H. Kim, and F. Zare, "Single-phase multilevel inverter based on switched-capacitor structure," *IET Power Electron.*, vol. 11, no. 11, pp. 1858–1865, Sep. 2018.
[83] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019.
[84] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.
[85] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019. doi: 10.1109/ACCESS.2019.2925277.
[86] A. Taheri and H. Samsami, "New topology of a switched-capacitor-based multilevel inverter with a single DC power supply," *IET Power Electron.*, vol. 12, no. 6, pp. 1571–1584, May 2019.

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