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LW-DEM: Designing a Low Power Digital-to-Analog Converter Using Lightweight Dynamic Element Matching Technique

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ABSTRACT The need for low-power wireless sensor networks (WSNs) continues to grow. Based on the fact that digital-to-analog converters (DACs) are essential elements in the WSN and consumes a lot of power, this paper presents a new low-power DAC design to realize the low-power WSN. To do that, this paper exploits the dynamic element matching (DEM) technique, one of the well-known techniques for high performance DACs, proposes a lightweight DEM (LW-DEM) technique that minimizes power and area overhead of the DEM technique. More specifically, this paper is motivated from the observation that input data of DACs tends to be sufficiently random that the input data can be used for the random selection of the current source instead of a pseudo-random number generator (PRNG) for the traditional DEM. Because the PRNG consumes a lot of power and occupies a large area in a DAC, elimination of the PRNG from a DAC and utilizing input data result in significant power saving and area reduction in the DAC while meeting the required performance of the low-power WSNs. This paper provides a detailed LW-DEM architecture and its operation principle. To demonstrate the efficacy of the proposed method, a prototype 12-bit DAC using the LW-DEM is implemented. The 12-bit DAC is fabricated in 65 nm CMOS technology and occupies only 0.065 mm^2 area. Measurement results with the prototype verify that the DAC using LW-DEM accomplishes 39% power saving and 52% area reduction in the randomizer, compared to a DAC using the conventional DEM. At the same time, the measured spurious-free dynamic range (SFDR) of the DAC using LW-DEM is better than 55 dB, demonstrating that the proposed DAC achieves almost same performance as a DAC using the conventional DEM.

INDEX TERMS Digital-analog conversion, DAC, dynamic element matching Technique, DEM, wireless sensor networks, transmitters, low-power design.

I. INTRODUCTION

With the explosive growth of the Internet of Things (IoT), wireless sensor networks (WSNs) are becoming important for the continued development of information and communication technologies. Various and precise sensors, sensor interfaces and measurement systems, which are the results of sensor networks, are in charge of IoT information collection [1], [2], and the low latency / low power wireless communication methods and devices that result from wireless networks are contributing to IoT communication [3], [4]. Consequently, the latest wireless sensor nodes, which are the cornerstone of the technical integration of the WSN, are playing a pivotal role in IoT data collection and communication.

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Despite the remarkable advancement of wireless sensor nodes, they still have a critical limitation: power consumption [5]. Since most wireless sensor nodes are battery-powered devices, service life is severely limited due to power consumption. Therefore, researches have been actively conducted to reduce power consumption of wireless sensor nodes. For example, ultra-low power and lightweight processors for the wireless sensor nodes are researched and developed [6]–[9]. Another approach to low-power sensor nodes is to adopt low-power network protocols [10], [11]. Focusing electronic components such as analog-to-digital converter (ADC) and digital-to-anlalog converter (DAC), which are typically power-hungry components in a wireless sensor node, and how to design them to lower their power consumption is another well-known approach [2], [12]–[15].

Modern IoT standards such as NB-IoT, LoRa, sigfox have a narrowband bandwidth rather than a fast data rate to connect many devices simultaneously. Since IoT standards typically have data bandwidths of less than a few MHz, the power-hungry electronic components need to approach a different perspective than previous studies focused on high-performance. In this paper, we pay attention to DAC, an integral component of a transmitter in the wireless sensor node, and present a new design method to achieve significant power reduction in DAC. To this end, we first focus on the current steering DAC, one of the most common DAC types in a transmitter, and analyze the limitations of traditional current steering DAC designs for power. More precisely, we identify the limitations of the traditional techniques and methods for DAC designs that put the greatest weight on the high performance represented by spurious-free dynamic range (SFDR) and sampling rate. Although the previous techniques for the high SFDR DAC have successfully achieved the goal, accompanying power and area overhead has increased. This is because the previous techniques require additional large area occupied circuitries that consume large amounts of power. On the other hand, the primary goal of this paper is to design a low power and small area DAC.

After analyzing the cause of the power and area overhead of each existing technology, we come up with a new design technique that can provide as much performance as the previous technology with much less power and area. The proposed technique is based on the dynamic element matching (DEM) technique, the most robust technique for high SFDR among the various previous techniques. For reference, the DEM technique has been suggested to overcome the mismatch problem that causes the SFDR degradation [16]–[19]. And it requires a randomizer for a random selection of the current source, which typically consists of a barrel shifter and a pseudo-random number generator (PRNG). Motivated from the fact that the PRNG is a heavy power consumer and occupies a large area in a DAC, plus our observation that input data of the DAC is already sufficiently random, we propose to use the input data for the random selection of the current source instead of the PRNG. In other words, the proposed technique achieves power and area saving by eliminating the PRNG but only requiring the barrel shifter in the DAC (i.e., thereby becoming lightweight), while the SFDR performance is almost maintained.

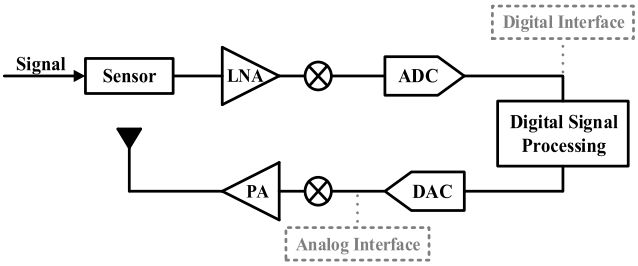


FIGURE 1. Block diagram of basic wireless sensor node.

In this paper, we call the proposed technique a lightweight DEM (LW-DEM) targeting low-power and small area DAC, and provide a detailed elucidation of the LW-DEM architecture and its circuit implementation. To verify the effectiveness of the LW-DEM, we prototype a 12-bit DAC using LW-DEM in 65 nm CMOS technology. This prototype DAC operates with 25MS/s so that it can cover the bandwidth of most IoT wireless communications. In addition, we prototype a 12-bit DAC using LW-DEM in 65 *nm* CMOS technology for verifying the efficacy of the LW-DEM. Measured data with the prototype DAC demonstrates that the LW-DEM achieves 39% power saving and 52% area reduction compared to a DAC using the conventional DEM technique, and the SFDR of the prototyping DAC is still greater than 55 dB, which is similar to the baseline DAC.

The remainder of this paper is organized as follows. Section II is dedicated to reviewing the conventional design techniques for the current steering DAC. Section III describes the details of the proposed DEM technique, where the LW-DEM architecture and operation principle are provided in Section III-A and a prototype DAC using LW-DEM is presented in Section III-B. Section IV provides measurement results with the LW-DEM prototyping DAC, while conclusions are drawn in Section V.

II. CONVENTIONAL DESIGN TECHNIQUES FOR DAC: A REVIEW

Transmitters are essential at the wireless sensor nodes, and DAC is an integral part of a transmitter. Traditional approaches to designing DACs have focused on improving DAC performance, and SFDR has been widely used as a performance metric for DACs. SFDR refers to the available dynamic range of a DAC before spurious noise is interfering or distorting the fundamental signal. SFDR is measured from the amplitude difference between fundamental and maximum harmonic or non-harmonic-related spurs from DC to the full Nyquist bandwidth.

In practice, there are several factors that degrade the SFDR, such as the finite output impedance of current sources, input code dependent switching transient, code-dependent loading variation, and mismatch of current sources [20]. To overcome

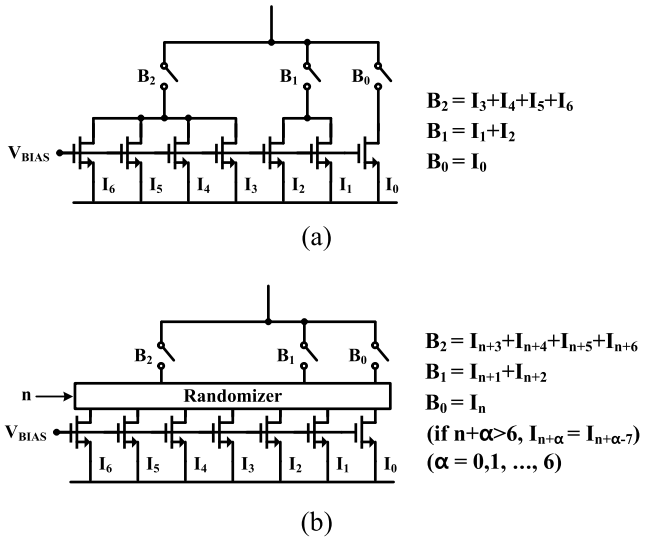


FIGURE 2. Diagram of (a) conventional binary weighted DAC (b) DAC using RRBS DEM technique.

the mismatch effect, increasing the size of current source is a straightforward method. However, this method requires a large area that causes parasitic and gradient mismatches. Another method to solve the mismatch effect is to use calibration techniques [21], [22]. Unfortunately, this method needs additional circuitry, which may result in power, and is therefore unsuitable for the low power wireless sensor node.

It reduces the effect of mismatching current sources, by randomly selecting current sources during operation (i.e., every clock cycle) and compensating for matching errors. Compared to other methods, the DEM is the most promising way to solve the mismatch problem because it requires a relatively small footprint and is easy to implement. Therefore, this paper focuses on the DEM, or more precisely, the random rotation-based binary-weighted selection (RRBS) DEM. The RRBS is the most typical technique for the DEM, which requires a randomizer compose with a barrel shifter and PRNG [19]. The details of the conventional RRBS DEM are described in the following subsection.

A. RRBS DEM TECHNIQUE

The RRBS DEM is based on the principle of the conventional binary weighted DAC. The comparison of the operating principle of a conventional binary weighted DAC and a DAC using the RRBS DEM are shown in FIGURE 2, where both 3-bit DACs are used as examples. In the 3-bit binary weighted DAC shown in FIGURE 2 (a), the current source(s) selected according to the input is fixed. For example, when the B_0 is input, the current source I_0 is selected and turned on. For B_1, the current sources I_1 and I_2 are turned on. Plus, when B_2 is input, the current sources I_3, I_4, I_5, and I_6 operate. This fixed design is inherently vulnerable to mismatch problems. In other words, if a mismatch exists in the current source, the same mismatch component will appear for each specific input. This mismatch is presented with harmonic components that deteriorate the SFDR performance.

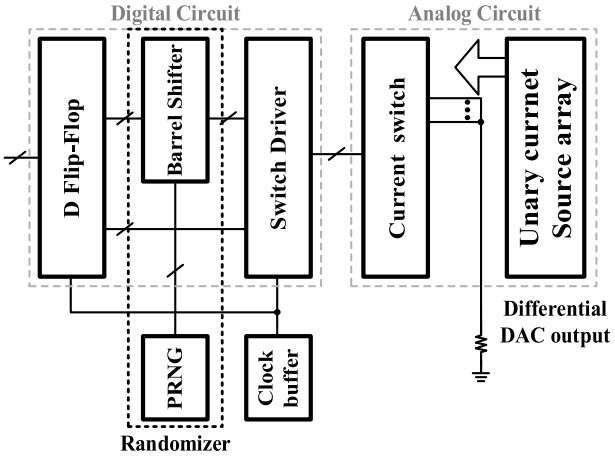


FIGURE 3. Architecture of the DAC using RRBS DEM.

The DEM is another solution of the mismatch problem [16]–[19].

On the other hand, the DAC using the RRBS DEM groups current sources randomly. By doing so, the harmonic components are converted into white noise. For example, as shown in FIGURE 2 (b), the current source corresponding to B_0 is determined according to the input of the randomizer n, and then the current sources corresponding to B_1 and B_2 are sequentially assigned. Therefore, even if the sum of noise and distortion is equal, the SFDR performance can be improved.

A common architecture of the DAC using RRBS DEM is shown in FIGURE 3. The DAC can be divided into analog parts and digital parts, and the digital circuit part in the DAC includes a randomizer that comprises a barrel shifter and PRNG. The rotation number is determined by the value generated by PRNG and decides on starting point of the current source.

Meanwhile, FIGURE 4 presents the operation principle of the DACs. As described above in FIGURE 2 (a), the binary input is assigned a fixed current source. Therefore, (I_0), (I_1, I_2), and (I_3, I_4, I_5, I_6) are respectively turned on in case of binary input codes B_0, B_1, and B_2. Compared to the conventional binary weighted DAC shown in the FIGURE 4 (a), the DAC with RRBS DEM shown in the FIGURE 4 (b) exploits the rotation number, R, that is generated PRNG. In this case when the left rotation is used, for example, when the first input value is five and the rotation number is four, the current group is determined as (I_4), (I_5, I_6), (I_0, I_1, I_2, I_3) according to B_1, B_2, and B_3, respectively. Therefore, the five current sources I_0, I_1, I_2, I_3, I_4 are turned on. Similarly, if the second input is six and the rotation number is seven, the current sources should be grouped into (I_0), (I_1, I_2), and (I_3, I_4, I_5, I_6), thereby $I_1 \sim I_6$ are turned on.

III. PROPOSED LW-DEM

The PRNG in the DAC with RRBS DEM is implemented with D flip-flops and several logic gates. To make the DAC random cycle longer, the higher-resolution PRNG is necessary, which in turn requires the more D flip-flops. In other words,

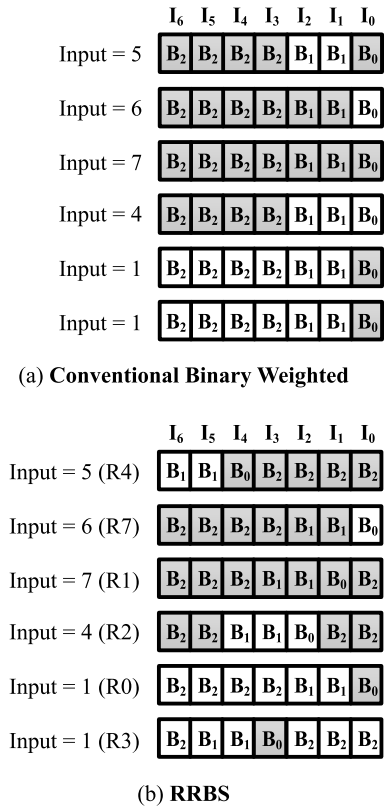


FIGURE 4. Operating principle of (a) conventional binary weighted DAC (b) DAC with RRBS DEM.

the power and area overhead due to the PRNG increases to allow the DAC to support longer random cycles. Moreover, a timing margin due to the PRNG that increases as the sample rate increases may cause a design problem. This disadvantage limits the DEM utilization and is especially critical for low power wireless sensor nodes. This paper provides a solution to address this limitation.

A. DESIGNING THE LW-DEM ARCHITECTURE AND OPERATION PRINCIPLE

Motivated from the analysis that the PRNG in the randomizer tends to cause the considerable power and area overhead in a DAC using the RRBS DEM, we propose to get rid of the PRNG in the DAC but exploits the input data that is already sufficiently random. By eliminating the PRNG, power and area overhead due to the PRNG should be disappeared, and utilizing the randomness of the input data to determine the rotation number takes charge in maintaining the SFDR performance of the DAC. In addition, since the proposed method uses one input code in one sample period as the PRNG used in the conventional DEM method generates a random bit once in a sample period, no additional overhead according to the sample rate occurs. The resulting architecture of the proposed DAC design is provided in FIGURE 5.

In order to utilize the input data in the randomizer, the input data must satisfy the following three conditions.

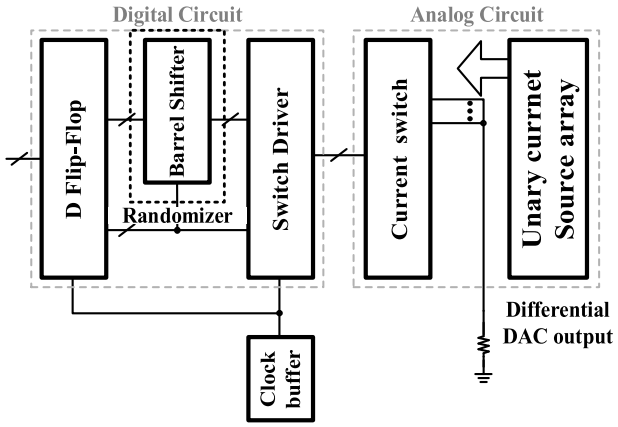


FIGURE 5. Proposed architecture for the DAC using DEM without PRNG.

i) Uncorrelation to the current source mismatch
ii) Low periodicity
iii) Random bitstream

With respect to the first condition, the most important role of DEM is to convert harmonics due to mismatches into white noise. If the input data is correlated to the mismatch of the current source, harmonics due to the mismatch may not be converted to white noise and other harmonics may be generated. Fortunately, the first qualification can be easily deduced because the mismatch of the current source is determined by the stochastic factors in the semiconductor process. To prove the second condition, we first pay attention to the coherent sampling that is commonly used to measure the dynamic performance of data converters. If the input data is generated with the coherent sampling technique, the input data pattern should repeat every $2^{12} - 1$ for 12-bit DAC, which is the sufficiently large number for randomization. With regard to the third condition, it may be very difficult to directly prove whether an arbitrary bitstream is random or not. Instead, we utilize the power spectral density (PSD) of the bitstream, so as to compare the PSDs of input code, PRNG, and the ideal random bitstream. The ideal random bitstream can be derived from a following equation [23]:

$$x(t) = \sum_k b_k p(t - kT_b) \tag{1}$$

where x is ideal random bitstream, a function of time t; b_k is k^{th} sign of bit which can be ± 1; and T_b and $p(t)$ denote the period of one bit and the rectangular pulse shape, respectively. If the positive and negative b_k occur at the same probability, and if $p(t)$ is a rectangular pulse in T_b repeated every T_b, the PSD of $x(t)$, S, can be expressed as a function of frequency f:

$$S_x(f) = T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b} \right]^2 \tag{2}$$

Simulation results of the PSDs of the ideal random bitstream, PRNG, and the input code according to different output frequencies and input bit orders are described

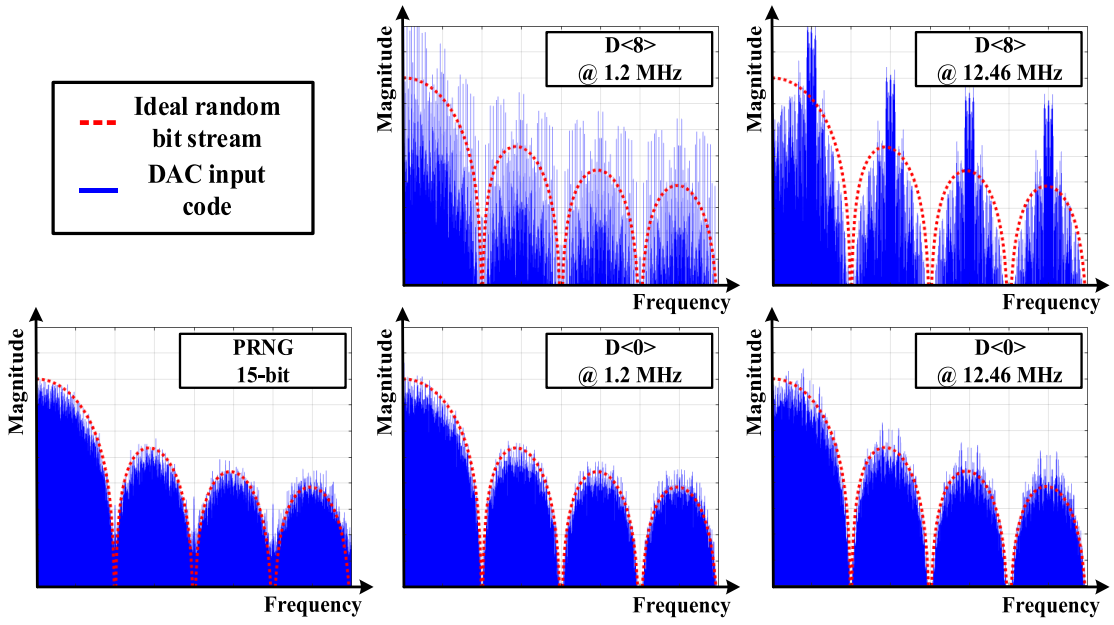


FIGURE 6. The PSDs of the ideal random bitstream, PRNG, and input code with to different frequencies and bit orders.

in FIGURE 6. As seen in the figure, the PSD of the input code using the LSB (cf. D⟨0⟩ @ both 1.2MHz and 12.46MHz) is similar to the ideal random bitstream, regardless of the output frequency. On the other hand, it is observed that the PSD of the input code using the MSB at high frequency (cf. the 3rd MSB D⟨8⟩ @ 12.46MHz) often alternates periodically between 0 and 1 (i.e., at low frequency, it does not). Therefore, since the MSB part of input data is affected by the output frequency, input data must be carefully selected for the randomizer. Details on how to select the input data are discussed in the following Section III-B.

Finally, we first design an operation principle that targets 6-bit DAC, which is described in FIGURE 7. The basic operation principle is the same as that of RRBS, but the 6-bit is segmented into 3 + 3. The rotation number is determined by the LSB 3-bit. Then, the rotation number controls the operation of MSB 3-bit. When the MSB 3-bit input value is five and the rotation number is five, the starting point B_0 moves five to the left and $I_1 \sim I_5$ are selected. If the input value is six and R is one, the starting point is moved once to the left.

B. DESIGNING A PROTOTYPE 12-BIT DAC USING LW-DEM

According to the proposed DAC architecture and its operating principle, we prototype a 12-bit DAC with LW-DEM. The architecture of the DAC prototype is designed to have 3 + 3 + 3 + 3 segmentation, which are 3-bit MSB, 3-bit ULSB, 3-bit LSB, and 3-bit LLSB, as shown in FIGURE 8. We decide to apply the LW-DEM to the 3-bit MSB, 3-bit ULSB and 3-bit LSB, but not 3-bit LLSB. This is based on the analysis that the effect of the 3-bit LLSB is small, because the weight is relatively small compared to that of the other high order bits. Then, a 3-bit randomizer that has only a

Proposed DEM

	I_6	I_5	I_4	I_3	I_2	I_1	I_0
Input = 5 (R5)	B_1	B_0	B_2	B_2	B_2	B_2	B_1
Input = 6 (R1)	B_2	B_2	B_2	B_1	B_1	B_0	B_2
Input = 7 (R4)	B_1	B_1	B_0	B_2	B_2	B_2	B_2
Input = 4 (R1)	B_2	B_2	B_2	B_1	B_1	B_0	B_2
Input = 1 (R0)	B_2	B_2	B_2	B_2	B_1	B_1	B_0
Input = 1 (R2)	B_2	B_2	B_1	B_1	B_0	B_2	B_2

<MSB 3-Bit>

6-Bit DAC input code

D5	D4	D3	D2	D1	D0
1	0	1	1	0	1
1	1	0	0	0	1
1	1	1	1	0	0
1	0	0	0	0	1
0	0	1	0	0	0
0	0	1	0	1	0

<MSB 3-Bit> <LSB 3-Bit>

FIGURE 7. The operating principle of the proposed DEM technique. A 6-bit DAC is used in this example.

barrel shifter is attached to each MSB, ULSB, and LSB part. Note that this 3-bit segmentation is advantageous not only in

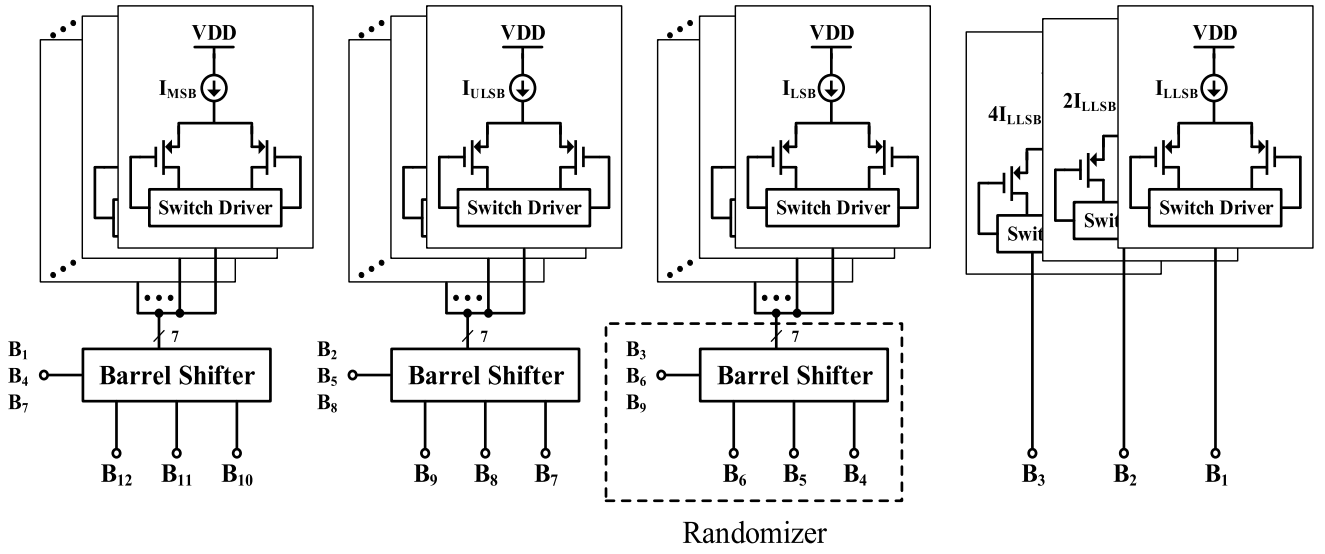


FIGURE 8. Architecture of the prototype 12-bit DAC using LW-DEM.

the footprint but also the parasitic side, since the it does not require the complicated wiring connections.

In order for sufficient randomization, the random numbers are generated using $B_1 \sim B_9$, as seen in FIGURE 8, but they are not determined by the MSB 3-bits. This is based on a general assumption that the MSB 3-bits hardly changes at a low input frequency. To validate the assumption, we perform MATLAB simulation, and FIGURE 9 shows the simulation results when the values of $B_4 \sim B_{12}$ and $B_1 \sim B_9$ are applied to the shifter, respectively. In the figure, (a) is for the results when $B_4 \sim B_{12}$ are used, while (b) is for the results when $B_1 \sim B_9$ are used. The simulation results show that the average SFDR is reduced by about 4 dB due to the reduction of random effects when using a 3-bit MSB.

To determine the rotation number of the shifters based on the DAC inputs, two different methods are taken into consideration, which are called Method-I and II. The Method-I focuses on the effect of the rotation step size, while the Method-II focuses on the effect of the weight of the current source. More precisely, as described in FIGURE 10 (a), the Method-I puts more weight on the first row than others. Therefore, $B_1 \sim B_3$ are allotted to the 4-step rotation number of the shifter. Because the MSB has a large weight as aforementioned, which has a significant impact on the performance of the DAC. In a consequence, the first row in FIGURE 10 (a) is sequentially filled with $B_1 \sim B_3$ in the right direction. Then, B_1, B_4, and B_7, which are the most dynamically changed, are allocated to the first column. On the other hands, the weight of the current source is emphasized in the Method-II. Thus, $B_1 \sim B_3$ are allotted to the MSB rotation number of the shifter. As shown in FIGURE 10 (b), $B_1 \sim B_3$ are arranged along the first column.

The areas of the Method-I and Method-II with the smallest randomization are marked with gray color in FIGURE 10. In the Method-I, although the area of the 1-step rotation is

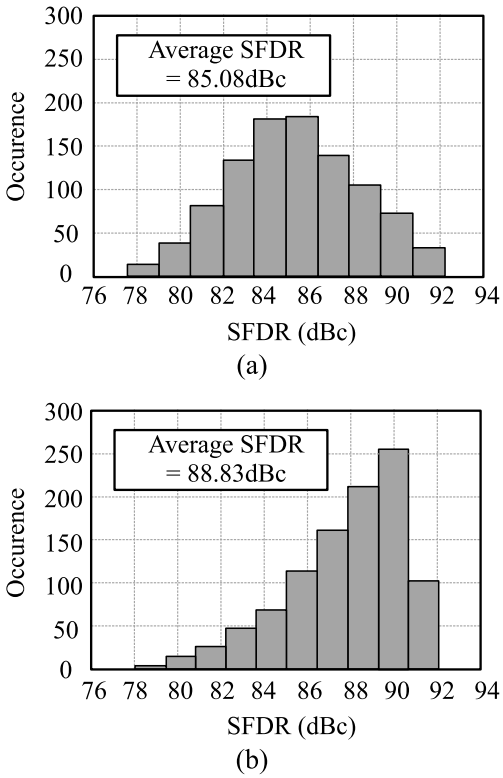


FIGURE 9. Average SFDR (a) by using $B_4 \sim B_{12}$ ⟨4:12⟩ or (b) by mixing properly $B_1 \sim B_9$ ⟨1:9⟩ for the shifting number.

grayed out, it can be ignored due to the small sensitivity. However, in the Method-II, the randomization of the LSB is the smallest, which means that the LSB is not substantially shuffled. As a result, in this paper, we choose the Method-I for the rotation number.

Meanwhile, glitches are another issue in the DAC, whereby a glitch may occur every time when the switch changes.

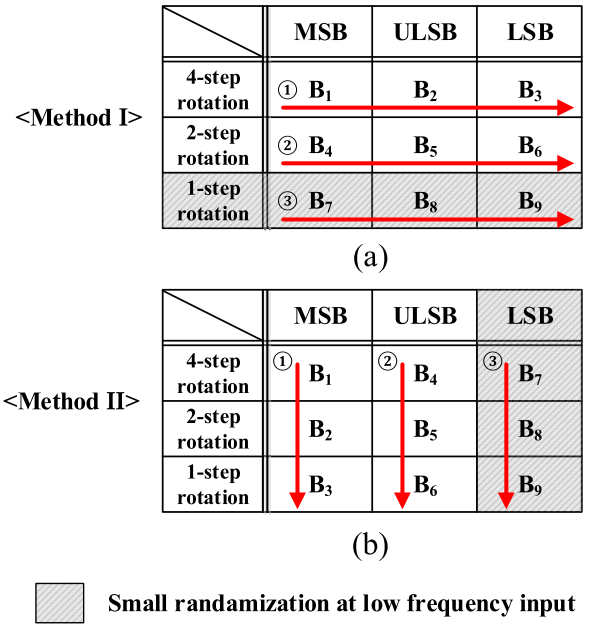


FIGURE 10. Two methods exploiting the DAC inputs to determine the rotation number of the shifters.

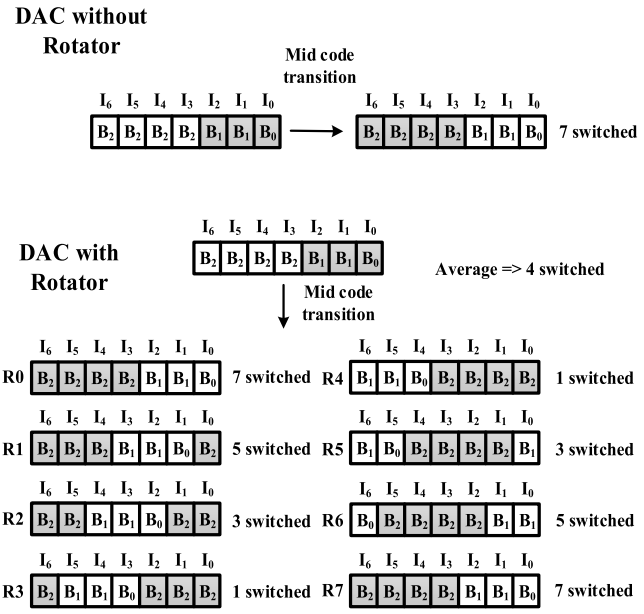


FIGURE 11. A 3-bit DAC example to show different number of switched current sources W/ and W/O rotator.

The glitch is an unwanted voltage output during the code transition, which is mainly caused by timing mismatch and parasitic capacitance of each current source [24]. The glitch generates nonlinearity and affects the DAC output, thereby degrading SFDR performance. One of the drawbacks of using the DEM technique is the switching glitch [16], [18], [25]. Although the previous work on the DEM technique have resolved the glitch problem, the additional complex logics proposed in the previous studies may not be suitable for low power sensor node applications. On the other hands, the proposed LW-DEM can overcome the glitch problem using a similar mechanism of RRBS without additional complex logic but utilizing only a rotator.

Since it is difficult to reduce the timing mismatch of the current sources having different weight, the number of the switched current source is must be reduced. For the sake of simplicity, let us consider an example of a 3-bit binary weighted DAC. The detailed operating principle of the 3-bit DAC is described in FIGURE 11. In this case, the largest glitch occurs in a mid-code transition such as 011 to 100. In other words, seven current courses of the 3-bit binary weighted DAC without rotator are switched. On the other hand, the number of switched current source of the DAC with rotator changes with the rotation number. Thus, on average, only four current sources changes, which is about half of the binary weighted DAC. Reducing the number of switched current sources in turn mitigates the glitch problem.

The DEM technique for minimized glitch has already been proposed in [16]. In this case, there is another disadvantage in that it requires a complex logic. However, the proposed structure overcomes the glitch problem because it has fewer switching times than the general binary weighted DAC and conventional RRBS DEM at Nyquist frequency. To verify this, we perform MATLAB simulation to see how the number of switching time differs between different DACs. The simulation results are reported in FIGURE 12. At the Nyquist frequency, the total number of switching times of the conventional binary weighted DAC is 16,246,552, and that of the DAC using RRBS DEM is 13,275,992. Whereas, the number of switching times of the DAC with LW-DEM is 13,033,176, which results in a reduction of 19.7% and 1.9%, respectively, compared with the conventional binary weighted DAC and the DAC using RRBS DEM.

Finally, the prototype 12-bit DAC using LW-DEM is implemented in 65 *nm* CMOS technology. The die photo of the implemented DAC is shown in FIGURE 13, which include a digital circuit, switch array, current source array, and bias circuit. The active area of the implemented DAC is 260 $um \times 250$ *um*. Especially, the digital circuit is composed of flip-flops, switch driver arrays, and shifters, occupying an area of 0.0036 mm^2. Note that, if the conventional RRBS is applied to the DAC and a 15-bit PRNG is thus equipped to the DAC, the conventional randomizer fabricated with the same 65 *nm* technology should occupy 0.0077 mm^2. Namely, the proposed DAC saves about 53% of the total area of randomizer, compared to the conventional DAC. In terms of power consumption, the measured power consumption of the shifter and PRNG are 181.2 μW and 118.8 μW, respectively, which can be interpreted that the proposed DAC achieved about 39% power saving.

IV. MEASUREMENT RESULTS

In the experimental work, The outputs of the DAC are coupled to a spectrum analyzer via a balun, and a 50 Ω output load is used. FIGURE 14 shows the measured power spectrum density (PSD) of the proposed DAC with a 1.2 MHz

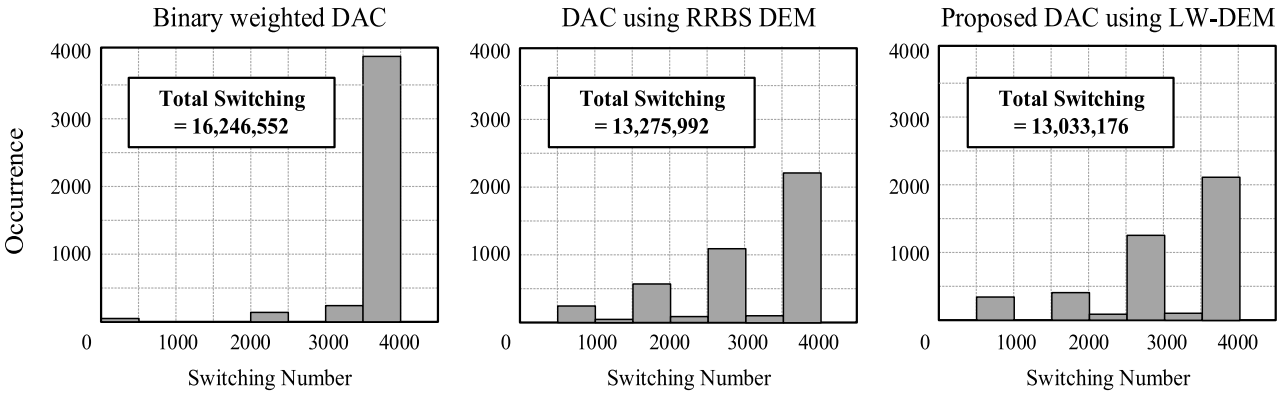


FIGURE 12. Occurrences of the switching activity at (a) the conventional binary weighted DAC, (b) the DAC using RRBS DEM, and (c) the proposed DAC using LW-DEM.

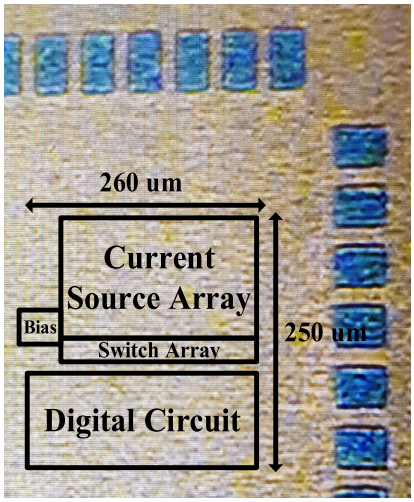


FIGURE 13. A die photo of the 12-bit DAC prototype.

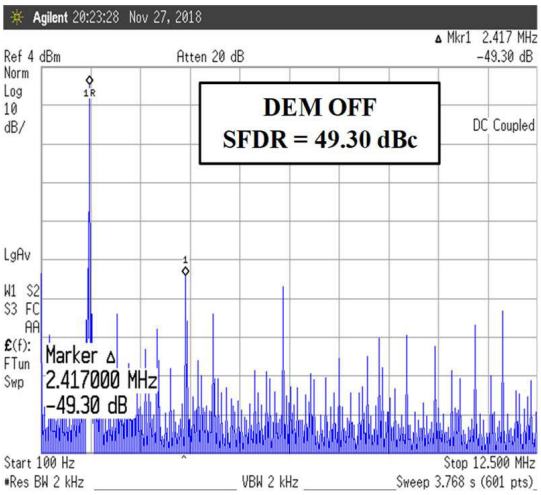
signal at 25 MS/s. FIGURE 14 (a) and (d) show the performance of a conventional binary weighted DAC when the DEM technique is disabled, where the measured SFDR are 49.30 dBc and 50.39 dBc for 1.2 MHz and 12.46 MHz input signal, respectively. Compared to them, the measured SFDRs from the DAC with the RRBS DEM technique (with an external 15-bit PRNG) are reported in FIGURE 14 (b), (e), each of which is with 1.2 MHz and 12.46 MHz input signal and the resulting SFDR is 60.09 dBc and 55.63 dBc, respectively. Finally, FIGURE 12 (c), (f) shows the measured SFDR with the DAC using the proposed LW-DEM technique. From the figure, we can check that the SFDR performance is 59.83 dBc and 55.79 dBc for each input signal, which are slightly less than those from the DAC with the RRBS DEM technique.

From FIGURE 14, we can check that the mismatch of current sources is displayed as harmonic tones at the case of the conventional binary weighted DAC, but the harmonic tones generated by the mismatch are distributed into the noise floor at the cases of the DAC using DEM. In addition, the LW-DEM improves the SFDR performance by about 10 dB compared to no DEM, which is similar to that of the conventional RRBS DEM. Finally, it can be confirmed from the simulation results that the LW-DEM can achieve sufficient randomization without PRNG in the fabricated DAC.

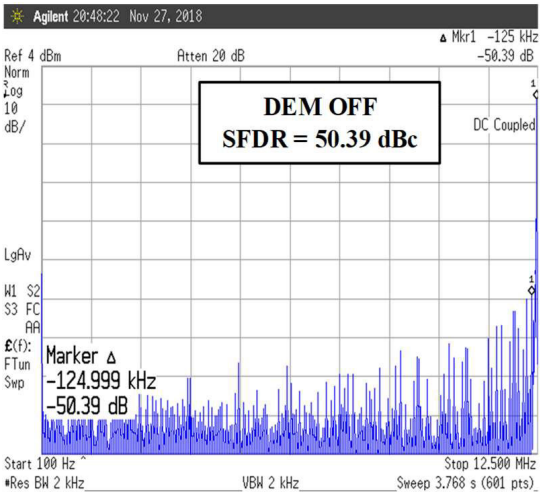
FIGURE 15 shows the SFDR of the DAC using the LW-DEM as a function of signal frequency up to the Nyquist frequency at 25 MS/s. The SFDR improvement is about 5 to 10 dB over the entire Nyquist frequency. Plus, compared to the conventional RRBS DEM technique, the performance of the LW-DEM technique is similar at all times.

TABLE 1 shows the performance comparison results with the recent papers [19], [26]–[28] focused on low power and small area DAC designs. In terms of low power operation, proposed DAC exhibits the lowest power consumption as shown in the comparison table. Compare with the conventional RRBS DAC [19], the proposed DAC consumes less than 64% of the power. In addition, the proposed DAC shows the best result for the area occupied. Considering that the area of a DAC is generally independent on the process technology (i.e., even if a DAC is designed with advanced process technology, it must maintain the area of the current source that occupies the largest area of a DAC to ensure a low mismatch of the current source [24].), and considering that the area of a DAC tends to exponentially increases with increasing resolution, the proposed 12-bit DAC is the smallest one among the DACs in the table. Meanwhile, the measured dynamic performance of the proposed DAC is reported to be slightly lower than DACs in [19], [26]. The reason why the proposed DEM technique exhibits the same level of performance during simulation as in Section III-B, but lower than expected performance is reported in the measurement results may be due to the timing mismatch or code dependent load variation (CDLV).

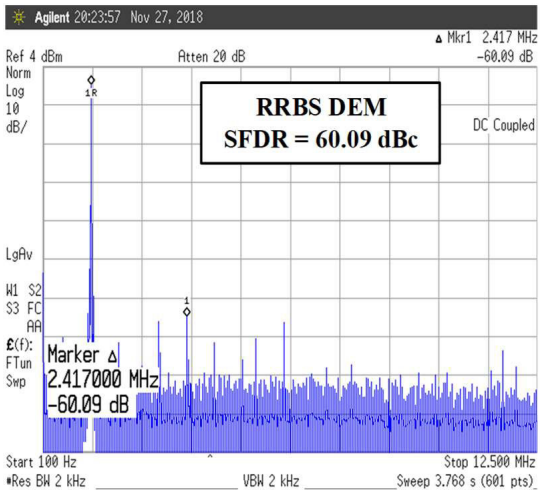
In terms of the static performance evaluation, static measurement of the prototype DAC is performed. FIGURE 16 shows the measured static input/output characteristics results with and without LW-DEM. Although the maximum values of errors (marked in blue in FIGURE 16) do not differ greatly from each other in FIGURE 16, they can have decisive effect on the DAC output. In other words, when the LW-DEM is disabled, the error tends to be fixed at positive or negative.



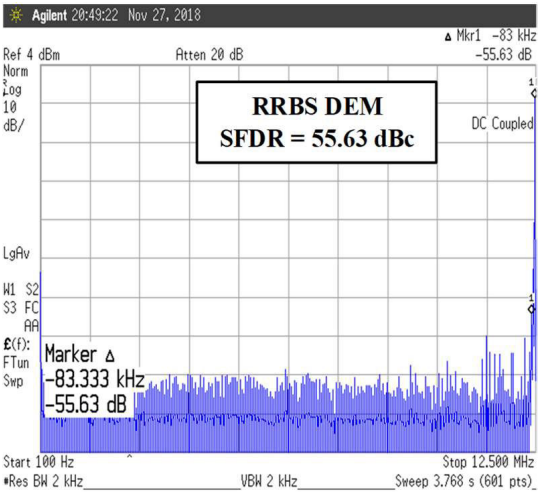
(a)



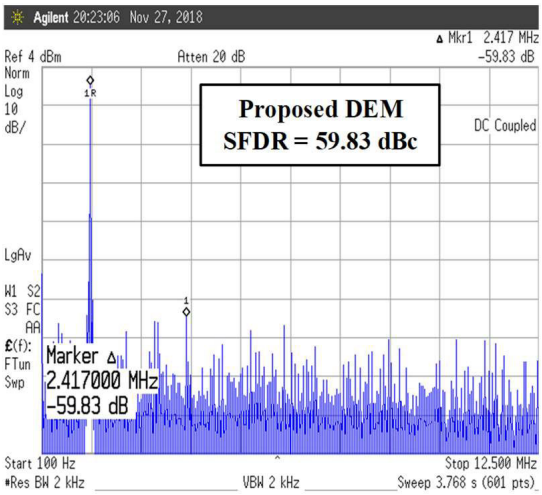
(d)



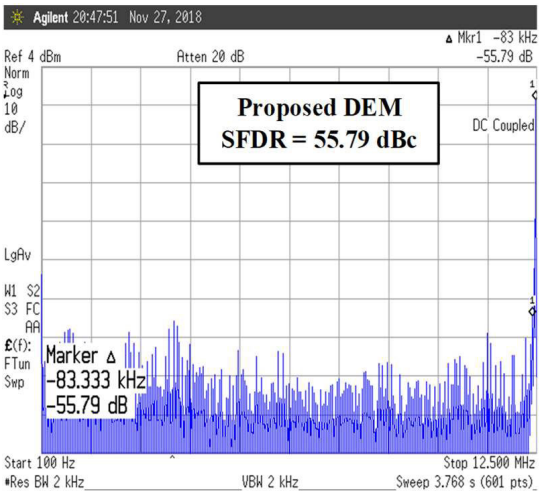
(b)



(e)



(c)



(f)

FIGURE 14. Measurement results of the spectrum for the SFDR with (a), (b), (c) 1.2MHz and (d, (e), (f) 12.46MHz signal at 25MS/s. The conventional binary weighted DAC without the DEM technique is used in (a) and (d), the DAC with RRBS DEM is used in (b), (e), and the proposed DAC with LW-DEM is used in (c), (f).

TABLE 1. Performance comparison.

	This work	[28]	[26]	[27]	[19]
		ITG, 2017	TVLSI, 2018	TVLSI, 2016	JSSC, 2012
Resolution	12	12	12	10	10
Technology (nm)	65	130	130	180	180
Sample rate (MS/s)	25	60	100	400	500
I_{load} (mA)	8	-	16	-	10
P_{total} (mW)	15.3	25	18	20.7	24
Area (mm^2)	0.065	0.1	0.21	0.8*	0.034*
$SFDR_{Min.}$ (dB)	55.8	-	62.1	49	61

* Note that these areas are for 10-bit resolution.

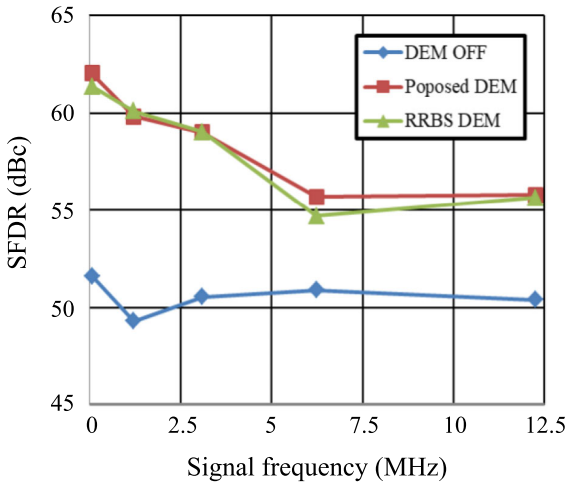


FIGURE 15. SFDR vs. signal frequency clocked at 25 MS/s.

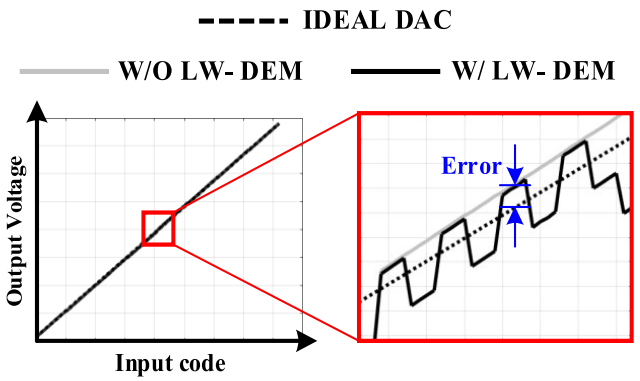


FIGURE 16. Measured static input/output charateristics of the ideal, W/O LW-DEM, and W/ LW-DEM DACs.

However, as shown in FIGURE 16, the error alternates between positive and negative when the LW-DEM is enabled. This means that the average of the DAC output is close to the ideal one. In a consequence, the SFDR can be improved up to 10 dB in prototype DAC in our work.

Experimental work with the prototype DAC have demonstrated that the proposed LW-DEM can achieve significant power saving and area reduction with negligible performance penalty. Therefore, the LW-DEM proved to be a very effective technique for designing the most suitable DAC for the low-power IoT devices.

V. CONCLUSION

In this paper, we have first reviewed the traditional DEM technique designed to improve the SFDR performance of DACs. We have noticed that the PRNG in the randomizer for the DEM technique inevitably consumes a lot of power and has a large area in a DAC, and have raised the question of how to reduce the power and area overhead of the randomizer but maintaining the performance of DACs. Through the intensive simulations, we have found that input data of a DAC tends to be sufficiently random, so that we can exploit the input data to randomly select the current source instead of using the PRNG. This allows PRNG to be removed from the randomizer, resulting in significant power saving and area reduction. We have called this method, a lightweight DEM (LW-DEM) technique, and have proposed a new DAC architecture along with its operation principle to exploit the LW-DEM. In order to demonstrate the power and area saving effects of the LW-DEM, a 12-bit DAC using LW-DEM has been implemented. The 12-bit DAC design has been carefully designed and fabricated in 65nm CMOS technology. Measured data with the prototype DAC have verified that it fulfills 39% power saving and 52% area reduction in the randomizer, compared to a DAC using the conventional RRBS DEM. At the same time, the measured performance of the prototype DAC shows that its SFDR is better than 55 dB, demonstrating that the LW-DEM achieves almost same performance as the conventional DEM technique.

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