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Model Predictive Control Method With NP Voltage Balance by Offset Voltage Injection for Three-Phase Three-Level NPC Inverter

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ABSTRACT This paper proposes a predictive control method with offset voltage injection for achieving a neutral point (NP) voltage balance of three-phase three-level neutral point clamped (NPC) inverter, without employing a weighting factor. In order to ensure the proper and reliable operation of the NPC inverter, the NP voltage balance should be regulated in addition to the sinusoidal output current. The conventional predictive control methods for NPC has suffered from tedious weighting factor selection. Besides, when the converter's parameters value and control condition changes, it is cumbersome to empirically redesign the weighting factor. Therefore, the proposed predictive control method without the weighting factor can successfully maintain the balance of NP voltage by utilizing an offset voltage, which is determined according to the difference between the upper and lower capacitor voltages. As a result, the proposed algorithm using the offset voltage injection can control the output currents and maintain the balance of NP voltage. Simulation and experiments are presented to prove the validity of the NP voltage balancing of the proposed control method.

INDEX TERMS Neutral point clamped (NPC) inverter, predictive control method, neutral point (NP) voltage balance, offset voltage injection.

I. INTRODUCTION

The recent increase in the application of high power systems and equipment in the industrial field reveals the limitations of two-level converters [1]–[3]. When using a two-level converter in a high-power system, switching losses occur, and the power efficiency decreases as the switching frequency increases, and due to the circuit's structural characteristics, the stress required to endure per switch increases, thus reducing the lifetime of the device [4], [5]. This requires more frequent maintenance and repair of the converter and limits the switching frequency. In order to overcome the limitations of the two-level converter, many multilevel converters have recently been studied [6]–[10]. In the multilevel converter, the voltage level of the converter is increased as compared to the two-level converter because the number of switches existing in each phase of the circuit increases [8]–[12]. This circuit structural feature allows multiple switches to distribute stress. Because of the increased levels, the input current has a lower total harmonic distortion (THD) than two-level converters, so multilevel converters have good current characteristics without increasing the filter size. Besides, the low current THD eliminates the need for higher switching frequencies, resulting in better power efficiency than two-level converters. Because of these advantages, it is advantageous to use multilevel converters rather than two-level converters in high power systems [10]–[14].

Recently, many researches have been done on the three-level NPC converter among multilevel converters [15]–[26]. The three-level NPC converter has four switches and two clamping diodes per phase, and two additional DC capacitors to make the converter three voltage levels. However, the disadvantage of three-level NPC converters is that the currents, as well as the capacitor voltage, should be controlled. The capacitor voltage unbalance not only reduces control performance but also increases the stress on the switch, which can increase the probability of the converter failing. Therefore, various control methods for controlling the current and

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capacitor voltage of three-level NPC converters were studied [15]–[17]. Among them, many model predictive control (MPC) methods have been studied to control the three-level NPC converter easily and simply [20]–[23]. MPC method selects the switching state, which can minimize cost function to control the converter.

There are terms for the current and capacitor voltage in the cost function, and the switching state is selected to minimize the error between the reference value and the predicted value. However, the conventional MPC method has a weighting factor that determines the control ratio of current and voltage in the cost function [27], and it is cumbersome to redesign when the parameter or control condition changes. To eliminate the weighting factor in the MPC method, several studies have been conducted [30]–[36]. In [35], the preselection algorithm is applied to reduce the computation time, and the capacitor voltage term is eliminated from the cost function to eliminate the weighting factor. The switching state of small vector is selected according to the capacitor voltage. In this control method, the capacitor voltage balance can be limited when the magnitude of the reference voltage vector is many large and small vectors are not selected. Besides, when there is a large phase difference between the reference voltage and the output current, the capacitor voltage balance can also be limited. In [36], a three-step algorithm is proposed to eliminate the weighting factor. There are three cost functions used in [36]. In the first cost function, K switching states with small errors are selected. In the second cost function, N switching states with small errors are selected from the K switching states. The optimal switching state is selected in the last cost function from the N switching states. Although this algorithm can eliminate the weighting factor by using three cost functions, the increase in computation time is inevitable due to the added cost function. Furthermore, in [37], the author proposes a predictive control method using injected offset voltage to achieve NP voltage balance in a three-phase three-level NPC rectifier, without employing the weighting factor in the cost function.

In this paper, a new MPC method to control the NP voltage balance of three-phase three-level NPC inverter by offset voltage injection is proposed. The proposed algorithm does not use the weighting factor in the cost function, unlike the conventional method. In the proposed method, the reference voltage is used to control output current to avoid weighting factors. However, when controlling only with the reference voltage, the current can be controlled, but the capacitor voltage cannot be controlled. Therefore, the offset voltage is injected into the reference voltage to further control the capacitor voltage. The difference between the two DC capacitor voltages can be successfully reduced by injecting the offset voltage into the reference voltage, which is used to control the input currents. The offset voltage is determined by the difference of the DC capacitor voltage. In addition, when the phase difference between the reference voltage and the output current occurs, the switching state candidates are excluded to maintain the capacitor voltage balance and selected according to the capacitor voltages. When the phase difference is larger than 60°, the capacitor voltage balance is maintained by changing the switching state of the small vector. As a result, the proposed method enables control of the capacitor voltage balance as well as control of the output current. The validity of the proposed method is verified through simulations and experiments.

The rest of the paper is organized as follows. Section II describes the topology and mathematical model for a three-phase three-level NPC inverter, and the associated conventional predictive control method. The previous approaches corresponding to avoid the weighting factor are discussed. Section IV introduces and discusses the proposed model predictive control method with NP voltage balance by offset voltage injection. The simulated and experimental results for the proposed approach are given in Section V, and the conclusion is provided in Section VI.

II. THREE_PHASE THREE_LEVEL NPC INVERTER SYSTEM AND CONVENTIONAL PREDICTIVE CONTROL METHOD

A. THREE-PHASE THREE_LEVEL NPC INVERTER

As mentioned in the introduction, a three-level NPC inverter is a suitable topology for use in high power systems. The reason lies in the circuit structure of the three-level NPC inverter. 2-level converters that were widely used have two switches in each phase. Therefore, one switch has to bear the voltage stress of $+V_{dc}/2$ or $-V_{dc}/2$. In addition, when the switching state changes from positive to negative, the switch can be momentarily subjected to voltage stress of V_{dc}, which can adversely affect the lifetime of the switch. However, each phase of the three-phase three-level NPC inverter consists of four switches and two diodes. Thus, unlike two-level converters, two switches can distribute the voltage stress of $+V_{dc}/2$ or $-V_{dc}/2$. Also, the three-level NPC inverter can have three voltage levels because the two center switches and two diodes allow the load to be connected to the NP of the dc-link. The three-level inverter has better THD (Total Harmonic Distortion) than the two-level converter because it has three voltage levels. However, when the zero voltage is selected, current flows through the NP, which can cause variations in upper and lower capacitor voltages. Therefore, the three-level inverter must control the balance of the upper and lower capacitor voltages as well as the current. Fig. 1 shows the topology of a three-phase three-level NPC inverter. As shown in Fig. 1, each phase of three-phase three-level NPC inverter consists of four switches (S_{x1}, S_{x2}, S_{x3} and S_{x4}) and two diodes (D_{x1} and D_{x2}). The midpoints of switches S_{x2} and S_{x3} of each phase are connected to the load and the midpoints of diodes D_{x1} and D_{x2} are connected to the NP. The upper and lower capacitor voltages located on the dc-link must be controlled to maintain balance. As shown in Table 1, the three-level inverter can produce three voltage levels which are P, O, and N depending on the switching status and generate pole voltages of $V_{dc}/2$, 0 and $-V_{dc}/2$, respectively.

TABLE 1. Operating status of the switch and pole voltage.

Switching State	Switching Status ($x = a, b, c$)				Pole Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_{x0}
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

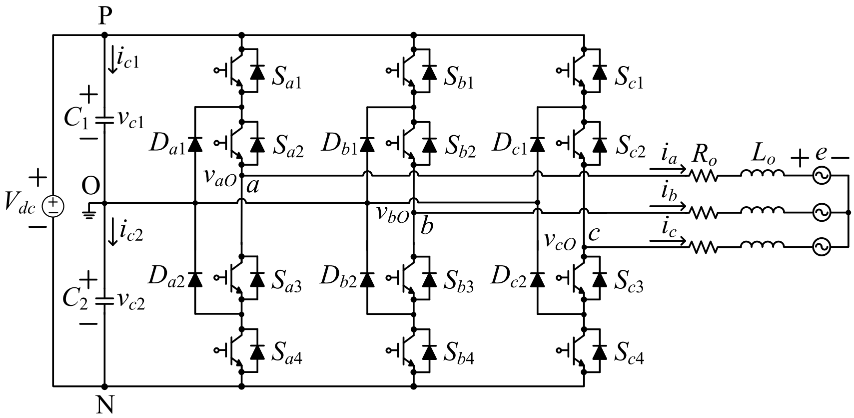

FIGURE 1. Three-phase three-level NPC inverter.

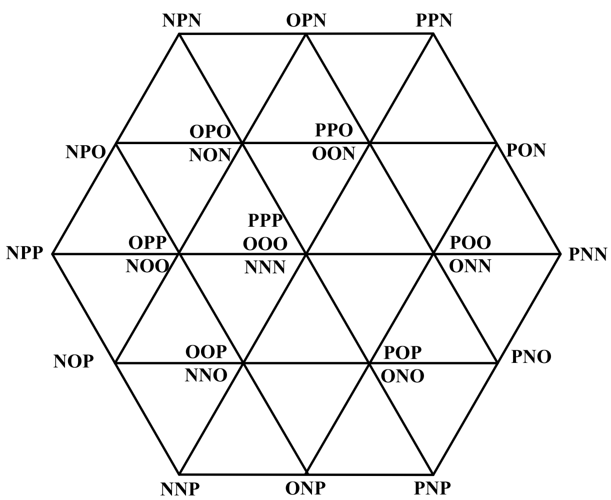

FIGURE 2. Space vector diagram of a three-phase three-level NPC Inverter.

Since each phase of the inverter can have three switching states, there are 27 possible switching combinations for a three-phase inverter. Fig. 2 shows a space vector diagram of the three-phase three-level NPC inverter. As shown in Fig. 2, there are 6 large vectors ([PNN], [PPN], [NPN], [NPP], [NNP], [PNP]), 6 medium vectors ([PON], [OPN], [NPO], [NOP], [ONP], [PNO]) and 3 zero vectors ([PPP], [OOO], [NNN]). In addition, there are 6 redundant switching state sets, which show that the two switching states in each set have the same vector magnitude and phase. Therefore, the current and the capacitor voltage change according to the voltage vector selected.

B. CONVENTIONAL MODEL PREDICTIVE CONTROL METHOD

The MPC (Model Predictive Control) method is a control method of controlling the converter by predicting future values using the converter model based on the fact that only a finite number of possible switching states can be made by the converter. All future values generated in each switching state are calculated and compared to the reference value to select the switching state with the lowest error. The MPC method selects the switching state in the future by calculating the switching state with the smallest error between the reference value and predicted value using the cost function. The cost function generally consists of the variables which need to be controlled. The conventional MPC method of three-phase three-level NPC inverter is as follows [27]. Considering the circuit of the three-phase three-level NPC inverter shown in Fig. 1, the model of the converter for each phase can be written as

$$v_{xO} = R_o i_x + L_o \frac{di_x}{dt} + e_x \quad (x = a, b, c), \tag{1}$$

where v_x, i_x and e_x are the pole voltage, the output current, and the back-electromotive force (back-emf), respectively. R_o and L_o are the output resistance and the output inductance, respectively. Using the constant sampling period T_s and Euler's formula, equation (1) in the discrete-time domain can be expressed as

$$v_x(k) = R_o i_x(k) + L_o \frac{i_x(k+1) - i_x(k)}{T_s} + e_x(k) \quad (x = a, b, c). \tag{2}$$

The future output current can be predicted by transforming the model in (2) for the current as

$$i_x(k+1) = i_x(k) + \frac{T_s}{L_o}\left(v_{xO} - R_o i_x(k) - e_x(k)\right) \quad (x = a, b, c), \qquad (3)$$

where v_{xO} is the pole voltage determined by the switching state, as shown in Table 1. Therefore, all possible future currents can be calculated by substituting all switching states in (3).

The model predictive control technique compares all switching state combinations to select the optimal switching state. The required large number of calculations might introduce a substantial time delay in the practical implementation of the MPC. This delay can deteriorate the operation of the system. For proper practical implementation of the MPC, delay compensation techniques should be applied. For the delay compensation, by shifting the model in (3) by one-step forward, the future current at the $(k+2)^{\text{th}}$ instant is obtained as [28], [29]

$$i_x(k+2) = i_x(k+1) + \frac{T_s}{L_o}\left(v_{xO}(k+1) - R_o i_x(k+1) - e_x(k+1)\right) \quad (x = a, b, c). \qquad (4)$$

Since the back-emf changes at a much lower frequency compared to the sampling frequency, it can be assumed that the future back-emf to be the same as the present back-emf value as [28]. The present back-emf can be deduced from (4) as follow

$$e_x(k+1) \cong \widehat{e_x}(k) = v_x(k) - R_o i_x(k) - \frac{L_o}{T_s}\left(i_x(k+1) - i_x(k)\right) \quad (x = a, b, c). \qquad (5)$$

The switching function according to the switch modules on a, b, and c phase can be defined as follows.

$$S_x = \begin{cases} S_x = 1 & (S_{x1}, S_{x2} : ON) \\ S_x = 0 & (S_{x2}, S_{x3} : ON) \\ S_x = -1 & (S_{x3}, S_{x4} : ON) \end{cases} \quad (x = a, b, c), \qquad (6)$$

where $S_{xj}(x = a, b, c; j = 1, 2, 3, 4)$ means the switching states of the four switches located on each phase. Using the switching state of the inverter and the output currents, the current flowing through the upper and lower capacitors can be expressed as (7) and (8).

$$i_{c1} = -\frac{S_a(S_a+1)}{2} i_a - \frac{S_b(S_b+1)}{2} i_b - \frac{S_c(S_c+1)}{2} i_c, \qquad (7)$$

$$i_{c2} = \frac{S_a(S_a-1)}{2} i_a + \frac{S_b(S_b-1)}{2} i_b + \frac{S_c(S_c-1)}{2} i_c, \qquad (8)$$

where i_{c1} and i_{c2} represent the current flowing through the upper and lower capacitors, respectively. i_a, i_b and i_c are the output currents for a, b, and c phase, respectively. According to the capacitor voltage formula, the upper and the lower capacitor voltages can be expressed as (9).

$$\frac{dv_{ci}}{dt} = \frac{1}{C} i_{ci} \quad (i = 1, 2), \qquad (9)$$

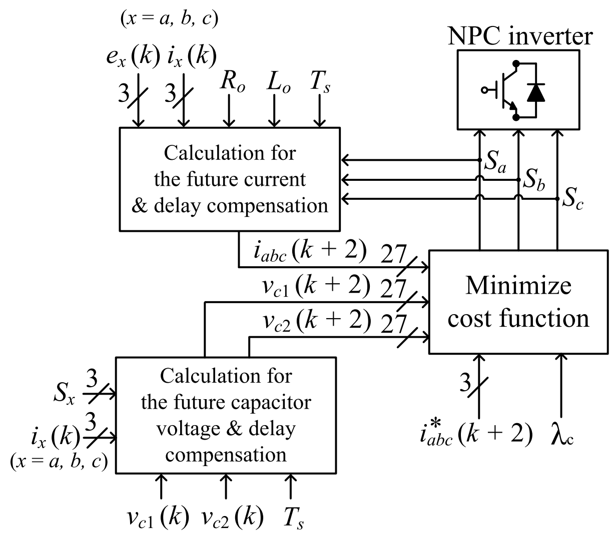

FIGURE 3. Control block of the conventional predictive method.

where C is the capacitance of the upper and lower capacitors.

The future capacitor voltage can be predicted from (9) as follows

$$v_{ci}(k+1) = v_{ci}(k) + \frac{T_s}{C} i_{ci}(k) \quad (i = 1, 2). \qquad (10)$$

For the delay compensation, by shifting the equation in (10) by one-step forward, the future capacitor voltages at the $(k+2)^{\text{th}}$ instant are obtained as [27], [28]

$$v_{ci}(k+2) = v_{ci}(k+1) + \frac{T_s}{C} i_{ci}(k+1), \quad (i = 1, 2) \qquad (11)$$

The cost function of the conventional predictive control method is as follows.

$$g_{con}(\mathrm{k}) = \left|i^*_{\mathrm{a}}(\mathrm{k}+2) - i_{\mathrm{a}}(\mathrm{k}+2)\right| + \left|i^*_{\mathrm{b}}(\mathrm{k}+2) - i_b(\mathrm{k}+2)\right| + \left|i^*_{\mathrm{c}}(\mathrm{k}+2) - i_{\mathrm{c}}(\mathrm{k}+2)\right| + \lambda_{\mathrm{c}}\left|v_{\mathrm{c}1}(\mathrm{k}+2) - v_{\mathrm{c}2}(\mathrm{k}+2)\right|, \qquad (12)$$

where i^*_{a}, i^*_{b} and i^*_{c} are the reference output currents on a, b and c phase, respectively, and λ_{c} is a weighting factor. The reference currents can be calculated from the Lagrange extrapolation using the present and the two past reference values as [29]

$$i^*_{\mathrm{abc}}(\mathrm{k}+2) = 3i^*_{\mathrm{abc}}(\mathrm{k}+1) - 3i^*_{\mathrm{abc}}(\mathrm{k}) + i^*_{\mathrm{abc}}(\mathrm{k}-1), \qquad (13)$$

where $i^*_{\mathrm{abc}}(\mathrm{k}+1)$, $i^*_{\mathrm{abc}}(\mathrm{k})$ and $i^*_{\mathrm{abc}}(\mathrm{k}-1)$ are the reference output currents at the $(k+1)^{\text{th}}$, k^{th}, and $(k-1)^{\text{th}}$ instant, respectively. Fig. 3 shows the control block of the conventional method.

In the conventional predictive control method, the weighting factor is required in the cost function because there are two control targets, which are output currents and the capacitor voltages. Also, control performance depends on the value of the weighting factor. Therefore, if control conditions or parameters change, the weighting factor must be redesigned, and in general, the weighting factor is empirically designed. Therefore, many studies have been conducted to eliminate the weighting factor.

III. PREVIOUS RESEARCHES TO AVOID THE WEIGHTING FACTOR

In model predictive control, the weighting factor is used when there are several targets to control. However, the performance of the controlling target depends on the value of the weighting factor. That is why it is always important to decide what weighting factor to use. Many studies have been conducted to eliminate the weighting factor [30]–[36]. Among them, the algorithm that eliminates the weighting factor is the most applied to the motor. This is because the motor cannot be controlled by controlling only one variable. In conventional model predictive torque control (MPTC) method, torque and stator fluxes had to be controlled. However, because torque and stator flux have different units, the weighting factor is used to determine the control weight between torque and stator flux in the cost function. To eliminate the weighting factor, in [30], voltage vector, which is calculated by using the model of torque and stator flux is used in the cost function. In [31], a virtual vector that is calculated by using the model of motor is used in the cost function to control motor, and two hysteresis comparators are used to determine which virtual vector to use. In [32], new reference stator flux is calculated by using torque and stator flux to eliminate torque in the cost function from the conventional method. In [33], torque and reactive torque are used in the cost function to control motor. Reactive torque is calculated by using the model of stator flux. In the conventional model predictive direct speed control, speed, d-axis, and q-axis components of current are used in the cost function. In [34], a voltage vector, which is calculated by using the model of the motor, is used in the cost function to control the speed of the motor. In addition to the motor, multilevel converters are one of the applications with many targets to control. Among them, the use of the weighting factor in the cost function is inevitable in NPC converter and nested neutral point clamped (NNPC) converter because these topologies must control both current and capacitor voltage [35], [36].

In [35], the capacitor voltage term in the cost function is eliminated to eliminate the weighting factor. Therefore, the voltage vector term in the cost function is only used to control the output currents. To maintain the capacitor voltage balance, the redundant switching state is selected properly. The redundant switching state has the same magnitude and angle of the voltage vector, but the change in capacitor voltage is opposite. Therefore, when selecting a voltage vector with redundant switching states, the appropriate switching state is selected according to the capacitor voltage. In addition, an algorithm that uses only adjacent vectors as switching state candidates was also applied to reduce the computation time. Fig. 4 shows the space vector diagram and divided sectors used in [35]. As shown in Fig. 4, the reference voltage is located at sector I-3. In this case, the switching state candidates are the switching states [PON], [PPN], and one of

TABLE 2. Switching state candidates when $v_{c1} \geq v_{c2}$.

Sector	Switching state candidates	Sector	Switching state candidates
I-1	[OOO], [POO], [PPO]	IV-1	[OOO], [OPP], [OOP]
I-2	[PPO], [POO], [PON]	IV-2	[OPP], [OOP], [NOP]
I-3	[PPO], [PON], [PPN]	IV-3	[OOP], [NOP], [NNP]
I-4	[POO], [PON], [PNN]	IV-4	[OPP], [NOP], [NPP]
II-1	[OOO], [OPO], [PPO]	V-1	[OOO], [OOP], [POP]
II-2	[OPO], [PPO], [OPN]	V-2	[OOP], [POP], [ONP]
II-3	[OPO], [OPN], [NPN]	V-3	[POP], [ONP], [PNP]
II-4	[PPO], [OPN], [PPN]	V-4	[OOP], [ONP], [NNP]
III-1	[OOO], [OPP], [OPO]	VI-1	[OOO], [POP], [POO]
III-2	[OPP], [OPO], [NPO]	VI-2	[POP], [POO], [PNO]
III-3	[OPP], [NPO], [NPP]	VI-3	[POO], [PNO], [PNN]
III-4	[OPO], [NPO], [NPN]	VI-4	[POP], [PNO], [PNP]

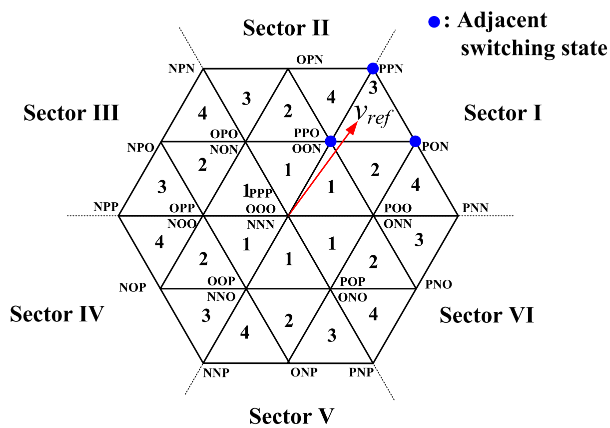

FIGURE 4. Space vector diagram and divided sectors used in [35].

[PPO] and [OON]. If only the adjacent vectors are used as candidates, the computation time of the algorithm can be greatly reduced. In this paper, computation time was saved up to 53.3%. The capacitor voltage determines whether the switching candidate is [PPO] or [OON]. Thus, the capacitor voltage balance can be maintained. Tables 2 and 3 show the switching state candidates according to the capacitor voltages for each sector.

However, the capacitor voltage balance can be limited when the magnitude of the reference voltage vector is large, and a small vector is not selected. The capacitor voltage is controlled by selecting the appropriate switching state when selecting a small vector. Therefore, if the small vector is not selected, the capacitor voltage cannot be controlled. Another limitation is when the phase difference between the reference

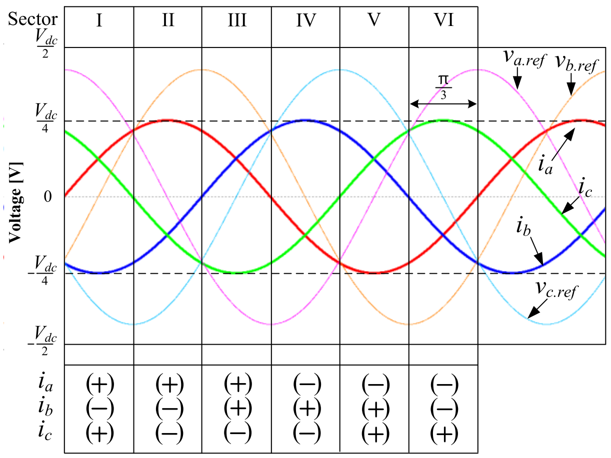

FIGURE 5. Sign of output current for each sector when phase difference between reference voltage and output current is 90°.

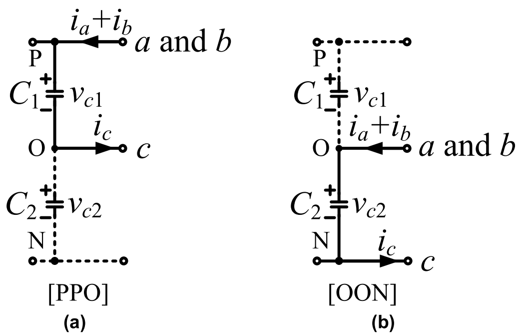

FIGURE 6. Output current flow in sector I-3 with switching status (a) [PPO] and (b) [OON] when phase difference between reference voltage and output current is 90°.

voltage and the current becomes large. When the phase difference between the reference voltage and the output current occurs, the variation of the capacitor voltage when selecting the small vector and the medium vector changes. Fig. 5 shows the sign of the output current for each sector when the phase difference between the reference voltage and output current is 90°. If the reference voltage vector is located in sector I-3 as shown in Table 2 and 3, the switching state candidates can be the switching states [PPO], [PON] and [PPN] with $v_{c1} \geq v_{c2}$ and [OON], [PON] and [PPN] with $v_{c1} < v_{c2}$. The signs of a, b and c-phase currents are (+), (−) and (+), respectively. The capacitor current flow in the switching states [PPO] and [OON] according to the current direction is shown in Fig. 6.

As shown in Fig. 6 (a), since the current flows into the upper capacitor, the upper capacitor is charged, and the lower capacitor voltage decreases. Therefore, when the switching state candidates of Table 2 are used according to the capacitor voltage proposed in [35], the capacitor voltage cannot be controlled. Similarly, as shown in Fig. 6 (b), because current flows into the lower capacitor, the lower capacitor is charged, and the upper capacitor voltage decreases. Using the switching state candidates of Table 3 cannot control the capacitor

TABLE 3. Switching state candidates when $v_{c1} < v_{c2}$.

Sector	Switching state candidates	Sector	Switching state candidates
I-1	[OOO], [ONN], [OON]	IV-1	[OOO], [NOO], [NNO]
I-2	[OON], [ONN], [PON]	IV-2	[NOO], [NNO], [NOP]
I-3	[OON], [PON], [PPN]	IV-3	[NNO], [NOP], [NNP]
I-4	[ONN], [PON], [PNN]	IV-4	[NOO], [NOP], [NPP]
II-1	[OOO], [NON], [OON]	V-1	[OOO], [NNO], [ONO]
II-2	[NON], [OON], [OPN]	V-2	[NNO], [ONO], [ONP]
II-3	[NON], [OPN], [NPN]	V-3	[ONO], [ONP], [PNP]
II-4	[OON], [OPN], [PPN]	V-4	[NNO], [ONP], [NNP]
III-1	[OOO], [NOO], [NON]	VI-1	[OOO], [ONO], [ONN]
III-2	[NOO], [NON], [NPO]	VI-2	[ONO], [ONN], [PNO]
III-3	[NOO], [NPO], [NPP]	VI-3	[ONN], [PNO], [PNN]
III-4	[NON], [NPO], [NPN]	VI-4	[ONO], [PNO], [PNP]

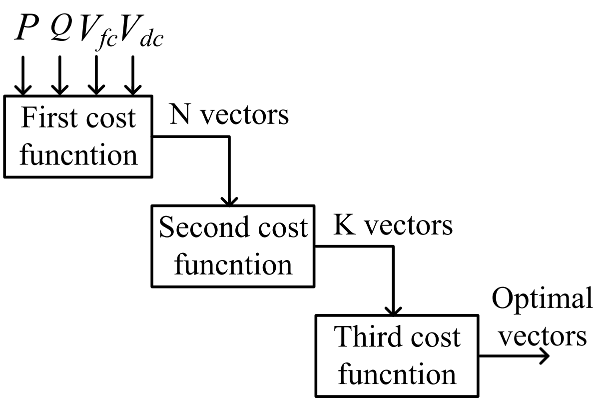

FIGURE 7. Control block of the proposed method in [36].

voltages. Thus, when there is a large phase difference between the reference voltage and the output current, the algorithm of [35] has a limitation in controlling the capacitor voltages.

In [36], the weighting factor is eliminated by using dividing the cost function into three. In the conventional algorithm of [36], there are four weighting factors in the cost function to control four variables, which are active power, reactive power, flying capacitor voltage, and dc-link capacitor voltage. The proposed algorithm uses three cost functions. The first cost function controls active power and reactive power. Second and third cost function control flying capacitor voltage and dc-link capacitor voltage, respectively. Fig. 7 shows the control block of the proposed method in [36].

As shown in Fig. 7, the first cost function, which only controls the flying capacitor voltage and dc-link capacitor voltage, selects N vectors with the smallest errors. In the second cost function, K vectors are selected to control active power and reactive power. In the third cost function, the optimal vector with the smallest error is selected to control the switching frequency. Three-step control can successfully eliminate the weighting factors in the cost function. However, the computation time is increased. In the conventional method, there is only one cost function, which considers 144 switching states. In the first cost function of three-step control, 144 switching states should be considered. In the second and third steps, N and K switching states should be considered, respectively. This causes an increase in computation time.

IV. PROPOSED NP VOLTAGE CONTROL ALGORITHM

One of the disadvantages of the conventional MPC method is that the weighting factor of the cost function needs to be designed. The weighting factor is a value that determines the weight of control between the output currents and the capacitor voltages. Therefore, if the control conditions or parameters change, the weighting factor also has to be redesigned. In this paper, an algorithm that simultaneously controls output currents and capacitor voltages without using weighting factors was proposed. The cost function of the proposed algorithm is based on pole voltage instead of (12) used in the conventional method. The proposed algorithm first controls the output current by generating a reference voltage using the reference current. Then, the capacitor voltages are controlled by injecting the offset voltage into the reference voltage.

A. CURRENT CONTROL ALGORITHM USING REFERENCE VOLTAGE

Assuming that the real output current follows the one-step future reference output current, $i^*(k+1)$, the reference voltage can be obtained by replacing the future output current in (2) with the reference output current as

$$v_x^*(k) = R_o i_x(k) + L_o \frac{i_x^*(k+1) - i_x(k)}{T_s} + e_x(k) \quad (x = \mathrm{a, b, c}), \qquad (14)$$

where v_x^* is the reference voltages for each phase and i_x^* is the reference output currents for each phase. For the delay compensation, by shifting the model in (15) by one-step forward, the reference voltage at the $(k+1)^{\text{th}}$ instant can be obtained as [28], [29]

$$v_x^*(k+1) = R_o i_x(k+1) + L_o \frac{i_x^*(k+2) - i_x(k+1)}{T_s} + e_x(k+1) \; (x = \mathrm{a, b, c}). \qquad (15)$$

The cost function using reference voltage is as follows.

$$\begin{aligned} g_{vol}(\mathrm{k}) = & \left|v_a^*(\mathrm{k}+1) - v_{\mathrm{a}O}(\mathrm{k}+1)\right| \\ & + \left|v_b^*(\mathrm{k}+1) - v_{\mathrm{b}O}(\mathrm{k}+1)\right| \\ & + \left|v_c^*(\mathrm{k}+1) - v_{\mathrm{c}O}(\mathrm{k}+1)\right|, \end{aligned} \qquad (16)$$

where $v_{\mathrm{a}O}$, $v_{\mathrm{b}O}$ and $v_{\mathrm{c}O}$ are pole voltages determined according to the switching states, as shown in Table 1. The switching

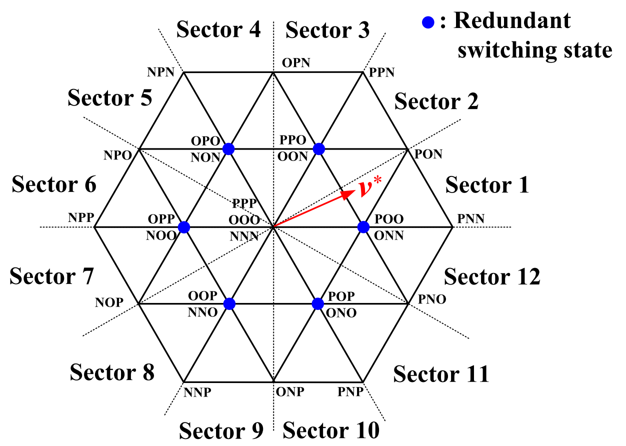

FIGURE 8. Reference voltage vector, redundant switching states and space vector diagram divided by sector.

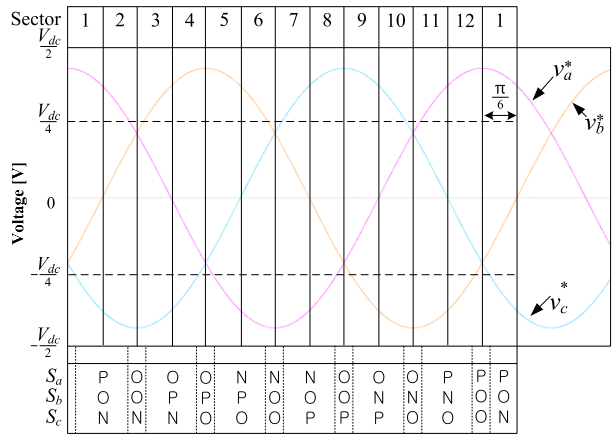

FIGURE 9. Three-phase reference voltage in time-domain and switching states determined by three-phase reference voltage.

states selected according to the magnitude of the reference voltage are as follows.

$$S_x = \begin{cases} 1 & (\text{P state}) \text{ if } \dfrac{V_{dc}}{4} \le v_x^* \le \dfrac{V_{dc}}{2} \\ 0 & (\text{O state}) \text{ if } -\dfrac{V_{dc}}{4} < v_x^* < \dfrac{V_{dc}}{4} \\ -1 & (\text{N state}) \text{ if } -\dfrac{V_{dc}}{2} \le v_x^* \le -\dfrac{V_{dc}}{4} \end{cases} \quad (x = \mathrm{a, b, c}). \qquad (17)$$

The reference voltage vector generated by (15) rotates at a constant frequency, as shown in Fig. 8 in the space vector diagram, and the space vector diagram can be divided into 12 sectors at 30-degree intervals. To see which switching state is selected by the reference voltage, Fig. 8 can be express as Fig. 9 in the time-domain.

To control the capacitor voltage, 6 redundant switching state sets, shown in Fig. 8 should be utilized. Redundant switching states are two switching states that have the same voltage vector but differ in the neutral current. As can be seen in Fig. 9, due to the magnitude of the reference voltage and (18), the switching states selected from the 6 redundant switching state sets are [POO], [OON], [OPO], [NOO], [OOP] and [ONO], and the switching states [ONN], [PPO], [NON], [OPP], [NNO] and [POP] are not selected. The output currents can be controlled by using only 6 switching states ([POO], [OON], [OPO], [NOO], [OOP], and [ONO]) without using all 12 switching states. This is because redundant switching states have the same voltage vector. However, since redundant switching states have a different flow of capacitor current, all 12 switching states must be selected to control the capacitor voltage. Therefore, in this paper, the control algorithm that selects the redundant switching state appropriately for capacitor voltage control using the offset voltage injection was proposed.

B. CAPACITOR VOLTAGE CONTROL ALGORITHM USING OFFSET VOLTAGE INJECTION

The variation of the upper and lower capacitor voltages can be expressed as follows by using (7), (8), and (10).

$$\Delta v_{c1} = \frac{T_s}{C} i_{c1} = \frac{T_s}{C}\left(-\frac{S_a(S_a+1)}{2} i_a - \frac{S_b(S_b+1)}{2} i_b - \frac{S_c(S_c+1)}{2} i_c\right), \tag{18}$$

$$\Delta v_{c2} = \frac{T_s}{C} i_{c2} = \frac{T_s}{C}\left(\frac{S_a(S_a-1)}{2} i_a + \frac{S_b(S_b-1)}{2} i_b + \frac{S_c(S_c-1)}{2} i_c\right). \tag{19}$$

The difference between the upper and the lower capacitor voltage can be defined as follows.

$$v_{diff} = v_{c1} - v_{c2}. \tag{20}$$

In addition, the difference between the change amount of the upper and the lower capacitor voltage can be defined as follows.

$$\Delta v_{diff} = \Delta v_{c1} - \Delta v_{c2} = -\frac{T_s}{C}\left(S_a^2 i_a + S_b^2 i_b + S_c^2 i_c\right). \tag{21}$$

According to Lyapunov stability, the condition for system stability is as follows [38].

$$\frac{dV}{dt} \le 0 \quad (V \ge 0), \tag{22}$$

where $V = v_{diff}^2$.

In order to maintain capacitor voltage balance, the difference between the upper and the lower capacitor voltage should satisfy the following

$$2 v_{diff} \frac{d v_{diff}}{dt} \le 0. \tag{23}$$

Using a constant sampling period T_s, (23) can be expressed in the discrete-time domain as follows.

$$v_{diff}(k) \frac{\Delta v_{diff}(k)}{T_s} \le 0. \tag{24}$$

Using (21), (25) can be expressed as follows.

$$\frac{v_{diff}}{C}(S_a^2 i_a + S_b^2 i_b + S_c^2 i_c) \ge 0. \tag{25}$$

TABLE 4. Switching status selected by offset voltage injection in sector 1.

v_{offset}	S_a	S_b	S_c
+	P	O	O
	P	O	N
−	O	N	N
	P	N	N

Therefore, to maintain the balance of the capacitor voltage, it is necessary to control the three-phase currents and three-phase switching states. For the convenience of explanation, Z is defined as

$$Z = S_a^2 i_a + S_b^2 i_b + S_c^2 i_c. \tag{26}$$

To control the capacitor voltage and the output current at the same time, the new reference voltage proposed in this paper is as follows.

$$v_{x,ref} = v_x^* + v_{offset} \quad (x = \mathrm{a, b, c}), \tag{27}$$

where $v_{x,ref}$ is the new reference voltages for each phase and v_{offset} is the offset voltage injected to control the capacitor voltages. The offset voltage injection makes it possible to select all 12 switching states in 6 redundant switching state sets to control the capacitor voltages. The range of offset voltage is as follows [26], [38].

$$-\frac{V_{dc}}{2} - v_x^* \le v_{offset} \le \frac{V_{dc}}{2} - v_x^* \quad (x = \mathrm{a, b, c}). \tag{28}$$

The new reference voltage $v_{x,ref}$ injected with the offset voltage must be less than $V_{dc}/2$ and larger than $-V_{dc}/2$. Therefore, the maximum and minimum values of offset voltage can be defined as follows.

$$-\frac{V_{dc}}{2} - v_{min}^* \le v_{offset} \le \frac{V_{dc}}{2} - v_{max}^*, \tag{29}$$

where v_{max}^* and v_{min}^* are the maximum and minimum values among the three-phase reference voltages, respectively. When the offset voltage larger than zero is injected, the magnitude of the reference voltage increases. Therefore, if the switching state without the offset voltage injection is N, O can be selected after the offset voltage injection. If the switching state without the offset voltage injection is O, P can be selected after the offset voltage injection. The reason why P cannot be selected after the offset voltage injection when the switching state without the offset voltage injection is N is that the maximum value of the offset voltage is determined in (28). Similarly, when the offset voltage is less than zero, the magnitude of the reference voltage decreases. Therefore, if the switching state without the offset voltage injection is P, O can be selected after offset voltage injection. If the switching state without the offset voltage injection is O, N can be selected after the offset voltage injection.

For sector1 in Fig. 8, the switching states that can be selected by injecting the offset voltage are shown in Table 4. As can be seen from Table 4, the switching states [POO] and [PON] can be selected when the offset voltage larger than

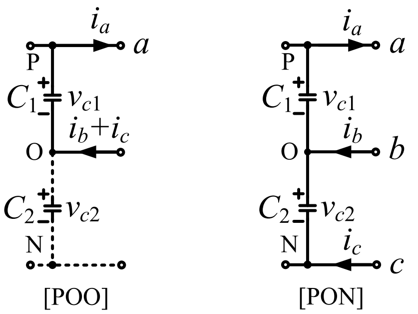

FIGURE 10. **Output current flow in sector1 with switching status (a) [POO] and (b) [PON] with $v_{offset} > 0$ when phase difference between reference voltage and output current is 0°.**

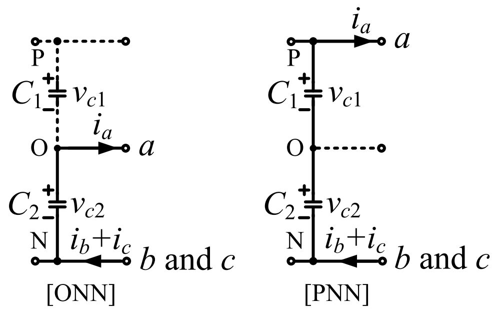

FIGURE 11. **Output current flow in sector1 with switching status (a) [ONN] and (b) [PNN] with $v_{offset} < 0$ when phase difference between reference voltage and output current is 0°.**

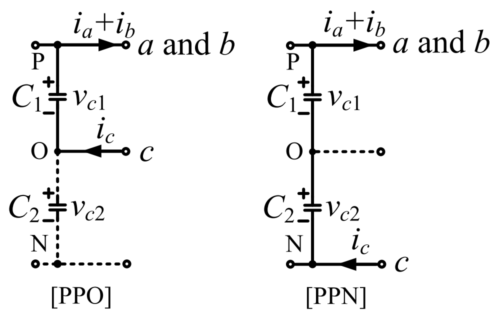

FIGURE 12. **Output current flow in sector2 with switching status (a) [PPO] and (b) [PPN] with $v_{offset} > 0$ when phase difference between reference voltage and output current is 0°.**

0 is injected in sector1, and the switching states [ONN] and [PNN] can be selected when the offset voltage less than 0 is injected. This makes it possible to select the switching state [ONN] that could not be selected before injecting the offset voltage, as shown in Fig. 9.

Substituting the switching state ([POO], [PON]) injected with the offset voltage larger than zero, and the output current in the sector1 of Fig. 8 into (26) is as follows.

$$Z = i_a > 0, \tag{30}$$
$$Z = i_a + i_c > 0. \tag{31}$$

In order for (30) and (31) to satisfy (25), v_{diff} must be larger than zero. The three-phase output current flow in the two cases is shown in Fig. 10. Fig. 10(a) and (b) show the three-phase current flow in the switching states [POO] and [PON], respectively. In Fig. 10(a), because the current flows only to the upper capacitor, the upper capacitor is discharged, and the lower capacitor voltage rises. As can be seen in Fig. 10 (b), $i_a = i_b + i_c$. Thus, the upper capacitor is discharged, and the lower capacitor voltage rises. Therefore, when $v_{diff} > 0$, two switching states can be selected to balance the capacitor voltage.

Equation (26) for the switching states [ONN] and [PNN] injected with the offset voltage less than zero are as follows.

$$Z = i_b + i_c < 0, \tag{32}$$
$$Z = i_a + i_b + i_c = 0. \tag{33}$$

In order for (32) and (33) to satisfy (25), v_{diff} must be less than zero. The three-phase output current flow in two switching states is shown in Fig. 11. Fig. 11(a) and (b) show the three-phase output current flow in the switching states [ONN] and [PNN], respectively. As shown in this Figure, in the switching states [ONN], current flows only to the lower capacitor, so the lower capacitor is discharged, and the upper capacitor voltage rises. The capacitor voltage of the switching state [PNN] does not change because no current flows to the NP. Therefore, when $v_{diff} < 0$, three switching states can be selected to balance the capacitor voltage.

As for sector2, substituting the switching state ([PPO], [PPN]) injected with the offset voltage larger than zero and the output current in the sector2 of Fig. 12 into (27) is as follows.

$$Z = i_a + i_b > 0, \tag{34}$$
$$Z = i_a + i_b + i_c = 0. \tag{35}$$

For (34) and (35) to satisfy (25), v_{diff} must be larger than zero. The three-phase output current flow in two switching states is shown in Fig. 12. Fig. 12(a) and (b) show the three-phase output current flow in the switching states [PPO] and [PPN], respectively. As shown in this Figure, in the switching states [PPO], current flows only to the upper capacitor, so the upper capacitor is discharged, and the lower capacitor voltage rises. The capacitor voltage of the switching state [PPN] does not change because no current flows to the NP. Therefore, when $v_{diff} > 0$, three switching states can be selected to balance the capacitor voltage.

Equation (26) for switching states [OON] and [PON] injected with the offset voltage less than zero are as follows.

$$Z = i_c < 0, \tag{36}$$
$$Z = i_a + i_c < 0. \tag{37}$$

For (36) and (37) to satisfy (25), v_{diff} must be less than zero. The three-phase output current flow in each switching state is shown in Fig. 13. Fig. 13(a) and (b) show the three-phase output current flow in the switching states [OON] and

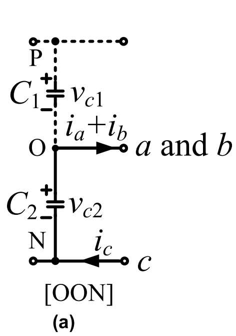

FIGURE 13. Output current flow in sector2 with switching status (a) [OON] and (b) [PON] with $v_{offset} < 0$ when phase difference between reference voltage and output current is 0°.

[PON], respectively. As can be seen from the Figure, the switching state [OON] causes the lower capacitor to be discharged because the current flows only to the lower capacitor, and the upper capacitor voltage rises. Since $i_c = i_a + i_b$ in the switching state [PON], the lower capacitor voltage is discharged, and the upper capacitor voltage rises. Therefore, in order to maintain the capacitor balance, the sign of the offset voltage must always be the same as the sign of v_{diff}, as shown in (38), and the same for sectors 3-12.

$$\operatorname{sgn}\left(v_{offset}\right) = \operatorname{sgn}\left(v_{diff}\right), \tag{38}$$

where sgn(·) is a function that represents a sign. Finally, the offset voltage proposed in this paper is as follows.

$$v_{offset} = \begin{cases} \dfrac{V_{dc}}{2} - v^*_{max} & (v_{c1} > v_{c2}) \\ -\dfrac{V_{dc}}{2} - v^*_{min} & (v_{c1} < v_{c2}). \end{cases} \tag{39}$$

The cost function of the proposed control algorithm is as follows.

$$\begin{aligned} g_{pro}(\mathrm{k}) = & \left|v_{a,ref}(\mathrm{k}+1) - v_{aO}(\mathrm{k}+1)\right| \\ & + \left|v_{b,ref}(\mathrm{k}+1) - v_{bO}(\mathrm{k}+1)\right| \\ & + \left|v_{c,ref}(\mathrm{k}+1) - v_{cO}(\mathrm{k}+1)\right|, \end{aligned} \tag{40}$$

where v_{aO}, v_{bO} and v_{cO} are the pole voltages that change depending on the switching states described in Table 1.

However, the inverter always has a phase difference between the reference voltage and the output current. Therefore, when the phase difference occurs between the reference voltage and the output current, (25) may not be satisfied. Fig. 14 shows a case where a phase difference of 30° occurs between the reference voltage and the output current.

As described above in the case where the phase difference is 0°, when the offset voltage less than 0 is injected in sector2, the switching state [PON] can be selected. As shown in Fig. 13(b), because $i_c = i_a + i_b$, the lower capacitor was discharged, and the capacitor could be balanced again. However, if there is a phase difference of 30° between the reference voltage and the output current, as shown in Fig. 14, the sign of the b-phase current in sector2 is (−), not (+).

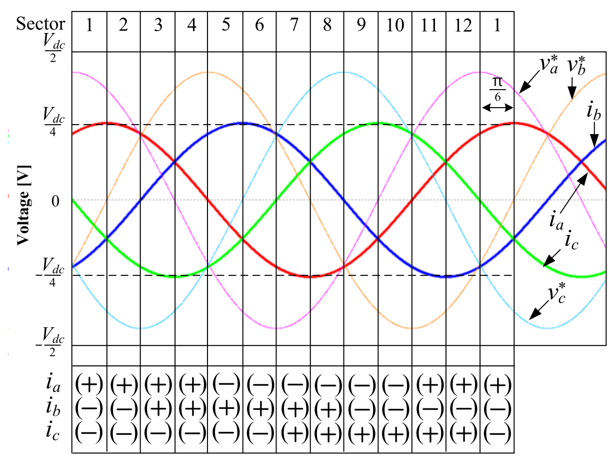

FIGURE 14. Sign of output current for each sector when phase difference between reference voltage and output current is 30°.

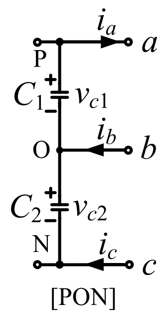

FIGURE 15. Output current flow in sector2 with switching status [PON] with $v_{offset} < 0$ when phase difference between reference voltage and output current is 30°.

The three-phase output current flow for this case is shown in Fig. 15.

In this case, since $i_a = i_b + i_c$, the upper capacitor is discharged, and the lower capacitor voltage rises. This does not satisfy (26). Therefore, in this paper, when the phase difference (θ_d) between the reference voltage and the output current occurs, the switching states that do not satisfy (26) are excluded from the switching state candidates to maintain the balance of the capacitor voltage. As a result, in sectors 2, 4, 6, 8, 10 and 12, the switching states [PON], [OPN], [NPO], [NOP], [ONP] and [PNO] should be excluded from the switching state candidates, respectively, in the case where the phase difference is 0° for maintaining the balance of the capacitor voltage. The same principle is applied when the phase difference between the reference voltage and output current is 60°. Furthermore, when the phase difference between the reference voltage and output current is 90°, this is the opposite of the situation when the phase difference is 0°, and the capacitor voltage balance also cannot be maintained. Thus, the switching state [PON] should also be excluded from the switching state candidates in sector 2. In addition, other even switching sectors should also exclude one switching state candidate for each sector. Fig. 16 shows a space vec-

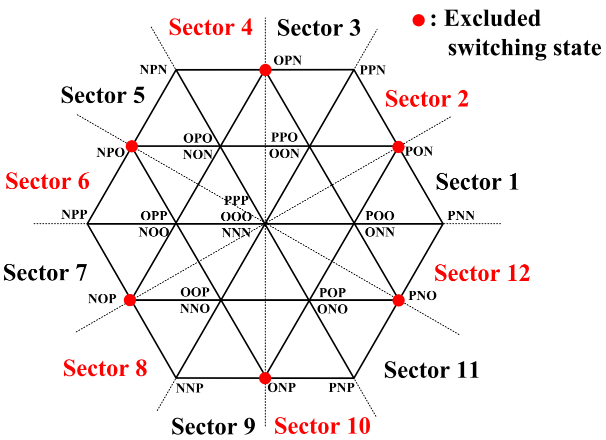

FIGURE 16. A space vector diagram showing the switching state candidates that are excluded in the phase difference with $0° < \theta_d \leq 90°$.

TABLE 5. Changed switching state according to the current condition for each even sector with phase difference $60° < \theta_d \leq 90°$.

Sector	Current condition	Selected switching state by cost function	Applied switching state to inverter
2	$i_c > 0$	[PPO] [OON]	[OON] [PPO]
4	$i_b < 0$	[OPO] [NON]	[NON] [OPO]
6	$i_a > 0$	[OPP] [NOO]	[NOO] [OPP]
8	$i_c < 0$	[OOP] [NNO]	[NNO] [OOP]
10	$i_b > 0$	[POP] [ONO]	[ONO] [POP]
12	$i_a < 0$	[POO]	[ONN]

tor diagram showing the switching state candidates that are excluded in the phase difference with $0° < \theta_d \leq 90°$.

When the phase difference becomes larger than 60°, there are regions in which the direction of the current flowing through the capacitor is changed. To maintain capacitor voltage balance, the applied switching state should be changed according to the direction of the current flowing through the capacitor, as shown in Table 5. The complete control diagram of the proposed approach is illustrated in Fig. 17 and the implementation steps are discussed as follows:

1) The three-phase output currents $i_x(k)$ $(x = a, b, c)$ and capacitor voltage $v_{ci}(k)$ $(i = 1, 2)$ at the k^{th} instant are measured;
2) The magnitude and frequency of the reference output current that flows through the load are defined by the user. The k^{th} instant reference currents are extrapolated to $(k+1)^{\text{th}}$ and $(k+2)^{\text{th}}$ instants as in [28], [29];
3) The reference voltage $v_x^*(k)$ at k^{th} instant is obtained by replacing the future output current in (2) with $(k+1)^{\text{th}}$ instant reference output current using (15) and the reference voltage $v_x^*(k+1)$ at $(k+1)^{\text{th}}$ instant is obtained using (15);

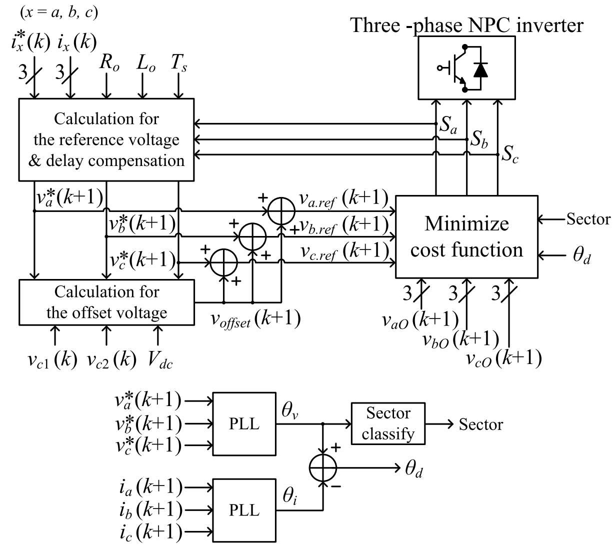

FIGURE 17. Control diagram of proposed control method.

TABLE 6. Parameter values for simulation.

Parameters	Values
V_{dc} (input voltage)	300 [V]
$\lvert i^* \rvert$ (peak value of output reference current)	5 [A]
R_o (output resistance)	23 [Ω]
L_o (output inductance)	18.5 [mH]
T_s (sampling period)	66.67 [μs]
C (dc-capacitance)	2200 [μF]
e (back-emf)	20 [V]

4) The offset voltage v_{offset} is calculated from (40) using the condition regarding the difference of capacitor voltage in (38);
5) The new reference voltage $v_{x,ref}(x = a, b, c)$, controlling the capacitor voltage and the output current, is calculated from (27);
6) The predicted output voltage variables are expressed in terms of switching states. These variables are included in the cost function (40) and evaluated for all possible switching states. The switching state that minimizes the cost function is selected and applied to the inverter directly.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

In this chapter, the proposed NP voltage control algorithm is compared and analyzed to prove the validity of the proposed method. The simulation was performed by changing only the algorithm to the three-level NPC inverter topology using PSIM program. Table 6 shows the parameter values used in the simulation.

In addition, the proposed method was compared with the conventional method to verify the performance of the proposed method. However, in the conventional method, the control performance depends on the value of the weighting factor (λ_c). If the value of the weighting factor is large, the ripple of the capacitor voltage is reduced, but the average THD value of three-phase output currents deteriorates. Conversely, if the value of the weighting factor is small, the average THD value of three-phase output currents is lowered, but the ripple of the capacitor voltage is deteriorated. The weighting factor was set to 0.1, which is used in [27].

The sampling time exerts a significant impact on the control performance of the MPC approach. A small sampling period will result in high performance of the system but require a fast control processor to ensure a large number of calculations necessary. This results in a rise in the cost of the system, causing a challenge in practical implementation as industrial applications. On the other hand, the performance of the system is deteriorated with a large sampling period. The performance of both conventional MPC and the proposed method under different sampling frequency was evaluated. Fig. 18 shows performance change in the average THD pf the three-phase output currents, the current error, the peak-to-peak value of capacitor ripple voltage, and the average number of switching, respectively. As can be seen, there is no significant difference in the performance of the current error, the peak-to-peak value of capacitor ripple, and the number of switching between the conventional MPC method and the proposed approach according to the variation of the sampling frequency. Although the average THD of the three-phase output currents of the proposed method is slightly higher than that of the conventional MPC method, the overall trend is similar. For these reasons, the sampling period is set to 66.66μs in simulation and experiment, which is suitable for both output performance of the system and a clock frequency of DSP TMS320F28335.

Fig. 19 shows the simulation results of the three-phase output current (i_a, i_b, i_c) and the line-to-line voltage (v_{ab}). Fig. 19 (a) and (b) show the conventional control method and the proposed method, respectively. As shown in Fig. 19, the three-phase output currents of both control methods are well controlled with a sinusoidal wave with peak value 5 A, and the line-to-line voltage is five levels. However, the average THD value of three-phase output currents of the proposed method are slightly higher than that of the conventional method. This is because the proposed method excludes the switching state candidate when a phase difference occurs between the reference voltage and the output current. If the switching state candidates are excluded, there may be situations where the inverter cannot select the optimal vector. Selecting another vector without selecting the optimal vector causes an increase in the average THD value of three-phase output currents. Therefore, the average THD value of three-phase output currents of the proposed method is slightly higher than that of the conventional method.

Fig. 20 shows the high-frequency spectrum of the a-phase output current. Fig. 20 (a) and (b) show the conventional control method and the proposed method, respectively. As can be seen from Fig. 20, the harmonic components of the a-phase current obtained by the proposed method is larger than that of the current obtained by the conventional method. This is because, as explained earlier in the average THD value of three-phase output currents, more harmonic components are generated because the optimal vector is not selected.

Fig. 21 (a) and (b) show the waveforms of the upper and lower capacitors (v_{c1}, v_{c2}) obtained by the conventional method and the proposed method, respectively. As shown in Fig. 21, both control methods have well controlled upper and lower capacitor voltage with $V_{dc}/2$. In addition, the ripple value of the capacitor voltage of the conventional method is similar to that of the proposed method.

In order to investigate the capacitor voltage balancing performance of the proposed algorithm, simulations of capacitor voltage balancing under voltage unbalance condition was presented. Capacitor voltage unbalance condition was created by connecting a 1-ohm resistor in parallel to the upper capacitor. By connecting the resistors in parallel for 0.1 s to create a capacitor voltage unbalance condition, and after 0.1 s, the resistor was removed to see if the control methods could rebalance the capacitor voltages. Fig. 22 shows the waveforms of the capacitor voltages and line-to-line voltage, which start voltage balancing at unbalanced conditions. Fig. 22 (a) and (b) are obtained by the conventional control method and the proposed method, respectively. As shown in Fig. 22, capacitor voltage unbalance occurs from 0.31 seconds, and capacitor voltage balancing starts from 0.32 seconds. Both control methods quickly balance the capacitor voltage, and the proposed method achieves a slightly faster-balancing speed.

In order to compare the transient response characteristics, the magnitude and fundamental frequency of three-phase reference currents of the conventional method and the proposed method were changed under steady-state conditions. Fig. 23 shows the transient response waveform with a step change of magnitude of three-phase reference currents from 3.5 A to 6 A. As shown in Figure, the magnitude of the current reference changes in 0.47 s, and both control methods exhibit fast transient response. In addition, it can be seen that the capacitor voltage is controlled to 150 V both before and after the step change. However, as the magnitude of the current reference increases, the ripple of the capacitor voltage also increases.

Fig. 24 shows the transient response waveform with a step change of fundamental frequency of three-phase reference currents from 60 Hz to 100 Hz. As shown in Figure, the fundamental frequency of the current reference changes in 0.47 s, and the capacitor voltage is controlled to 150 V both before and after the step change. In addition, there is no significant difference in the ripple of the capacitor voltage even after the frequency changes from 60 Hz to 100 Hz. Both control methods show a fast-transient response and no difference in speed.

In order to clarify the capacitor voltages balancing feature of the proposed method, the simulation results obtained by the proposed method and the control method in [35] were compared under different phase. Fig. 25 shows the three-phase output currents (i_a, i_b, i_c) and capacitor voltages

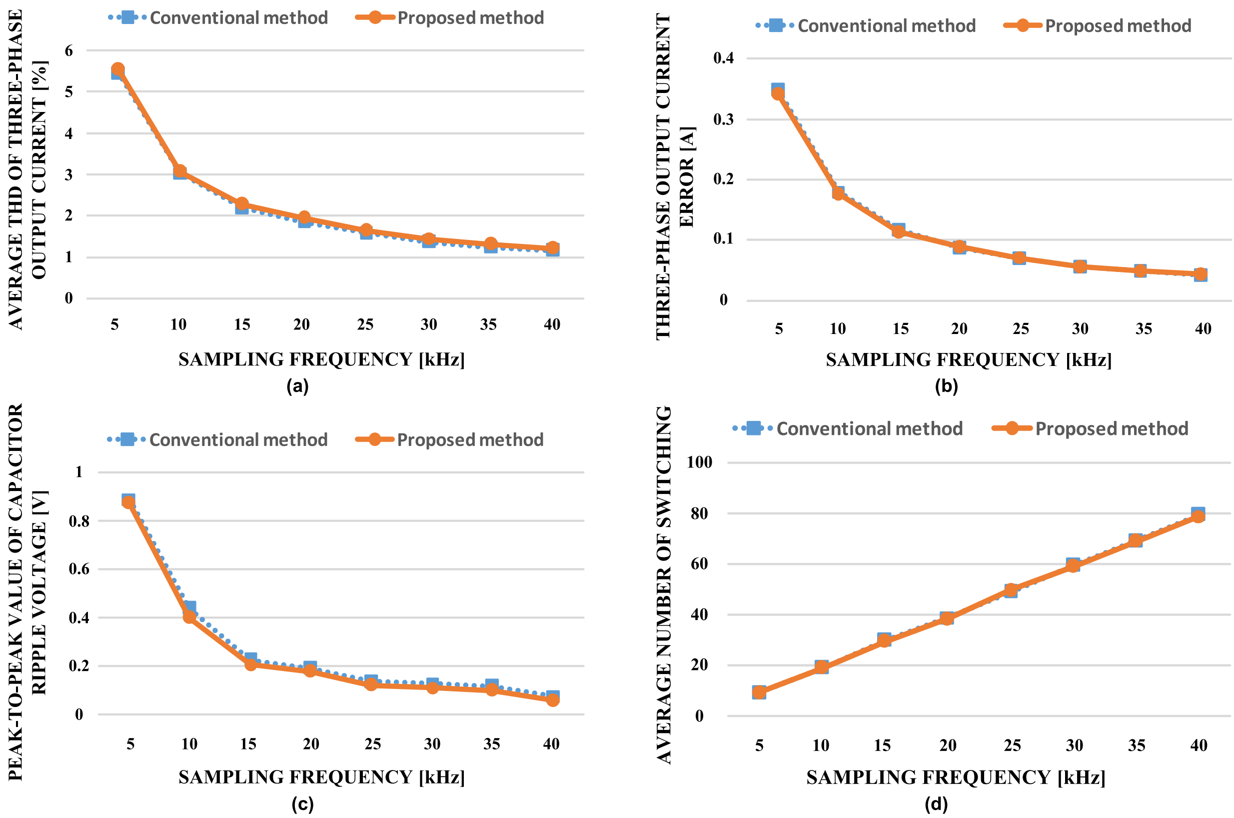

FIGURE 18. Comparison results between conventional method and proposed method vs. sapling frequency; (a) average THD of three-phase output current; (b) three-phase output current error; (c) peak-to-peak values of capacitor ripple voltages; (d) average number of switching.

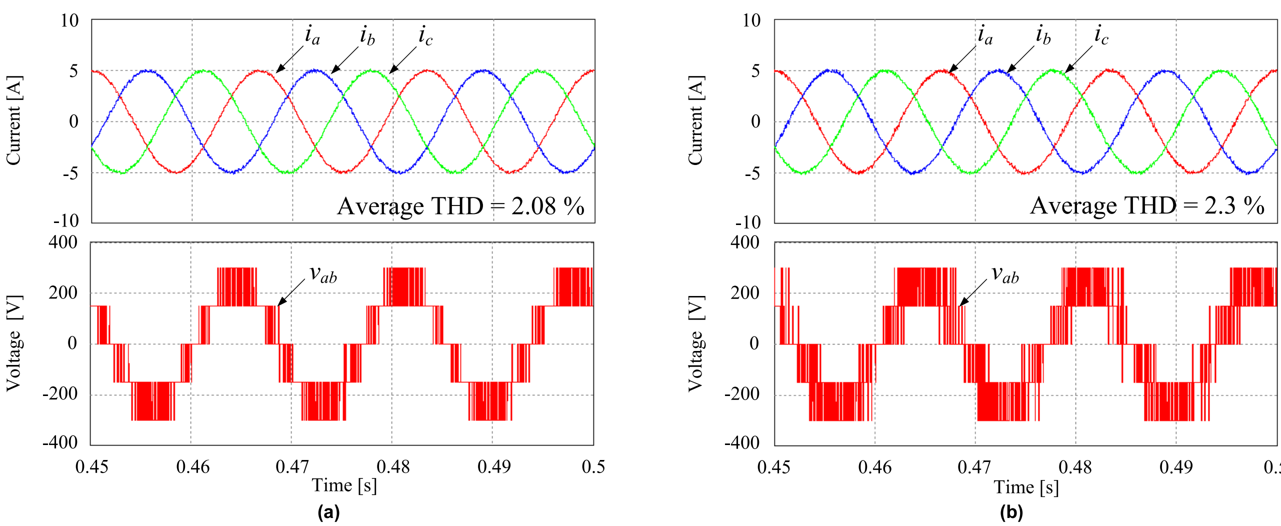

FIGURE 19. Simulation results of the output currents of each phase (i_a, i_b, i_c) and line-to-line voltage (v_{ab}) obtained by (a) conventional method and (b) proposed method.

(v_{c1}, v_{c2}) obtained by the proposed method and the control method in [35] with the phase difference 30° and 70° when the modulation index is 1. The average THD of the three-phase output current of the control method in [35] is slightly lower than that of the proposed method. However, peak-to-peak values of capacitor ripple voltages of the control method in [35] is higher than that of the proposed method as shown. Especially in the phase difference is 70°, the capacitor voltages in [35] significantly deteriorate. This is because of the limitation of the control method in [35] with a high modulation index and phase difference, as explained earlier.

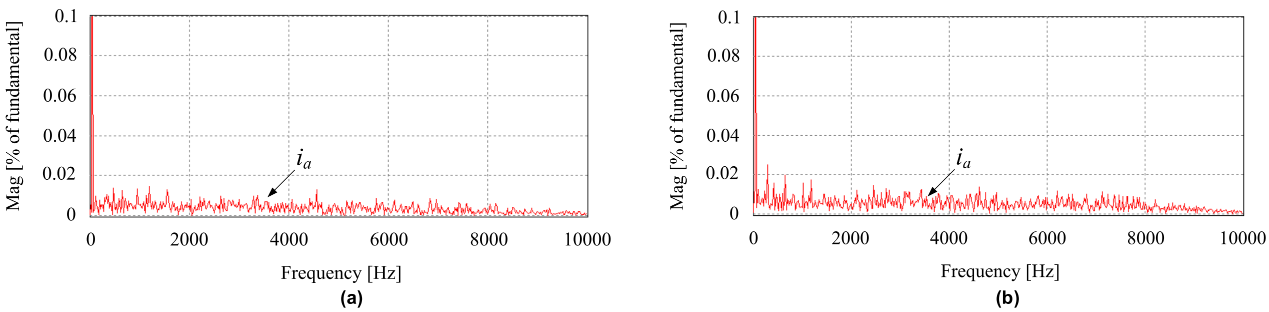

FIGURE 20. Simulation results of frequency spectrum of a-phase output current (i_a) obtained by (a) conventional method and (b) proposed method.

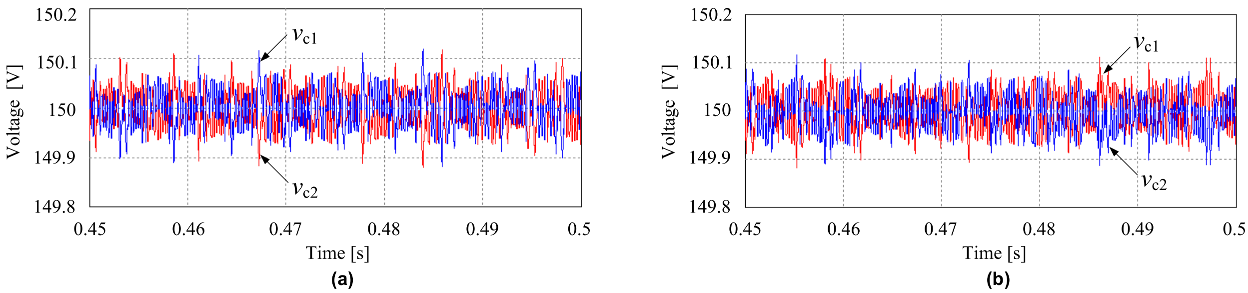

FIGURE 21. Simulation results of capacitor voltages (v_{c1}, v_{c2}) obtained by (a) conventional method and (b) proposed method.

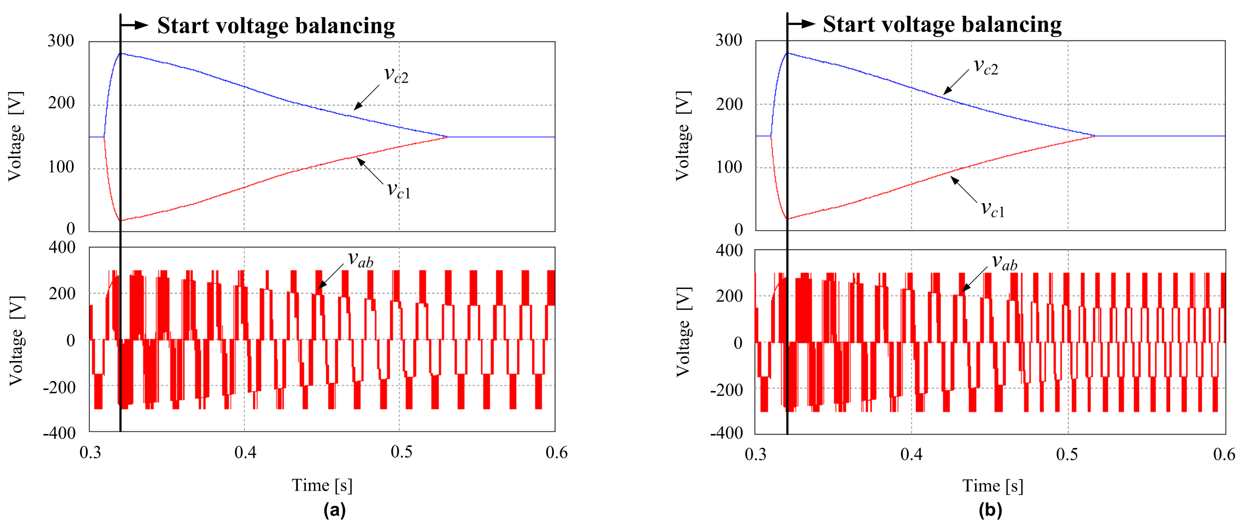

FIGURE 22. Simulation results of line-to-line voltage (v_{ab}) and capacitor voltages (v_{c1}, v_{c2}) balancing under voltage unbalance condition obtained by (a) conventional method and (b) proposed method.

Fig. 26 shows the capacitor voltage balancing under voltage unbalance condition obtain by the proposed method and the control method in [35] with the phase difference 30° and 70°. As shown in Fig. 26(a) and (b), both control methods can quickly balance the capacitor voltage, and the balancing speed of the proposed method is slightly faster than that of the control method in [35]. However, as in Fig. 26(c) and (d), the balancing speed of the control method in [35] is much lower than that of the proposed method. This is because the voltage unbalance region in Fig. 25(d) disturbs the capacitor voltage balancing.

Fig. 27 shows the dynamic response with step change of magnitude (from 3.5A to 5A) of the reference output currents with the phase difference 30° and 70°. As shown in Figure, both control methods have a fast transient response and no significant difference in speed. The only difference is the peak-to-peak values of capacitor voltage ripple voltages.

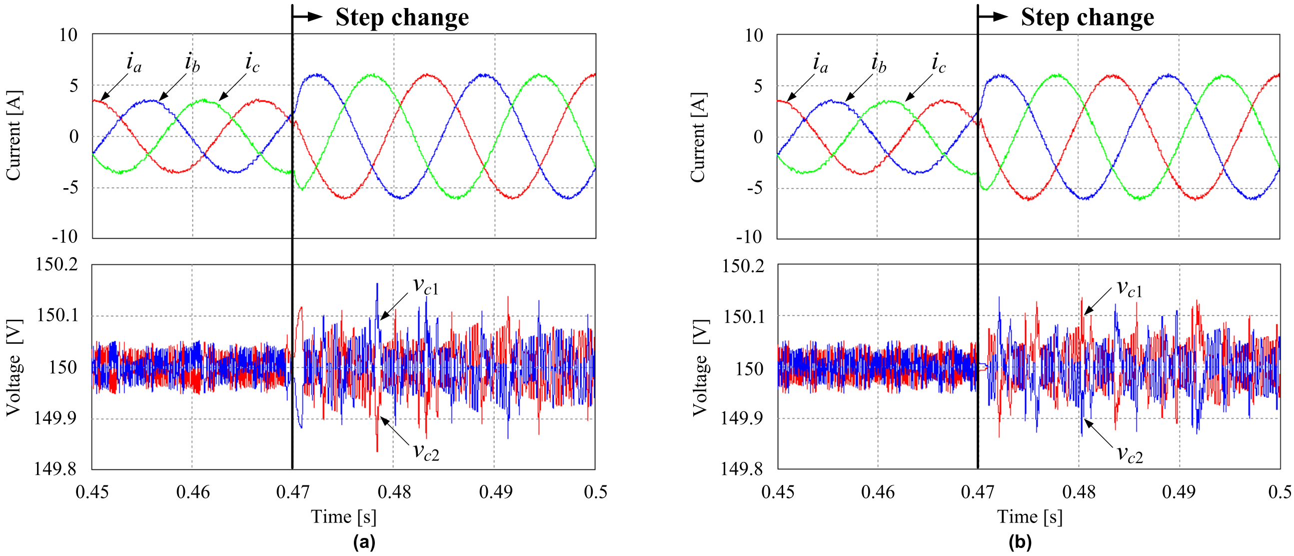

FIGURE 23. Simulation results of three-phase output currents (i_a, i_b, i_c) and capacitor voltages (v_{c1}, v_{c2}) with step change of peak value of the output reference currents (from 3.5 A to 6 A) obtained by (a) conventional method and (b) proposed method.

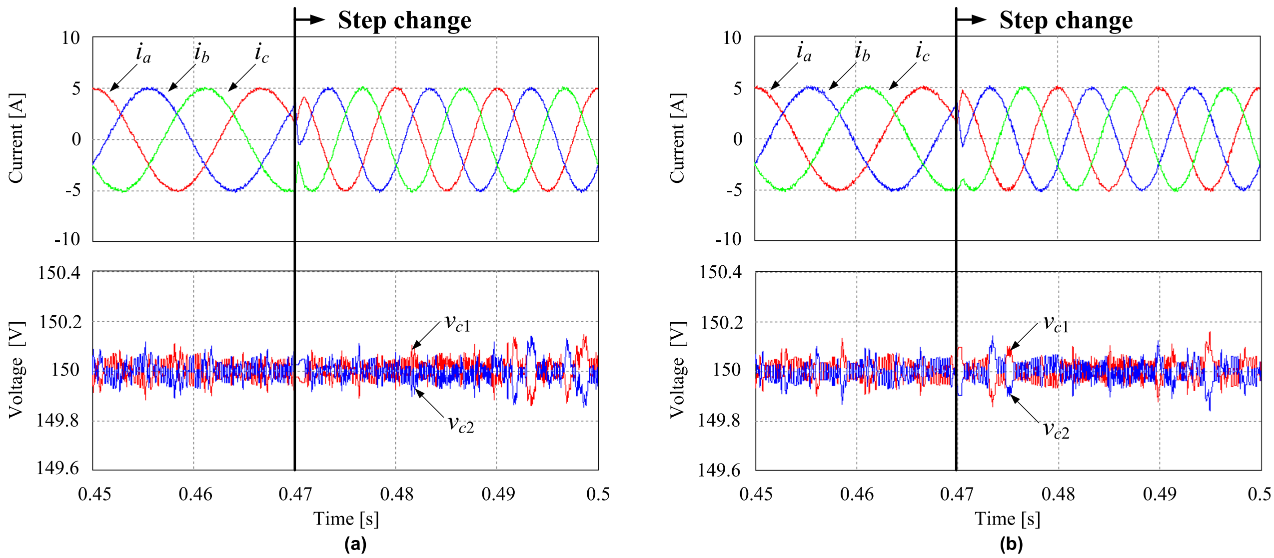

FIGURE 24. Simulation results of three-phase output currents (i_a, i_b, i_c) and capacitor voltages (v_{c1}, v_{c2}) with step change of fundamental frequency of the output reference currents (from 60 Hz to 100 Hz) obtained by (a) conventional method and (b) proposed method.

TABLE 7. Parameter values for simulation.

Parameters	Values
V_{dc} (input voltage)	300 [V]
$\lvert i^* \rvert$ (peak value of output reference current)	5 [A]
R_o (output resistance)	23 [Ω]
L_o (output inductance)	18.5 [mH]
T_s (sampling period)	66.67 [μs]
C (dc-capacitance)	2200 [μF]

B. EXPERIMENTAL RESULTS

Experiments were performed to verify the validity of the proposed method. Table 7 shows the parameter values used in the experiment. Unlike the simulation, the experiment was conducted without back-emf. The inverter was controlled using a DSP (Digital Signal Process) board (TMS320F28335). Fig. 28 shows the experimental set-up.

Fig. 29 shows the waveforms of the three-phase output current (i_a, i_b, i_c) and the line-to-line voltage (v_{ab}) obtained from the experiment. Fig. 29 (a) and (b) are the experimental results obtained by the conventional method and the proposed method, respectively. As shown in Fig. 25, the three-phase output current waveforms of the conventional control method and the proposed method are controlled with a sinusoidal waveform with a peak value of 5 A, and the line-to-line voltage is also five levels. In addition, similar to the simulation results in Fig. 19, average THD of the three-phase

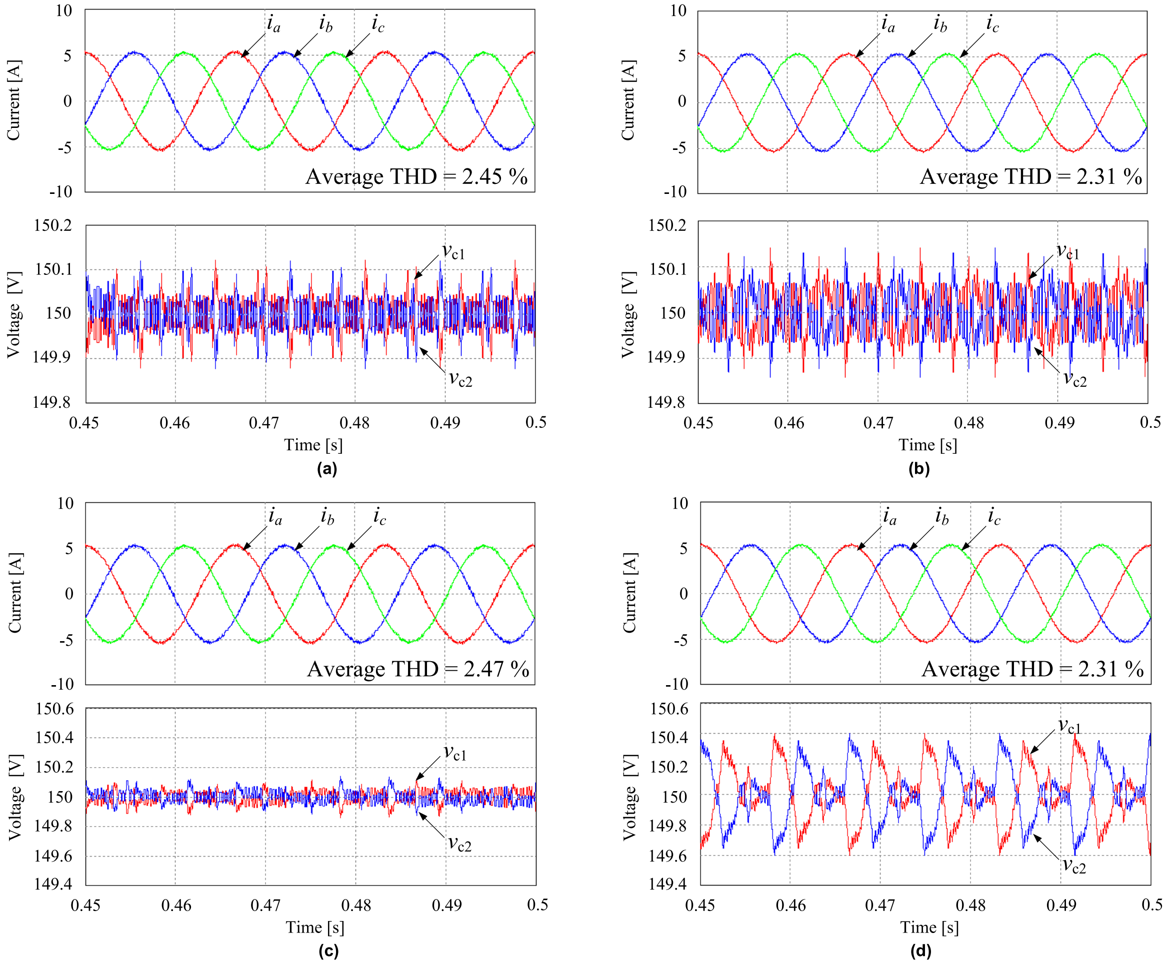

FIGURE 25. Simulation results of the three-phase output currents (i_a, i_b, i_c) and capacitor voltages (v_{c1}, v_{c2}) obtained by (a) proposed method and (b) control method in [35] with the phase difference 30° and modulation index 1, (c) proposed method and (d) control method in [35] with the phase difference 30° and modulation index 1.

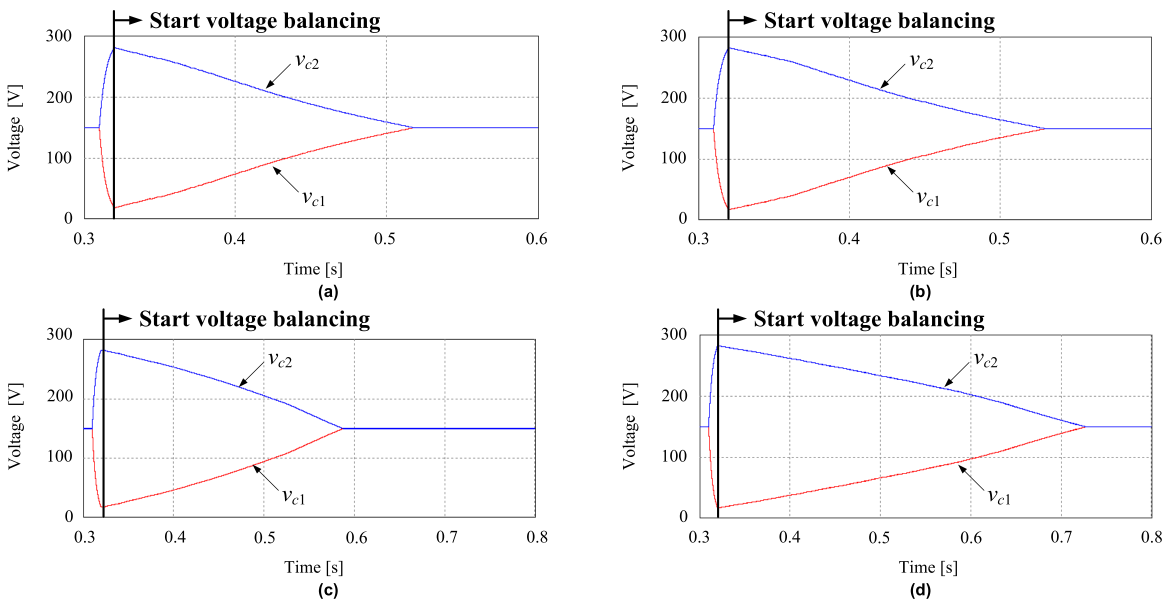

FIGURE 26. Simulation results of line-to-line voltage (v_{ab}) and capacitor voltages (v_{c1}, v_{c2}) balancing under voltage unbalance condition obtained by (a) proposed method and (b) control method in [35] with the phase difference 30°, (c) proposed method and (d) control method in [35] with the phase difference 70°.

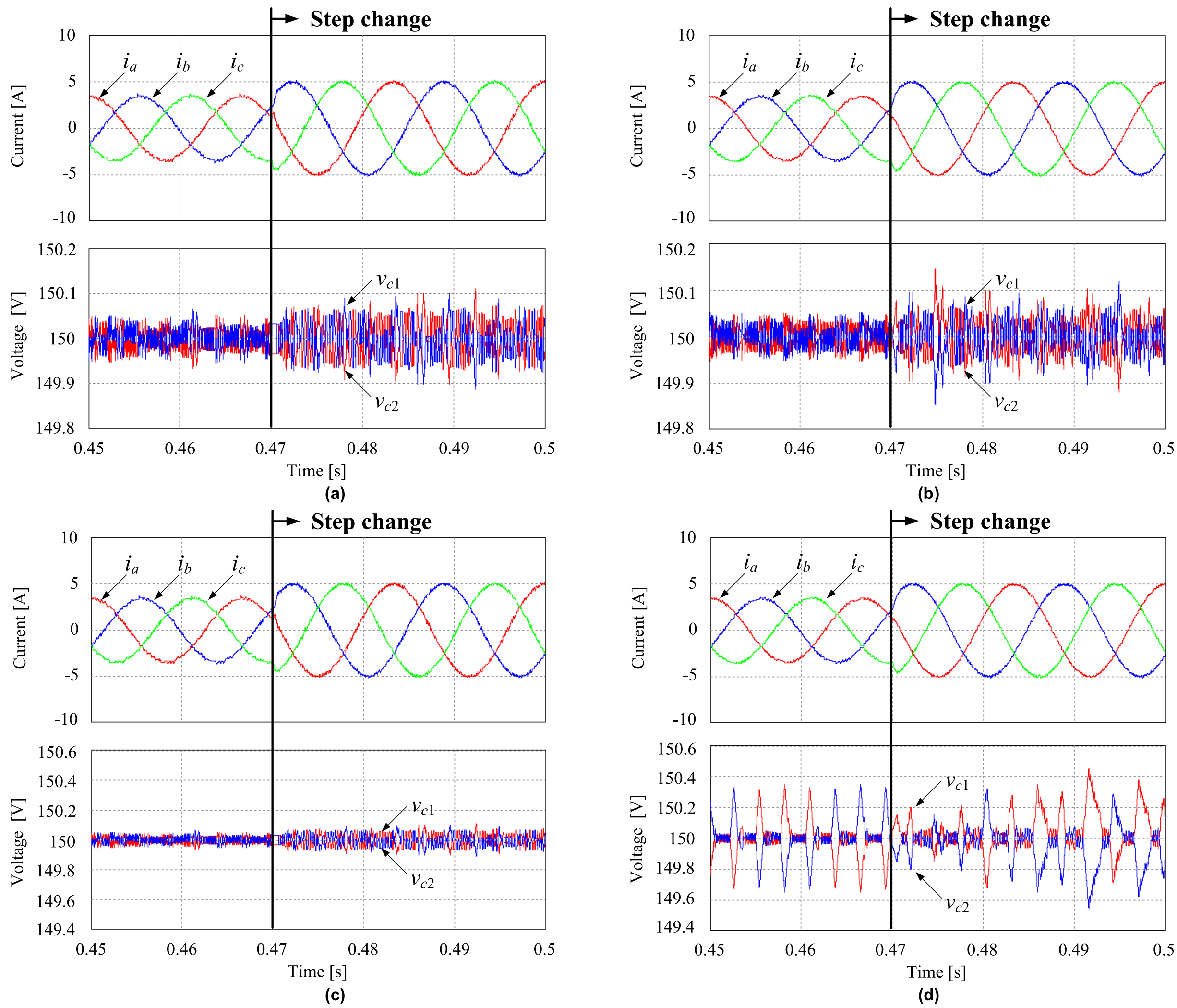

FIGURE 27. Simulation results of three-phase output currents (i_a, i_b, i_c) and capacitor voltages (v_{c1}, v_{c2}) with step change of peak value of the output reference currents (from 3.5 A to 5 A) obtained by (a) proposed method and (b) control method in [35] with the phase difference 30°, (c) proposed method and (d) control method in [35] with the phase difference 70°.

output current of the proposed method is slightly higher than that of the conventional method. This is because, like the reason described before, some switching state candidates of the proposed method are excluded so that there may be a situation where the optimal vector is not selected.

Fig. 30 shows the waveform and harmonic spectrum of the a-phase output current. As shown in the Figure, there is no significant difference in the frequency components.

Fig. 31 shows the waveforms of the upper and lower capacitor voltages (v_{c1}, v_{c2}). Fig. 31 (a) and (b) are waveforms obtained by the conventional method and the proposed method, respectively. As shown in Fig. 31, the upper and lower capacitor voltages are controlled to $V_{dc}/2$ in both the conventional control method and the proposed method and the ripple values are also similar.

Experiments were conducted to verify the capacitor voltage balance performance and transient response of the proposed method. Fig. 32 shows the experimental results of the capacitor voltages, which start voltage balancing at unbalanced conditions. To make the capacitor voltage imbalance condition, an electronic load was connected in parallel to the lower capacitor. The resistance of the load was set to 1 Ω. As shown in Fig. 32, the electronic load was activated to create a capacitor voltage imbalance, and the electronic load was disabled to eliminate the effect of the load. Both control methods quickly eliminate capacitor voltage imbalance, and the capacitor voltage is again balanced. There is also no significant difference in the rate at which the capacitor voltages are again balanced.

Two experiments were conducted to verify the transient response of the proposed method. Fig. 33 shows the transient response waveform with a step change of magnitude of three-phase reference currents from 3.5 A to 6 A. As shown in Figure, in both control method, the real output current quickly follows the reference current from 3.5 A to 6 A. Also, the peak-to-peak values of capacitor ripple voltages after the change in the magnitude of the reference output current

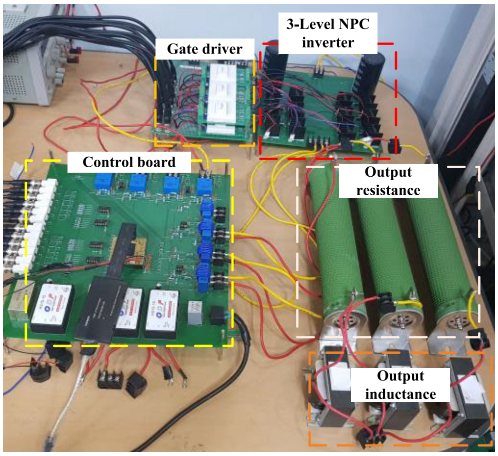

FIGURE 28. Prototype setup of three-phase three-level NPC inverter.

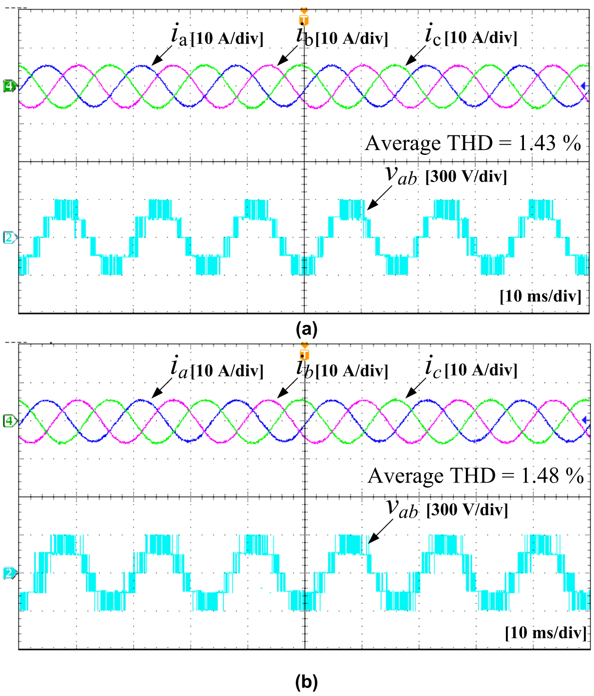

FIGURE 29. Experimental results of three-phase output currents (i_a, i_b, i_c), and line-to-line voltage (v_{ab}) obtained by (a) conventional method and (b) proposed method.

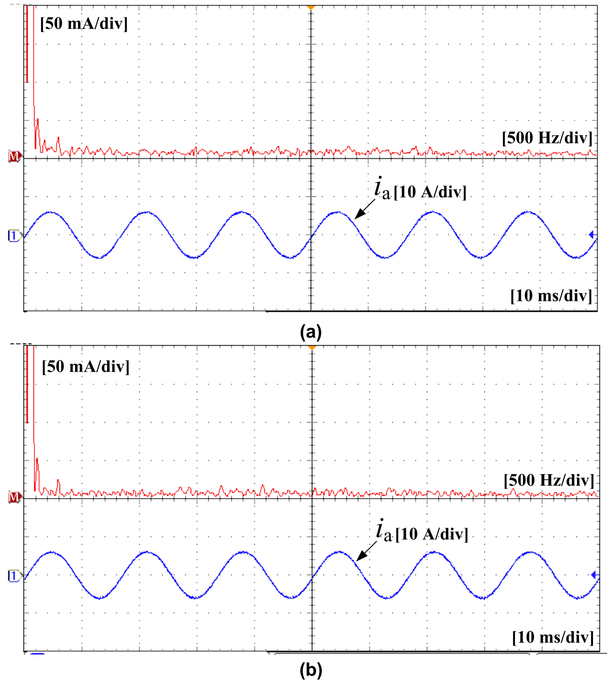

FIGURE 30. Experimental results of frequency spectrum of the output current of a-phase (i_a) obtained by (a) conventional method and (b) proposed method.

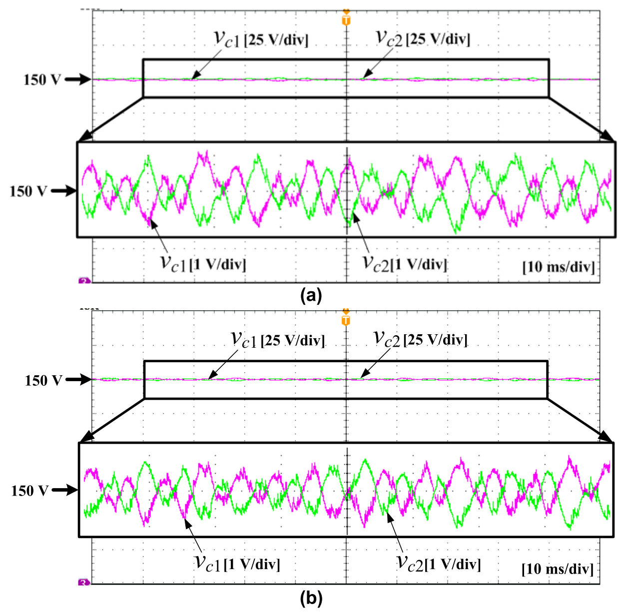

FIGURE 31. Experimental results of capacitor voltages (v_{c1}, v_{c2}) obtained by (a) conventional method and (b) proposed method.

is slightly higher than the peak-to-peak values of capacitor ripple voltages before the change.

Fig. 34 shows the transient response waveform with a step change of the fundamental frequency of three-phase reference currents from 60 Hz to 100 Hz. As shown in Figure, in both two control methods, the real output current quickly follows the reference current with the frequency from 60 Hz to 100 Hz.

The proposed method excludes switching state candidates when phase difference occurs between the reference voltage and output current, as shown in Table 5. Therefore, as the phase difference changes, so does the performance. Fig. 35 shows the three-phase output currents (i_a, i_b, i_c) and capacitor voltages (v_{c1}, v_{c2}) obtained by the proposed method with the phase difference with 30° and 70°, respectively. As shown in Figure, the average THD of three-phase output current and peak-to-peak values of capacitor ripple voltages of the phase difference with 30° and 70° are similar. This is because excluded switching state candidates are the same as

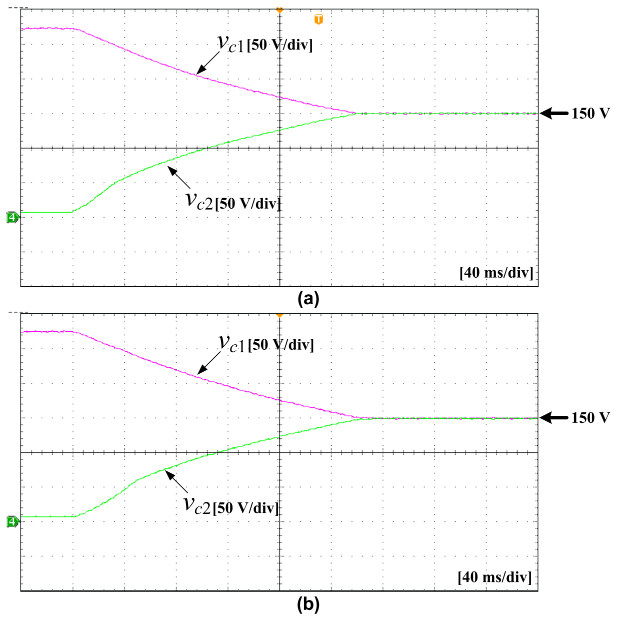

FIGURE 32. Experimental results of capacitor voltages (v_{c1}, v_{c2}) balancing under voltage unbalanced condition obtained by (a) conventional method and (b) proposed method.

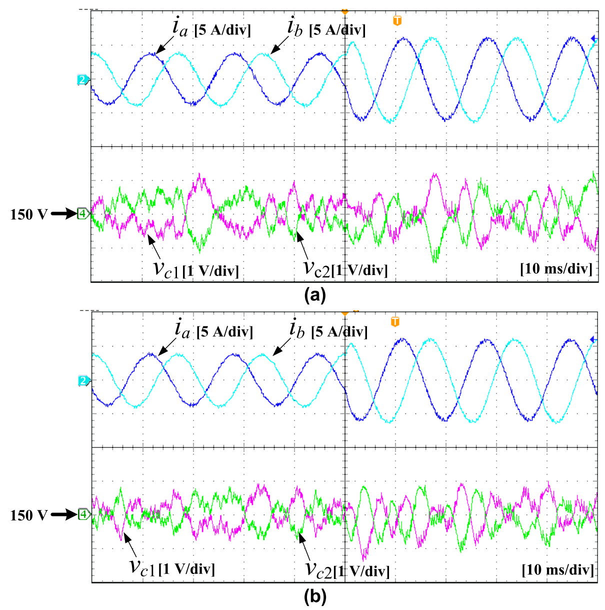

FIGURE 33. Experimental results of output currents (i_a, i_b) and capacitor voltages (v_{c1}, v_{c2}) with step change of peak value of the reference currents (from 3.5 A to 6 A) obtained by (a) conventional method and (b) proposed method.

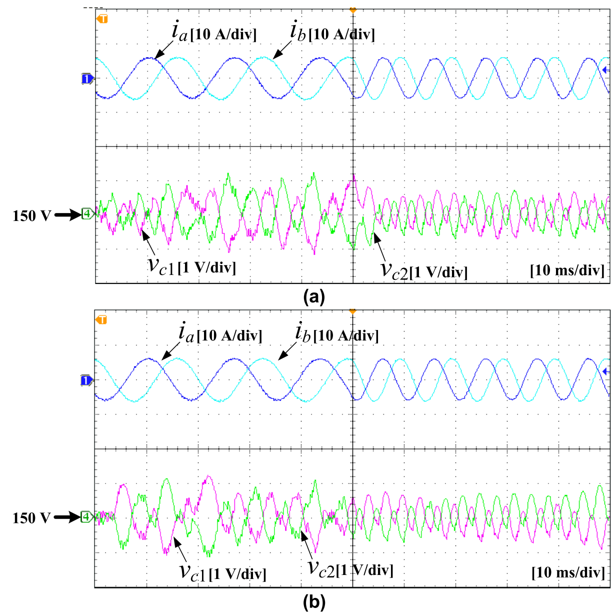

FIGURE 34. Experimental results of output currents (i_a, i_b) and capacitor voltages (v_{c1}, v_{c2}) with step change of fundamental frequency (from 60 Hz to 100 Hz) obtained by (a) conventional method and (b) proposed method.

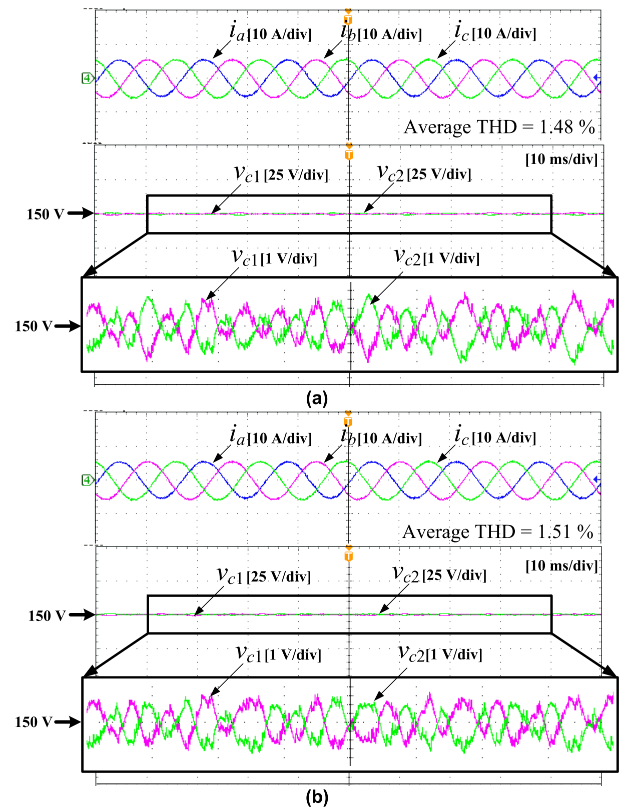

FIGURE 35. Experimental results of three-phase output currents (i_a, i_b, i_c), and upper and lower capacitor voltages (v_{c1} and v_{c2}) obtained by proposed method with the phase difference (a) 30° and (b) 70°.

shown in Table 5. Also when the phase difference is 70°, and the capacitor current direction is reversed, the switching state of a small vector is selected in reverse to control the capacitor voltages. As a result, in both phase difference 30° and 70°. The performance of the algorithm does not change.

Fig. 36 shows the experimental results of the capacitor voltages, which start voltage balancing at unbalanced conditions obtained by the proposed method with the phase difference (a) 30° and (b) 70°. As shown in Fig. 26, the speed of the capacitor voltage balance when the phase difference is 70° is the same as the speed of the capacitor voltage balance when

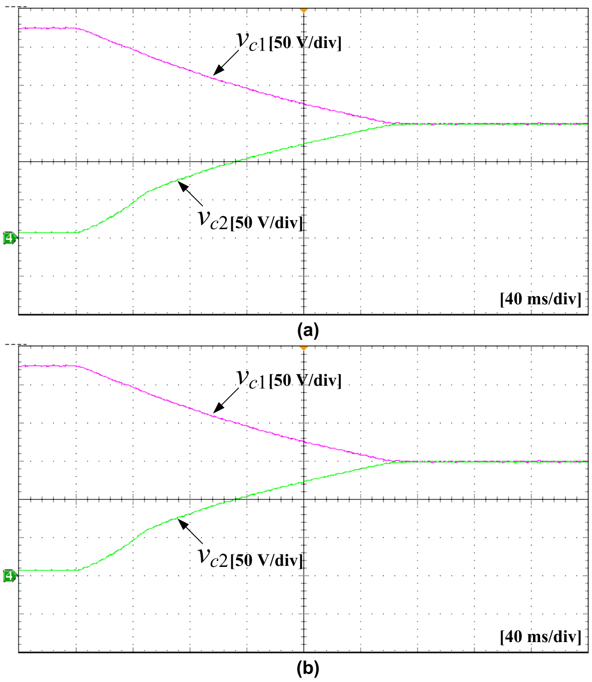

FIGURE 36. Experimental results of capacitor voltages (v_{c1}, v_{c2}) balancing under voltage unbalanced condition obtained by proposed method with the phase difference (a) 30° and (b) 70°.

TABLE 8. Calculation time of conventional and proposed method.

Parameters	Conventional method	Proposed method
Computational time [μs]	25.94	46.83

the phase difference is 30°. This is because the switching state selected is almost similar.

In terms of the computational time, Table 8 shows the calculation time of the conventional and proposed methods. The number of clocks of the conventional and proposed methods were measured in the DSP board in the experimental implementation, and they were converted to the required implementation time to perform the two control schemes. As can be seen from Table 8, the proposed approach requires higher calculation time than the conventional MPC method. This can be explained that the calculation for the offset voltage increases the computational burden. However, the proposed approach eliminates the time-consuming and tedious weighting factor tuning work and does not need to redesign the MPC control for every single change of the system.

VI. CONCLUSION

In this paper, a predictive control method for controlling the NP voltage balance of three-phase three-level NPC inverter by offset voltage injection was proposed. One of the most important control elements of the three-level NPC inverter is the NP voltage, and the NP voltage should always be balanced. The proposed method reduces the difference between the two DC capacitor voltages by injecting the offset voltage to the reference voltage. The offset voltage is determined by the difference between the upper and lower capacitor voltages. In addition, when the phase difference between the reference voltage and the output current occurs, the switching candidate is excluded to maintain the balance of the capacitor voltage. As a result, the proposed method can control not only the output currents but also the NP voltage balance. Simulations and experiments are performed to demonstrate the validity of the proposed method.

REFERENCES

[1] A. Steimel, "Electrical railway traction in Europe," *IEEE Ind. Appl. Mag.*, vol. 2, no. 6, pp. 6–17, Nov./Dec. 1996.

[2] R. J. Hill, "Electric railway traction—Part II. Traction drives with three-phase induction motors," *Power Eng. J.*, vol. 8, no. 3, pp. 143–152, Jun. 1994.

[3] A. D. Cheok, S. Kawamoto, T. Matsumoto, and H. Obi, "High power AC/DC converter and DC/AC inverter for high speed train applications," in *Proc. TENCON Conf.*, 2000, pp. 423–428.

[4] S. Kwak and J.-C. Park, "Predictive control method with future zero-sequence voltage to reduce switching losses in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1558–1566, Mar. 2015.

[5] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[6] S. Kwak, S.-E. Kim, and J.-C. Park, "Predictive current control methods with reduced current errors and ripples for single-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 11, no. 5, pp. 1006–1016, Oct. 2015.

[7] K. Tian, B. Wu, M. Narimani, D. D. Xu, Z. Cheng, and N. R. Zargari, "A capacitor voltage-balancing method for nested neutral point clamped (NNPC) inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2575–2583, Mar. 2016.

[8] B. Gutierrez and S. Kwak, "Model predictive control with preselection technique for reduced calculation burden in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9176–9187, Nov. 2018.

[9] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[10] M. R. Nasiri, S. Farhangi, and J. Rodríguez, "Model predictive control of a multilevel CHB STATCOM in wind farm application using diophantine equations," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1213–1223, Feb. 2019.

[11] A. Bahrami and M. Narimani, "A new five-level T-Type nested neutral point clamped (T-NNPC) converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10534–10545, Nov. 2019.

[12] G. Tan, Q. Deng, and Z. Liu, "An optimized SVPWM strategy for five-level active NPC (5L-ANPC) converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 386–395, Jan. 2014.

[13] J. Xu, C. Zhao, Y. Xiong, C. Li, Y. Ji, and T. An, "Optimal design of MMC levels for electromagnetic transient studies of MMC-HVDC," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1663–1672, Aug. 2016.

[14] Z. Wang, S. Fan, Y. Zheng, and M. Cheng, "Design and analysis of a CHB converter based PV-battery hybrid system for better electromagnetic compatibility," *IEEE Trans. Magn.*, vol. 48, no. 11, pp. 4530–4533, Nov. 2012.

[15] I. S. de Freitas, M. M. Bandeira, L. D. M. Barros, C. B. Jacobina, E. C. dos Santos, F. Salvadori, and S. A. da Silva, "A carrier-based PWM technique for capacitor voltage balancing of single-phase three-level neutral-point-clamped converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3227–3235, Jul./Aug. 2015.

[16] R. M. Tallam, R. Naik, and T. A. Nondahl, "A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1734–1743, Nov./Dec. 2005.

[17] U.-M. Choi, H.-H. Lee, and K.-B. Lee, "Simple neutral-point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. Energy Convers.*, vol. 28, no. 2, pp. 434–443, Jun. 2013.

[18] W. Song, S. Wang, X. Ge, C. Xiong, and X. Feng, "Single-phase three-level space vector pulse width modulation algorithm for grid-side railway traction converter and its relationship of carrier-based pulse width modulation," *IET Electr. Syst. Transp.*, vol. 4, no. 3, pp. 78–87, Sep. 2014.

[19] N.-Y. Dai, M.-C. Wong, and Y.-D. Han, "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 440–449, Mar. 2006.

[20] E.-S. Jun and S. Kwak, "A highly efficient single-phase three-level neutral point clamped (NPC) converter based on predictive control with reduced number of commutations," *Energies*, vol. 11, no. 12, p. 3524, Dec. 2018.

[21] M. Habibullah, D. D.-C. Lu, D. Xiao, and M. F. Rahman, "Finite-state predictive torque control of induction motor supplied from a three-level NPC voltage source inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 479–489, Jan. 2017.

[22] M. Habibullah, D. D.-C. Lu, D. Xiao, J. E. Fletcher, and M. F. Rahman, "Predictive torque control of induction motor sensorless drive fed by a 3L-NPC inverter," *IEEE Trans. Ind. Informat.*, vol. 13, no. 1, pp. 60–70, Feb. 2017.

[23] J.-H. Lee, J.-S. Lee, H.-C. Moon, and K.-B. Lee, "An improved finite-set model predictive control based on discrete space vector modulation methods for grid-connected three-level voltage source inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1744–1760, Dec. 2018.

[24] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Method to minimize the low-frequency neutral-point voltage oscillations with time-offset injection for neutral-point-clamped inverters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1678–1691, Mar./Apr. 2015.

[25] J.-S. Lee and K.-B. Lee, "Time-offset injection method for neutral-point AC ripple voltage reduction in a three-level inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1931–1941, Mar. 2016.

[26] J.-S. Lee, S. Yoo, and K.-B. Lee, "Novel discontinuous PWM method of a three-level inverter for neutral-point voltage ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3344–3354, Jun. 2016.

[27] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive Control of a Three-Phase neutral-point-clamped Inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2697–2704, Dec. 2007.

[28] J.-C. Kim, S.-K. Moon, and S. Kwak, "Direct model-based predictive control scheme without cost function for voltage source inverters with reduced common-mode voltage," *Int. J. Electron.*, vol. 105, no. 4, pp. 629–644, Sep. 2017.

[29] S. Kwak and S.-K. Mun, "Model predictive control methods to reduce common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5019–5035, Sep. 2015.

[30] X. Zhang and B. Hou, "Double vectors model predictive torque control without weighting factor based on voltage tracking error," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2368–2380, Mar. 2018.

[31] X. Wu, W. Song, and C. Xue, "Low-complexity model predictive torque control method without weighting factor for five-phase PMSM based on hysteresis comparators," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1650–1661, Dec. 2018.

[32] Y. Zhang and H. Yang, "Two-Vector-Based model predictive torque control without weighting factors for induction motor drives," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1381–1390, Feb. 2016.

[33] L. Guo, X. Zhang, S. Yang, Z. Xie, L. Wang, and R. Cao, "Simplified model predictive direct torque control method without weighting factors for permanent magnet synchronous generator-based wind power system," *IET Electr. Power Appl.*, vol. 11, no. 5, pp. 793–804, May 2017.

[34] X. Zhang and Y. He, "Direct voltage-selection based model predictive direct speed control for PMSM drives without weighting factor," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7838–7851, Aug. 2019.

[35] Y. Yang, H. Wen, M. Fan, M. Xie, and R. Chen, "Fast finite-switching-state model predictive control method without weighting factors for T-type three-level three-phase inverters," *IEEE Trans. Ind. Informat.*, vol. 15, no. 3, pp. 1298–1310, Mar. 2019.

[36] W. Wu, D. Wang, and L. Liu, "A multi-layer sequential model predictive control of three-phase two-leg seven-level T-type nested neutral point clamped converter without weighting factors," *IEEE Access*, vol. 7, pp. 162735–162746, Nov. 2019.

[37] E.-S. Jun, M. H. Nguyen, and S. Kwak, "Three-phase three-level neutral point clamped rectifier with predictive control method without employing weighting factor," *Appl. Sci.*, vol. 10, no. 15, p. 5149, Jul. 2020.

[38] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083–1095, Mar. 2013.

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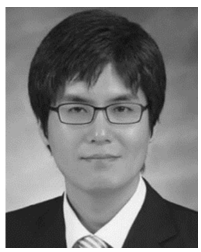

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