applied sciences

MDPI

Article

Three-Phase Three-Level Neutral Point Clamped Rectifier with Predictive Control Method without Employing Weighting Factor

Eun-Su Jun, Minh Hoang Nguyen and Sangshin Kwak *

School of Electrical and Electronics Engineering, Chung-ang University, Seoul 06974, Korea; elizame3@naver.com (E.-S.J.); nguyenminhhoanghp93@gmail.com (M.H.N.)

* Correspondence: sskwak@cau.ac.kr

Received: 22 June 2020; Accepted: 23 July 2020; Published: 27 July 2020

Abstract: A predictive control method using injected offset voltage to achieve neutral point (NP) voltage balance of three-phase three-level neutral point clamped (NP) rectifiers, without employing a weighting factor, is proposed in this study. One of the biggest problems with the three-level NP rectifiers is the dc link capacitor voltage imbalance. Therefore, it is necessary to maintain the balance of the NP voltage in addition to synthesize the three-phase sinusoidal input current by control methods. Conventional predictive control methods for the NP rectifiers have used a weighting factor in a cost function that determines the control ratio of the input currents and the capacitor voltage balance. As a result, it is burdensome to empirically redesign the weighting factor when the rectifiers' parameter values and control conditions change. Unlike the conventional methods, the proposed approach without the weighting factor can significantly eliminate differences between two DC capacitor voltages by utilizing an offset voltage, which is generated by using the difference between the upper and lower capacitor voltages. Consequently, the proposed approach using the offset voltage injection can control the input currents and retain the balance of NP voltage. Simulation and experiments are presented to verify the correctness of the NP voltage balancing of the proposed control method.

Keywords: neutral point clamped rectifier; predictive control method; offset voltage injection

1. Introduction

A recent increase in applications of high voltage systems and equipment in industrial fields has revealed limitations of two-level rectifiers [1–4]. To resolve the drawbacks of the two-level rectifiers, many multi-level rectifiers have been studied to increase the voltage levels of rectifiers as compared to the two-level rectifiers because of the increased number of switches existing in each phase [5–11]. This circuit structural feature allows multiple switches to distribute stresses. In addition, due to the increased levels, input current waveforms have a lower total harmonic distortion (THD) than the two-level rectifiers, yielding improved current characteristics without increasing the filter size. Furthermore, the reduced THD eliminates the need for higher switching frequencies, which can increase efficiency more than the two-level rectifiers. Three-phase three-level neutral point clamped (NP) rectifiers have four switches and two clamping diodes per phase, and two additional DC capacitors, in which capacitor voltages should be balanced and three-phase input currents should be synthesized in a sinusoidal form [12–14]. The unbalance of capacitor voltages not only reduces control performance, but also increases stresses on the switches, which can increase the probability of the rectifier failing. Therefore, various control methods for controlling both the input current and the capacitor voltage of the three-phase three-level NP rectifiers have been studied [15–19]. Predictive control methods, which

select an optimal switching state minimizing a cost function to satisfy rectifier performance, have also been investigated to control the NP rectifier [20–23]. So as to simultaneously fulfil the sinusoidal input current generation and the NP voltage balancing, a cost function for the NP rectifiers consists of two terms for the input current and the capacitor voltage, which are adjusted by a weighting factor that determines a control ratio between two terms. It is burdensome to empirically redesign the weighting factor in cases that parameters or control conditions change. Thus, this paper addresses a predictive control method which can eliminate this hassle.

In this paper, a predictive control method with offset voltage injection for achieving neutral point (NP) voltage balance of three-phase three-level neutral point clamped (NP) rectifiers is proposed. The proposed algorithm does not use a weighting factor as the cost function of the conventional approach. Instead, the proposed method individually develops an offset voltage which is decided by the difference between the upper capacitor voltage and lower capacitor voltage, in addition to produce a reference voltage which is used to control the three-phase sinusoidal input currents. Then, the offset voltage, which is injected to the reference voltage in the proposed scheme, can successfully reduce the difference between the two capacitor voltages. Consequently, the proposed algorithm using the offset voltage injection can control the input currents and retain the balance of the NP voltage. Validity of the proposed method is verified through simulations and experiments.

2. Conventional Predictive Control Method

Figure 1 shows a three-phase three-level NP rectifier. The ac input side of the circuit structure in Figure 1 gives an equation as

$$v_{sx} = R_i i_x + L_i \frac{di_x}{dt} + v_x (x = a,\ b,\ c) \tag{1}$$

where v_{sx}, i_x, R_i, L_i and v_x represent the source voltage, the input current, the input resistance, the input inductance, and the phase voltage of the rectifier, respectively. Using a constant sampling period T_s and Euler's formula, the Equation (1) is described in the discrete time domain as

$$v_{sx}(k) = R_i i_x(k) + L_i \frac{i_x(k+1) - i_x(k)}{T_s} + v_x(k).\ (x = a,\ b,\ c) \tag{2}$$

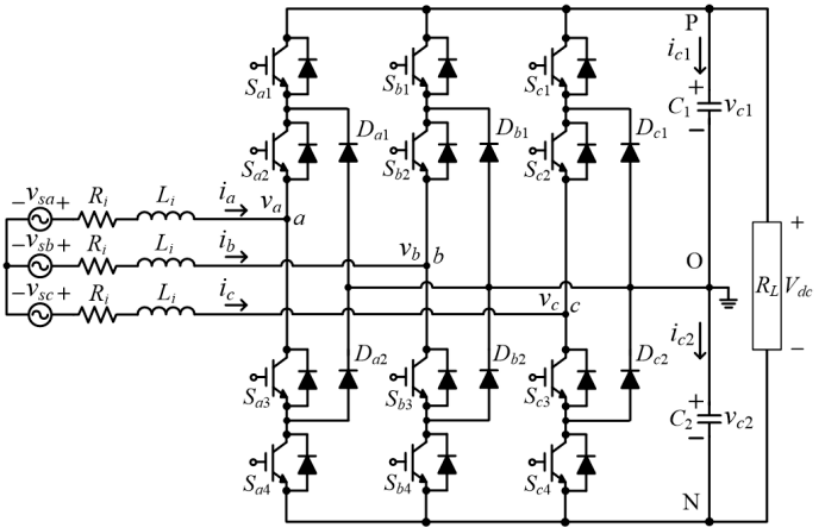

Figure 1. Three-phase three-level NP rectifier.

By rearranging (2), one can obtain

$$i_x(k+1) = \left(1 - \frac{R_i T_s}{L_i}\right) i_x(k) + \frac{T_s}{L_i}(v_{sx}(k) - v_x(k)).(x = a,\ b,\ c) \tag{3}$$

where v_x which is the rectifier pole voltage with respect to the node O in Figure 1, can be determined based on the switching states as presented in Table 1.

Table 1. States and pole voltage of NP rectifier depending on switch status.

Switching State	Switching Status (x = a,b,c)				Pole Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_x
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

The predictive control technique evaluates all switching state combinations to select an optimal switching state. Therefore, computational time included in the evaluation algorithm is compensated in the delay compensation techniques, in which the future current at the (k + 2)th step is used for the predictive control method [24,25]. The future current at the (k + 2)th step is acquired through shifting the model of (3) for one step forward as

$$i_x(k+2) = \left(1 - \frac{R_i T_s}{L_i}\right) i_x(k+1) + \frac{T_s}{L_i}(v_{sx}(k+1) - v_x(k+1)).\ (x = a,\ b,\ c) \tag{4}$$

A switching function according to switching operation of each phase in the rectifier can be defined as

$$S_x = \begin{cases} S_x = 1 & (S_{x1}, S_{x2}:\ ON) \\ S_x = 0 & (S_{x2}, S_{x3}:\ ON) \\ S_x = -1 & (S_{x3}, S_{x4}:\ ON) \end{cases} .\ (x = a,\ b,\ c) \tag{5}$$

where S_{ax}, S_{bx}, and S_{cx} $(x = 1,\ 2,\ 3,\ 4)$ refer to switching states of the four switches located on the a, b and c phase. The rectifier switching states and the input currents can be used to describe the currents flowing through the upper and lower capacitors as shown in (6) and (7).

$$i_{c1} = \frac{S_a(S_a+1)}{2} i_a + \frac{S_b(S_b+1)}{2} i_b + \frac{S_c(S_c+1)}{2} i_c. \tag{6}$$

$$i_{c2} = -\frac{S_a(S_a-1)}{2} i_a - \frac{S_b(S_b-1)}{2} i_b - \frac{S_c(S_c-1)}{2} i_c. \tag{7}$$

where i_{c1}, and i_{c2} represent the currents flowing through the upper and lower capacitors, respectively. In addition, the upper capacitor voltage and the lower capacitor voltage can be expressed as

$$\frac{dv_{ci}}{dt} = \frac{1}{C} i_{ci}\ (i = 1,\ 2) \tag{8}$$

where C is the capacitance of the upper capacitor and lower capacitor. v_{c1} and v_{c2} represent the voltage of the upper and lower capacitors, respectively. With a sampling period T_s, the variation of the capacitor voltage is expressed in the discrete time domain as follows.

$$\frac{dv_{ci}}{dt} \approx \frac{v_{ci}(k+1) - v_{ci}(k)}{T_s}.\ (i = 1,\ 2) \tag{9}$$

Using (9), (8) can be expressed as follows, and the capacitor voltage of the next step can be estimated as

$$v_{ci}(k+1) = v_{ci}(k) + \frac{T_s}{C} i_{ci}(k). \ (i = 1,\ 2) \tag{10}$$

To apply the delay compensation technique, the future capacitor voltage at the (k + 2)th step is acquired through shifting (10) for one step forward as

$$v_{ci}(k+2) = v_{ci}(k+1) + \frac{T_s}{C} i_{ci}(k+1). \ (i = 1,\ 2) \tag{11}$$

The cost function of the conventional predictive method is as follows.

$$\begin{aligned} g = \left|i_a^*(k+2) - i_a(k+2)\right| + \left|i_b^*(k+2) - i_b(k+2)\right| + \left|i_c^*(k+2) - i_c(k+2)\right| \\ + \lambda_c \left|v_{c1}(k+2) - v_{c2}(k+2)\right|. \end{aligned} \tag{12}$$

where i_a^*, i_b^* and i_c^* represent the reference input currents for the a, b and c phase, respectively. Moreover, λ_c is a weighting factor that defines the control proportion of the input currents and the capacitor voltages. The reference input currents can be obtained from Lagrange extrapolation using previous reference input currents as follows [26]

$$i_{abc}^*(k+2) = 3i_{abc}^*(k+1) - 3i_{abc}^*(k) + i_{abc}^*(k-1). \tag{13}$$

3. Proposed Predictive Control Method for NP Voltage Balance by Offset Voltage

Equations (14) and (15) describe the capacitor voltage variations, following (6), (7) and (10), as

$$\Delta v_{c1} = \frac{T_s}{C} i_{c1} = \frac{T_s}{C}\left(\frac{S_a(S_a+1)}{2} i_a + \frac{S_b(S_b+1)}{2} i_b + \frac{S_c(S_c+1)}{2} i_c\right). \tag{14}$$

$$\Delta v_{c2} = \frac{T_s}{C} i_{c2} = \frac{T_s}{C}\left(-\frac{S_a(S_a-1)}{2} i_a - \frac{S_b(S_b-1)}{2} i_b - \frac{S_c(S_c-1)}{2} i_c\right). \tag{15}$$

A difference between the upper and lower capacitor voltages is defined as

$$v_{diff} = v_{c1} - v_{c2}. \tag{16}$$

The difference between the variation of upper and lower capacitor voltages can be also defined as

$$\Delta v_{diff} = \Delta v_{c1} - \Delta v_{c2} = \frac{T_s}{C}\left(S_a^2 i_a + S_b^2 i_b + S_c^2 i_c\right). \tag{17}$$

According to Lyapunov stability, the condition for system stability is as [27]

$$\frac{dV}{dt} \le 0.\ V \ge 0 \tag{18}$$

where $V = v_{diff}^2$. From (18), the difference between the upper capacitor voltage and the lower capacitor voltage should satisfy the following, in order to maintain capacitor voltage balance:

$$2v_{diff}\frac{dv_{diff}}{dt} \le 0 \tag{19}$$

In the discrete-time domain, (19) can be presented as follows.

$$v_{diff}(k)\frac{\Delta v_{diff}(k)}{T_s} \le 0 \tag{20}$$

Using (17), (20) can be written by the difference of the two capacitor voltage variations v_{diff} and a function related with the input currents and the switching functions of the rectifier M, as

$$\frac{v_{diff}}{C}M \leq 0 \tag{21}$$

where $M = S_a^2 i_a + S_b^2 i_b + S_c^2 i_c$. Therefore, it can be seen from (21) that the capacitor voltage balance can be maintained by adjusting the rectifier switching states, S_a, S_b, and S_c, by considering the three-phase input currents and the difference of the two capacitor voltage variations. In order to control the rectifier based on the reference voltage in the proposed method, the Equation (2) can be expressed as follows using the reference currents.

$$v_x^*(k) = v_{sx}(k) - R_i i_x(k) - L_i \frac{i_x^*(k+1) - i_x(k)}{T_s}. \ (x = a,\ b,\ c) \tag{22}$$

where v_x^* is the reference voltage for each phase. To apply the delay compensation technique, the future reference voltage at the (k + 2)th step can be obtained by shifting (22) by one step forward as

$$v_x^*(k+1) = v_{sx}(k+1) - R_i i_x(k+1) - L_i \frac{i_x^*(k+2) - i_x(k+1)}{T_s}. \ (x = a,\ b,\ c) \tag{23}$$

Switching state selections according to positions of the reference voltage is decided as

$$S_x = \begin{cases} 1 \text{ (P state)} & \text{if } \frac{V_{dc}}{4} \leq v_x^* \leq \frac{V_{dc}}{2} \\ 0 \text{ (O state)} & \text{if } -\frac{V_{dc}}{4} < v_x^* < \frac{V_{dc}}{4} \\ -1 \text{ (N state)} & \text{if } -\frac{V_{dc}}{2} \leq v_x^* \leq -\frac{V_{dc}}{4} \end{cases} \quad (x = a,\ b,\ c). \tag{24}$$

Figure 2 shows sectors, input current polarity, switching states and maximum and minimum reference voltages of the three-phase NP rectifiers operating with unity power factor, where v_{max}^* and v_{min}^* represent the maximum and minimum values of three-phase reference voltages, respectively. As shown in Figure 2, the voltages, v_{max}^* and v_{min}^*, change every 120°. Furthermore, the rectifier changes the switching state every 60° on the basis of the position of the reference voltages and (24). It can be known that the rectifier selects six switching states as shown in Figure 2, PNO, PON, OPN, NPO, NOP and ONP, according to (24). In addition to the reference voltage v_x^* for the reference current tracking in (22), a new reference voltage proposed in this paper is defined with an offset voltage injection as

$$v_{x.ref} = v_x^* + v_{offset} (x = a,\ b,\ c) \tag{25}$$

where $v_{x,ref}$ and v_{offset} are a new reference voltage proposed in this paper and an offset voltage to be injected to maintain the capacitor voltage balance, respectively. The range of the offset voltage is, because the new reference voltage $v_{x,ref}$ with the offset voltage injection must be lower than $\frac{V_{dc}}{2}$ and higher than $-\frac{V_{dc}}{2}$, as

$$-\frac{V_{dc}}{2} - v_x^* \leq v_{offset} \leq \frac{V_{dc}}{2} - v_x^*. \ (x = a,\ b,\ c) \tag{26}$$

The maximum and minimum values of the offset voltage are defined as

$$-\frac{V_{dc}}{2} - v_{min}^* \leq v_{offset} \leq \frac{V_{dc}}{2} - v_{max}^*. \tag{27}$$

In cases where the positive offset voltage is injected, the magnitude of the reference voltage increases. For instance, if an initial switching state is N, a new state O can be selected after the positive offset voltage is injected. However, a state P cannot be selected after the offset voltage is injected, because the maximum offset voltage is limited as (27). Similarly, when the injected offset voltage is lower than zero, the reference voltage reduces. For instance, if a switching state before the negative offset voltage injection is P, the negative offset voltage injection enables a new state O to be selected after the injection. In addition, a switching state O without the negative offset voltage injection can change into a new state N after the offset voltage injection.

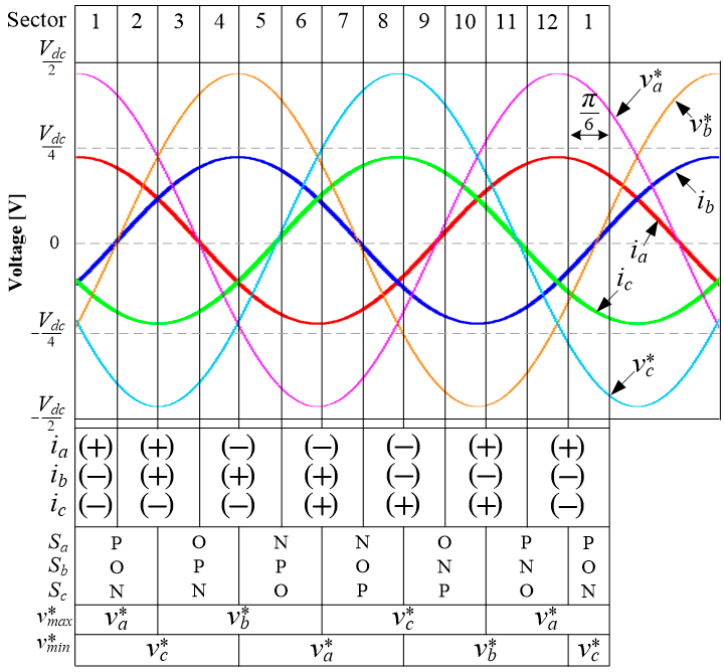

Figure 2. Sectors, input current polarity, switching states, maximum and minimum reference voltages of the rectifier with unity power factor.

Table 2 shows the switching states that can be selected after injecting a positive or negative offset voltage, when the rectifier operates at the sector 1 in Figure 2. As shown in Figure 2, the switching state in the sector 1, before the offset voltage is injected, is (PON). After the positive offset voltage is injected to the state (PON) in the sector 1, the two states, (POO) and (PON), can be possible because of the boundary conditions of the offset voltage in (27) and the locations of the reference voltages in Figure 2. Likewise, the negative offset voltage injection in the sector 1 can result in the two states, (OON) and (PNN), from (27) and Figure 2.

Table 2. States after the offset voltage is injected, the sign of the injected offset voltage, and the sign of input currents in a case of sector 1.

v_{offset}	S_a	i_a	S_b	i_b	S_c	i_c
+	P	+	O	−	O	−
	P		O		N	
−	O		N		N	
	P		N		N	

In cases where the positive offset voltage is injected into the reference voltage v_x^* in the sector 1, new switching states can be (POO) and (PON) as shown in Table 2. The function M in (21) for the switching states (PPO) and (PON), by considering the polarity of the input currents in the sector 1, are given by (28) and (29), respectively.

$$S_a^2 i_a + S_b^2 i_b + S_c^2 i_c = i_a + i_b > 0 \tag{28}$$

$$S_a^2 i_a + S_b^2 i_b + S_c^2 i_c = i_a + i_c > 0 \tag{29}$$

Therefore, when $v_{diff} < 0$, meaning $v_{c1} < v_{c2}$, injecting the offset voltage higher than zero satisfies (21). Figure 3a,b show the capacitor current flow when the switching states are (POO) and (PON). In Figure 3a, the current flows only to the upper capacitor. Thus, the associated capacitor is charged. As shown in Figure 3b with $i_a = i_b + i_c$, the upper capacitor charges. Thus, the new switching states after injecting the positive offset voltage in the sector 1, when the voltage difference v_{diff} is lower than zero, can reduce the voltage difference by increasing the upper capacitor voltage, which can maintain the capacitor voltage balance.

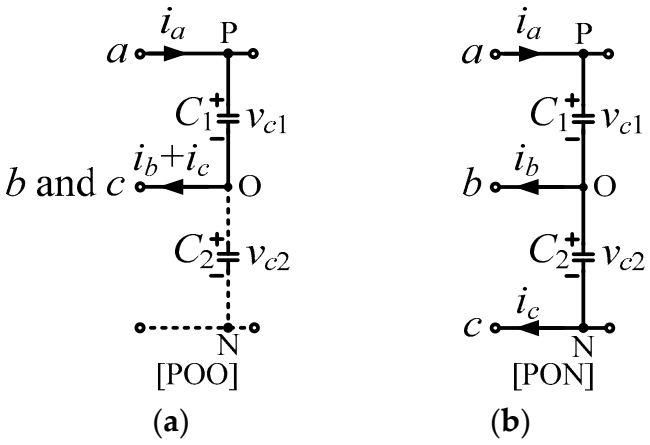

Figure 3. Capacitor current flow of sector 1 with switching status: (**a**) (POO); (**b**) (PON).

On the other hand, injecting the negative voltage v_{offset} into the reference voltage v_x^* in the sector 1 can generate new switching states (ONN) and (PNN) as shown in Table 2. The function M for the switching states (ONN) and (PNN) by considering the polarity of the input currents in the sector 1 are (30) and (31), respectively.

$$S_a^2 i_a + S_b^2 i_b + S_c^2 i_c = i_b + i_c < 0 \tag{30}$$

$$S_a^2 i_a + S_b^2 i_b + S_c^2 i_c = i_a + i_b + i_c = 0 \tag{31}$$

Therefore, if the negative offset voltage is injected when the voltage difference $v_{diff} > 0$, meaning $v_{c1} > v_{c2}$, the new switching states generated after the offset voltage injection satisfies (21). Figure 4a,b show the capacitor current path with the switching states (ONN) and (PNN), respectively. As shown in Figure 4a, the lower capacitor is charged by the current flowing and the voltage v_{c2} is increased. As a result, the voltage difference v_{diff}, which was greater than zero, can be reduced, leading to the capacitor voltage balancing. Figure 4b shows the switching state (PNN), and the capacitor voltage does not change because no current flows through the neutral point, which gives no harmful effects on the capacitor voltage balancing.

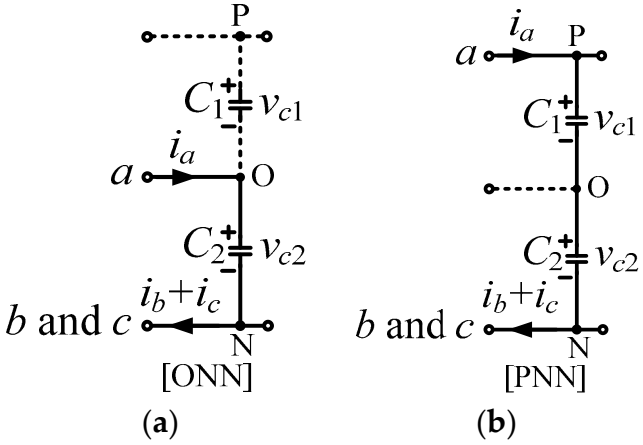

Figure 4. Capacitor current flow of sector 1 with switching status: (**a**) (ONN); (**b**) (PNN).

Based on the same approach used in sector 1, relationships between the capacitor voltage difference and the sign of the offset voltage can be established in the other sectors from 2 to 12 in Figure 2. The sign of the offset voltage to retain the balance of the capacitor voltage can be defined, with the opposite sign of the capacitor voltage difference. Using (27) and sign information of the offset voltage, the offset voltage injected to the reference voltage is determined by the reference voltage and the dc-link voltage dependent on the capacitor voltages. Finally, the cost function of the proposed approach, which does not include the weighting factor to adjust the input current generation and the capacitor voltage balancing, is given by

$$g = \left|v_{a,ref}(k+1) - v_a(k+1)\right| + \left|v_{b,ref}(k+1) - v_b(k+1)\right| + \left|v_{c,ref}(k+1) - v_c(k+1)\right|. \quad (32)$$

4. Simulation and Experiment Results

In order to verify validity of the proposed predictive control method, simulation and experimental results using the three-phase three-level NP rectifier are presented. In the simulations and experiments, the ac input voltage = 100 (V), the reference output voltage V^*_{dc} = 200 (V), the input resistance R_i = 3 (Ω), the input inductance L_i = 15 (mH), the sampling period T_s = 50 (μs), the dc capacitance C = 2200 (μF) and the fundamental frequency of the input currents = 60 (Hz). Figure 5 shows simulation waveforms obtained by the NP rectifiers with the proposed control method. As shown in Figure 5a, the proposed control method with no weighting factors can produce sinusoidal input current waveforms in phase with the input voltage, leading to the unity power factor. In addition, the line-to-line rectifier voltage waveforms exhibit five levels. The frequency spectrum of the input current is depicted in Figure 5b, where the three-phase three-level NC rectifier yields spread frequency components due to the proposed predictive control algorithm. Figure 5c shows how the capacitor voltages are balanced by the proposed predictive control method with no weighting factor under a condition that the capacitor voltages were intentionally unbalanced, where the proposed control algorithm quickly eliminates capacitor voltage imbalance after the voltage balancing algorithm starts. Furthermore, Figure 5d shows the transient response waveform of the three-phase input currents and the capacitor voltages with a step change of the output reference voltage from 200 to 160 V.

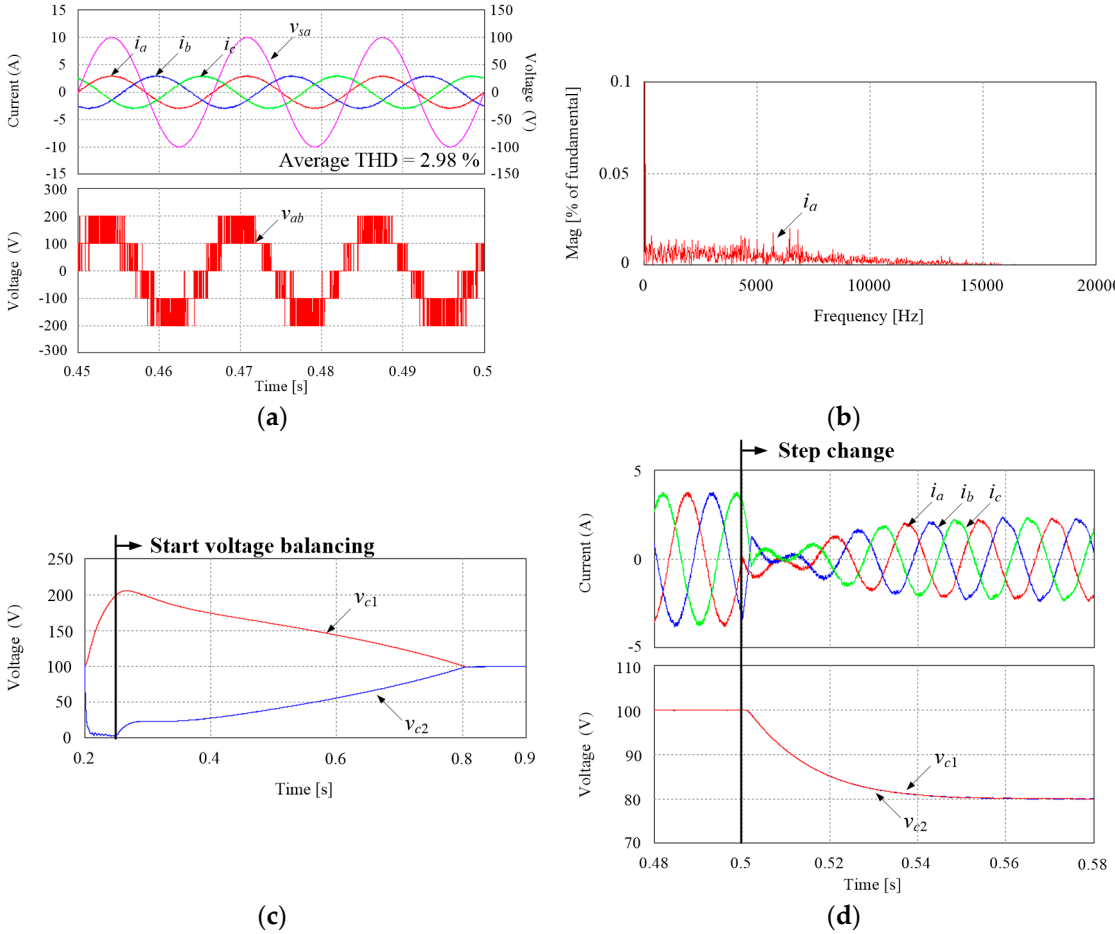

Figure 5. Simulation results of (**a**) three-phase input currents, *a*-phase input voltage, and line-to-line rectifier voltage (**b**) frequency spectrum of input current (**c**) capacitor voltages under conditions with intentional voltage unbalances (**d**) input currents and capacitor voltages with step change of output reference voltage from 200 to 160 V.

Validity of the proposed algorithm was verified with a prototype of three-phase three-level NP rectifier built in the laboratory, operated with a Digital Signal Processor (DSP) board (TMS320F28335). Figure 6 shows experimental waveforms resulted from the proposed predictive control method employing no weighting factor. In Figure 6a, sinusoidal three-phase input currents are synthesized, which are in phase with the input voltage, leading to the unity power factor. Therefore, it is seen that the proposed method operating without the weighting factor generates sinusoidal input currents. Frequency analysis waveforms of the input currents of the proposed control method is also shown in Figure 6b. The experimental waveform in Figure 6c illustrates how quickly the capacitor voltages are balanced by the proposed method without a weighting factor to make the capacitor voltage balance when the capacitor voltages were intentionally unbalanced. As can be seen from Figure 6c, the proposed control method quickly eliminates capacitor voltage imbalance after the voltage balancing algorithm starts. Figure 6d shows transient response waveforms for the output voltage by the proposed algorithm, where the magnitude of the output voltage was exposed to a step-change from 200 to 160 V.

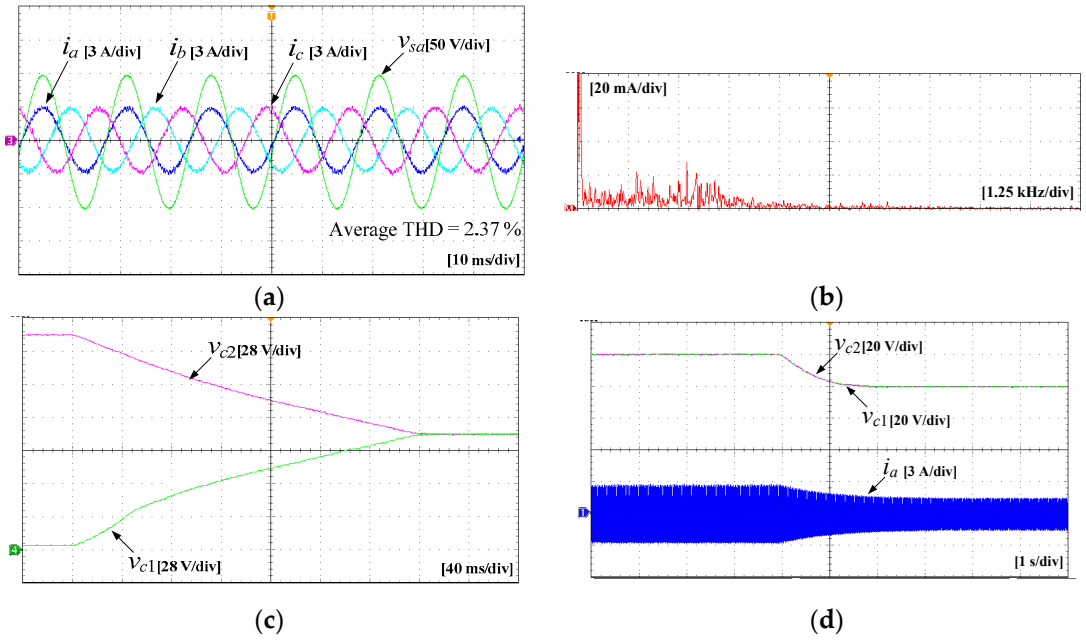

Figure 6. Experimental results of the proposed predictive control method with no weighting factor (**a**) three-phase input currents and *a*-phase input voltage (**b**) frequency spectrum of input current (**c**) capacitor voltages and line-to-line rectifier voltage (**c**) capacitor voltages balancing under voltage unbalanced condition (**d**) capacitor voltages and input current with step change of reference output voltage from 200 to 160 V.

5. Conclusions

In this paper, the predictive control method that controls the three-phase three-level NP rectifier by adding the offset voltage to the reference voltage was proposed. The proposed predictive method can operate the NP rectifier without employing the weighting factor, whereas the conventional method with the weighting factor term in the cost function is exposed to burdensome redesign procedures of the weighting factor whenever the control conditions are changed. The offset voltage in the proposed method was defined to reduce the voltage difference of the upper and lower capacitor voltages. The generated reference voltages with the injected offset voltage not only generate the sinusoidal input currents with a unity power factor by generating five level line-to-line rectifier voltages, but also maintain the balance of the capacitor voltages when the capacitor voltage unbalance occurs. The validity of the proposed algorithm was verified through the simulation and experiment.

Author Contributions: Conceptualization, S.K.; methodology, S.K., E.-S.J.; software, E.-S.J.; validation, E.-S.J.; formal analysis, E.-S.J.; investigation, S.K., E.-S.J.; resources, S.K.; data curation, E.-S.J., M.H.N.; writing—Original draft preparation, E.-S.J., M.H.N.; writing—Review and editing, M.H.N.; visualization, E.-S.J.; supervision, S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the National Research Foundation of Korea (NRF), grant funded by the Korean government (MSIT) (2020R1A2C1013413).

Acknowledgments: This research was supported by the National Research Foundation of Korea (NRF), grant funded by the Korean government (MSIT) (2020R1A2C1013413).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hill, R.J. Electric railway traction. Part 2: Traction drives with three-phase induction motors. *Power Eng. J.* **1994**, *8*, 143–152. [CrossRef]
2. Steimel, A. Electric railway traction in Europe. *IEEE Ind. Appl. Mag.* **1996**, *2*, 6–17. [CrossRef]

3. Cheok, A.D.; Kawamoto, S.; Matsumoto, T.; Obi, H. High power AC/DC rectifier and DC/AC inverter for high speed train applications. In Proceedings of the 2000 TENCON Proceedings. Intelligent Systems and Technologies for the New Millennium (Cat. No.00CH37119), Kuala Lumpur, Malaysia, 24–27 September 2000; Volume 1, pp. 423–428.
4. Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-Point-Clamped PWM Inverter. *IEEE Trans. Ind. Appl.* **1981**, *IA-17*, 518–523. [CrossRef]
5. Lai, J.S.; Peng, F.Z. Multilevel rectifiers-a new breed of power rectifiers. *IEEE Trans. Ind. Appl.* **1996**, *32*, 509–517.
6. Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
7. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Pérez, M.A. A Survey on Cascaded Multilevel Inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2197–2206. [CrossRef]
8. Carrasco, J.M.; Franquelo, L.G.; Bialasiewicz, J.T.; Galvan, E.; PortilloGuisado, R.C.; Prats, M.A.M.; Leon, J.I.; Moreno-Alfonso, N. Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1002–1016. [CrossRef]
9. Rodriguez, J.; Bernet, S.; Wu, B.; Pontt, J.O.; Kouro, S. Multilevel Voltage-Source-Rectifier Topologies for Industrial Medium-Voltage Drives. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2930–2945. [CrossRef]
10. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Pérez, M.A.; Leon, J.I. Recent Advances and Industrial Applications of Multilevel Rectifiers. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580. [CrossRef]
11. Cairone, F.; Gagliano, S.; Bucolo, M. Experimental study on the slug flow in a serpentine microchannel. *Exp. Therm. Fluid Sci.* **2016**, *76*, 34–44. [CrossRef]
12. De Freitas, I.S.; Bandeira, M.M.; Barro, L.M.; Jacobina, C.B.; dos Santos, E.C.; Salvadori, F.; da Silva, S.A. A Carrier-Based PWM Technique for Capacitor Voltage Balancing of Single-Phase Three-Level Neutral-Point-Clamped Rectifiers. *IEEE Trans. Ind. Appl.* **2015**, *51*, 3227–3235. [CrossRef]
13. Tallam, R.M.; Naik, R.; Nondahl, T.A. A Carrier-Based PWM Scheme for Neutral-Point Voltage Balancing in Three-Level Inverters. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1734–1743. [CrossRef]
14. Choi, U.-M.; Lee, H.-H.; Lee, K.-B. Simple Neutral-Point Voltage Control for Three-Level Inverters Using a Discontinuous Pulse Width Modulation. *IEEE Trans. Energy Convers.* **2013**, *28*, 434–443. [CrossRef]
15. Wang, S.; Ge, X.; Xiong, C.; Song, W.; Feng, X. Single-phase three-level space vector pulse width modulation algorithm for grid-side railway traction rectifier and its relationship of carrier-based pulse width modulation. *IET Electr. Syst. Transp.* **2014**, *4*, 78–87.
16. Dai, N.-Y.; Wong, M.-C.; Han, Y.-D. Application of a three-level NP inverter as a three-phase four-wire power quality compensator by generalized 3DSVM. *IEEE Trans. Power Electron.* **2006**, *21*, 440–449. [CrossRef]
17. Choi, U.-M.; Blaabjerg, F.; Lee, K.-B. Method to Minimize the Low-Frequency Neutral-Point Voltage Oscillations with Time-Offset Injection for Neutral-Point-Clamped Inverters. *IEEE Trans. Ind. Appl.* **2015**, *51*, 1678–1691. [CrossRef]
18. Lee, J.-S.; Lee, K.-B. Time-Offset Injection Method for Neutral-Point AC Ripple Voltage Reduction in a Three-Level Inverter. *IEEE Trans. Power Electron.* **2016**, *31*, 1931–1941. [CrossRef]
19. Lee, J.-S.; Yoo, S.; Lee, K.-B. Novel Discontinuous PWM Method of a Three-Level Inverter for Neutral-Point Voltage Ripple Reduction. *IEEE Trans. Ind. Electron.* **2016**, *63*, 3344–3354. [CrossRef]
20. Jun, E.-S.; Kwak, S. A Highly Efficient Single-Phase Three-Level Neutral Point Clamped (NP) Rectifier Based on Predictive Control with Reduced Number of Commutations. *Energies* **2018**, *11*, 3524. [CrossRef]
21. Habibullah, M.; Lu, D.D.-C.; Xiao, D.; Rahman, M.F. Finite-State Predictive Torque Control of Induction Motor Supplied from a Three-Level NP Voltage Source Inverter. *IEEE Trans. Power Electron.* **2017**, *32*, 479–489. [CrossRef]
22. Habibullah, M.; Lu, D.D.-C.; Xiao, D.; Fletcher, J.E.; Rahman, M.F. Predictive Torque Control of Induction Motor Sensorless Drive Fed by a 3L-NP Inverter. *IEEE Trans. Ind. Inf.* **2017**, *13*, 60–70. [CrossRef]
23. Lee, J.-H.; Lee, J.-S.; Moon, H.-C.; Lee, K.-B. An Improved Finite-Set Model Predictive Control Based on Discrete Space Vector Modulation Methods for Grid-Connected Three-Level Voltage Source Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 1744–1760. [CrossRef]

24. Jun, E.; Kwak, S.; Baek, J. Model Predictive Control Method with NP Voltage Balance by Offset Voltage Injection for Single-phase Three-level Neutral Point Clamped Converters. In Proceedings of the 28th IEEE International Symposium on Industrial Electronics, Vancouver, BC, Canada, 12–14 June 2019; pp. 914–919.
25. Kim, J.-C.; Moon, S.-K.; Kwak, S. Direct model-based predictive control scheme without cost function for voltage source inverters with reduced common-mode voltage. *Int. J. Electron.* **2018**, *105*, 629–644. [CrossRef]
26. Rodriguez, J.; Pontt, J.; Silva, C.A.; Correa, P.; Lezana, P.; Cortes, P.; Ammann, U. Predictive Current Control of a Voltage Source Inverter. *IEEE Trans. Ind. Electron.* **2007**, *54*, 495–503. [CrossRef]
27. Song, W.; Feng, X.; Smedley, K.M. A Carrier-Based PWM Strategy with the Offset Voltage Injection for Single-Phase Three-Level Neutral-Point-Clamped Rectifiers. *IEEE Trans. Power Electron.* **2013**, *28*, 1083–1095. [CrossRef]