IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 8, 2020, accepted July 17, 2020, date of publication July 23, 2020, date of current version August 5, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3011475

Cost-Effective Matrix Rectifier Operating With Hybrid Bidirectional Switch Configuration Based on Si IGBTs and SiC MOSFETs

BRYAN GUTIERREZ AND SANG-SHIN KWAK, (Member, IEEE)
School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea

Corresponding author: Sang-Shin Kwak (sskwak@cau.ac.kr)

This work was supported in part by the National Research Foundation of Korea (NRF) through the Korea Government (MSIT) under Grant 2020R1A2C1013413; and in part by the Korean Government (MSIP) under Grant 2017R1A2B4011444.

ABSTRACT For so many years, silicon (Si) IGBTs have been widely utilized in power converters for low-to-medium voltage high-power applications. However, the ever-increasing requirements to improve power density, power quality, and efficiency of power converters have urged researchers to explore alternative technologies such as silicon-carbide (SiC) MOSFETs. SiC devices fill the mentioned gaps with increased voltage blocking capability, higher switching speed, and lower on-state resistance; yet, their price is much more elevated. Both technologies are adopted in matrix rectifiers (MRs), which have recently gained attention for on-board electric vehicle (EV) charger and battery energy storage system (BESS) applications because of their controllable bidirectional power flow and compact size. A MR contains bidirectional switches made up of two power devices, doubling the device count and cost to conventional voltage source converters (VSCs). In this paper, we compare in terms of efficiency four types of MRs, each one consisting of a specific bidirectional switch configuration. Among these switches, we propose a cost-effective hybrid configuration consisting of Si IGBTs and SiC MOSFETs for straightforward commutations during the charging mode of matrix rectifiers. Also, the proposed configuration is compared to other typical bidirectional switch configurations. To perform these comparisons, the switching energy losses in 1200 V commercial IGBTs and MOSFETs, constituting the bidirectional switches, are measured through the double-pulse test (DPT). Performance comparisons of the MRs are supported through a simulator and verified via experimental work, where the proposed arrangement results in a cost-effective solution in MRs operating with switching frequencies up to 50 kHz and further.

INDEX TERMS Bidirectional switch, double-pulse test, energy efficiency, matrix rectifier, silicon carbide.

I. INTRODUCTION

In years to come, the unpredictable power generated by the increasing penetration of variable renewable energy (VRE), may require power systems to have additional degrees of grid flexibility to maintain the equilibrium between power generation and consumption. To reach such flexibility, surplus VRE generated over low power demands can be initially stored, through various storage technologies, to eventually assist the power grid during high-demand periods. [1], [2]. An attractive solution is the battery energy storage system (BESS) because it does not only operate to store energy but, by means of a bidirectional power converter, it can also realize fast and smooth load leveling, power quality improvement, and voltage support to power grids with high penetration of VRE [3]–[8].

Meanwhile, with the rapid market expansion of the electric vehicle (EV) industry and the development of smart grids, the concept of utilizing the numerous existing EV battery chargers connected to the power grid, as BESS-like assistance, has gained attention in the last years. Consequently, two courses of action have been investigated to control the EV charger's power converter: grid-to-vehicle (G2V) operation and vehicle-to-grid (V2G) operation. G2V operation takes place when the power grid charges the EV battery, whereas V2G operation, like the BESS, provides support to the power grid with the energy stored in the EV battery [9], [10].

The associate editor coordinating the review of this manuscript and approving it for publication was Ahmad Elkhateb.

Both the BESS and the EV chargers require highly efficient power converters to transfer energy from the battery to the power grid and vice-versa. Thus, the realization of power converters through wide-bandgap (WBG) devices such as silicon-carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) would reduce the power losses and improve the efficiency of the converters in BESS and EV chargers [11], [12]. However, at this moment, the cost of WBG devices utilized to implement the power converters are much more elevated compared to the conventionally utilized silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) and MOSFETs. Also, typically, voltage source converters (VSCs) have been used to supply bidirectional ac-dc power in these systems and, because of the boost-type nature of the VSCs, they may require an additional stage with a bulky dc-link to properly regulate the voltage of the battery [13]. As a result, VSCs could be less efficient, less reliable, and bulkier.

To overcome the drawbacks caused by two-stage power converters, engineers have paid attention to the matrix rectifier (MR) as a solution. MRs operated as current source converters, can regulate in a single stage the battery's voltage with their natural step-down operation. Simultaneously, through a LC filter located in the power grid side, the MR achieves sinusoidal ac currents. Unity power factor could also be obtained by application of control algorithms targeting this issue [13], [14]. Thus, the MR is a compact and efficient solution with two-way controllable power flow. Yet, the bidirectional switches, made up of two semiconductor packs in an anti-serial arrangement, add up the semiconductor count in the MR, which increases the production cost of the converter.

In this paper, the efficiency and power loss comparisons of different configurations of bidirectional switches are presented and analyzed in detail. Among these configurations, we propose a cost-effective bidirectional switch made up of a combination of Si IGBT and SiC MOSFET semiconductor technologies. The MR's topology, controller, and bidirectional switches employed in this study are described in Section II. The power loss measurements among the power devices used within the conventional and proposed bidirectional switches are shown in Section III. The simulated performance comparisons of the four MRs are presented in Section IV. The experimental validation is shown in Section V and the conclusions in Section VI.

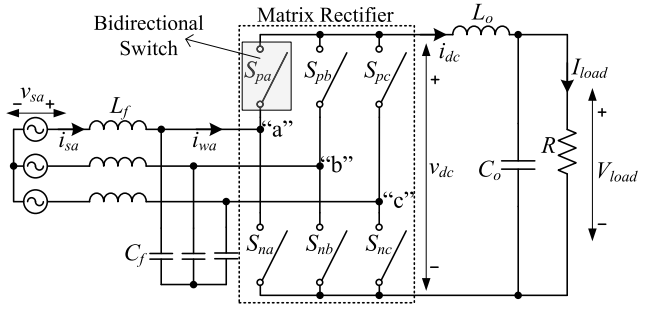


FIGURE 1. Circuit configuration of the matrix rectifier.

II. THE MATRIX RECTIFIER

A. TOPOLOGY AND CONTROLLER

The topology of the MR with generic bidirectional switches is presented in Fig. 1. In this figure, a three-phase voltage source v_{sj} supplies the system, where the subscript j represents the phase ($j = a, b, c$). The inductor L_f and the capacitor C_f represent the input filter of the MR. This filter mitigates the switching components present at the MR's input current i_{wj}. Therefore, the source current i_{sj} is sinusoidal with diminished total harmonic distortion (THD). At the other end of the MR, the inductor L_o and capacitor C_o constitute the converter's output filter, which filters out the switching components contained at the MR's output current i_{dc}. Thus, ideally, the filtered current charging the battery I_{load} and the battery voltage V_{load} have only a dc component without switching ripples nor fluctuations. The MR itself is comprised of six bidirectional switches S_{xj}, where x denotes the upper or lower arm of the MR ($x = p, n$).

To supply a steady flow of charge to the battery, the MR operates as a current source rectifier with a constant current (CC) controller as depicted in Fig. 2, where the reference current is defined by $i_{dc}{}^*$. The space vector modulation (SVM) is adopted to generate the switching states in the MR. To accomplish this, the CC-SVM block requires the phase reference angle θ and the modulation index m_i to produce a reference current vector $\boldsymbol{I_w}^*$. The angle θ is obtained by processing the three-phase input voltages v_{sj} in a phase-locked loop (PLL) while the proportional-integral (PI) controller produces the modulation index m_i [13]. Thereupon, the SVM computes the time duration (dwell time) that each adjacent current vector to the reference $\boldsymbol{I_w}^*$ must undergo during the controller's sampling period T_{sp}. For instance, if $\boldsymbol{I_w}^*$ were in sector II, the adjacent current vectors will be $\boldsymbol{I}_2$, $\boldsymbol{I}_3$, and $\boldsymbol{I}_0$. Table 1 shows every possible switching state and current vector in the MR. Notice that $\boldsymbol{I}_0$ can be realized by three different switching states (redundant states). Accordingly, the proper selection of redundant states and distribution of current vectors with their respective dwell times, employing the double-sided switching pattern, ensures smooth and efficient commutations within the MR [15].

B. IMPLEMENTATION OF THE BIDIRECTIONAL SWITCH AND CURRENT PATH IN MATRIX RECTIFIERS

The bidirectional switches are realized by the common-emitter anti-serial alignment of different semiconductor devices as displayed in Fig. 3, where the four types of bidirectional switches employed in this study are portrayed. Fig. 3 (a) shows two Si IGBT/Si diode co-packs (Si-IGBT) making up the bidirectional switch. In Fig. 3 (b), the bidirectional switch is realized by Si IGBT/SiC diode co-packs (Si-IGBT/SiC). SiC MOSFETs with their respective body diodes (SiC-MOSFET) constituting the bidirectional switches are presented in Fig. 3 (c). Lastly, we propose in Fig. 3 (d) a cost-effective hybrid bidirectional switch

TABLE 1. Switching states and current vectors in the matrix rectifier

Vector	On-state switches	i_{wa}	i_{wb}	i_{wc}
$\boldsymbol{I_1}$	S_{pa}, S_{nb}	i_{dc}	$-i_{dc}$	0
$\boldsymbol{I_2}$	S_{pa}, S_{nc}	i_{dc}	0	$-i_{dc}$
$\boldsymbol{I_3}$	S_{pb}, S_{nc}	0	i_{dc}	$-i_{dc}$
$\boldsymbol{I_4}$	S_{pb}, S_{na}	$-i_{dc}$	i_{dc}	0
$\boldsymbol{I_5}$	S_{pc}, S_{na}	$-i_{dc}$	0	i_{dc}
$\boldsymbol{I_6}$	S_{pc}, S_{nb}	0	$-i_{dc}$	i_{dc}
$\boldsymbol{I_0}$	S_{pa}, S_{na}	0	0	0
$\boldsymbol{I_0}$	S_{pb}, S_{nc}	0	0	0
$\boldsymbol{I_0}$	S_{pc}, S_{nc}	0	0	0

(SiC-MOSFET/Si-IGBT) based on the IGBTs and MOSFETs shown in Fig. 3 (a) and Fig. 3(c), respectively.

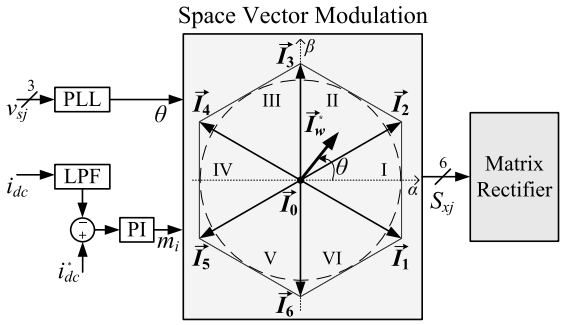


FIGURE 2. Block diagram of the CC-SVM for the matrix rectifier.

During the powering mode of the MR, which is generally the most frequent operation, the power only flows from the ac side to the dc side of the converter. For instance, Fig. 4 depicts the current path in the Si-IGBT-based MR when vector $\boldsymbol{I_1}$ is applied. Notice that only the lower transistor and the upper diode in each on-state bidirectional switch operate. Thus, to reduce the complexity of commutations of the matrix rectifier, the upper transistor could be turned off during the charging mode [9]. To ensure high efficiency during the MR's charging operation, the conduction and switching behaviors of the lower transistor and upper diode inside bidirectional switches must be considered during the design stage of the MR. Consequently, aiming to obtain a cost-effective solution, we propose in Fig. 3 (d) a hybrid configuration, which is advantageous as demonstrated in the succeeding sections.

III. ACQUIRING ENERGY AND POWER LOSSES IN THE SEMICONDUCTOR DEVICES

To proceed with this study, we have selected three commercial 1200 V semiconductor devices making up all the bidirectional switches presented in Fig. 3. For the sake of a fair comparison, all these devices come with comparable voltage and current ratings, and they are suitable to operate under the frequencies considered in this paper. Table 2 lists the typical values of the selected semiconductor devices, which are provided by the manufacturers' datasheets.

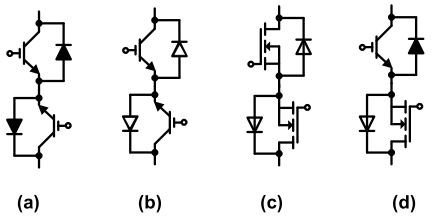


FIGURE 3. Implementation of bidirectional switches S_{xj} in matrix rectifiers. (a) Si-IGBT (Si IGBT/Si diode). (b) Si-IGBT/SiC (Si IGBT/SiC diode). (c) SiC-MOSFET. (d) SiC-MOSFET/Si-IGBT.

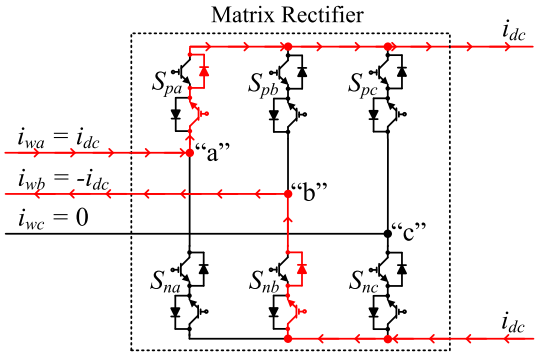


FIGURE 4. Current path through the matrix rectifier applying the switching state of vector $\boldsymbol{I_1}$.

A. ENERGY LOSSES IN THE DEVICES

During normal operation of any hard-switching power converter, the power losses in their semiconductor devices are comprised of the following two parts: switching loss and conduction loss [16]. The transition towards the initiation (turn-on) and cessation (turn-off) of conduction in the semiconductor devices denote the switching losses. When the current flowing through the transistor starts to increase from zero to a certain value, and the blocking voltage gradually reduces to zero, the turn-on energy loss E_{on} occurs as depicted in Fig. 5 (a) and it is calculated as

$$E_{on} = \int_{\tau_1}^{\tau_2} P_{on} dt = \int_{\tau_1}^{\tau_2} v_{CE} \times i_C dt = \int_{\tau_1}^{\tau_2} v_{DS} \times i_D dt \quad (1)$$

where v_{CE} is the IGBT's collector-emitter voltage, v_{DS} is the MOSFET's drain-source voltage, and i_C and i_D are the collector and drain current in the IGBT and MOSFET, respectively. Conversely, Fig. 5 (b) shows the transistor's current decreasing toward zero and the blocking voltage progressively increasing. In this case, a turn-off energy loss E_{off} is registered and can be calculated by the following equation:

$$E_{off} = \int_{\tau_3}^{\tau_4} P_{off} dt = \int_{\tau_3}^{\tau_4} v_{CE} \times i_C dt$$

$$= \int_{\tau_3}^{\tau_4} v_{DS} \times i_D dt. \quad (2)$$

Note that the observed tail current in Fig.5 (b) is nonexistent for MOSFETs. While it is widely known that turn-on losses are neglectable for diodes, their turn-off losses are significant and must be considered. As observed in Fig. 5 (c), after the current in the diode drops to zero with a constant rate di/dt, it undershoots up to the maximum reverse recovery current I_{rr} amid the increasing reverse voltage in the diode causing what is known as the diode's reverse recovery loss E_{rr}, which is calculated as

$$E_{rr} = \int_{\tau_5}^{\tau_6} P_{rr} dt = \int_{\tau_5}^{\tau_6} (v_F \times i_F)\, dt \quad (3)$$

where, i_F and v_F denote the forward current and the forward voltage in the anti-parallel diode, respectively. Note that -v_F is equal to the collector-emitter voltage v_{CE} of the respective device. The integration intervals in these equations (delimited by τ_1, τ_2, τ_3, τ_4, τ_5, and τ_6) are established in the following sub- section adopting the SEMIKRON guidelines to determine the switching energy losses [17].

After the turn-on transition has been completed, the current in the bidirectional switch flows through the on-state resistance of one transistor and one diode generating the conduction losses Q_T and Q_D in the transistor and diode, respectively. However, the on-state resistance in semiconductor devices is not fixed but varies with the current (i_C, i_D or i_F), which causes the conduction voltage drop (v_{CE}, v_{DS} or v_F) to vary in a non-linear manner [16]. Additionally, the currents flowing through the semiconductor devices in power converters are never steady because of their inherited switching operation and fundamental ac components. Therefore, to accurately obtain the conduction energy loss, we must calculate it within a small-time interval T_{sim} (much smaller than T_{sp}) where the current is nearly constant. Fig. 6 shows an exaggerated curve of the on-state power dissipation (P_T or P_D) whose area corresponds to the conduction energy loss (Q_T or Q_D) and it can be obtained as follows:

$$Q_T = \sum v_{CE} \times i_C \times T_{sim} = \sum v_{DS} \times i_D \times T_{sim} \quad (4)$$

$$Q_D = \sum v_F \times i_F \times T_{sim}. \quad (5)$$

B. MEASURING SWITCHING ENERGY LOSSES

Power semiconductor devices' datasheets provide engineers with valuable information like ratings and typical values in the devices. Nevertheless, as seen in Table 2, the data on switching energy loss is limited to specific conditions and parameters selected by the manufacturer such as blocking voltage, gate driver's gate resistance, gate voltage, etc. Thus, to accurately execute an objective comparison in terms of energy losses and efficiency among the four types of MRs, the energy losses in each device presented in Table 2 must be determined under equal conditions. To determine such values, the DPT is adopted [12], [18]–[20]. Fig. 7 (a) depicts the circuit utilized for the DPT, where T_1 and D_1 represent the upper device package and T_2 and D_2 are contained in the lower device package. The gate driver SKHI 22B(R) is used to drive T_2 while T_1 is kept in off-state. The first pulse sets T_2 on and it allows the inductor L to ramp up its current i_L (equal to i_C or i_D in this scenario) to a level that is contingent upon the duration of the pulse. When the first pulse ends and the gate voltage starts dropping, E_{off} can be obtained from T_2. Once the gate voltage reaches zero, the current i_L (equal to i_F in this scenario) circulates in a loop through D_1. Subsequently, during the positive edge of the second pulse, E_{rr} and E_{on} can be measured in D_1 and T_2, respectively. An energy storage capacitor C is used in the set-up to quickly provide energy to the inductor. To mitigate the parasitic inductances across the wiring paths of the circuit, the capacitor C is comprised of many parallel capacitors and it is connected to the nearest points to the devices [21]–[23]. The complete list of components with their respective specifications used for the DPT in this paper are listed in Table 3.

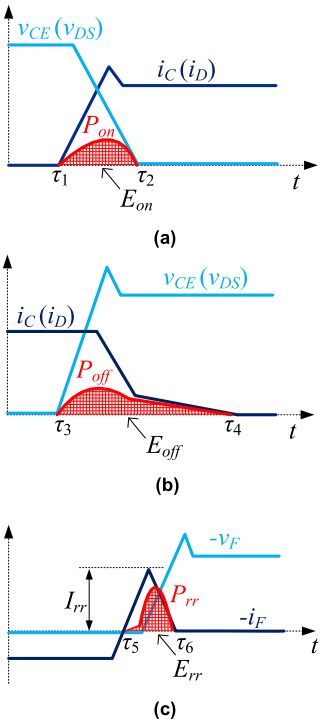


FIGURE 5. Ideal waveforms of the switching transitions. (a) Turn-on transition of the transistor. (b) Turn-off transition of the transistor. (c) Reverse recovery transition of the diode.

1) THE SILICON IGBT WITH ANTI-PARALLEL SILICON DIODE (SI-IGBT)

Two Si-IGBT devices (IXA37IF1200HJ) were inserted in the test board presented in Fig. 7. The switching energy losses E_{on}, E_{off}, and E_{rr} in this device were measured considering the parameters established in Table 3 and a collector current i_C up to approximately 10 A. For the first measurement, we adjusted the width of the first pulse to 10 μs in order to increase i_C up to 2.2 A. Thereafter, we measured E_{off}

TABLE 2. Datasheet's ratings and typical values of the selected devices

Parameters	Symbol	Si-IGBT IXA37IF1200HJ		Si-IGBT/SiC GA35XCP12		SiC-MOSFET SCT3040KL	
		Condition	Value	Condition	Value	Condition	Value
Transistor							
Voltage rating	V_{CES}, V_{DSS}	-	1200 V	-	1200 V	-	1200 V
Current rating	I_C, I_D	T_c = 90˚C	37 A	T_c = 105˚C	35 A	T_c = 100˚C	39 A
Drain-Source on-state resistance	$R_{DS(on)}$	-	-	-	-	I_D = 20 A V_{GS} = 18 V T_j = 25 ˚C	40 mΩ
Collector-Emitter saturation voltage	$V_{CE(sat)}$	I_C = 35 A V_{GE} = 15 V T_j = 25 ˚C	1.8 V	I_C = 35 A V_{GE} = 15 V T_j = 25 ˚C	3 V	-	-
Turn-on energy loss	E_{on}	V_{CE} = 600 V I_C = 35 A V_{GE}= ±15 V R_G= 27 Ω T_j = 125˚C	3.8 mJ	V_{CE} = 800 V I_C = 35 A V_{GE}= -8 V/15 V R_G= 22 Ω T_j = 125˚C	2.66 mJ	V_{DS} = 600 V I_D = 20 A V_{GS}= 0 V/18 V R_G= 0 Ω T_j = 25˚C	283 μJ
Turn-off energy loss	E_{off}		4.1 mJ		4.35 mJ		118 μJ
Diode							
Forward voltage	V_F	I_F = 30 A T_j = 25 ˚C	1.95 V	I_F = 35 A T_j = 25 ˚C	2.6 V	I_F = 20 A T_j = 25 ˚C	3.2 V
Peak reverse recovery current	I_{rr}	V_R = 600 V di/dt = -600 A/μs I_F= 30 A T_j = 125 ˚C	30A	V_R = 650 V di/dt = -300 A/μs I_F= 35 A T_j = 125 ˚C	3.01 A	V_R = 600 V di/dt = -1100 A/μs I_F= 20 A T_j = 25 ˚C	9 A

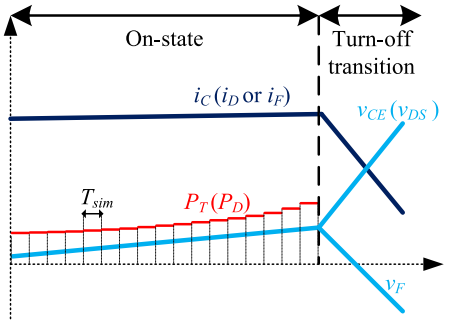


FIGURE 6. Magnified waveforms during conduction of transistors and diodes with their respective conduction power loss P_T and P_D.

TABLE 3. Circuit components and instruments utilized in the DPT

Item	Type/Model	Value
Power supply (V_{CC})	N8741A	100 V
Storage capacitor (C)	C4ATJBW5150A3NJ	15 μF × 6
Inductor (L)	Air core	500 μH
Gate driver	SKHI22B(R)	-
- Gate resistance (R_G)	-	15 Ω
- Gate voltage (V_{GE}, V_{GS})	-	-7 V/15 V
Function generator	DG1022	25 MHz
Oscilloscope	MSO3054	500 MHz
Voltage probe	P5200A	50 MHz
- Propagation delay	-	21 ns
Current probe	TCPA300/TCP312	100 MHz
- Propagation delay	-	17 ns

during the falling edge of the first pulse, and E_{on} and E_{rr} over the rising edge of the second pulse. Similarly, to obtain measurements at $i_C = 4.2$ A, the pulse width must be increased to 20 μs. In this manner, we continuously increased the pulse width until obtaining sufficient data points.

Fig. 8 depicts the current, voltage, and switching power dissipation waveforms used to calculate the energy losses at $i_C = 8.2$ A (pulse width of 40 μs). In order to obtain the energy losses during commutations, we applied (1), (2), and (3) into the oscilloscope math tool. Yet, to accurately carry on with these computations, their respective integration intervals must be appointed [17]. In the case of E_{on}, the integration interval starts when v_{GE} is around 10% of its on-state voltage ($V_{GE(on)}$) until at least 2% of the blocking voltage V_{CC}. As a result, Fig. 8 (a) can show us that (1) results in $E_{on} = 71.5$ μJ. As for E_{off}, by means of (2) and Fig. 8 (b) with the integration interval from 90 % of $V_{GE(on)}$ until i_C is at least 2% of 8.2 A (on-state collector current), E_{off} yields an energy loss of 225 μJ. Notice that the tail current in Fig. 8 (b) has a long duration yielding large integration interval and elevated E_{off}. Lastly, the integration interval for (3) is set between the first and second zero level crossing events of the current i_F. Thus, Fig 8. (c) displays that E_{rr} is 21.7μJ for $i_F = 8.2$A. Also, we can observe that I_{rr} is elevated and its magnitude is the same as the magnitude of overshoot appearing during the turn-on transition in Fig. 8 (a). Therefore, E_{rr} has a direct impact on E_{on} [24], [25].

2) THE SILICON IGBT WITH ANTI-PARALLEL SILICON CARBIDE DIODE (SI-IGBT/SIC)

To measure the energy losses E_{on}, E_{off}, and E_{rr} in the Si-IGBT/SiC, two GA35XCP12 devices were inserted in the test

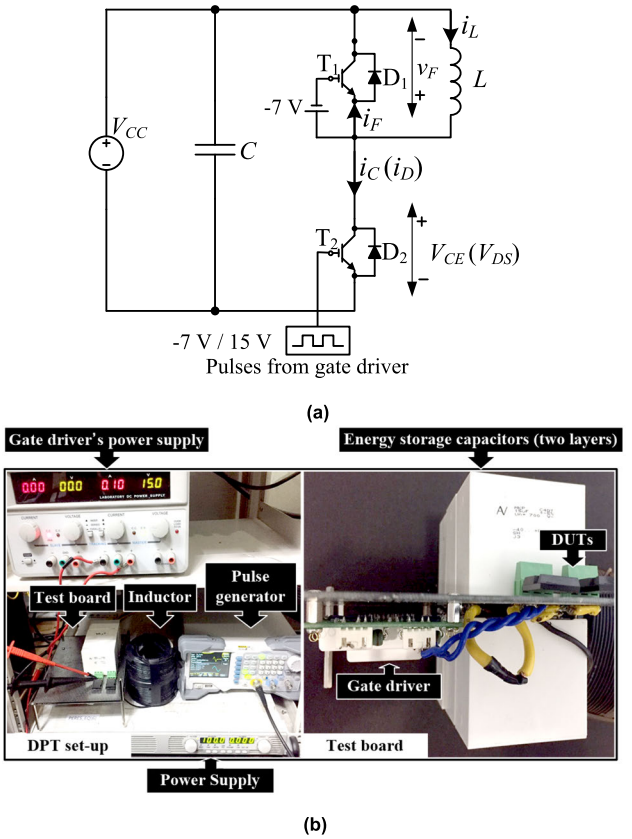


FIGURE 7. DPT set-up. (a) Circuit diagram. (b) Test circuit.

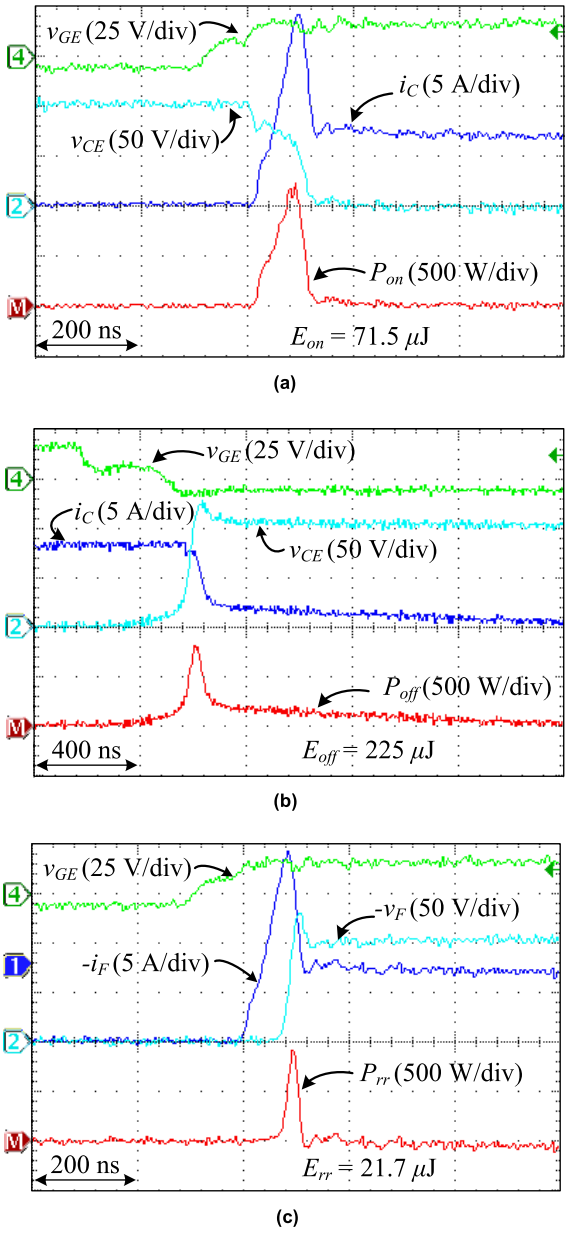


FIGURE 8. Switching waveforms during the DPT of the Si-IGBT device. (a) Turn-on transition. (b) Turn-off transition. (c) Reverse recovery transition of the freewheeling Si diode.

board of Fig. 7. For the sake of acquiring comparable data to the previously measured device, energy losses were collected with the same parameters listed in Table 3 and the collector currents i_C up to approximately 10 A.

The integration intervals in (1), (2), and (3) are determined by the methodology adopted for the Si-IGBT device. Having defined the integration intervals for the waveforms presented in 9 (a), Fig. 9 (b), and Fig. 9 (c) the energy losses were obtained as $E_{on} = 41\ \mu$J, $E_{off} = 166\ \mu$J, and $E_{rr} = 4.1\ \mu$J for $i_C = i_F = 8.2$ A. Similar to the Si-IGBT device, the tail current has a big impact on E_{off}. However, because of the SiC diode contained in the Si-IGTB/SiC device, E_{rr} is greatly reduced, thus, E_{on} is influenced by this loss reduction.

3) THE SILICON CARBIDE MOSFET (SIC-MOSFET)

Like the IGBT devices, the energy losses in the SiC-MOSFET device (SCT3040KL) were collected taking into consideration the parameters in Table 3 and the currents i_D up to 10 A. The methodology used for the IGBTs was also applied to determine the integration intervals for (1), (2), and (3). However, i_D, v_{DS}, and v_{GS} are employed instead of i_C, v_{CE}, and v_{GE}, respectively. Notice that, unlike the IGBT devices, the tail current is nonexistent, which greatly reduces the turn-off energy loss in the SiC-MOSFET. In addition, the SiC body diode integrated in the device allows low E_{rr}, which yields to reduced E_{on}. The energy losses for $i_D = i_F = 8.2$A were obtained as $E_{on} = 30.9\ \mu$J, $E_{off} = 19\ \mu$J, and $E_{rr} = 2.8\ \mu$J. The waveforms of these switching transitions are displayed in Fig. 10.

C. COMPARISON OF SWITCHING ENERGY LOSSES

With all the experimental data points gathered on switching energy losses from the previous sub-section, we can plot in Fig. 11 the devices' switching energy loss comparison under equal conditions that are listed in Table 3. Fig. 11 (a) depicts the turn-on energy loss E_{on} in the devices, where we observe that the SiC-MOSFET has the lowest turn-on energy loss compared to the Si-based IGBT devices. Despite the

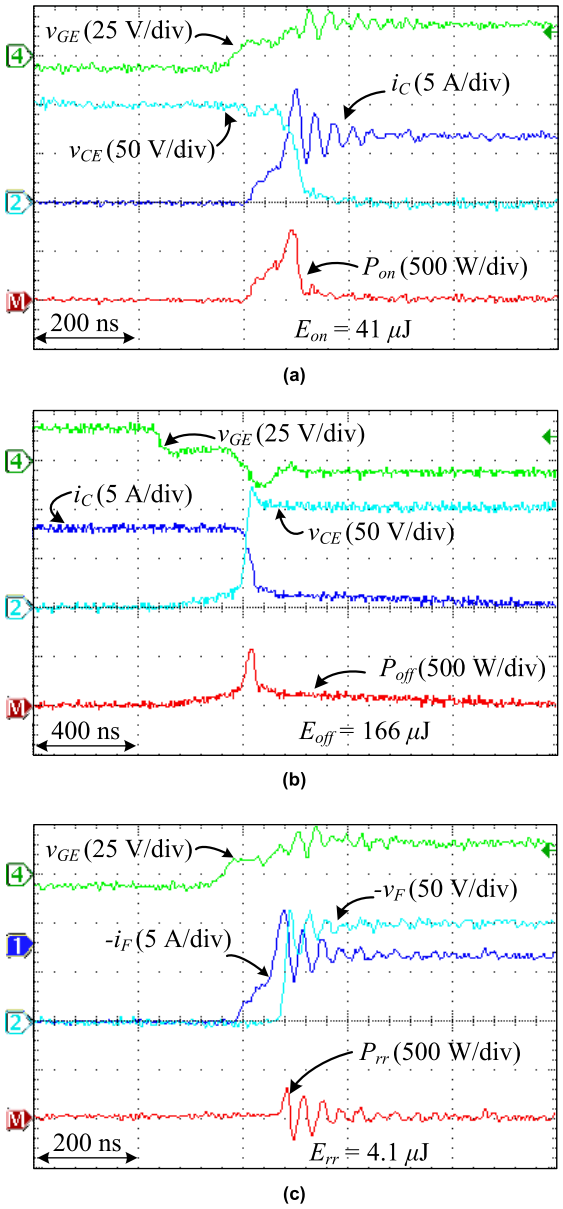


FIGURE 9. Switching waveforms during the DPT of the Si-IGBT/SiC device. (a) Turn-on transition. (b) Turn-off transition. (c) Reverse recovery transition of the freewheeling SiC diode.

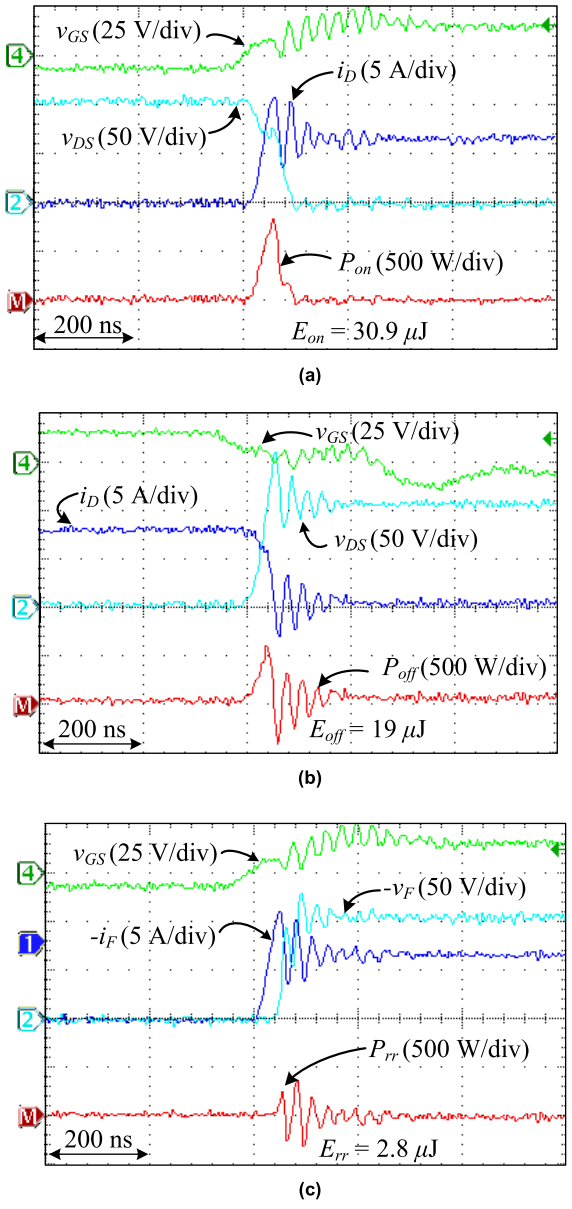
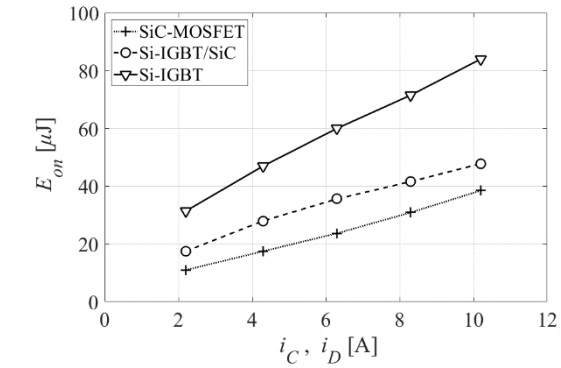
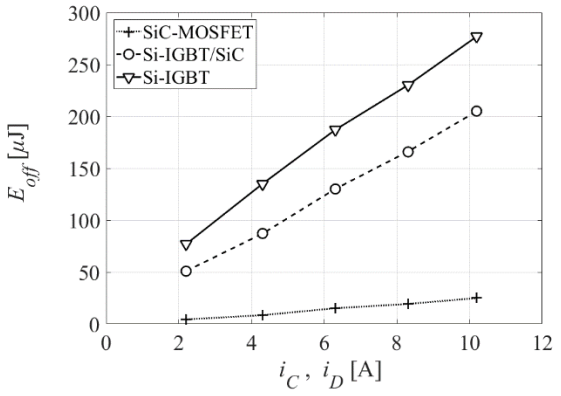


FIGURE 10. Switching waveforms during the DPT of the SiC-MOSFET device. (a) Turn-on transition. (b) Turn-off transition. (c) Reverse recovery transition of the freewheeling SiC body diode.

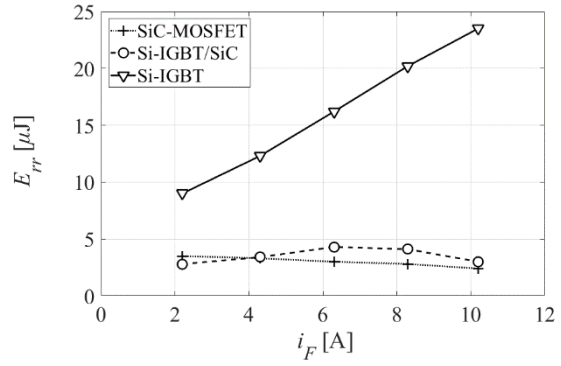
contrasting manufacturers' test conditions, we can observe a similar tendency in the SiC-MOSFET's E_{on} in Table 2. Furthermore, despite having a higher blocking voltage in the test conditions of Table 2, the Si-IGBT/SiC device has reduced E_{on} compared to the Si-IGBT device. Likewise, Fig. 11 (b) demonstrates that the turn-off energy loss E_{off} of the SiC-MOSFET is greatly minor in comparison with the Si-based devices, which is caused by the absence of the tail current. By observing E_{off} in Table 2, we can infer that, at equal blocking voltage conditions, the Si-IGBT device would have larger E_{off} compared to the Si-IGBT/SiC device, which is observed in Fig. 11 (b). Fig. 11 (c) displays the reverse recovery loss E_{rr} of the diodes in each device. We can see that only the device with Si-based diode has an increased E_{rr}, whereas both devices containing SiC diodes have reduced and similar energy losses because of the reduction of the peak reverse recovery current I_{rr} as the conducting forward current increases, which is seen in Fig. 11 (d) [24]. Also, Table 2 reveals a large I_{rr} in the Si-IGBT compared to its counterparts. We can infer from Fig. 11, that any power converter implemented purely with SiC-based MOSFETs would have superior efficiency as the switching frequency f_{sw} increases compared to the Si technologies. However, as presented in Section II, the current paths in the course of operation must be considered to select the most effective devices for the MR.



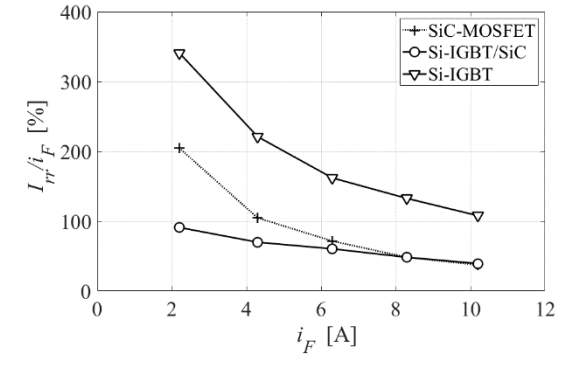
(a)



(b)

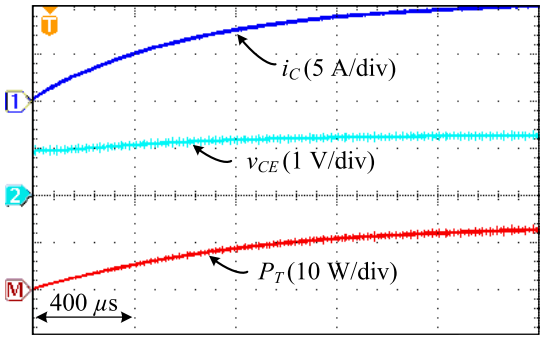


(c)

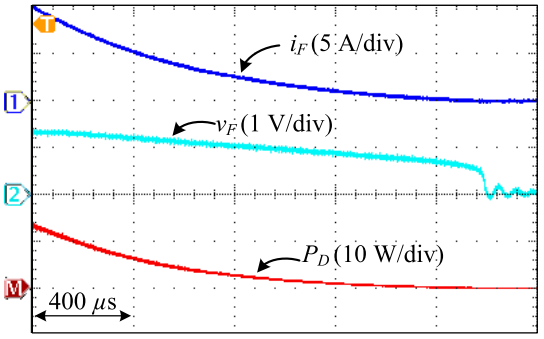


(d)

FIGURE 11. Comparison of switching energy losses at different currents i_C, i_D, and i_F. (a) Turn-on energy loss. (b) Turn-off energy loss. (c) Reverse recovery loss of diodes. (d) Reverse recovery current.

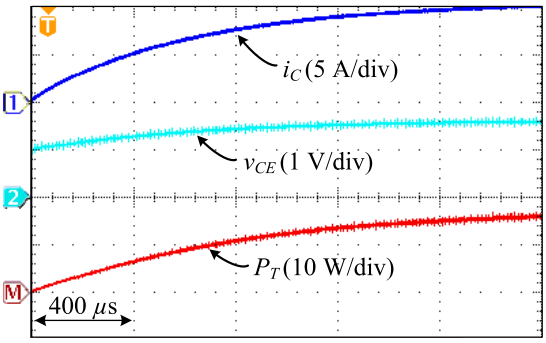


(a)

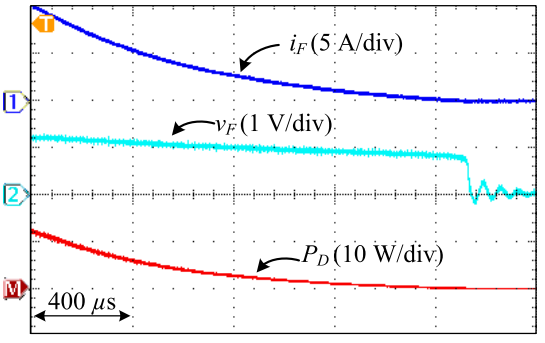


(b)

FIGURE 12. Conduction curves of the semiconductors inside the Si-IGBT device (a) Si transistor. (b) Freewheeling Si diode.



(a)



(b)

FIGURE 13. Conduction curves of the semiconductors inside the Si-IGBT/SiC device (a) Si transistor. (b) Freewheeling SiC diode.

Lastly, through the *polyfit*() function in MATLAB software, we can obtain the approximated model of the switching energy losses versus the current in the devices.

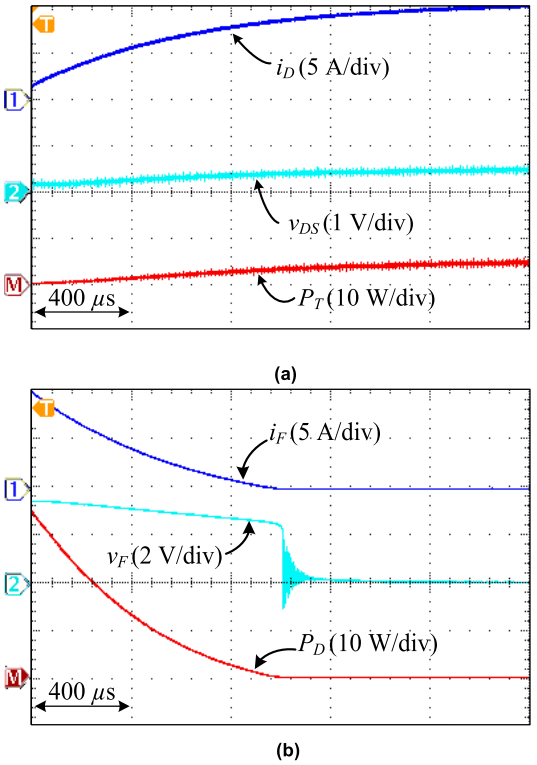


FIGURE 14. Conduction curves of the semiconductors inside the SiC-MOSFET device (a) SiC transistor. (b) Freewheeling SiC body diode.

D. MEASURING CONDUCTION LOSSES

In this paper, the uncovering of the conduction losses was carried out by simply measuring and registering the data of the current in each device (i_C, i_D, and i_F) and its respective forward voltage drop (v_{CE}, v_{DS}, and v_F) in the DPT set-up shown in Fig. 7. Accordingly, the conduction loss of the transistors was measured in T2 by slowly ramping up the current in L up to 10 A. Conversely, the conduction loss caused by the diodes was measured in D1 by allowing the current stored in L to discharge through D1's forward resistor. Consequently, the conduction loss curves of the Si-IGBT, Si-IGBT/SiC, and SiC-MOSFET were obtained and portraited in Fig. 12, Fig. 13, and Fig. 14, respectively.

E. COMPARISON OF CONDUCTION LOSSES

To contrast our results with many commercially available devices, we have collected the conduction loss data of various manufacturers' Si IGBTs, SiC MOSFETs, and SiC diodes in Table 4, Table 5, and Table 6, respectively. Also, with the acquired experimental data points on conduction power loss of transistors and diodes, we can build a model of the power dissipation (P_T and P_D) versus the current in the devices, which is plotted in Fig. 15. In Fig. 15 (a), we can observe that the power dissipation of the SiC-MOSFET is lower than those on the Si-based counterparts. Naturally, as observed in Table 4 and Table 5, SiC MOSFETs with larger $R_{DS(on)}$ would have their power dissipation increased, matching the power dissipation of most Si IGBTs. On the other hand, as seen in Fig. 15 (b), the power dissipation in the body diode of the SiC-MOSFET is much larger than those in the Si and SiC diodes. Besides that, Table 5 shows us that even SiC MOSFETS with low $R_{DS(on)}$ would also have considerable high-power dissipation in their body diodes. This is because, unlike IGBT devices, the applied voltage at the gate terminal has a significant impact on the conduction loss of the MOSFET's body diode. Therefore, the effect on the body diode's conduction loss must be taken into consideration during the design stage of MRs operating with commutation schemes with reduced complexity for the charging mode. Power loss and efficiency of the SiC MOSFET's body diode can change with different gate voltage applied at the upper transistor, at the expense of increased commutation complexity of bidirectional switches.

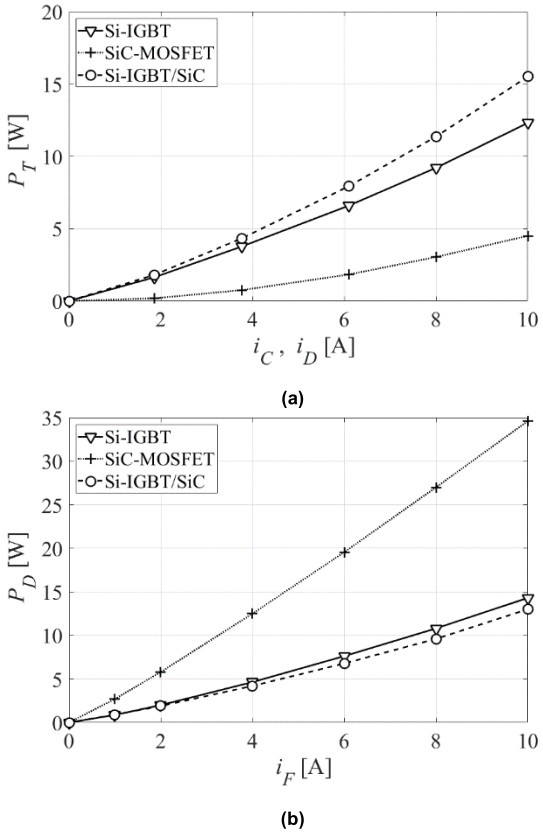


FIGURE 15. Comparison of conduction power losses at different currents i_C, i_D, and i_F. (a) Dissipation through transistors. (b) Dissipation through diodes.

IV. COMPARISONS OF ENERGY AND POWER LOSSES IN THE MATRIX RECTIFIERS THROUGH THE SIMULATOR

In this section we will simulate energy and power losses, and efficiency of the following MR configurations:

i) MR-I: comprised of the Si-IGBT (see Fig. 3 (a))
ii) MR-II: comprised of the Si-IGBT/SiC (see Fig. 3 (b))
iii) MR-III: comprised of the SiC-MOSFET (see Fig. 3 (c))
iv) MR-IV: comprised of the SiC-MOSFET and the Si-IGBT (see Fig. 3 (d))

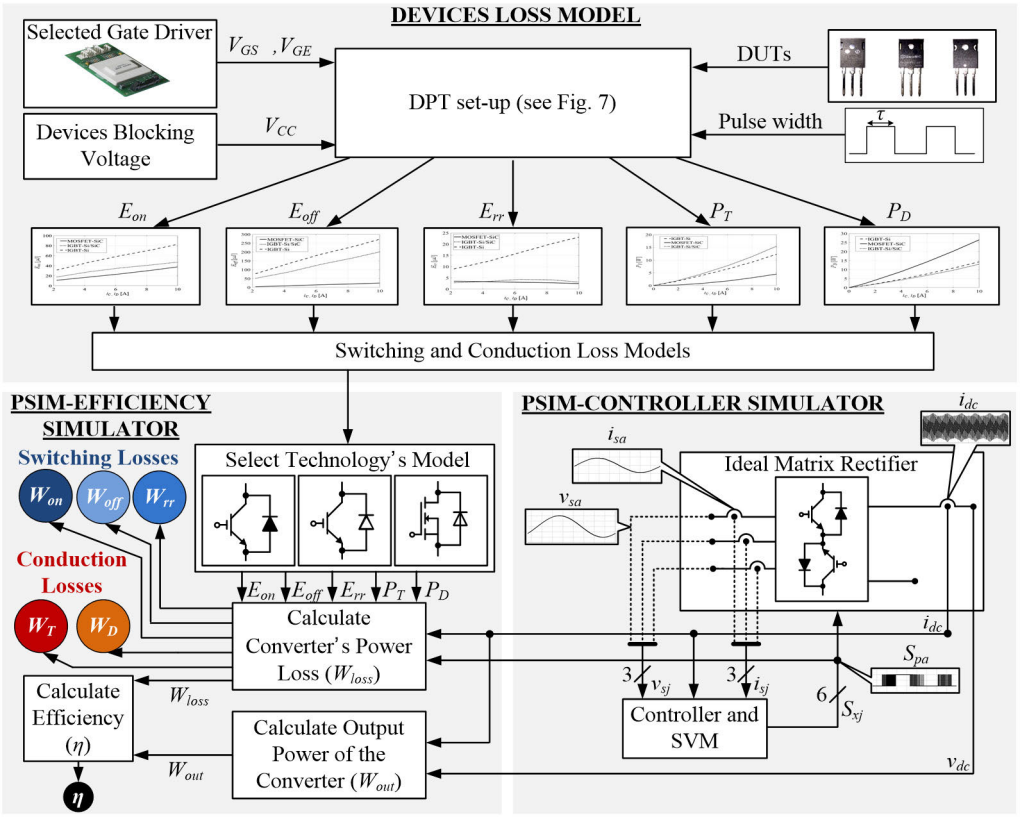


FIGURE 16. Complete simulator's block diagram for the matrix rectifier with different semiconductor technologies as bidirectional switches.

TABLE 4. Datasheet's typical $V_{CE(sat)}$, typical V_F , P_T and P_D of commercial Si IGBT devices. V_{CES} = 1200 V, $V_{GE(on)}$ = 15 V, T_j = 25 °C

Manufacturer	Part number	Si IGBT		Si reverse diode	
		$V_{CE(sat)}$	P_T at I_C = 30 A	V_F	P_D at I_F = 30 A
Littelfuse	IXDH30N120D1	2.4 V (I_C = 30 A)	70 W	2.5 V (I_F = 30 A)	75 W
Infineon	IKW25N120H3	2.05 V (I_C = 25 A)	65 W	1.8 V (I_F = 12.5 A)	76 W
ON	NGTB40N120FL2WG	2 V (I_C = 40 A)	56 W	2 V (I_F = 40 A)	55 W
ROHM	RGS80TSX2DHR	1.7 V (I_C = 40 A)	48 W	1.65 V (I_F = 40 A)	44 W
SEMIKRON	SKM50GB12V	1.84 V (I_C = 50 A)	49 W	2.22 V (I_F = 50 A)	58 W

TABLE 5. Datasheet's typical $R_{DS(on)}$, typical V_{SD}, P_T and P_D of commercial SiC MOSFET devices. V_{DSS} = 1200 V, T_j = 25 °C

Manufacturer	Part number	SiC MOSFET		SiC body diode	
		$R_{DS(on)}$	P_T at I_D = 30 A ($V_{GS(on)}$ =18~20 V)	V_F	P_D at I_F = 30 A ($V_{GS(off)}$ = 0 V)
Littelfuse	LSIC1M0120E0080	80 mΩ (I_D = 20 A)	75 W	3.8 V (I_F = 10 A)	165 W
Infineon	IMW120R045M1	45 mΩ (I_D = 20 A)	35 W	4.1 V (I_F = 20 A)	132 W
ON	NTHL040N120SC1	39 mΩ (I_D = 35 A)	39 W	3.8 V (I_F = 17.5 A)	124 W
ROHM	SCT3080KL	80 mΩ (I_D = 10 A)	68 W	3.2 V (I_F = 10 A)	144 W
SEMIKRON	SK45MH120TSCp	45 mΩ (I_D = 22 A)	40 W	4.1 V (I_F = 22 A)	128 W
CREE	C2M0040120D	40 mΩ (I_D = 40 A)	41 W	3.3 V (I_F = 20 A)	116 W

TABLE 6. Datasheet's typical V_F and P_D of commercial SiC diodes. V_R = 1200 V, T_j = 25 °C

Manufacturer	Part number	SiC diode	
		V_F	P_D at I_F = 30 A
Littelfuse	LSIC2SD120E30CC	1.5 V (I_F = 15 A)	52W
Infineon	IDW40G120C5B	1.4 V (I_F = 20 A)	48 W
ON	FFSH40120ADN-F155	1.4 V (I_F = 20 A)	50 W
ROHM	SCS240KE2	1.4 V (I_F = 20 A)	49 W
SEMIKRON	SKKE60S12	1.4 V (I_F = 80 A)	32 W
CREE	C4D40120D	1.5 V (I_F = 20 A)	56 W

TABLE 7. Circuit parameters in the simulator and experiments

Parameter/Item	Value/Model
Peak phase voltage (V_s)	100 V
Input line frequency (f)	60 Hz
Output power (W_{out})	525 W
Input inductor (L_f)	2.5 mH
Input capacitor (C_f)	60 μF
Output inductor (L_o)	2 mH
Output capacitor (C_o)	40 μF
Load resistor (R)	21 Ω
Simulator sampling time (T_{sim})	0.1 μs

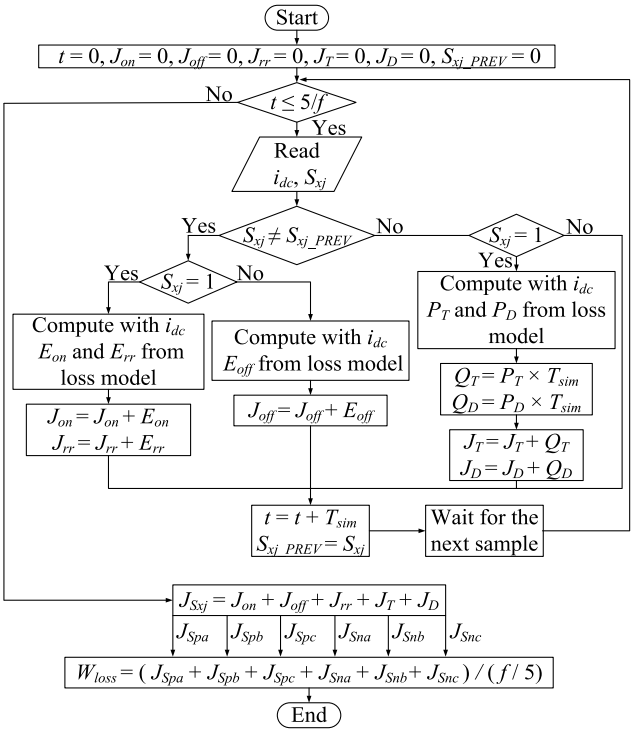


FIGURE 17. (a) Flowchart for the calculation of the semiconductor power loss in the matrix rectifier. (b) Flowchart for the output power calculation.

To implement the energy and power loss simulator of the MR, the circuit diagram shown in Fig. 1 was simulated by the

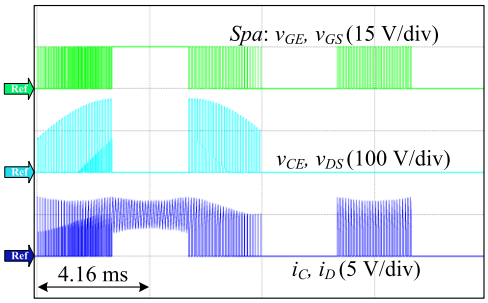


FIGURE 18. Switching waveforms of the lower IGBT/MOSFET inside S_{pa} during a fundamental period at f_{sw} = 10 kHz.

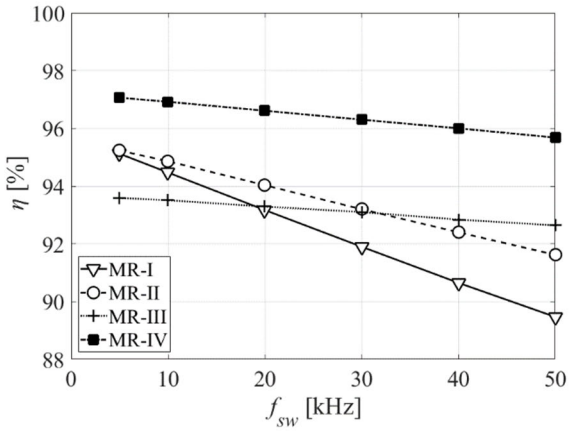


FIGURE 19. Simulated efficiency comparison of the four MR configurations versus f_{sw}.

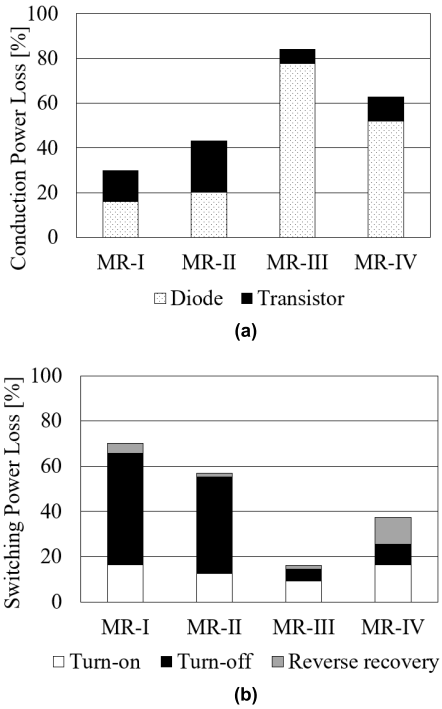


FIGURE 20. Power loss breakdown in each matrix rectifier as a percentage of total power loss Wl_{oss} per converter at f_{sw} = 50 kHz.

PSIM software with the circuit parameters listed in Table 7. The complete block diagram of the simulator employed in this paper is displayed in Fig. 16 and the flowchart of the algorithm used to determine the energy and power losses in

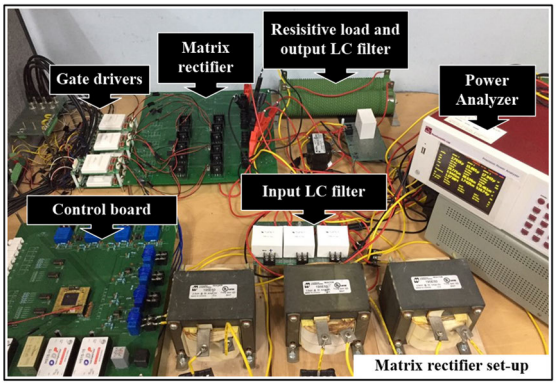


FIGURE 21. Experimental set-up of the various MR configurations for efficiency comparison.

any of the four MR configurations is illustrated in Fig. 17 (a). The algorithm's computations were performed during five fundamental periods, where the partial energy losses of the six bidirectional switches S_{xj} were progressively added and stored in J_{on}, J_{off}, J_{rr}, J_T, and J_D. Thereafter, the total power losses in the matrix rectifier W_{loss} was obtained by dividing the total accumulated energy loss by its time of accumulation. Similarly, Fig. 17 (b) presents a straightforward algorithm to determine the MR's output power W_{out}. Thus, we can obtain the efficiency of the MR through the following expression:

$$\eta = \frac{W_{out}}{W_{out} + W_{loss}} \times 100\%. \tag{6}$$

The waveforms of the gate voltage, blocking voltage, and the current flowing through the lower transistor in S_{pa} during a fundamental period are depicted in Fig. 18. We can observe that, as indicated in Fig. 4, the current flows only in one direction during the charging mode of the MR. Note that, unlike VSCs, the blocking voltage of the switches is not fixed but it varies. In this simulator, we approximate 100 V as the blocking voltage during commutations to obtain the power losses and efficiency in every matrix rectifier. Through this assumption, we expect to find rough estimates of the behavior of the efficiency and the breakdown of energy and power losses in the MR configurations introduced in this section.

Fig. 19 shows the efficiency comparison of the four MR configurations in terms of switching frequency f_{sw}. These outcomes were obtained by (6) and the algorithm presented in Fig. 17. It is observed that, at 5 kHz switching frequency, the proposed switch in the MR-IV is superior to the other configurations with nearly 97% efficiency. Yet, as the switching frequency increases, its efficiency decreases at a slightly higher rate compared to the MR-III. The conduction loss caused by the body diode, together with the off-state gate voltage in its respective transistor for the sake of a simple commutation scheme, causes the MR-III to underperform at 5 kHz switching frequency. Nevertheless, its rate of change with the increasing switching frequency is the smallest among every configuration. This suggests that the MR-III could outperform the MR-IV at switching frequencies much higher than 50 kHz. The MR–I and MR–II configurations have comparable efficiencies of around 95% at 5 kHz switching frequency. However, the MR-I and the MR-II have dramatically increased losses with the increasing switching frequency because of the Si devices switching.

To understand the behavior of the power losses within the presented MR configurations, Fig. 20 shows the power loss breakdown in terms of conduction and switching losses within the MRs at $f_{sw} = 50$ kHz. The breakdown was acquired by isolating the partial power losses W_{on}, W_{off}, W_{rr}, W_T, and W_D as a percentage of the total losses in each converter W_{loss}. We can observe that most losses in the MR-I come from switching losses. The MR-II, thanks to the incorporated SiC diode, has reduced switching losses and balances out conduction and switching losses within the converter. Notice that both converters have significantly increased turn-off losses because of the tail currents in IGBTs. In the MR-III, we can observe that the body diodes are responsible for nearly 80% of the total losses in the converter while the transistor's conduction loss and the total switching power losses remained low. In the case of the MR-IV with the proposed bidirectional switch, the Si diode's conduction loss accounts for nearly 50 % of the total power loss while the transistor's conduction loss and the switching losses have comparable values. We can agree that the MR-III has the best switching power loss performance. Nevertheless, because of the impoverished performance of the SiC-MOSFET's body diode for simple commutations in MRs, the MR-IV is the fittest to operate within the presented switching frequencies as observed in Fig. 19.

V. EXPERIMENTAL VALIDATION

The experimental measurements of the efficiency and power loss in the four MR types are presented in this section. The comparisons are based on experimental measurements via the power analyzer PPA5500 to the set-up shown in Fig. 21.

The experimental waveforms showing the source current i_{sa}, the output current i_{dc}, and the gate voltage of S_{pa} are shown in Fig. 22 for every configuration at 5 kHz and 50 kHz switching frequency.

The experimental efficiency comparison of the four MRs is depicted in Fig. 23. The resemblance with the simulated results of Fig. 19 is evident. However, we must address some of the discrepancies displayed in the experimental figure. First, the junction temperature T_j of the devices in experiments is higher than the 25 °C utilized for the DPT and the simulator. Moreover, this temperature increases further with the switching frequency. Thus, the Si-based transistors and diodes experience reduced conduction power losses at higher temperatures and low currents as observed in the datasheets IXA37IF1200HJ and GA35XCP12, which explains the slight improvement over the simulated results in MR-I and MR-II. Second, the blocking voltage of the transistors in the MR is not constant but varies from 0 V to 180 V as observed in Fig. 18. Commutations at low blocking voltages increase significantly the gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and drain-source capacitance C_{ds} inside SiC MOSFETs as depicted in the datasheet

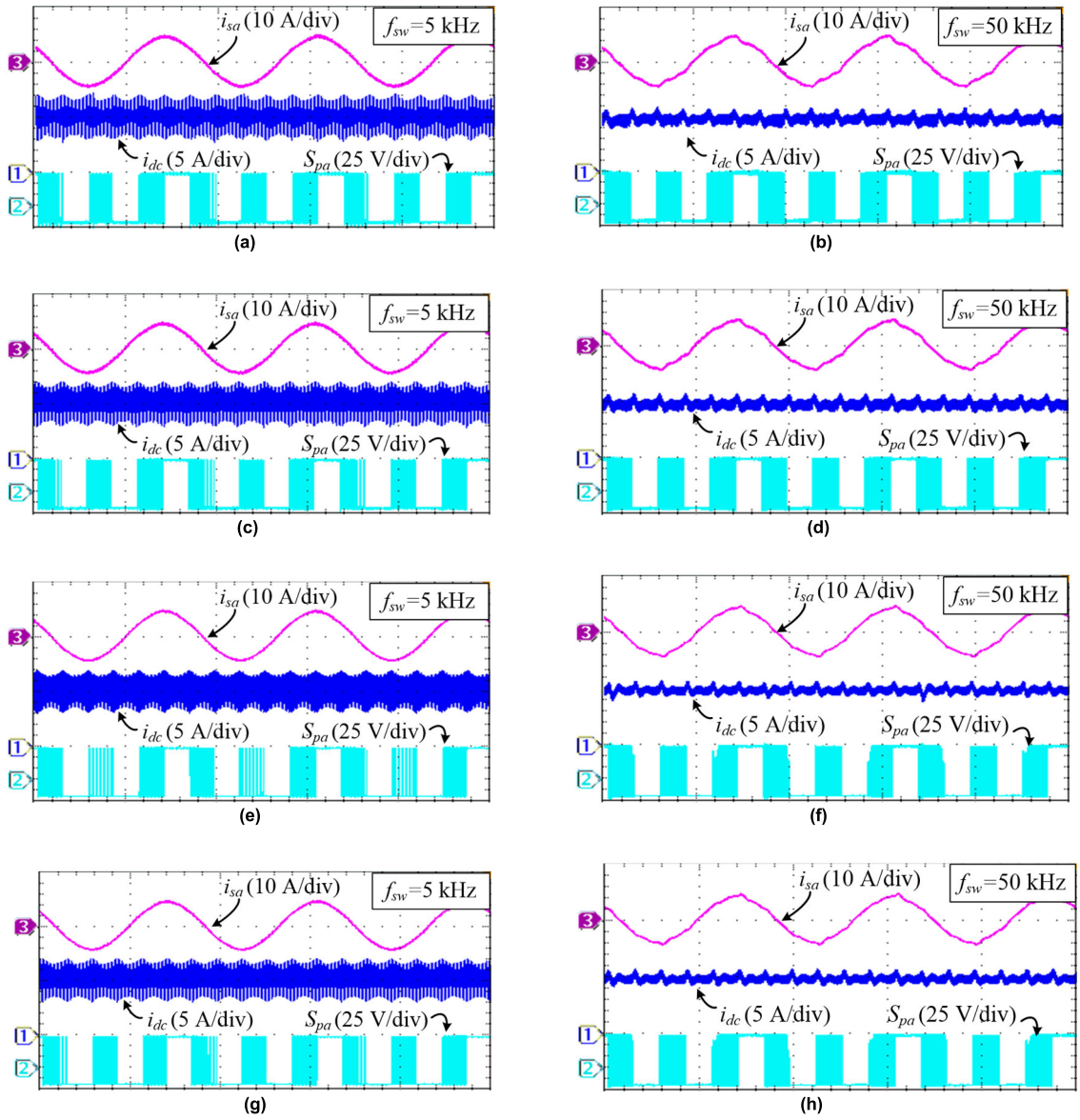


FIGURE 22. Experimental waveforms. (a) MR-I at f_{sw} = 5 kHz. (b) MR-I at f_{sw} = 50 kHz. (c) MR-II at f_{sw} = 5 kHz. (d) MR-II at f_{sw} = 50 kHz. (e) MR-III at f_{sw} = 5 kHz. (f) MR-III at f_{sw} = 50 kHz. (g) MR-IV at f_{sw} = 5 kHz. (h) MR-IV at f_{sw} = 50 kHz.

SCT3040KL. Because of the high switching speed in SiC devices, increments in these parasitic elements could rise the switching power losses in the devices, which reveals the slight increase of the slope in the MR-III and the MR-IV in Fig. 23 [21]. Despite these minor divergences, the proposed MR-IV exhibits the best efficiency throughout the frequency range shown in Fig. 19 and Fig. 23 and would continue having the best performance for switching frequencies much higher than 50 kHz.

Comparisons of total power losses per bidirectional switch normalized to the total power loss of the bidirectional switches inside the MR-III and the MR-I are plotted in Fig. 24 (a) and (b), respectively. We observe in Fig. 24 (a) that, at 5 kHz switching frequency, the bidirectional switch in the MR-IV dissipates 31%, 39%, and 53% less total power

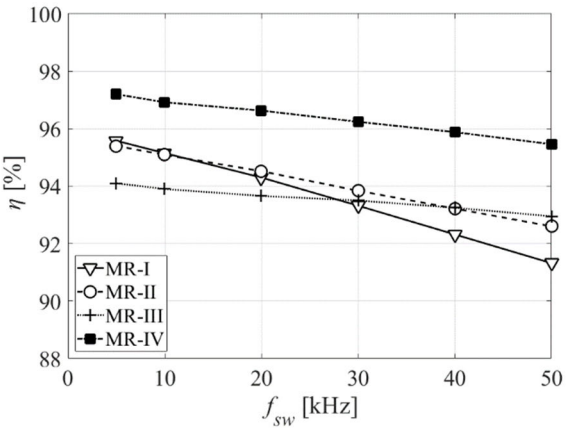


FIGURE 23. Experimental efficiency comparison of the four MR configurations versus f_{sw}.

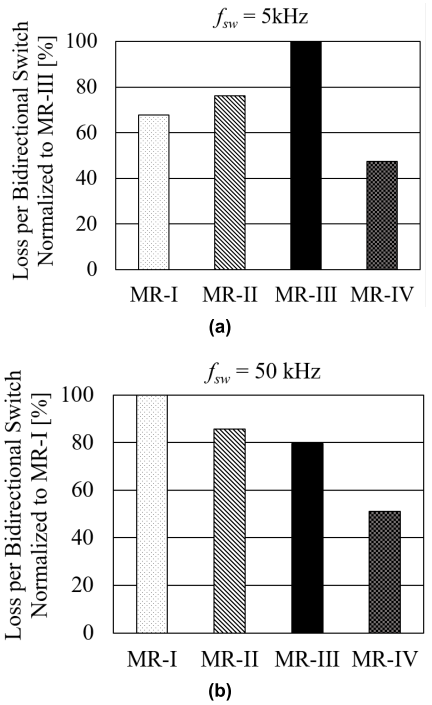


FIGURE 24. Total losses per bidirectional switch in the four MR configurations. (a) Losses normalized to the loss in the MR-III at $f_{sw} = 5$ kHz. (b) Losses normalized to the loss in the MR-I at $f_{sw} = 50$ kHz.

than the switches in the MR-I, the MR-II, and the MR-III, respectively. On the other hand, with an increased switching frequency of 50 kHz, the proposed switch dissipates 48%, 38%, and 35% less than its counterparts in the MR-I, the MR-II, and the MR-III, respectively. It is important to note that, as for today, the SiC technologies such as SiC MOSFETs typically cost between four up to forty times more than equally rated Si IGBTs. In fact, the cost of SiC MOSFETs increases exponentially with the rated current of the device, while the Si IGBTs' cost increases linearly at a slower pace with the rated current [26]. Thus, the proposed bidirectional switch results in a cost-effective solution that cuts down the cost of pure SiC-based devices while maintaining high efficiency in the MR. Clearly, the MR-III operated with complex four-step commutations, would have its performance improved because of the reduced conduction loss in the body diodes thanks to the positive $V_{GS(\text{on})}$. However, this benefit comes at the expense of increased hardware and software complexity and the additional SiC MOSFET compared to the proposed bidirectional switch.

VI. CONCLUSION

In this paper, a hybrid configuration for the bidirectional switches contained in matrix rectifiers was proposed. The proposed configuration was compared to conventional bidirectional switches regarding the converter's efficiency and power losses. To attain a quantitative comparison, the discrete power devices contained in the bidirectional switches were tested using the double-pulse test, from which their switching energy loss characteristics were obtained. Consequently, a simulator was implemented to distinguish the energy loss distribution inside the devices of the matrix rectifier operating from 5 kHz up to 50 kHz switching frequency. The proposed configuration was demonstrated, through simulations and experiments, to be the most cost-effective solution for matrix rectifiers with simple commutation scheme. For instance, compared to the pure SiC MOSFET configuration, the proposed bidirectional switch has significantly reduced cost, and undergoes 53% and 35% less power loss at 5 kHz and 50 kHz switching frequency, respectively.

REFERENCES

[1] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B.-M. Hodge, and B. Hannegan, "Achieving a 100% renewable grid: Operating electric power systems with extremely high levels of variable renewable energy," *IEEE Power Energy Mag.*, vol. 15, no. 2, pp. 61–73, Mar. 2017.

[2] E. Hsieh and R. Anderson, "Grid flexibility: The quiet revolution," *Electr. J.*, vol. 30, no. 2, pp. 1–8, Mar. 2017.

[3] B. M. Grainger, G. F. Reed, A. R. Sparacino, and P. T. Lewis, "Power electronics for grid-scale energy storage," *Proc. IEEE*, vol. 102, no. 6, pp. 1000–1013, Jun. 2014.

[4] V. A. Boicea, "Energy storage technologies: The past and the present," *Proc. IEEE*, vol. 102, no. 11, pp. 1777–1794, Nov. 2014.

[5] M. Farhadi and O. Mohammed, "Energy storage technologies for high-power applications," *IEEE Trans. Ind. Appl*, vol. 52, no. 3, pp. 1953–1961, May/Jun. 2016.

[6] G. Wang, G. Konstantinou, C. D. Townsend, J. Pou, S. Vazquez, G. D. Demetriades, and V. G. Agelidis, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1778–1790, Oct. 2016.

[7] J. Rocaert, R. Capo-Misut, R. S. Munoz-Aguilar, J. I. Candela, and P. Rodriguez, "Control of energy storage systems integration electromechanical batteries and supercapacitors for gri-connected applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1853–1862, Mar./Apr. 2019.

[8] J. D. Boles, Y. Ma, J. Wang, D. Osipov, L. M. Tolbert, and F. Wang, "Converter-based emulation of battery energy storage systems (BESS) for grid applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4020–4032, Jul./Aug. 2019.

[9] M. Su, H. Wang, Y. Sun, J. Yang, W. Xiong, and Y. Liu, "AC/DC matrix converter with an optimized modulation strategy for V2G applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5736–5745, Dec. 2013.

[10] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Operation modes for the electric vehicle in smart grids and smart homes: Present and proposed modes," *IEEE Trans. Veh. Technol.*, vol. 65, no. 3, pp. 1007–1020, Mar. 2016.

[11] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC-DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.

[12] X. Wang, C. Jiang, B. Lei, H. Teng, H. K. Bai, and J. L. Kirtley, "Power-loss analysis and efficiency maximization of a silicon-carbide MOSFET-based three-phase 10-kW bidirectional EV charger using Variable-DC-Bus control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 880–892, Sep. 2016.

[13] J.-C. Kim and S. Kwak, "Direct power control method with minimum reactive power reference for three-phase AC-to-DC matrix rectifiers using space vector modulation," *IEEE Access*, vol. 7, pp. 67515–67525, 2019.

[14] K. You, D. Xiao, M. F. Rahman, and M. N. Uddin, "Applying reduced general direct space vector modulation approach of AC–AC matrix converter theory to achieve direct power factor controlled three-phase AC–DC matrix rectifier," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 2243–2257, May/Jun. 2014.

[15] B. Feng, H. Lin, X. Wang, X. An, and B. Liu, "Optimal zero-vector configuration for space vector modulated AC-DC matrix converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2012, pp. 219–297.

[16] A. Anurag, S. Acharya, and S. Bhattacharya, "An accurate calorimetric loss measurement method for SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1644–1656, Jun. 2020.
[17] A. N. AN1403. (2014). *Determining Switching Losses of SEMIKRON IGBT Modules*. [Online]. Available: https://www.semikron.com
[18] J. Kim, D. Shin, and S.-K. Sul, "A damping scheme for switching ringing of full SiC MOSFET by air core PCB circuit," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4605–4615, Jun. 2018.
[19] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.
[20] M. H. Ahmed, M. Wang, M. A. S. Hassan, and I. Ullah, "Power loss model and efficiency analysis of three-phase inverter based on SiC MOSFETs for PV applications," *IEEE Access*, vol. 7, pp. 75768–75781, Jun. 2019.
[21] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
[22] S. Hazra, A. De, L. Cheng, and J. Palmour, "High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.
[23] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019.
[24] A. N. 14103EBY01. (2014). *SiC Power Devices and Modules*. [Online]. Available: https://www.rohm.com
[25] P. J. Grbovic, F. Gruson, N. Idir, and P. L. Moigne, "Turn-on performance of reverse blocking IGBT (RB IGBT) and optimization using advanced gate driver," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 970–980, Apr. 2010.
[26] A. Deshpande and F. Luo, "Practical design considerations for a Si IGBT+ SiC MOSFET hybrid switch: Parasitic interconnect influences, cost, and current ratio optimization," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 724–737, Jan. 2019.

BRYAN GUTIERREZ received the B.S. degree in electronics engineering from the Department of Electronics Engineering, Pontificia Universidad Católica del Perú, Lima, Peru, in 2012, and the M.S. degree in electrical and electronics engineering from the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul, South Korea, in 2017. He is currently a Research Assistant with the Power Electronics and Renewable Energy Systems laboratory, Chung-Ang University. His research interests include the control of modular multilevel converters, analysis of hybrid active power filters, and power converters based on wide-bandgap semiconductors.

SANG-SHIN KWAK (Member, IEEE) received the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2005. From 1999 to 2000, he was a Research Engineer with LG Electronics, Changwon, South Korea. He was also with the Whirlpool Research and Development Center, Benton Harbor, MI, USA, in 2004. From 2005 to 2007, he was a Senior Engineer with the Samsung SDI Research and Development Center, Yongin, South Korea. From 2007 to 2010, he was an Assistant Professor with Daegu University, Gyeongsan, South Korea. Since 2010, he has been with Chung-Ang University, Seoul, South Korea, where he is currently a Professor. His research interests include topology design, modeling, control, and analysis of ac/dc, dc/ac, and ac/ac power converters, including resonant converters for adjustable-speed drives and digital display drivers, and modern control theory applied to digital-signal-processing-based power electronics.