Article

Comparative Study on the Separate Extraction of Interface and Bulk Trap Densities in Indium Gallium Zinc Oxide Thin-Film Transistors Using Capacitance–Voltage and Current–Voltage Characteristics

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Abstract: The interface and bulk trap densities were separately extracted from self-aligned top-gate (SA-TG) coplanar indium gallium zinc oxide (IGZO) thin-film transistors (TFTs) using the low-frequency capacitance–voltage (*C–V*) characteristics and space-charge-limited current (SCLC) under the flat-band condition. In the method based on the *C–V* curve, the energy distribution of the interface trap density was extracted using the low-frequency *C–V* characteristics, and that of the bulk trap density was obtained by subtracting the density of interface trap states from the total subgap density of states (DOS) at each energy level. In the SCLC-based method, the energy distribution of the bulk trap density was extracted using the SCLC under the flat-band condition at high drain-to-source voltages, and that of the interface trap density was obtained by subtracting the density of bulk trap components from the total subgap DOS at each energy level. In our experiments, the two characterization techniques provided very similar interface and bulk trap densities and showed that approximately 60% of the subgap states originate from the IGZO/SiO$_2$ interface at the conduction band edge in the fabricated IGZO TFTs, although the two characterization techniques are based on different measurement data. The results of this study confirm the validity of the characterization techniques proposed to separately extract the interface and bulk trap densities in IGZO TFTs. Furthermore, these results show that it is important to reduce the density of interface trap states to improve the electrical performance and stability of fabricated SA-TG coplanar IGZO TFTs.

Keywords: IGZO TFT; density of interface trap states; density of bulk trap states; low-frequency *C–V* characteristics; SCLC

1. Introduction

Since the first report in 2004, indium gallium zinc oxide (IGZO) thin-film transistors (TFTs) have attracted significant attention owing to their excellent electrical properties, high uniformity, and easy fabrication processes [1]. Recently, IGZO TFTs have been widely used as the backplanes in active-matrix organic light-emitting diode (AMOLED) displays [2,3]. However, the electrical stability of IGZO TFTs needs to be further improved to broaden their applications. In TFTs fabricated with disordered semiconductors, such as IGZO, it is very important to obtain precise information about the subgap density of states (DOS) because it strongly affects the electrical properties and stabilities of TFTs [4,5]. To date, a number of studies have been conducted to extract the energy distribution of the subgap DOS in IGZO TFTs using various characterization techniques [6–10]. However, most previous studies

reported the total density of subgap states, which includes the bulk trap states and gate insulator/channel interface trap states. Crucially, it is important to find the exact origin of the subgap states to further improve the electrical properties and stabilities of IGZO TFTs. Only a few groups have reported separate values for the interface and bulk subgap DOSs in IGZO TFTs using low-frequency capacitance–voltage (*C*–*V*) characteristics [11] and the space-charge-limited current (SCLC) under the flat-band condition [12]. However, the methods for extracting the trap densities are based on different characterization data, which often yield different results because of differences in the detectability of the different types of subgap states. Hence, it is very important to compare the values of the interface and bulk subgap DOSs obtained using different characterization techniques to confirm the validity of these techniques and the accuracy of the extracted trap densities.

In this study, we compare the energy distributions of the interface and bulk subgap DOSs extracted using low-frequency *C*–*V* characteristics and the SCLC under the flat-band condition. Experiments were conducted using self-aligned top-gate (SA-TG) coplanar IGZO TFTs, which are widely used in the backplanes of commercially available AMOLED televisions [13–15]. Our experimental results demonstrate that the interface and bulk subgap DOSs extracted using the two different techniques exhibit very similar values. The results of this study confirm the accuracy of the extracted interface and bulk subgap DOSs and the validity of the two characterization methods for separately extracting these DOSs in IGZO TFTs.

2. Experimental

Figure 1 shows a schematic of the cross section of the fabricated SA-TG coplanar IGZO TFTs. First, a 250-nm-thick Mo layer was deposited and patterned to form the bottom gate electrode (i.e., a light shielding layer) on a polyimide substrate. Next, a buffer layer (SiN_x/SiO_2 = 30/200 nm) was deposited using plasma-enhanced chemical vapor deposition (PECVD). A 40-nm-thick IGZO layer (In:Ga:Zn = 1:1:1 at.%) was deposited onto the buffer layer by radio-frequency (RF) sputtering. Subsequently, a 140-nm-thick SiO_x layer was deposited by PECVD as a gate insulator, followed by the deposition of a gate metal (Ti/Mo = 30/250 nm). After deposition and patterning of the gate electrode and gate insulator, 300-nm-thick SiO_x and 200-nm-thick SiN_x layers were sequentially deposited as a passivation layer by PECVD and patterned to form via holes. A metal layer (Ti/Al/Ti = 30/600/60 nm) was deposited and patterned as the source and drain electrodes. Finally, the devices were thermally annealed at 340 °C to achieve stable and uniform electrical performance. The channel width (*W*) and length (*L*) of the device were designed to be 10 and 5 μm, respectively. The current–voltage (*I*–*V*) characteristics of the TFTs were measured in the dark at room temperature using an Agilent 4156C semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA).
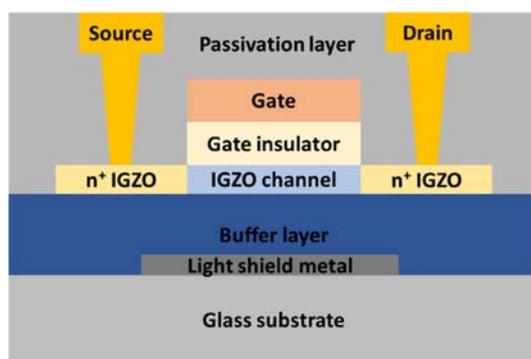
Figure 1. Device structure of the fabricated SA-TG coplanar IGZO TFT.

Figure 2 shows the measurement system for the low-frequency *C*–*V* characteristics of the TFTs. A small alternating current (AC) voltage from the function generator (Agilent 33210A) was superimposed on the direct current (DC) voltage provided by a DC power

supply (Keysight E3646A, Santa Clara, CA, USA), and this voltage signal was applied to the gate electrode of the IGZO TFT located on a probe station. The charging and discharging currents through the source and drain electrodes are expressed as $j\omega C_{GC}A = A/R_f$, where $\omega = 2\pi f$, f is the frequency of the AC signal, C_{GC} is the gate-to-source/drain capacitance, A is the amplitude of the AC signal, and R_f is the feedback resistance [16]. The signal amplitude and the difference in the phase angles of the sinusoidal current and voltage were confirmed using a digital multimeter (Agilent 34401A, Agilent Technologies Inc., Santa Clara, CA, USA) and lock-in amplifier (EG&G 5210, EG&G, Oak Ridge, TN, USA). C_{GC} can be determined from the obtained value for A.
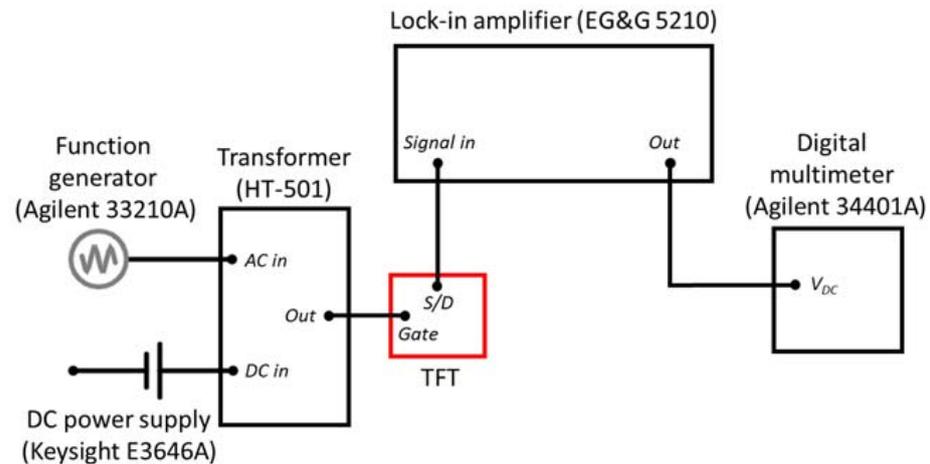
Figure 2. Schematic of the low-frequency *C–V* measurement system.

3. Results and Discussion

Figure 3 shows semilogarithmic and linear-scale transfer curves measured from the fabricated IGZO TFT at a drain-to-source voltage (V_{DS}) of 0.1 V. The electrical parameters extracted from a representative device were as follows: a field-effect mobility (μ_{FE}) of 5.9 cm^2/(V·s), a threshold voltage (V_{TH}) of 0.25 V, and a subthreshold swing (*SS*) of 0.08 V/dec. Here, μ_{FE} was determined using the maximum transconductance method, and V_{TH} was defined as the gate-to-source voltage (V_{GS}) that induces a drain current (I_D) of 1 nA at V_{DS} = 0.1 V [17]. Figure 4 shows the *C–V* characteristics measured between the gate and source/drain electrodes of the fabricated IGZO TFTs at a low frequency of 103 Hz, where the value of the measurement frequency was chosen to minimize the interference from the power-line harmonics, as per the results of previous reports for a lock-in amplifier [18].
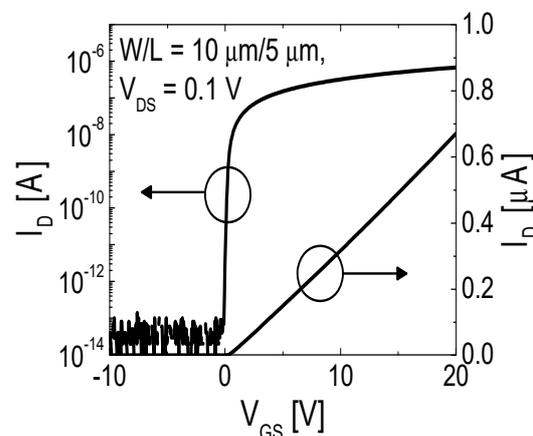
Figure 3. Transfer curve (logarithmic and linear scale) measured from the fabricated IGZO TFT at V_{DS} = 0.1 V.
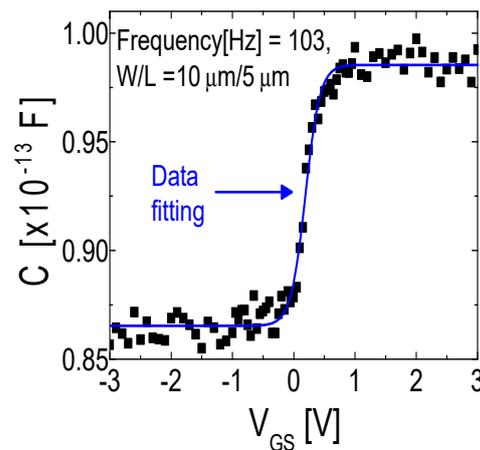
Figure 4. *C–V* curve measured between gate and source/drain electrodes of the fabricated IGZO TFT at 103 Hz.

In the technique based on the *C–V* curve, the total density of subgap states is systematically decomposed into interface and bulk trap densities using low-frequency *C–V* data. The Poisson equation and Gauss's law are numerically solved, and the interface trap density is extracted by fitting the calculated *C–V* curve to the measured one [11,19]. The density of the bulk trap components in the IGZO channel layer is determined by subtracting the density of the interface trap states from the total density of subgap trap states extracted using the transfer curves measured from the TFTs [20]. This technique involves the derivation of two independent equations to solve for the interface trap capacitance (C_{it}) and channel capacitance (C_S). The first equation was obtained from the equivalent circuit in Figure 5a, in which C_{GC} is modeled as

$$\frac{1}{C_{GC}} = \frac{1}{C_{OX}} + \frac{1}{C_S + C_{it}},\tag{1}$$

where C_{OX} is the capacitance of the gate insulator [11,19]. From Equation (1), C_{it} can be re-expressed as

$$C_{it} = \frac{C_{GC}C_{OX}}{C_{OX} - C_{GC}} - C_s = \frac{C_{GC}C_{OX}}{C_{OX} - C_{GC}} - (C_D + C_n),\tag{2}$$

where $C_S = C_D$ (the capacitance of the trapped carriers) + C_n (the capacitance of the free carriers) [19]. The second equation for C_{it} and C_S was derived using the Poisson equation and Gauss's law [21]. Figure 5b shows the energy band diagram of the fabricated IGZO TFTs along the channel depth direction. Applying the Poisson equation along the *x* direction from the channel/gate dielectric interface in Figure 5b, we obtain

$$\left.\frac{\partial \varphi}{\partial x}\right|_{x=0} = \left[\frac{2q}{\varepsilon_0 \varepsilon_{IGZO}} \int_0^{\varphi_S} (n_{free} + n_{trap})d\varphi\right]^{1/2},\tag{3}$$

where ε_0 is the vacuum permittivity, ε_{IGZO} is the dielectric constant of IGZO, q is the electronic charge, φ is the electrostatic potential, and n_{free} and n_{trap} are the densities of free and localized trapped electrons, respectively [22].

The trapped charge per unit area (Q_D) and free charge per unit area (Q_n) are expressed by

$$Q_D = q\int_0^{t_{IGZO}} n_{trap}dx = -q\int_0^{\varphi_S} \frac{n_{trap}}{d\varphi/dx}d\varphi,\tag{4}$$

$$Q_n = q\int_0^{t_{IGZO}} n_{free}dx = -q\int_0^{\varphi_S} \frac{n_{free}}{d\varphi/dx}d\varphi.\tag{5}$$

Adding both sources of charge,

$$Q_D + Q_n = -q\int_0^{\varphi_S} \frac{1}{d\varphi/dx}(n_{free} + n_{trap})d\varphi.\tag{6}$$

Applying Gauss's law to the channel/gate dielectric interface,

$$\varepsilon_0 \varepsilon_{\text{IGZO}} E_S = -\varepsilon_0 \varepsilon_{\text{IGZO}} \left. \frac{\partial \varphi}{\partial x} \right|_{x=0} = \frac{C_{\text{OX}}(V_{\text{GS}} - V_{\text{FB}} - \varphi_S)}{WL} - Q_{\text{it}}, \tag{7}$$

where Q_{it} is the interface trap charge per unit area, V_{FB} is the flat-band voltage, and E_S is the electric field at the IGZO/gate dielectric interface. By substituting Equations (3) and (7) into Equation (6) and differentiating both sides of the equation with respect to φ_S, we obtain the second equation for C_{it} and C_S as

$$\begin{aligned} C_S = C_D + C_n \quad &= WL\left(\frac{dQ_D}{d\varphi_S} + \frac{dQ_n}{d\varphi_S}\right) \\ &= \frac{1}{2\eta}\left[C_{\text{OX}}\left(\frac{dV_{\text{GS}}}{d\varphi_S} - 1\right) + C_{\text{it}}\right], \end{aligned} \tag{8}$$

where η is a fitting factor [11,19]. The surface potential φ_S in Equation (8) can be expressed as a function of V_{GS} using the transfer characteristics obtained from the TFTs [23]:

$$\varphi_S = V_{\text{th}} \int_{V_{\text{FB}}}^{V_{\text{GS}}} \left(\frac{\partial \ln I_D(V_{\text{GS}})}{\partial V_{\text{GS}}}\right) dV_{\text{GS}}, \tag{9}$$

where V_{th} is the thermal voltage. Then, we can obtain an equation for C_{it} by simultaneously solving Equations (2) and (8) [19]:

$$C_{\text{it}} = \frac{2\eta - 1}{2\eta + 1} \frac{C_{\text{GC}} C_{\text{OX}}}{C_{\text{OX}} - C_{\text{GC}}}, \tag{10}$$

and the interface trap density (D_{it}) can be expressed as

$$D_{\text{it}} = \frac{C_{\text{it}}}{q^2 WL}. \tag{11}$$
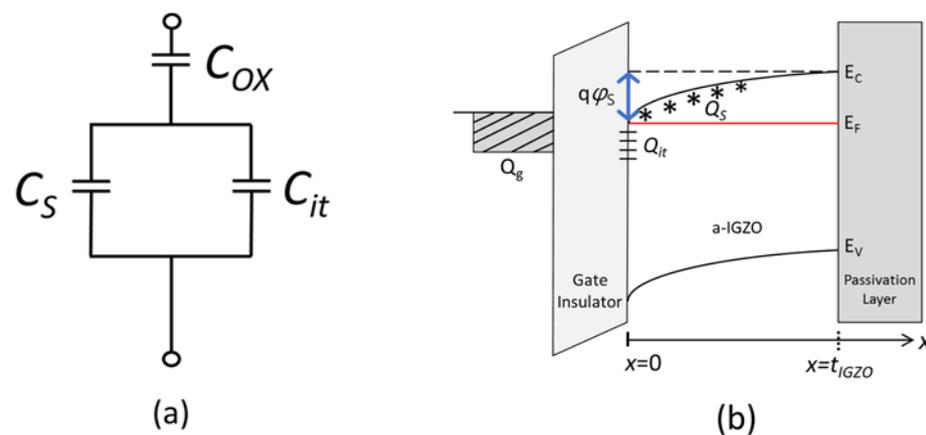
Figure 5. (**a**) Equivalent circuit for C_{GC} with C_{OX}, C_S, and C_{it}; (**b**) Energy band diagram along the channel depth direction.

By substituting the low-frequency *C–V* data measured from the TFT in Figure 4 into Equations (10) and (11), the energy distribution of the interface trap states, $D_{\text{it}}(E)$, is calculated as shown in Figure 6a. To determine the density of bulk trap components in the IGZO TFT, we calculated the total density of subgap trap states, which includes the interface and bulk trap states, from the subthreshold characteristics of the IGZO TFT using the following equation and subtracted D_{it} from it:

$$\begin{aligned} D_{\text{it}} + t_S N_b \quad &= \frac{C_{\text{OX}}}{q^2 WL}\left(\frac{q}{kT \ln 10} SS - 1\right) \\ &= \frac{C_{\text{OX}}}{q^2 WL}\left(\frac{q}{kT}\left(\frac{\partial \ln I_{D,\text{sub}}}{\partial V_{\text{GS}}}\right)^{-1} - 1\right), \end{aligned} \tag{12}$$

where t_S is the thickness of the channel layer, N_b is the density of bulk trap states, k is the Boltzmann constant, T is the measurement temperature, and $I_{D,\text{sub}}$ is the subthreshold drain current [20,24]. Figure 6b depicts the energy distributions of the total subgap DOS

$D_{\text{it}} + t_{\text{S}} \times N_{\text{b}}$, D_{it}, and $t_{\text{S}} \times N_{\text{b}}$ extracted from the fabricated IGZO TFT. Figure 6b shows that approximately 57% of all subgap states are interface trap states at the conduction band edge (E_{C}) in the fabricated SA-TG coplanar IGZO TFT.
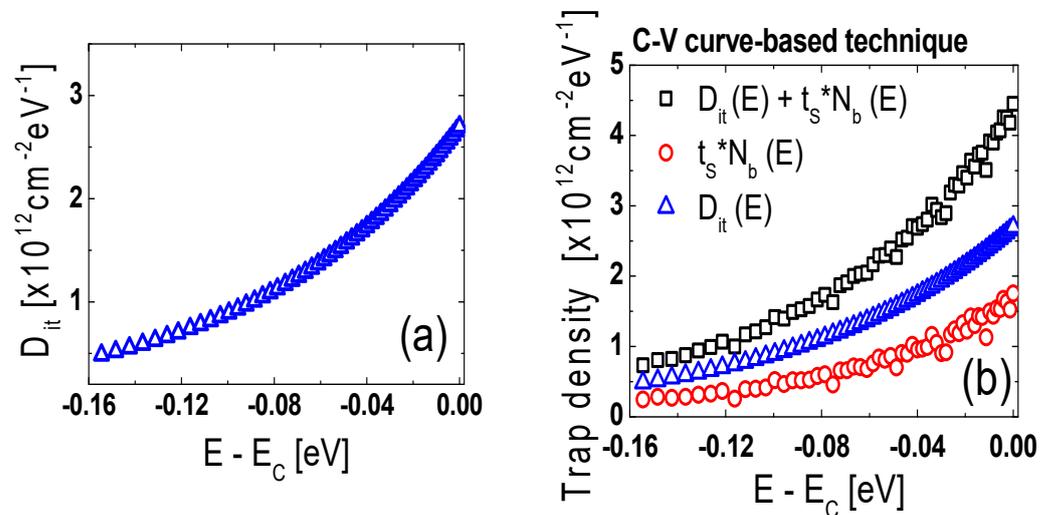
Figure 6. (**a**) Energy distribution of the density of interface trap states D_{it} obtained using the technique based on the *C–V* curve. (**b**) Energy distributions of the total subgap DOS $D_{\text{it}} + t_{\text{S}} \times N_{\text{b}}$, D_{it}, and the density of bulk trap components $t_{\text{S}} \times N_{\text{b}}$ obtained using the technique based on the low-frequency *C–V* curve.

In the SCLC-based technique, the total density of subgap states is systematically decomposed into interface and bulk trap densities using SCLC data [12,25]. In this method, we determined the energy distribution of N_{b} in the IGZO TFT from the SCLC measured under the flat-band condition at a high V_{DS} [25]. The density of interface traps in the IGZO channel layer was determined by subtracting the density of bulk trap components from the total density of subgap trap states extracted using the transfer curves measured from the TFTs.

Figure 7 shows a log–log plot of the I_{D}–V_{DS} curve measured under the flat-band condition after applying the flat-band voltage ($V_{\text{FB}} = -0.05$ V) to the gate terminal of the TFT. In Figure 7, the measured data can be fitted to the relation $I_{\text{D}} \propto V_{\text{DS}}{}^{m}$, where $m{\sim}1$ at low V_{DS} (<5.6 V) and $m{\sim}4.04$ at high V_{DS} (>5.6 V). The value of $m{\sim}1$ at $V_{\text{DS}} < 5.6$ V indicates that the *I–V* characteristics are ohmic at low V_{DS}, and that of 4.04 at $V_{\text{DS}} > 5.6$ V indicates that the trap-limited SCLC due to the exponential energy distribution of the trap states within the semiconductor is the dominant current conduction mechanism at high V_{DS} [26]. An SCLC occurs in semiconductors with low carrier mobilities when the injected charge density exceeds the density of intrinsic free carriers within the semiconductor [27]. From the trap-limited SCLC model, the energy distribution of the density of trap states is exponential and given by

$$N_{\text{b}}(E) = N_{\text{t}} \exp\left(\frac{E - E_{\text{C}}}{kT_{\text{t}}}\right) \quad where, \ \ T_{\text{t}} = \gamma T. \tag{13}$$

The resulting SCLC flowing through the bulk region of the semiconductor between the source and drain terminals under the flat-band condition in the TFT structure is expressed as

$$I = qW t_{\text{s}} \mu_{\text{n}} N_{\text{c}} \left(\frac{2\gamma + 1}{\gamma + 1}\right)^{\gamma + 1} \left(\frac{\gamma}{\gamma + 1}\right)^{\gamma} \left(\frac{\varepsilon_0 \varepsilon_{\text{IGZO}}}{q N_{\text{t}} k T_{\text{t}}}\right)^{\gamma} \frac{V^{\gamma + 1}}{L^{2\gamma + 1}}, \tag{14}$$

where N_{t} is the density of bulk trap states at E_{C}, T_{t} is the effective temperature of the trap distribution, μ_{n} is the bulk carrier mobility, N_{C} is the effective DOS at E_{C}, and $T_{\text{t}}/T = m - 1$ (where T is the measurement temperature). For the fabricated IGZO TFT, γ and kT_{t} were found to be 3.04 and 0.077 eV, respectively. By substituting the dimensional parameters

(W = 10 μm, L = 5 μm, and t_S = 40 nm) and electrical parameters (μ_n = 5.9 cm^2/(Vs), N_C = 5 × 10^{18} cm^{-3}, ε_{IGZO} = 10, and ε_0 = 8.854 × 10^{-14} F/cm) of the fabricated IGZO TFT into Equations (13) and (14), $N_b(E)$ is calculated as shown in Figure 8a. Figure 8b shows the energy distribution of the total subgap DOS $D_{it} + t_S \times N_b$, D_{it}, and $t_S \times N_b$ for the fabricated IGZO TFT. Here, $D_{it}(E)$ was obtained by subtracting $t_S \times N_b(E)$ from the total subgap DOS at each energy level. Similar to the results obtained from the *C–V* method in Figure 6b, Figure 8b shows that approximately 61% of the total subgap states are interface trap states at E_C in the fabricated SA-TG coplanar IGZO TFT.
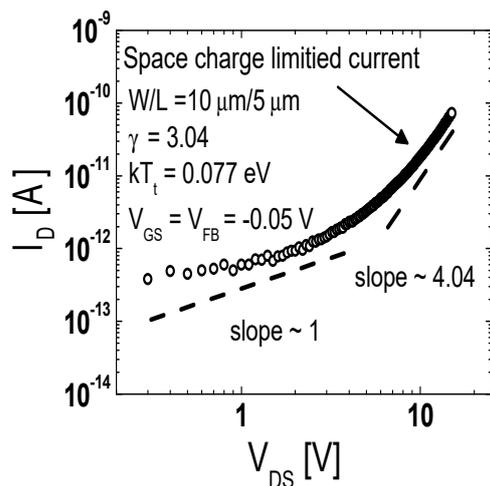
Figure 7. Log–log plot of the I_D–V_{DS} curve measured from the fabricated IGZO TFT under the flat-band condition.
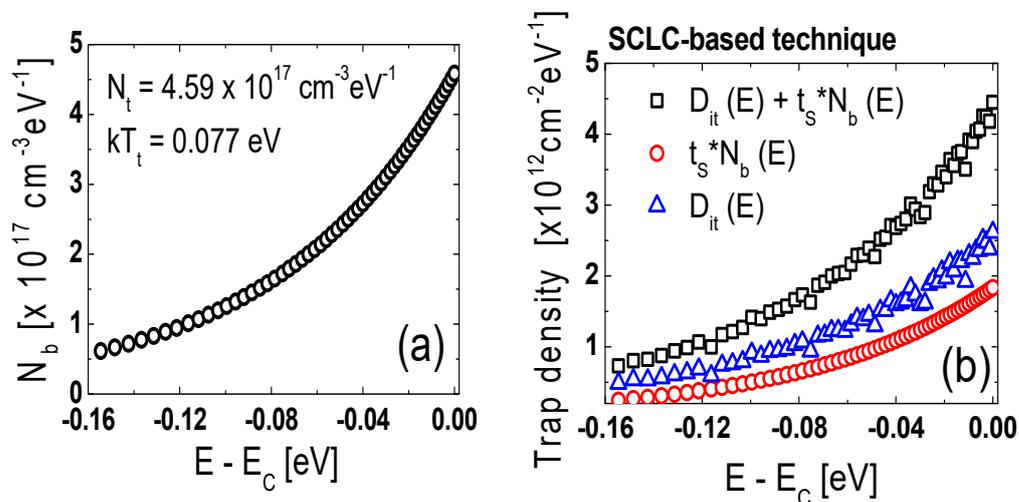
Figure 8. (**a**) Energy distribution of the density of bulk trap states N_b calculated with the SCLC-based technique. (**b**) Energy distributions of the total subgap DOS $D_{it} + t_S \times N_b$, the density of interface trap states D_{it}, and the density of bulk trap components $t_S \times N_b$ obtained using the SCLC-based technique.

Figure 9a,b show $D_{it}(E)$ and $N_b(E)$ for the fabricated IGZO TFT for different extraction methods based on different measurement results. The two characterization techniques provide very similar values of interface and bulk trap densities at every energy level (D_{it} = 2.5 × 10^{12} cm^{-2} eV^{-1}, N_b = 4.1 × 10^{17} cm^{-3} eV^{-1} at E_C for the technique based on the low-frequency *C–V* curve and D_{it} = 2.7 × 10^{12} cm^{-2} eV^{-1}, N_b = 4.59 × 10^{17} cm^{-3} eV^{-1} at E_C for the SCLC-based technique), although the two characterization techniques are based on different measurement data.
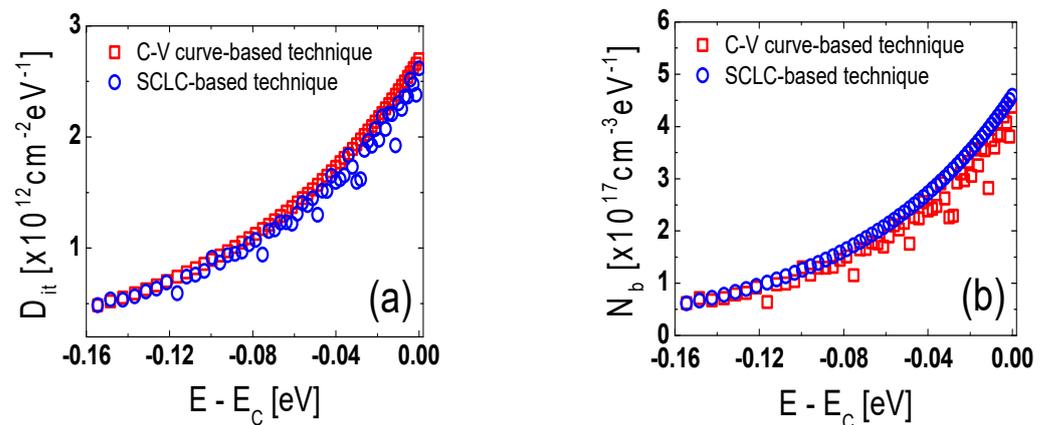
Figure 9. Energy distributions of (**a**) D_{it} and (**b**) N_b extracted using the technique based on the low-frequency *C–V* curve and the SCLC-based technique.

4. Conclusions

In this study, we separately determined the energy distributions of the interface and bulk trap densities from an SA-TG coplanar IGZO TFT using low-frequency *C–V* characteristics and the SCLC under the flat-band condition. Our experimental results showed that the values of D_{it} and N_b obtained using the two different techniques exhibited very similar values at every energy level (D_{it} = 2.5 × 10^{12} cm^{-2} eV^{-1}, N_b = 4.1 × 10^{17} cm^{-3} eV^{-1} at E_C for the technique based on the low-frequency *C–V* curve and D_{it} = 2.7 × 10^{12} cm^{-2} eV^{-1}, N_b = 4.59 × 10^{17} cm^{-3} eV^{-1} at E_C for the SCLC-based technique), although they are based on different measurement data. From both characterization techniques, it may be concluded that ~60% of the subgap states are attributed to the interface states at E_C in the fabricated SA-TG coplanar IGZO TFT. The results of this study confirm the validity of the characterization techniques for separately extracting the interface and bulk trap densities in IGZO TFTs and show that the density of interface trap states needs to be reduced to improve the electrical properties and stabilities of the fabricated IGZO TFTs.

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