Quantitative Analysis of Positive-Bias-Stress-Induced Electron Trapping in the Gate Insulator in the Self-Aligned Top Gate Coplanar Indium–Gallium–Zinc Oxide Thin-Film Transistors

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Abstract: We experimentally extracted the positive bias temperature stress (PBTS)-induced trapped electron distribution within the gate dielectric in self-aligned top-gate (SA-TG) coplanar indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) using the analytical threshold voltage shift model. First, we carefully examined the effects of PBTS on the subgap density of states in IGZO TFTs to exclude the effects of defect creation on the threshold voltage shift due to PBTS. We assumed that the accumulated electrons were injected into the gate dielectric trap states near the interface through trap-assisted tunneling and were consequently moved to the trap states, which were located further away from the interface, through the Poole–Frenkel effect. Accordingly, we quantitatively analyzed the PBTS-induced electron trapping. The experimental results showed that, in the fabricated IGZO TFTs, the electrons were trapped in the shallow and deep trap states simultaneously owing to PBTS. Electrons trapped in the shallow state were easily detrapped after PBTS termination; however, those trapped in the deep state were not. We successfully extracted the PBTS-induced trapped electron data within the gate dielectric in the fabricated SA-TG coplanar IGZO TFTs by using the proposed method.

Keywords: IGZO TFTs; PBTS; gate dielectric; subgap density of states; trapped electron distribution

1. Introduction

In the last decade, indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) have attracted significant attention because of their excellent electrical properties, low fabrication temperatures, and good large-area uniformities [1–3]. Recently, IGZO TFTs have been used for the backplane of active-matrix organic light-emitting diode (AMOLED) displays and for digital X-ray detectors [4–6]. However, with an increase in the application area of IGZO TFTs, the requirements for the electrical stability of IGZO TFTs have become more stringent. When used for the backplane of AMOLED displays or digital X-ray detectors, IGZO TFTs are frequently subjected to positive bias temperature stress (PBTS); therefore, it is crucial to understand the PBTS-induced instability mechanism in IGZO TFTs. Under PBTS, numerous electrons accumulate near the gate dielectric, and some electrons move toward the gate dielectric and become trapped in the dielectric trap states [7]. The trapped electrons partially screen the applied electric field from the gate terminal. Therefore, a large gate voltage is required to activate the TFT, thereby shifting the transfer curve in the positive direction [8]. To date, only a few studies have quantitatively analyzed PBTS-induced electron trapping in the gate dielectric in IGZO TFTs. Some previous studies have successfully established analytical models for the extraction of a detailed trapped

electron distribution within the gate dielectric after PBTS [9,10]. However, the assumptions made in these studies are somewhat problematic. They assumed that the trapped electrons in the gate dielectric are the primary reason for the transfer curve shift under PBTS and that electrons are trapped in the trap state only at a single energy level. However, studies on IGZO TFTs have reported that the defect state creation within the IGZO channel can also induce the transfer curve shift under PBTS even when there is no change in the subthreshold swing (*SS*) values [11]. Moreover, it has been reported that carriers can be simultaneously trapped in multiple dielectric trap states with different energy levels under electrical stresses in metal-oxide-semiconductor structure devices [12].

In this study, we experimentally extracted the PBTS-induced trapped electron distribution within the gate dielectric by considering the effects of PBTS on the subgap density of states (DOS) in IGZO TFTs. Furthermore, we assumed that electrons can be simultaneously trapped in multiple dielectric trap states with different energy levels under PBTS in the fabricated IGZO TFTs. In this study, the accumulated electrons were assumed to be injected into the gate dielectric trap states near the interface through trap-assisted tunneling and then moved to the trap states located further away from the interface by the Poole–Frenkel (P–F) effect [13,14]. Using the proposed method, we successfully extracted the PBTS-induced trapped electron distribution within the gate dielectric in self-aligned top-gate (SA-TG) coplanar IGZO TFTs, which are now widely used in commercially available AMOLED displays [15–17]. The results of this study are expected to contribute to the improvement of PBTS stability in IGZO TFTs.

2. Experimental Section

SA-TG coplanar IGZO TFTs were fabricated as shown in Figure 1. First, a buffer layer (SiN_X/SiO_2 = 30/200 nm) was deposited by plasma-enhanced chemical vapor deposition (PECVD) on a glass substrate. A 40-nm-thick IGZO layer (In:Ga:Zn = 1:1:1 at.%) was deposited by RF sputtering on a buffer layer. A 120-nm-thick SiO_X layer was deposited by PECVD as a gate insulator, followed by the sequential deposition of a gate metal (Ti/Mo = 30 nm/250 nm). After the deposition and patterning of the gate electrode and gate insulator, 300-nm-thick SiO_X and 200-nm thick SiN_X were sequentially deposited as passivation layers by PECVD and patterned to form via holes. A metal layer (Ti/Al/Ti = 30/600/60 nm) was deposited and patterned as the source and drain electrodes. Finally, the devices were thermally annealed at 340 °C to achieve a stable and uniform electrical performance. The channel width (*W*) and length (*L*) were 3 and 5 μm, respectively. The electrical parameters of the representative device were as follows: field-effect mobility (μ_{FE}) of 8.1 cm^2/Vs, threshold voltage (V_{TH}) of 0.15 V, and *SS* of 0.19 V/dec. Here, μ_{FE} was determined using the maximum transconductance method, and V_{TH} was defined as the gate-to-source voltage value (V_{GS}) inducing a drain current (I_D) of 1 nA at a V_{DS} of 0.1 V. The energy distribution of the subgap DOS was extracted using the monochromatic photonic *C–V* (MPCV) technique [18]. For MPCV characterization, a light source of 3 mW with a wavelength corresponding to the energy of 2.8 eV was used, and the *C–V* curves were measured at 100 kHz. The ΔV_{TH} decomposition was performed by the stress time-divided measurement technique [19]. The current–voltage and capacitance–voltage (*C–V*) characteristics of the TFTs were extracted using an Agilent 4156C semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA) and a 4284A precision LCR meter (Agilent Technologies, Santa Clara, CA, USA), respectively. All measurements were performed under dark ambient conditions unless stated otherwise.
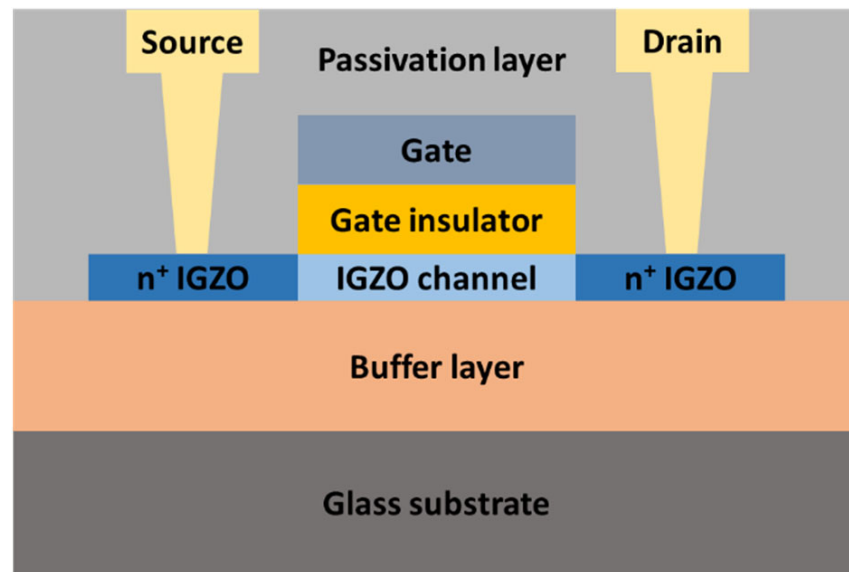
Figure 1. Structure of the fabricated SA-TG coplanar IGZO TFT.

3. Results and Discussion

First, we examined the effects of PBTS on the subgap DOS in the fabricated SA-TG coplanar IGZO TFTs. Figure 2 shows the time evolution of the transfer curves for the fabricated SA-TG coplanar IGZO TFTs under a constant V_{GS} and V_{DS} of 40 V and 0 V, respectively, at 80 °C. The transfer curve shifted in the positive direction with an increase in the stress time; the *SS* value exhibited no significant change. Previous studies on well-passivated IGZO TFTs have reported that the PBTS-induced parallel shift of the transfer curves can primarily be attributed to the creation of acceptor-like states below the Fermi level in the IGZO channel layer or the electron injection from IGZO into the gate dielectric [20,21].
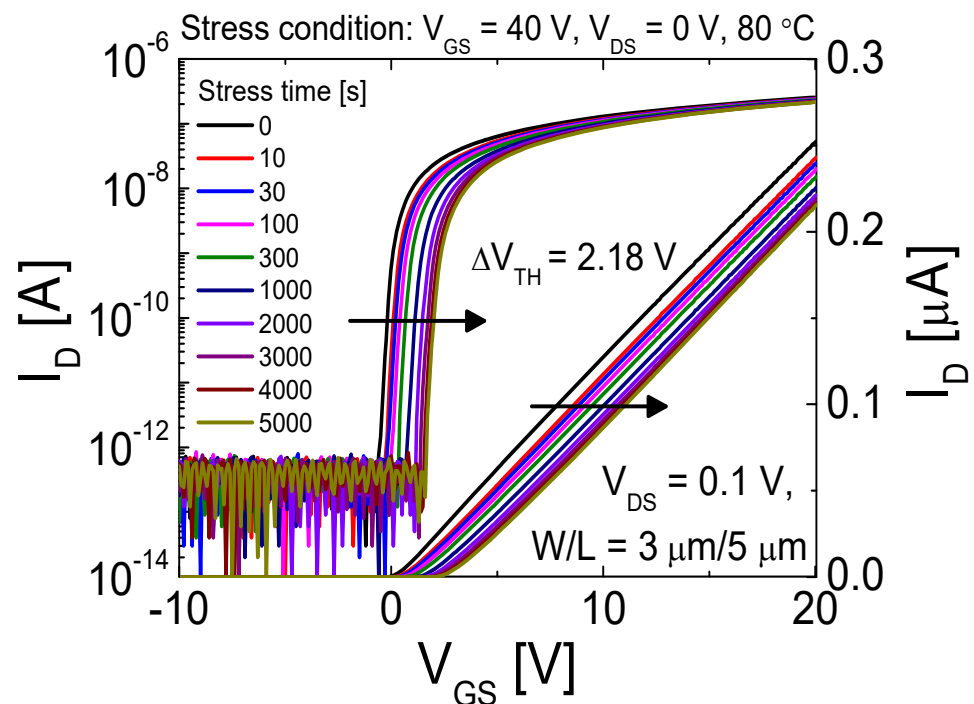

Figure 2. Time evolution of the transfer curves for the fabricated SA-TG coplanar IGZO TFT under a constant V_{GS} of 40 V and V_{DS} of 0 V at 80 °C.

Therefore, the effects of PBTS on the subgap DOS in the channel layer must be examined before quantitatively analyzing the PBTS-induced trapped electron distribution within the gate dielectric in IGZO TFTs. Figure 3a,b demonstrate the energy distribution of the subgap DOS extracted using the MPCV technique before and after the application of the PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C) for a stress time (t_{st}) of 5000 s. The results presented in Figure 3 show that the difference between the energy distribution of the subgap DOS extracted from the TFT before and after PBTS was minimal, indicating that the electron injection from the channel (IGZO) to the gate dielectric (SiO$_2$) in the fabricated SA-TG IGZO TFTs caused the PBTS-induced transfer curve shift observed in Figure 2.
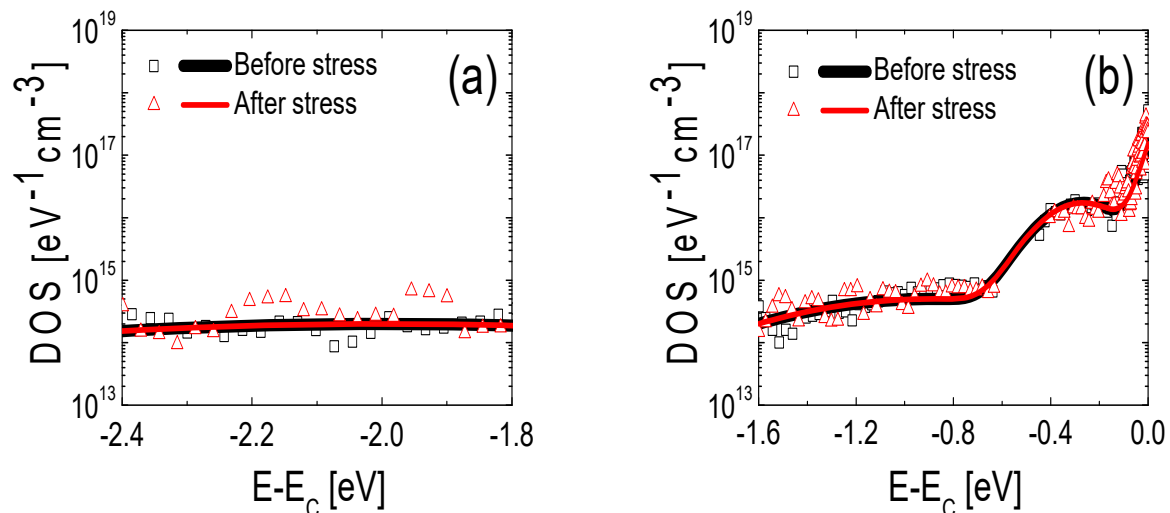
Figure 3. Energy distribution of subgap DOS in IGZO near (**a**) the valence band maximum (E_V) and (**b**) the conduction band minimum (E_C) obtained using MPCV before and after the application of the PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C) for 5000 s. Dotted symbols and lines denote the experimental data and fitting curves, respectively.

Subsequently, we validated the assumption made in previous reports that electrons are trapped in the dielectric trap states only at a single energy level during PBTS in IGZO TFTs [10]. Figure 4 illustrates the time evolution of the threshold voltage shift (ΔV_{TH}) during the stress (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C, t_{st} = 5000 s) and subsequent recovery (V_{GS} = 0 V, V_{DS} = 0 V, 80 °C, t_{st} = 10,000 s) phases. The results reveal that the ΔV_{TH} value decreased rapidly in the early stage of the recovery phase and was saturated at a certain value, implying that a part of trapped electrons were easily detrapped during this phase, but the remaining electrons were intact.
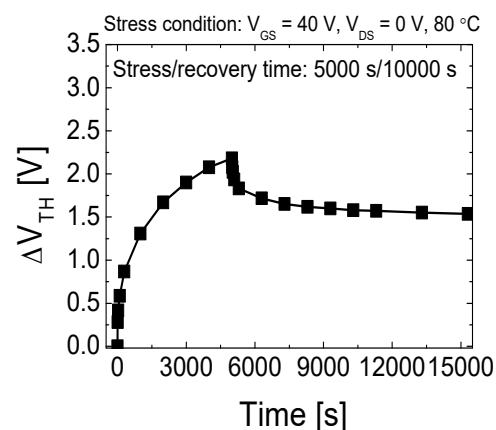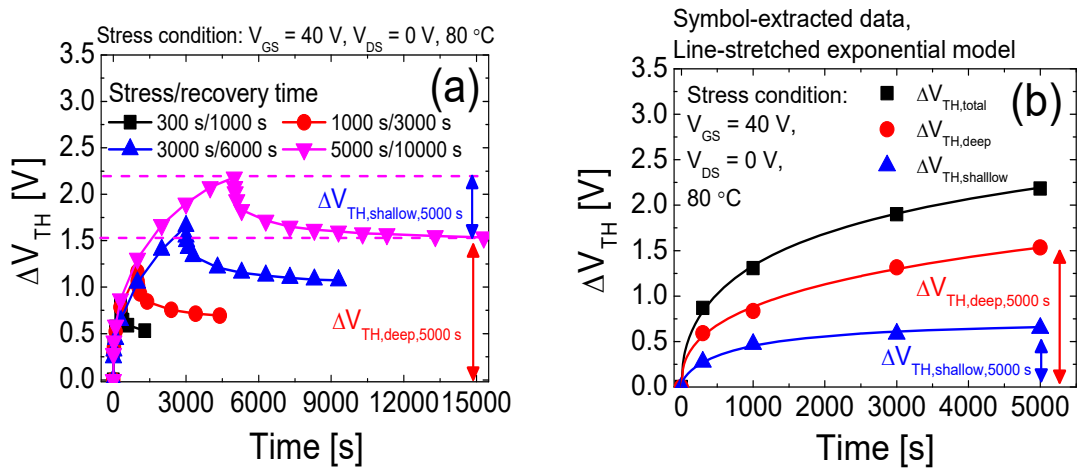

Figure 4. Time evolution of ΔV_{TH} during the stress (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C, t_{st} = 5000 s) and subsequent recovery (V_{GS} = 0 V, V_{DS} = 0 V, 80 °C, t_{st} = 10,000 s) phases.

Figure 5a shows the time evolution of ΔV_{TH} at different stress/recovery time pairs, and Figure 5b shows the time evolution of the PBTS-induced ΔV_{TH} by both the recoverable and non-recoverable trapped electrons, obtained by applying the stress-time-divided measurement technique to Figure 5a. Figure 5b shows that the time evolution of both ΔV_{TH} for the recoverable and non-recoverable trapped electrons were well-fitted by the stretched-exponential function. Generally, the stretched-exponential time dependence of ΔV_{TH} is observed when electrons are trapped in the trap states at a single energy level [22,23]. The stretched-exponential equation for the $\Delta V_{TH}(t)$ is defined as:

$$\Delta V_{TH}(t) = \Delta V_{TH,0}\left[1 - \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right],\qquad(1)$$

where $\Delta V_{TH,0}$ is the ΔV_{TH} at infinite time, β is the stretched-exponential exponent, and $\tau = \tau_0 \times \exp(E_a/kT)$ represents the characteristic trapping time of carriers, and E_a is the average effective energy barrier that electrons in the IGZO TFT channel need to overcome before they can enter the insulator, and τ_0 is the thermal prefactor for emission over the barrier. The lines in Figure 6a,b show that the recoverable trap component and the non-recoverable trap component was well fitted with the stretched exponential model functions. As shown in Figure 6c, the temperature dependence of the τ was confirmed, E_a was 0.29 eV for the recoverable trap and 0.78 eV for the non-recoverable trap.


Figure 5. (**a**) Time evolution of ΔV_{TH} at different stress/recovery time pairs. (**b**) Time evolution of the PBTS-induced ΔV_{TH}s for the recoverable and non-recoverable trapped electrons obtained by applying the stress-time-divided measurement technique to (**a**).
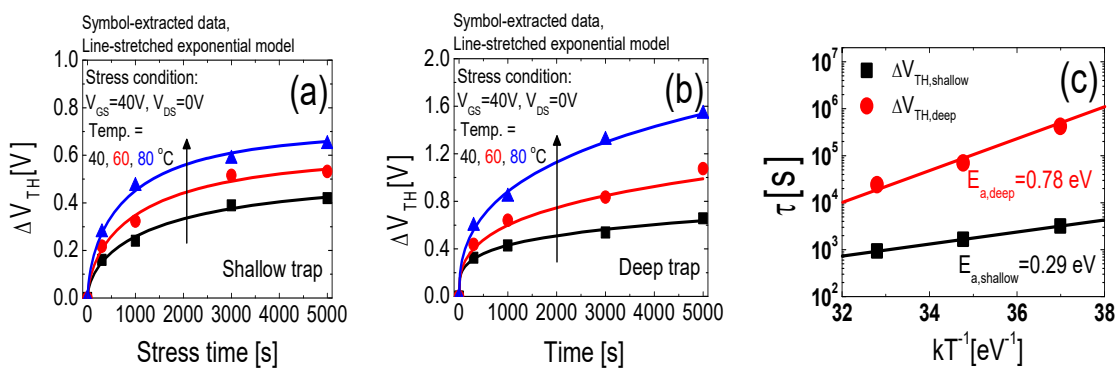
Figure 6. (**a**) Dependence of ΔV_{TH} (*t*) on stress temperature for the electrons trapped in the shallow trap under PBTS (V_{GS} = 40 V, V_{DS} = 0 V, t_{st} = 5000 s). (**b**) Dependence of ΔV_{TH} (*t*) on stress temperature for the electrons trapped in the deep trap under PBTS. (**c**) Characteristic time constant as a function of the PBTS temperature to extract the effective energy barrier (activation energy), for each trap.

Therefore, we can assume that the electrons were simultaneously trapped in the two dielectric trap states with different energy levels under PBTS in the fabricated IGZO TFTs. Hereafter, the gate dielectric trap where the trapped electrons can and cannot be easily detrapped during the recovery phase will be called as "shallow trap" and "deep trap", respectively.

Finally, we extracted the PBTS-induced trapped electron distribution in the shallow and deep SiO$_2$ gate dielectric traps in the fabricated SA-TG coplanar IGZO TFTs. Figure 7a presents the energy band diagram of the IGZO TFT under PBTS, where x represents the direction from the IGZO/SiO$_2$ interface to SiO$_2$. The energy level E_T of the electron trap is defined by ΔE_{OT} [eV], which indicates the energy difference between E_T and the SiO$_2$ conduction band minimum ($E_{C, oxide}$). The Fermi energy level (E_F) and E_T cross at x_0, which is extracted using the response time of the traps at the interface; the detailed methodology is provided in [24]. There were three different cases of trapped electrons in gate dielectrics under PBTS in IGZO TFTs. As depicted in Figure 7a, under a small V_{GS} for a short t_{st}, the electrons could not transfer to the position x_0 and tunnel back easily to IGZO; as V_{GS} and t_{st} increased, the electrons tunneled deeper into the gate dielectric, and could not tunnel back easily to IGZO until they were trapped in E_T below E_F [10]. Further, as V_{GS} and t_{st} continued to increase, the trap states located near x_0 were filled with electrons and thus could no longer capture them. The trapped electrons located below E_F transferred to deeper positions by P–F conduction within the gate dielectric, as shown in Figure 7b [14,25].
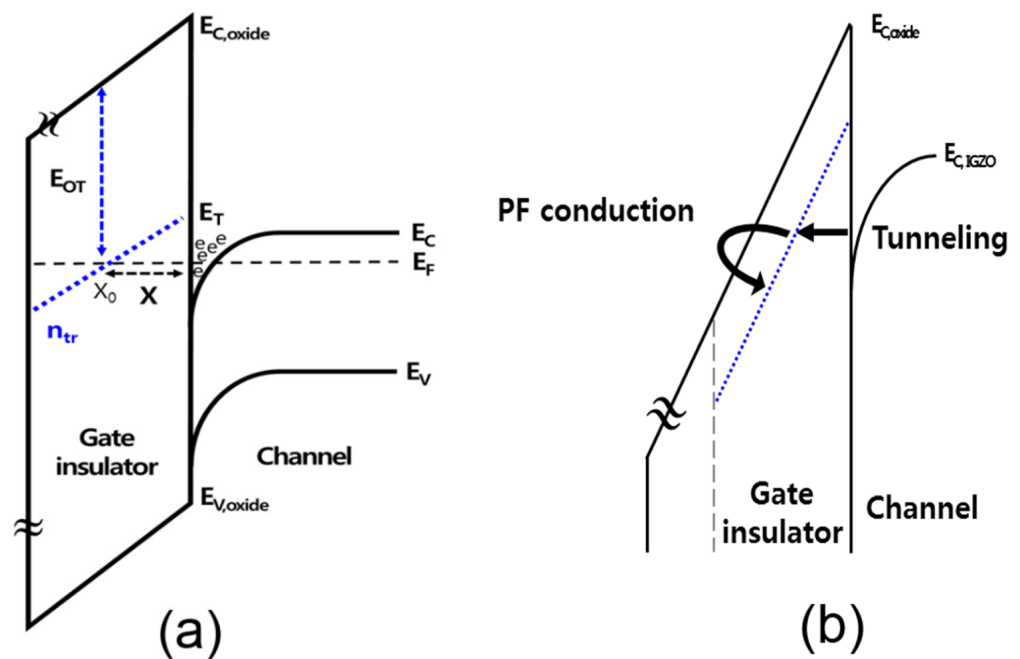
Figure 7. (**a**) Energy band diagram for the IGZO TFT under PBTS, in which x represents the direction from the IGZO/SiO$_2$ interface to SiO$_2$. (**b**) PBTS-induced electron tunneling from IGZO to SiO$_2$ and PF conduction of trapped electrons in SiO$_2$.

Accordingly, the trapped electron distribution in the gate dielectric under PBTS can be expressed by the following equation [26,27]:

$$\frac{\partial n_{tr}}{\partial t} = G - \frac{\partial J_n}{q \cdot \partial x} \tag{2}$$

where n_{tr} represents the concentration of the filled trap states in SiO$_2$ at time t and position x, J_n is the transport current density in SiO$_2$, G is the generation rate of the trapped electrons, and q represents the electron charge.

The generation rate of the trapped electrons, G, is expressed based on the Shockley–Read–Hall recombination equation as follows [24,28]:

$$G = \sigma(x) \cdot v_s \cdot n_s \cdot (N_T - n_{tr}) = \sigma_0 \cdot \exp(-ax) \cdot v_s \cdot n_s \cdot (N_T - n_{tr}) \tag{3}$$

where $\sigma(x) = \sigma_0 \times \exp(-ax)$ represents the location-dependent capture cross-section, σ_0 is the capture cross-section at the semiconductor/gate dielectric interface, and a is the decay parameter, which depends on the tunneling effective mass of an electron and barrier height. In addition, v_s represents the velocity at which the electrons move to the gate dielectric, and n_s and N_T are the electron density in the channel layer and trap density in the gate dielectric, respectively.

The PBTS-induced transport current density in the gate dielectric is described by the P–F conduction [13,14,26].

$$J_n = n_{tr} \cdot q \cdot \Delta z \cdot r \cdot \exp\left[-\frac{1}{\zeta kT}\left(E_{OT} - \beta E^{1/2} \right) \right] \tag{4}$$

where $\beta = (q^3/(\pi \varepsilon_0 \varepsilon_{SiO2}))^{1/2}$. Δz is the mean distance between two adjacent SiO_2 trap states, r is the characteristic P–F attempt frequency of the trapped electrons, T is the temperature, and ζ is the P–F factor. Additionally, k denotes the Boltzmann's constant (8.62×10^{-5} eV), ε_0 denotes the vacuum permittivity (8.854×10^{-14} F/cm), and ε_{SiO2} denotes the relative permittivity of SiO_2 (3.9). Because a significant portion of V_{GS} falls on SiO_2, the electric field in SiO_2 (E) is expressed as $E \approx V_{GS}/t_{ox}$, where t_{ox} is the thickness of SiO_2. By substituting Equations (3) and (4) into (2) and solving the differential equation, we obtain:

$$n_{tr} = N_T \cdot \{1 - \exp[-\exp(-a(x - x_1))]\} \tag{5}$$

$$x_1 = \frac{1}{a} \ln\left\{ \frac{K_2}{aK_1} \cdot [\exp(aK_1 t) - a] \right\} \tag{6}$$

$$K_1 = \Delta z \cdot r \cdot \exp\left[-\frac{1}{\zeta kT_{st}}\left(E_{OT} - \beta E^{1/2} \right) \right] \tag{7}$$

$$K_2 = S_0 v_s n_s \tag{8}$$

Thus, Equations (5)–(8) represent the spatial and temporal trapped electron distributions in the gate dielectric. The PBTS-induced threshold voltage shift at time t, $\Delta V_{TH}(t)$, can be expressed in terms of n_{tr} and x as

$$\Delta V_{TH}(t) = \int_{x_0}^{x_1} \frac{q \cdot n_{tr}}{\varepsilon_0 \varepsilon_{SiO_2}/(t_{OX} - x)} dx$$
$$= \frac{q \cdot n_{tr}}{\varepsilon_0 \varepsilon_{SiO_2}} \cdot (x_1 - x_0) \cdot \left(t_{OX} - \frac{x_1 + x_0}{2} \right) \tag{9}$$

where the parameters n_{tr}, x_0, x_1, and E_{OT} in Equations (5)–(9) are obtained as a function of the PBTS condition and t_{st} [26]. The results presented in Figures 4–6 show that the electrons were simultaneously trapped in the two dielectric trap states with different energy levels, called shallow and deep traps, under PBTS, in the fabricated IGZO TFTs. Therefore, we independently extracted the parameters n_{tr}, x_0, x_1, and E_{OT} for the electrons trapped in each gate dielectric trap under a specific PBTS condition. These parameters can be obtained from the separately extracted $\Delta V_{TH}(t)$ values at that specific PBTS condition and T and V_{GS} (or E)-dependence of each $\Delta V_{TH}(t)$.

Figure 8a–d demonstrate the dependence of $\Delta V_{TH}(t)$ on T and V_{GS} for the electrons trapped in the shallow and deep traps under PBTS. By substituting the results in Figures 5b and 8a–d into Equations (5)–(9), we could extract the n_{tr}, x_0, x_1, and E_{OT} parameters for each trap under specific PBTS conditions (in this study, $V_{GS} = 40$ V, $V_{DS} = 0$ V, 80 °C, $t_{st} = 5000$ s). Figure 8 illustrates the extracted trapped electron distribution in the shallow and deep gate dielectric traps after the application of the PBTS ($V_{GS} = 40$ V, $V_{DS} = 0$ V, 80 °C) for 5000 s. Table 1 summarizes the n_{tr}, x_0, x_1, and E_{OT} values for the electrons in

each type of trap. Although further study is necessary, the extracted E_{OT} values for each gate dielectric trap suggest that the shallow and deep traps (Figure 9) possibly originated from the oxygen vacancy defect and E′ center defect in SiO_2, respectively [29–32].
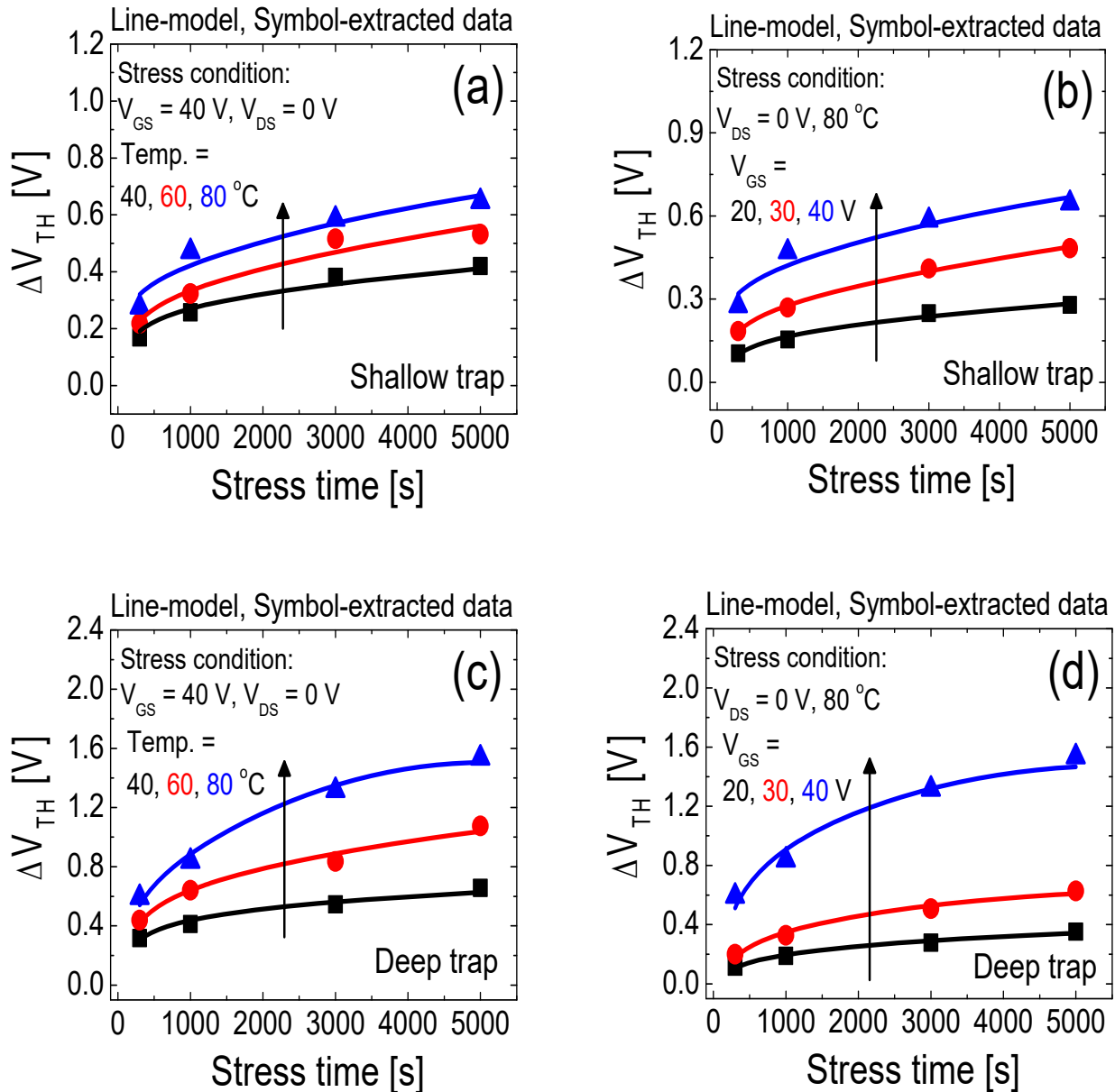

Figure 8. Dependencies of ΔV_{TH} (t) on (**a**) T and (**b**) V_{GS} for the electrons trapped in the shallow trap under PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C). Dependencies of ΔV_{TH} (t) on (**c**) T and (**d**) V_{GS} for the electrons trapped in the deep trap under PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C).

Table 1. Extracted values of n_{tr}, x_0, x_1, and E_{OT} for electrons trapped in shallow and deep traps under PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C) in the fabricated IGZO TFT.

Parameter	Shallow Trap	Deep Trap
n_{tr} (cm^{-3})	2.49×10^{18}	3.63×10^{18}
E_{OT} (eV)	3.41	1.63
x_0 (nm)	1.2	2.3
x_1 (nm)	3.3	5.9
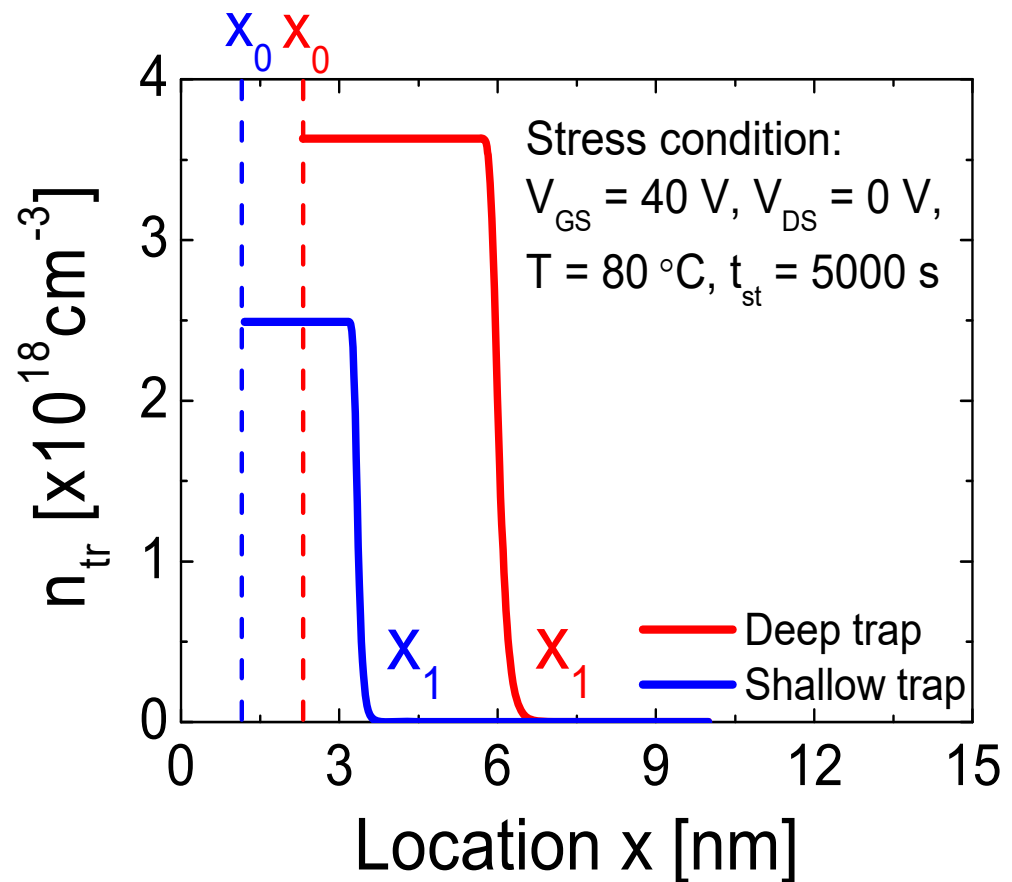
Figure 9. Extracted trapped electron distribution in the shallow and deep gate dielectric traps after the application of the PBTS (V_{GS} = 40 V, V_{DS} = 0 V, 80 °C) for 5000 s in the fabricated SA-TG coplanar IGZO TFT.

4. Conclusions

In this study, we quantitatively analyzed PBTS-induced electron trapping in the gate dielectric in SA-TG coplanar IGZO TFTs. First, we investigated the effects of PBTS on the subgap DOS in IGZO TFTs. Then, we examined the PBTS-induced ΔV_{TH} values originating from electron trapping in shallow and deep gate dielectric traps. The data on the PBTS-induced trapped electrons in shallow and deep trap states was obtained from the analytical threshold voltage shift model based on trap-assisted tunneling and P–F effects. The extracted model parameters were n_{tr} = 2.49 × 10^{18} cm^{-3}, x_0 = 1.2 nm, x_1 = 3.3 nm, and E_{OT} = 3.41 eV for the electrons trapped in shallow traps and n_{tr} = 3.63 × 10^{18} cm^{-3}, x_0 = 2.3 nm, x_1 = 5.9 nm, and E_{OT} = 1.63 eV for the electrons trapped in deep traps. The results of this study are expected to be helpful in determining the physical origin of the gate dielectric traps, which degrade the PBTS stability in IGZO TFTs.

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