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Fully Integrated Dual-Mode X-Band Radar Transceiver Using Configurable Receiver and Local Oscillator

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ABSTRACT In this paper, a fully-integrated dual-mode X-band radar transceiver that supports Doppler radar and frequency modulated continuous wave (FMCW) radar is proposed. To remove large off-chip DC-blocking capacitors in the Doppler mode, the double-conversion technique and local oscillator (LO) chopping technique are introduced. These techniques remove the DC offset and makes the transceiver more robust to the TX to RX leakage. In addition, they also improve the noise figure (NF) by filtering out 1/f noise of the analog baseband. The FMCW radar is realized using a direct-conversion receiver and a chirp generator. The chirp generator consists of a frequency sweep generator (FSG) and a fractional-N phase-locked loop (PLL). All the analog baseband components including a programable gain amplifiers (PGA) and 1/R⁴ range compensation filters are integrated on the chip as well as a bandgap and low-dropout regulators. The operating frequency is from 9.7 to 12.3 GHz, which consumes 216 mW in Doppler mode and 201.6 mW in FMCW mode from a 1.2-V supply voltage. The maximum chirp bandwidth is 750 MHz and the maximum receiver gain is 76 dB with 6-dB gain step. The chip size of the transceiver is 7.68 mm² including all the pads.

INDEX TERMS CMOS, X-band, fully-integrated transceiver, Doppler radar, FMCW radar, dual-mode radar, noise figure.

I. INTRODUCTION

In recent years, the applications of radar sensors have been extended to various security systems, automated home appliances, autonomous driving assistance systems (ADAS), and unmanned aerial vehicles (UAVs) [1]–[9]. Especially, X-band radar has been widely utilized in automation devices and security systems that need to detect movement of objects [10]–[18].

Doppler radar measures the velocity of a moving object by transmitting a fixed frequency, then receiving and down-

converting the reflected signal from the target. The Doppler information exists in very low frequencies, from a few Hz to hundreds of Hz. Doppler radar has been widely adopted in low-cost motion sensors for detecting the presence of a moving object, because the decision circuit can be realized with a simple component such as a comparator or a low bit-number analog-to-digital (ADC) converter. However, the frequency of the Doppler signal is so low that it is very difficult to distinguish the Doppler signal from the DC. Thus, very large DC decoupling capacitors are required between the down conversion mixer and analog baseband (ABB) as shown in Figure 1(a). The DC decoupling capacitors make it very difficult to integrate the Doppler radar into a single chip.

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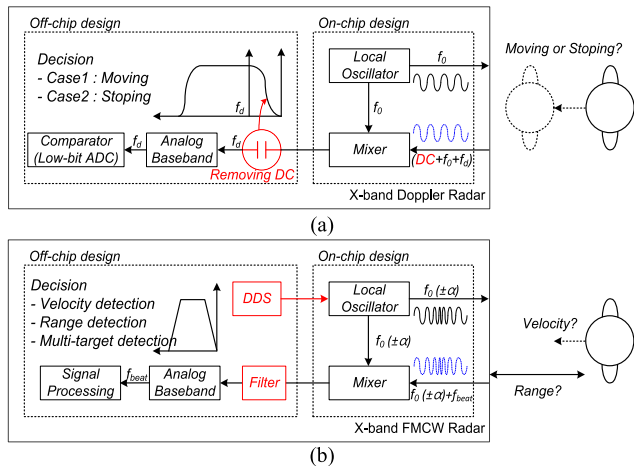


FIGURE 1. (a) Doppler radar and (b) FMCW radar.

In addition, the Doppler radar is sensitive to $1/f$ flicker noise due to low Doppler frequency.

Frequency modulated continuous wave (FMCW) radar provides distance information as well as velocity information, allowing users to use more sophisticated and versatile applications. However, FMCW radar requires complex signal processing such as 1-D or 2-D digital Fourier transform and an adaptive threshold algorithm to maintain a constant false alarm rate against background noise, clutter, and interference. Therefore, a dedicated processing device such as a digital signal processor, field programmable gate array, or application processor is required. Since the baseband frequency of the FMCW radar is usually over several hundred kHz due to the chirping, it does not need large DC-decoupling capacitors, unlike Doppler radar. However, FMCW radar does require a chirp generator, which is implemented by a digital direct synthesizer (DDS) or a phase-locked loop (PLL) as shown in Figure 1(b) [13]–[16]. Furthermore, a range compensation filter, known as $1/R^4$ filter is needed in the baseband to prevent the receiver from saturating when detecting nearby objects.

In this paper, a fully integrated X-band radar transceiver that supports Doppler radar and FMCW radar simultaneously is proposed. The transceiver was implemented using $0.13\text{-}\mu\text{m}$ CMOS technology. The proposed radar integrated all the components needed for Doppler radar and FMCW radar on a single chip, except for the DC supply capacitors and the loop-filter capacitor for the PLL.

This paper is organized as follows. Section II describes the dual mode radar system. The circuit implementations are discussed in Section III. Section IV shows measurement results and a conclusion is presented in V.

II. DUAL MODE RADAR

Figure 2 shows a block diagram of the proposed dual-mode X-band radar transceiver. The transceiver is composed of a receiver (RX), a LO, and auxiliary circuits such as a bandgap-reference (BGR), current and voltage reference generators

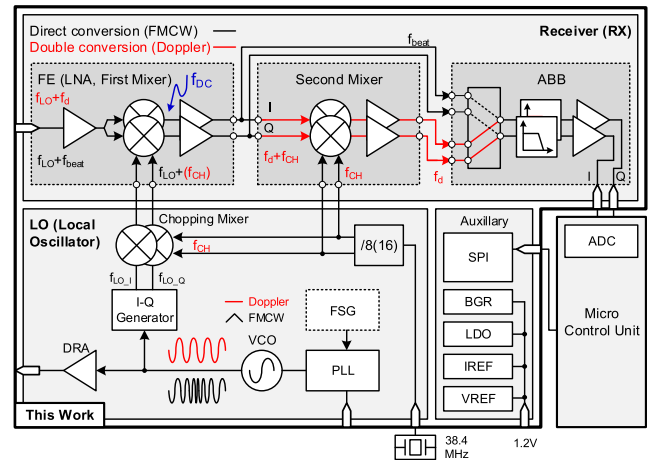


FIGURE 2. The block diagram of the proposed dual-mode X-band radar transceiver.

(IREF, VREF), low dropout regulators (LDOs), and a SPI. The RX is composed of a front-end (FE), second mixer, and ABB. The LO consists of a voltage-controlled oscillator (VCO), PLL, a frequency sweep generator (FSG), I-Q generator, and driving amplifier (DRA). The transmitter (TX) is realized using a DRA. The main role of the LO is to generate a fixed TX frequency when operating with a Doppler radar and a linear chirp when operating as a FMCW radar. The proposed LO adapts an FSG with a fraction-N PLL to generate chirp signals. The BGR generates internal references for bias current and voltage. And the LDOs provides the isolated supply voltages between the blocks. SPI block controls all the function the blocks.

When operating as a Doppler radar, the RX is configured to the double-conversion mode by activating the second mixer. The LO chopping mixer provides a chopping frequency, $f_{LO} + f_{CH}$ for the first mixer. The frequency divider of the reference clock of 38.4 MHz provides a de-chopping frequency, f_{CH} to the second mixer. This chopping technique makes the transceiver more robust to the TX to RX leakage by moving the DC blocker to the chopping frequency and removing it. The Doppler frequency f_d and DC offset f_{DC} mainly coming from the TX to RX leakage are intentionally shifted by the chopping frequency f_{CH} at the FE. Since the DC offset is up-converted to the frequencies of $+f_{CH}$ and $-f_{CH}$, and they are added in the opposite phase at the second mixer, this DC offset is removed in front of the ABB. Thus, the proposed radar transceiver can realize the Doppler radar without large DC-coupling capacitors. In addition, the signal-to-noise ratio (SNR) is improved because the Doppler signal is amplified at the chopping frequency before the ABB that has high $1/f$ flicker noise.

When operating as a FMCW mode, the RX is configured to the direct-conversion mode by bypassing the second mixer. And the LO chopping mixer is also disabled but the FSG is enabled. The ABB consists of a biquad lowpass filter (LPF) and programable gain amplifier (PGA) with DC offset

cancellators (DCOCs). The DCOCs can be selectively turned on and off in each stage. The range compensation filter is realized using high pass characteristics of the DCOC included in the ABB [19]–[26]. The low-pass cut-off frequency of the ABB is set about 2 MHz and the gain can be changed up to 36 dB in 6 dB steps. The two mode can be switched easily each other through a serial-to-parallel interface (SPI).

The receiving power, P_R of the radar can be obtained using a well-known radar equation [27].

$$P_R = \frac{\sigma A_T A_R \lambda^2}{(4\pi)^3 L_{ATM} R^4} \times P_T \quad (1)$$

where σ is the radar cross section of the detected object, A_T and A_R are the gains of TX antenna and RX antenna, respectively, λ is the wavelength of carrier frequency, P_T is the transmitting power, L_{ATM} is the loss in atmosphere at 10.525 GHz, and R is the target distance. At 10–11 GHz, the atmosphere loss is about 0.01 dB/km [27]. The radar cross section of a person is assumed 1 m². The transmitting power of the radar transceiver is 5 dBm. Assuming both the gain of transmitting antenna and receiving antenna is 10 dBi, the received power is expressed as follows:

$$P_{R,dBm} \approx -37 - 40 \times \log(R) \quad (2)$$

When the detection range is considered as 1–15 m, the receiving power is estimated from –84 to –37 dBm. If the gain of the entire receiver including the ABB is over 76 dB, the dynamic range burden of the ADC can be relaxed.

III. CIRCUIT IMPLEMENTATIONS

A. CONFIGURABLE LOCAL OSCILLATOR (LO)

The chirp generator is used for generating a linearly modulated frequency, which has been realized using a DDS or frequency division-ratio control in a PLL. The advantage of DDS is that it has a high frequency resolution and fast response time. However, the output frequency of the DDS is generated by accumulating the phase of a high-speed external clock, and the power consumption increases due to this clock. In addition, the chip size increases due to the higher order LPF for removing the harmonics of the DDS output signal. To overcome the drawbacks of the DDS, the proposed radar transceiver adapted the division ratio control of the fractional-N PLL [10].

The block diagram of the proposed chirp generator is shown in Figure 3. In the proposed chirp generator, an FSG is added to a fractional-N PLL to control the frequency division ratio. The FSG linearly changes the division ratio of the PLL with external control parameters. The parameter of PD determines whether the FSG is operating or not. The parameters of $Mode$, D , M , and K are used to define the shape of the chirp. When the FSG is activated, the LO provides a chirp signal for an FMCW radar mode. The FSG repeatedly adds or subtracts the fractional value F_code of the sigma-delta modulator (SDM) with $\pm\alpha$. If the FSG is not activated, the frequency division ratio is fixed, and the LO provides a single frequency signal for Doppler radar mode. Figure 4 shows a

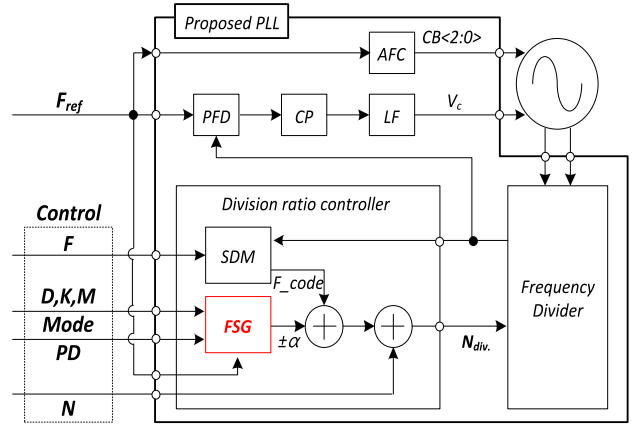


FIGURE 3. The block diagram of the proposed chirp generator using a fractional-N phase-locked loop and frequency sweep generator.

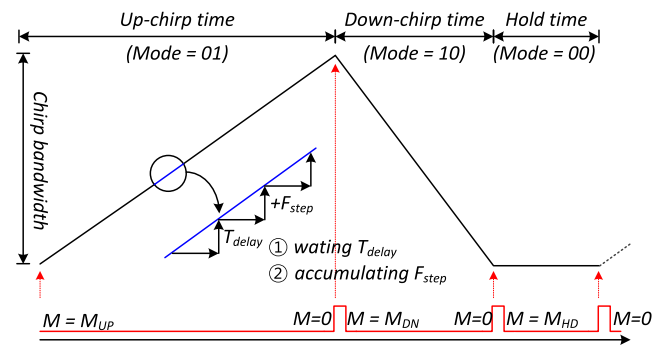


FIGURE 4. A linear frequency modulated waveform.

chirp waveform for FMCW radar mode. The mode M in FSG has three states: up chirp, down chirp, and hold. It repeats the wait for a fixed time T_{dealy} and accumulation of a frequency F_{step} . By changing the mode, a variable chirp waveform can be generated.

The block diagram of the FSG is described in Figure 5(a). The FSG is composed of a delay counter, accumulator, step counter, shift register, and shift register controller. The input of the FSG is a 32-bits digital code, which is stored in the shift register. MSB 2-bits $Mode$ determines the chirp mode, and the next 16-bits represent the repeating number of steps (M). The 6-bits are used to control T_{delay} (D) and the last 8 bits are used to determine F_{step} (K). In Figure 5(b), the timing chart of the FSG is explained. The delay counter generates D_{CLK} after counting the rising edge of the reference clock by the set value (D). T_{delay} is equal to the period of D_{CLK} . If the set value (K) of the accumulator is 1, the output frequency of the LO will change by the resolution of the PLL. The step counter counts the rising edge of D_{CLK} by the total step (M), and then generates S_{CLK} . When S_{CLK} occurs, the shift register controller is ready to generate the down chirp because a chirp has ended. The shift register controller checks the $Mode$ when the rising edge of S_{CLK} occurs and automatically changes the value of each counter and accumulator.

The FSG consumes less power because it operates at a lower frequency than a DDS that uses a high-speed clock.

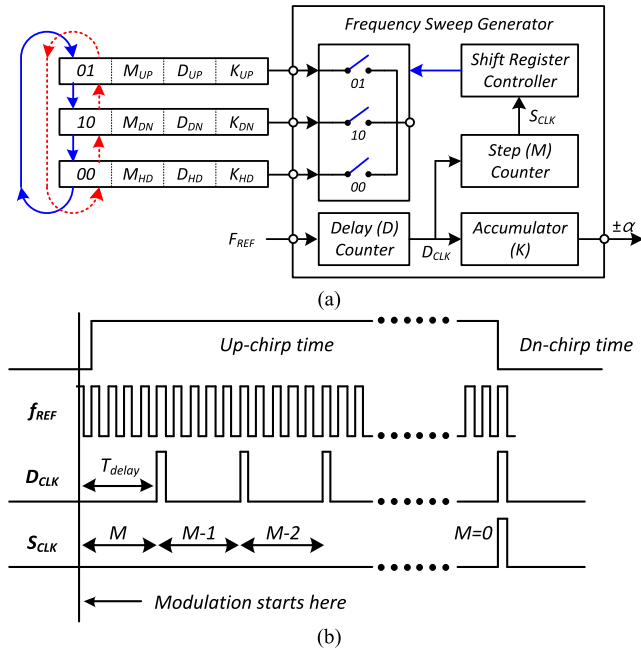


FIGURE 5. (a) the block diagram and (b) timing chart of the FSG.

TABLE 1. Specifications of the proposed PLL.

Category	Specification
Output frequency range (GHz)	9.7 to 12.3
Reference clock frequency (MHz)	38.4
PLL loop bandwidth (kHz)	500
PLL in-band phase noise (dBc/Hz)	-80
Chirp time (ms)	0.1 to 1
Chirp bandwidth for X-band (GHz)	10.5 to 10.55
Maximum chirp bandwidth (MHz)	750 (@ 0.8 ms chirp time)
Frequency resolution (Hz)	293

In addition, the FSG is implemented with simple low-speed digital circuits such as counter, accumulator, and shift register. Thus, the required additional chip area is small.

The VCO employs a 3-bit capacitor bank to enlarge the operating frequency range. The code of the capacitor bank is determined by automatic frequency calibrator (AFC), and the frequency tuning range of the VCO is 9.7–12.3 GHz. The frequency divider consists of current-mode logic (CML) and multi-modulus frequency dividers. For the fractional division ratio, a 1-1-1 multi-stage noise shaping (MASH) 20-bit SDM is used. The reference clock is 38.4 MHz, and the frequency resolution of the PLL is 293 Hz. Considering the nonlinearity and the accuracy problem, the loop bandwidth of the PLL is 500 kHz and the in-band phase noise performance is about -80 dBc/Hz [28]–[32]. The specifications of the proposed dual-mode PLL are summarized in Table 1.

B. CONFIGURABLE RECEIVER

In order to implement a dual mode radar on a single chip, the receiver is designed to change its configuration according

to the radar mode. In the Doppler radar mode, a double-conversion technique is employed to relax the DC offset problem. In the FMCW radar mode, a direct-conversion technique is used and an analog baseband and 1/R⁴ range compensation filter that occupy a large chip area are integrated on a chip using biquad LPF and DCOC structures. Thus, the entire radar transceiver can be implemented on a single integrated chip (IC).

1) DOPPLER MODE

The Doppler frequency is the frequency difference between the RX and TX, which is so small, usually less than 100 Hz, that it is very difficult to distinguish the Doppler signal from the DC offset without using a several μF or greater capacitor. The DC offset is originated from TX-to-RX leakage, LO-to-RX leakage, and the differential mismatch of the mixer in the FE. the proposed transceiver introduces a double-conversion technique using frequency chopping to remove the DC offset at the FE.

Figure 6 shows the block diagram of the proposed RX in Doppler radar mode. Compared to a direct-conversion receiver composed of LNA, mixer and ABB, the proposed architecture uses an additional second mixer and LO chopping mixer. The IQ generator produces quadrature LO signals. The quadrature LO signals, f_{LO} are mixed with the quadrature chopping signals, f_{CH} in the LO chopping mixer. Consequently, the frequency of the LO shifts to f_{LO} + f_{CH}. The chopping frequency is generated by dividing the frequency of the external crystal oscillator by 16 times in the on-chip frequency divider.

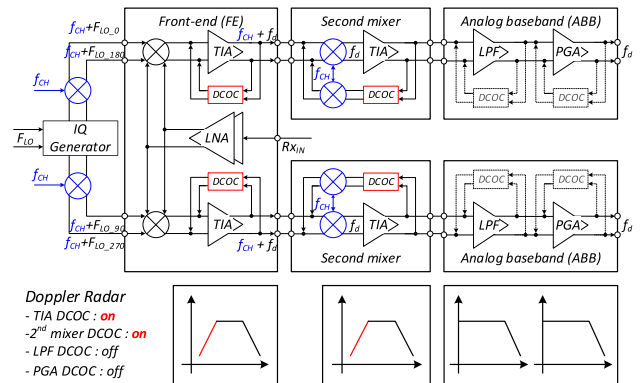


FIGURE 6. The block diagram of the receiver when the proposed configurable RX operates as a Doppler mode.

The FE consists of a two-stage LNA, passive mixers, and TIAs with DCOC. The second mixer includes passive mixers and TIAs with DCOCs. The TIA and DCOC used in the FE and second mixer have the same structure. The ABB comprises biquad LPFs and PGAs. The frequency conversion in the proposed receiver chain is illustrated in Figure 7. In a conventional direct-conversion receiver, the Doppler information is converted to a frequency, f_d near DC frequency at the output of the mixer. Thus, a very large series capacitor is usually required before the baseband amplifier stage. The capacitor

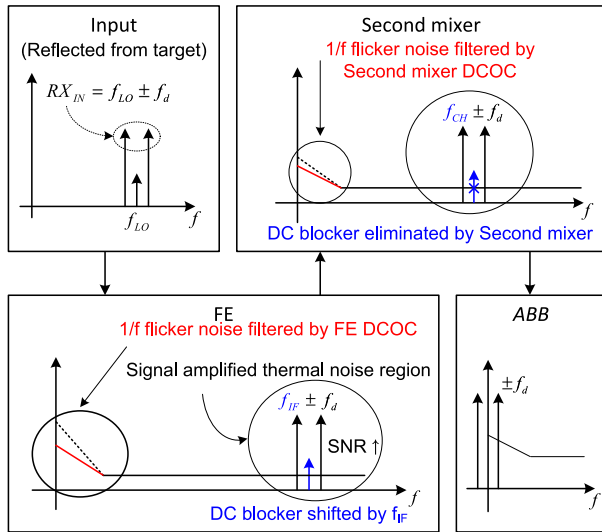


FIGURE 7. The explanation about advantages of Doppler radar.

is usually realized on the PCB not on the chip because of large capacitance. The proposed receiver upconverts the dominant DC offset that comes from TX to RX leakage to a chopping frequency, f_{CH} using LO chopping technique, and eliminates it in the second mixer. The DC output of the second mixer is feedback to the input through up-mixers and subtracted with the upconverted DC offset. Since the DC offset rejection occurs at the chopping frequency, not at the DC frequency, the proposed receiver structure does not require large capacitors, so a fully-integrated receiver can be implemented without large off-chip capacitors.

Since the Doppler signal in the proposed receiver has more gain through the double-conversion with the FE and second mixer than through direct-conversion before down-converted to the baseband frequency, high receiver's NF can be achieved as well as high SNR. Since the chopping frequency is higher than the flicker corner frequency, the influence on the flicker noise of the ABB is also reduced, so that the false alarm rate (FAR) of the sensor can be lowered in the Doppler mode. In Doppler mode, the DCOCs of the FE and second mixer are enabled and the DCOCs in the ABB is disabled. This is because the FE and the second mixer handle high frequency signals, but the ABB handles lower frequencies than the DCOC's cut-off frequency.

Figure 8 shows the schematic of two-stage LNA, in which the transformer parameters used in the inter-stage and output stage are given. All inductors for the input and output matchings are designed using transformers. The input transformer acts as a single-to-differential converter. Although this transformer has a matching loss due to the coupling factor, it entails several advantages in LNA design: First, the DC blocking capacitors in the bias circuits can be removed. Second, wideband matching is possible. Finally, electrostatic discharge (ESD) problems at the input port can be avoided because the DCs between the internal LNA input node and the external RF input pad are isolated.

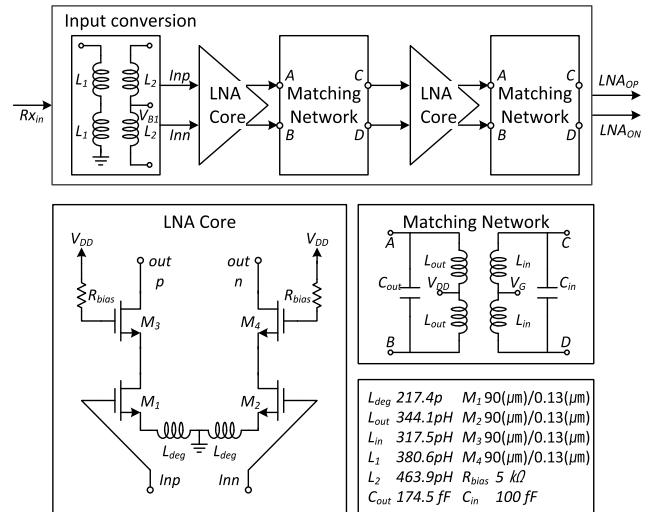


FIGURE 8. The block diagram and schematic of two-stage LNA.

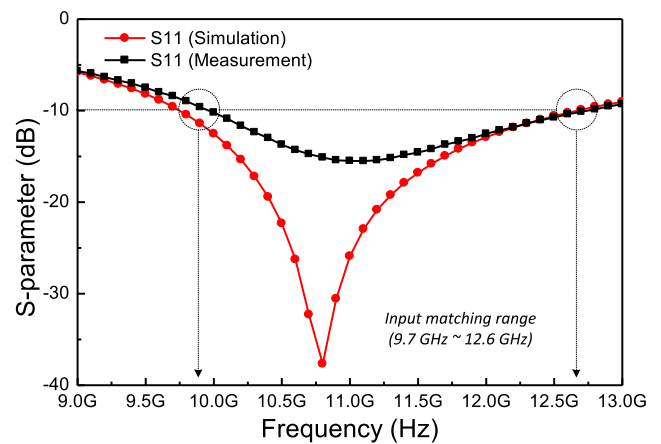


FIGURE 9. The simulation and measurement results of the 2-stage LNA input matching.

Figure 9 shows the simulation and measurement results of the LNA input matching. The red line is the simulation result. The measurement results of the LNA are obtained by using an LNA test circuit. The input matching of the LNA is represented by S_{11} . The frequency range where S_{11} is less than -10 dB is 9.7–12.6 GHz. Figure 10 shows the NF simulation results of the transceiver with and without the LO chopping technique. When operating as Doppler radar, the NF improvement is from 3 to 5 dB in the detection frequency range. As the NF increases, the SNR of the detected signal decreases. The SNR affects the probability false alarm and detection in the radar. Assuming the same false alarm probability, a 3-dB improvement in SNR dramatically increases the detection probability [27].

Figure 11 shows the block diagram of a TIA with DCOC. The gain of the FE is controlled by changing the feedback resistor, R in four steps. When changing R , the cut-off frequency of the TIA also changes according to the following

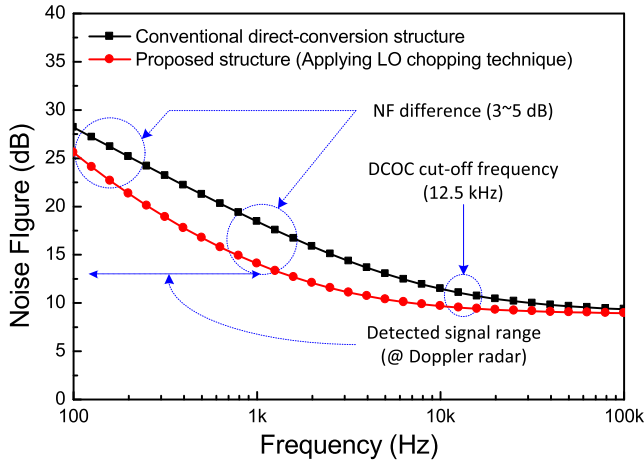


FIGURE 10. The NF simulation results of the radar transceiver with and without the LO chopping technique.

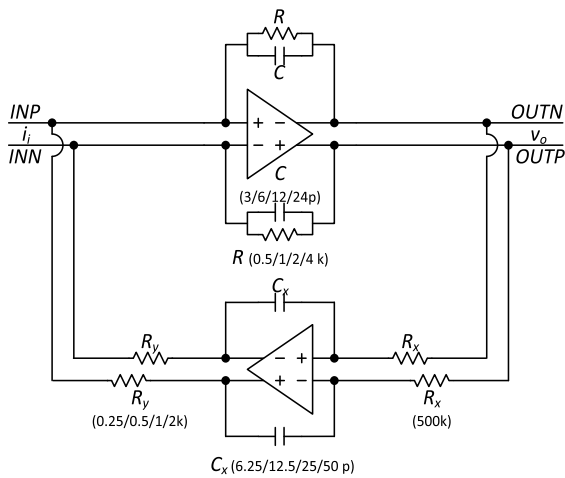


FIGURE 11. The block diagram of the TIA with DCOC.

transfer-function.

$$A_{TIA} = \frac{v_o}{i_i} = \frac{R}{sCR + 1} \quad (3)$$

Therefore, to change the gain while maintaining the cut-off frequency, the value of C must be decreased by an increment of R . If the feedback resistor R is doubled and the feedback capacitor C is reduced in half, the gain of the TIA increases by 6 dB while the bandwidth is fixed.

Additionally, when the DCOC is enable, the cut-off frequency of the DCOC should not be varied when changing the gain step of the TIA. The cut-off frequency of the DCOC can be calculated by the overall gain transfer-function including DCOC.

$$A_{TIA_DCOC} = \frac{sC_x R_x R_y}{s^2 C C_x R_x R_y + s \frac{C_x R_x R_y}{R} + 1} \quad (4)$$

The gain transfer-function has two poles and one zero. Since there is one zero at the origin, the cut-off frequency of the DCOC is determined by the first pole location. If all the

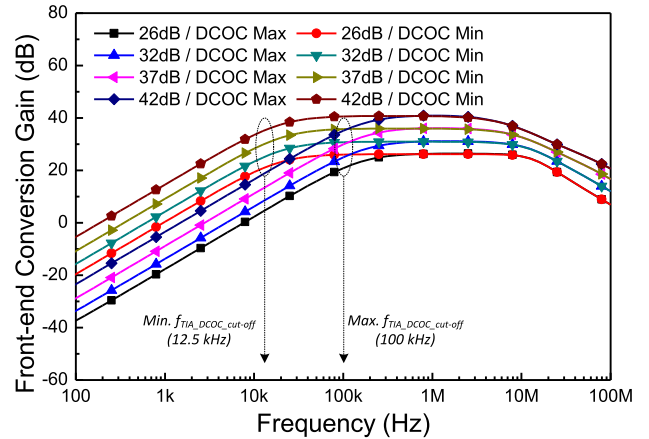


FIGURE 12. The simulation result of the FE gain with DCOC operation.

poles are existing in the real axis and the second pole is much larger than the first pole, the first pole frequency is calculated as follows:

$$f_{TIA_DCOC_cut-off} = \frac{1}{2\pi} \times \frac{R}{C_x R_x R_y} \quad (5)$$

The ratio of R and R_y must be kept constant to maintain the DCOC cut-off frequency constant while controlling the gain of the TIA. Also, to change the DCOC cut-off frequency while the gain of the TIA is fixed, R_x or C_x must be changed. Since the R_x resistor must hold a large value to sense only the DC voltage, C_x is implemented as a variable capacitor. The DCOC cut-off frequency can be calculated by substituting the values of R_x , C_x , R_y , R shown in Figure 10.

Figure 12 shows the simulated FE conversion gain with DCOC cut-off frequencies of 12.5 kHz and 100 kHz. Both high and low cut-off frequencies are kept constant when changing the gain step. The range of the FE conversion gain is 26 to 42 dB in 6 dB steps. In addition, the cut-off frequency of the DCOC can be changed from 12.5 to 100 kHz by doubling the previous cut-off frequency. Figure 13 shows the transient output voltage waveforms in the TIA. To verify the recovering capability of the DCOC in the worst case, a maximum available DC offset is created by setting equal LO and RX frequencies and increasing the RF power. Initially, the output voltage difference of the TIA increases to the maximum DC offset of about 800 mV, but the DC offset is reduced and eliminated by the DCOC after 30 μ sec.

2) FMCW RADAR MODE

The detection power in the radar receiver depends on the distance between the radar and the object as given in equation (1). Even with the same RCS, the detected power is higher than with distant objects. Thus, the gain should be reduced so that the FE does not saturate due to the signal reflected from a nearby object. Additionally, it is necessary to keep the SNR constant according to the distance. A range compensation filter with high-pass filtering characteristic performs this role in the FMCW radar. As shown in

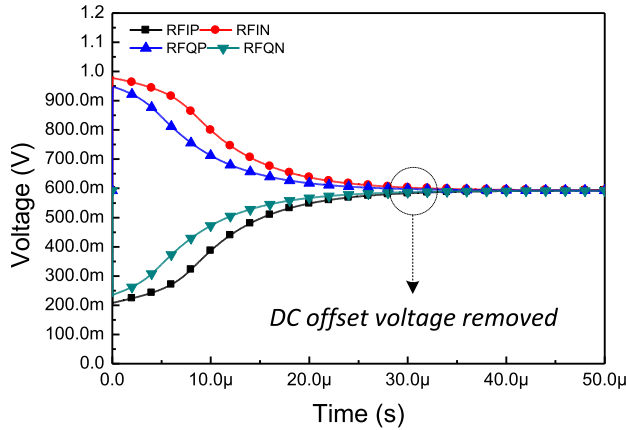


FIGURE 13. The simulation result of the DCOC operation in time domain.

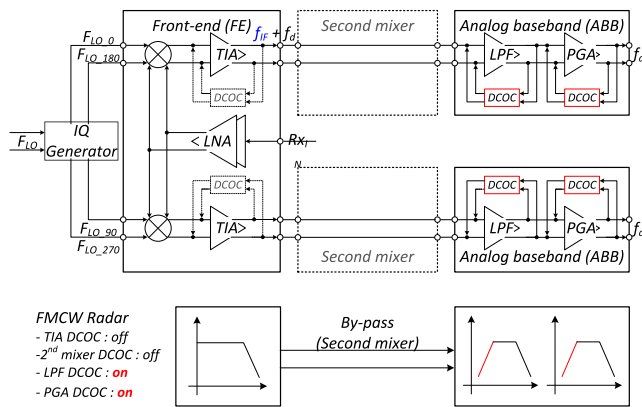


FIGURE 14. The block diagram of the receiver when operating as a FMCW radar.

equation (2), a range compensation filter with a 40-dB slope is required.

Figure 14 shows the block diagram when the proposed configurable RX operates in FMCW mode. The difference between the FMCW mode and the Doppler mode is that the LO chopping mixer is not used and the second mixer is bypassed. Also, since the frequency response of one-step DCOC is the same as that of HPF with a 20-dB slope, the DCOCs of the LPF and PGA are used to implement the range compensation filter. The on-chip range compensation filter is realized by selectively turning on and off the DCOCs via SPI.

The ABB consists of a biquad LPF and a PGA. The ABB gain is variable with 6 dB step up to 36 dB. Figure 15 and Figure 16 show the block diagrams of a biquad LPF and PGA with DCOC, respectively. The transfer-function of biquad LPF is as follows:

$$A_{LPF} = \frac{v_o}{v_i} = -\frac{R_3}{R_1} \times \frac{1}{s^2 + s\frac{1}{CR_4} + \left(\frac{1}{C\sqrt{R_2R_3}}\right)^2} \quad (6)$$

where the gain of the LPF is controlled by the ratio of R_1 and R_3 , and the cut-off frequency of the LPF is determined by the feedback capacitor C , R_2 and R_3 . The overall

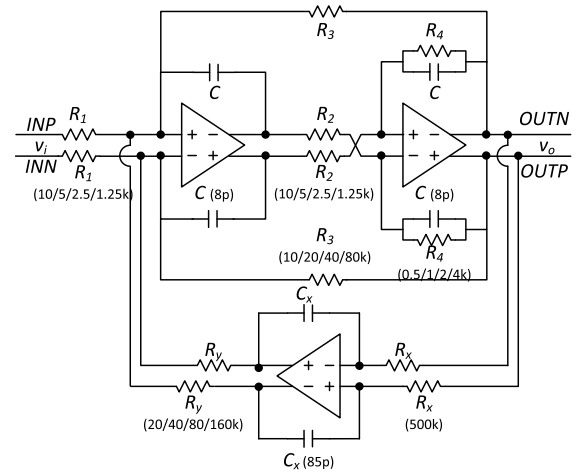


FIGURE 15. The block diagram of the biquad LPF with DCOC.

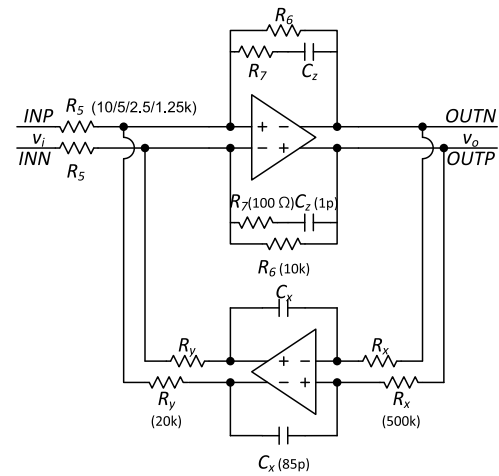


FIGURE 16. The block diagram of the PGA with DCOC.

transfer-function including DCOC is as follows:

$$A_{LPF_DCOC} = -\frac{R_3 \cdot \frac{1}{s^2 C^2 R_2 R_3 + s \frac{R_2 R_3}{R_4} C + 1}}{1 + R_3 \cdot \frac{1}{s^2 C^2 R_2 R_3 + s \frac{R_2 R_3}{R_4} C + 1} \cdot \frac{1}{s C_x R_x R_y}} \quad (7)$$

Assuming that the cut-off frequency of the DCOC is determined by the first pole, and this pole is much smaller than the other two poles, equation (7) is expressed as:

$$A_{LPF_DCOC} \cong -\frac{s R_1 C_x R_x R_y}{s \frac{C_x R_x R_y}{R_3} + 1} \quad (8)$$

The DCOC cut-off frequency is determined by C_x , R_x , R_y , and R_3 . Even if the gain step of the LPF changes, the ratio of R_3 and R_y must be kept constant to fix the DCOC cut-off frequency. The transfer-function of the PGA is as follows:

$$A_{PGA} = -\frac{R_6}{R_5} \times \frac{s C_2 R_7 + 1}{s C_z (R_6 + R_7) + 1} \quad (9)$$

where the gain of the PGA is controlled by the ratio of R_5 and R_6 , and the bandwidth is determined by R_6 , R_7 and C_z .

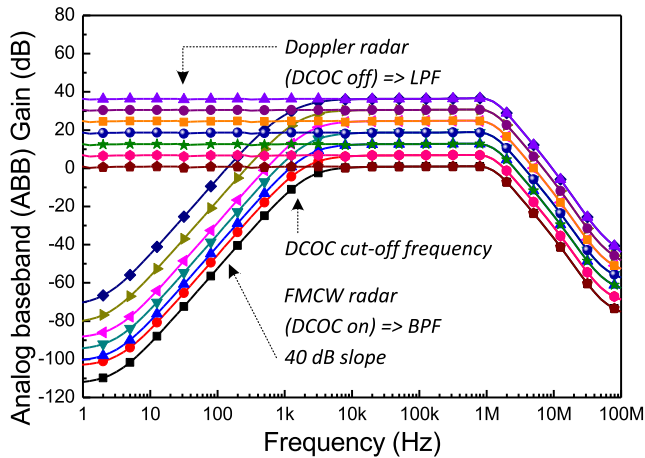


FIGURE 17. The simulation results of the ABB with or without DCOC operation.

Since the product of C_z and R_6 is negligibly small, the total transfer-function including DCOC is as follows:

$$A_{PGA_DCOC} = \frac{sC_x R_x R_y R_5}{s \frac{C_x R_x R_y}{R_6} + 1} \quad (10)$$

The DCOC cut-off frequency is not changed because R_6 , R_y , R_x , C_x are fixed. Also, this value is equal to the DCOC cut-off frequency of the LPF. The gain of the PGA is only controlled by R_5 with fixed value R_6 .

Figure 17 shows the simulated gains of the ABB with and without DCOC operation. The frequency characteristic of the ABB is changed to BPF or LPF depending on the state of the DCOC. All DCOCs included in the ABB are designed to have the same cut-off frequency. The cut-off frequency of the LPF and PGA calculated using the transfer function is about 1.85 kHz. The cut-off frequency of the DCOC is 1.85 kHz. The gain graph has a low frequency slope of +40 dB/decade. Since the cut-off frequency of the DCOC is so low, the size of the required capacitors for the DCOC takes up a large part of the ABB. Thus, the stacked metal-insulator-metal (MIM) and metal-oxide semiconductor (MOS) capacitors are used together to increase the capacitor density and reduce the chip size.

IV. MEASUREMENT RESULTS

The proposed single-chip multi-function X-band radar transceiver that has a configurable receiver was implemented using 1P8M 130-nm CMOS technology as shown in Figure 18. The top metal (M8) and second metal (M7) layers were used in the design of the transformer, high frequency signal interconnection, and power line. The proposed radar transceiver was glued onto a PCB and gold-bonded in a chip-on-board (COB) form. The chip size, including all pads, was 7.68 mm². All the pads including the RF pads are electro-discharge (ESD) protected. A 3.3-V supply voltage is applied to the internal LDOs, which distribute the required voltages to each core circuit. The total power consumption is 216 mW

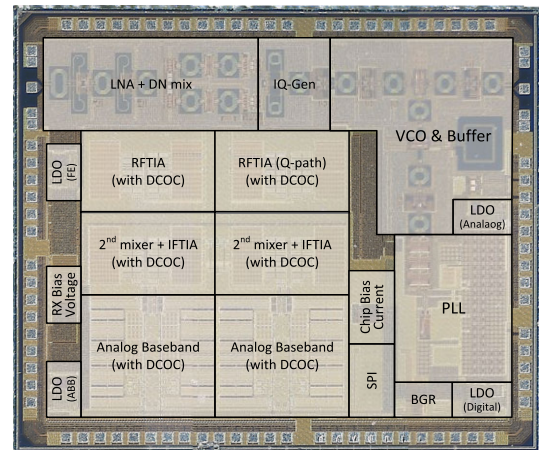


FIGURE 18. The photograph of the proposed single-chip X-band radar transceiver.

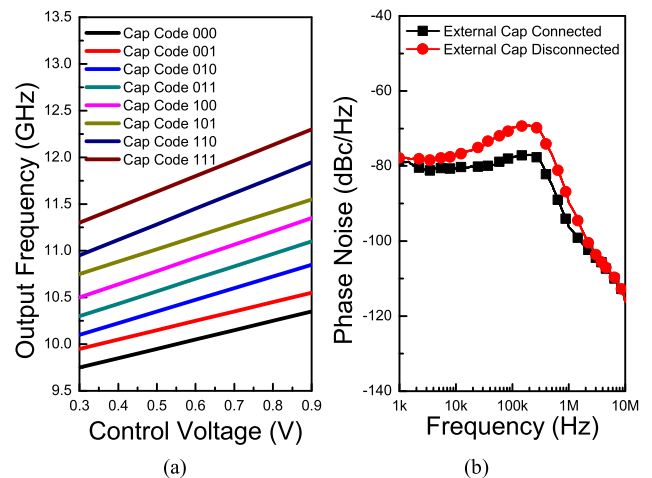
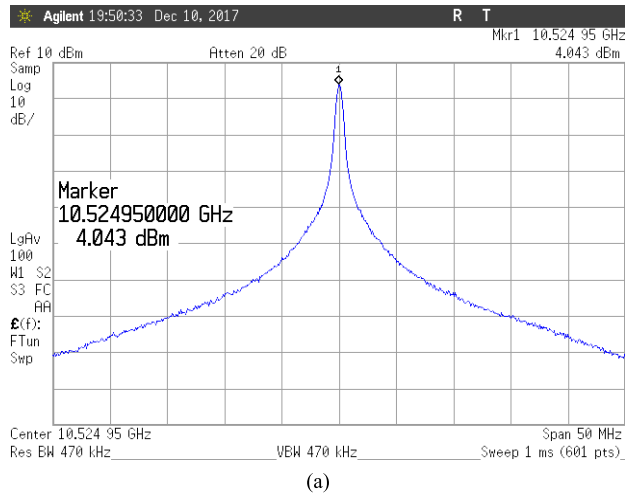


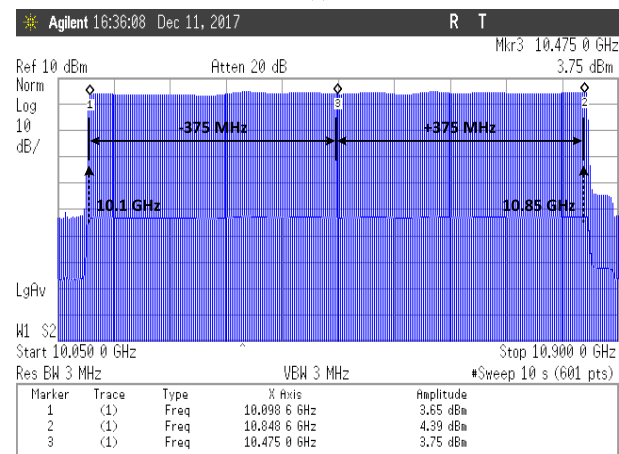
FIGURE 19. (a) The measured output frequency range and the phase noise plot at the frequency of 10.525 GHz.

for Doppler radar and 201.6 mW for FMCW radar. To isolate the internal power of each block, an LDO is used for each of the analog and digital circuits of LO, FE, and ABB.

The output frequency spectrum and the phase noise plot are measured by an Agilent E4440A spectrum analyzer. Frequency modulation waveforms in the time domain were obtained by Keysight E5052B signal source analyzer. The measured output frequency range was from 9.7 GHz to 12.3 GHz under 1.2-V supply voltage conditions. As shown in Figure 19(a), A 3-bit capacitor bank was employed in the VCO to enlarge the operating frequency range. The gain of the VCO increased due to the influence of the parasitic capacitance. Figure 19(b) shows the phase noise plots measured at the frequency of 10.525 GHz. The red line shows that the VCO phase noise degrades near the 100 kHz offset frequency due to the influence of the BGR noise. The black line is the phase noise plot after connecting a 10- μ F capacitor from the outside to reduce BGR noise. The phase noise within the loop bandwidth of about 500 kHz is < -80 dBc/Hz.



(a)



(b)

FIGURE 20. The measurement results of the dual-mode LO output frequency when operating as (a) a Doppler radar and (b) a FMCW radar.

Figure 20 shows the measurement results of the dual-mode LO in the frequency domain. When operating as Doppler radar, the fixed-output frequency is generated as shown in Figure 20(a). Figure 20(b) shows a chirp spectrum with the modulation bandwidth of 750-MHz, which is the maximum bandwidth for a FMCW radar. Figure 21 shows the measured frequency and frequency error in the time domain when the up- and down-chirp period is 800 μ sec and the modulation bandwidth is 750 MHz. The root-mean square (RMS) frequency error appears periodically because the frequency error has different polarity in up-chirp and down-chirp. The RMS frequency error is estimated by subtracting the measured frequency with targeted frequency. The RMS frequency error is ± 2.94 MHz. Therefore, the measured waveform has an almost constant frequency difference from the ideal graph due to constant time delay.

Figure 22(a) illustrates the measured receiver gain when the DCOC is on and off. The cut-off frequency of the DCOC is 12.5 KHz. Also, since the DCOC of the FE and the Second mixer are used, a 40-dB slope appears. Figure 22(b) shows the measured gain graph of the receiver under the condition

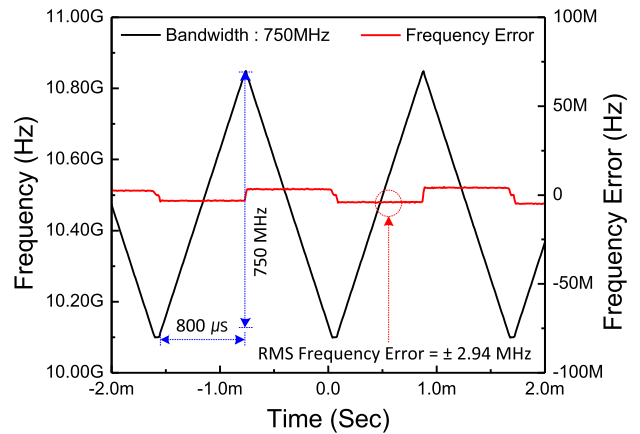
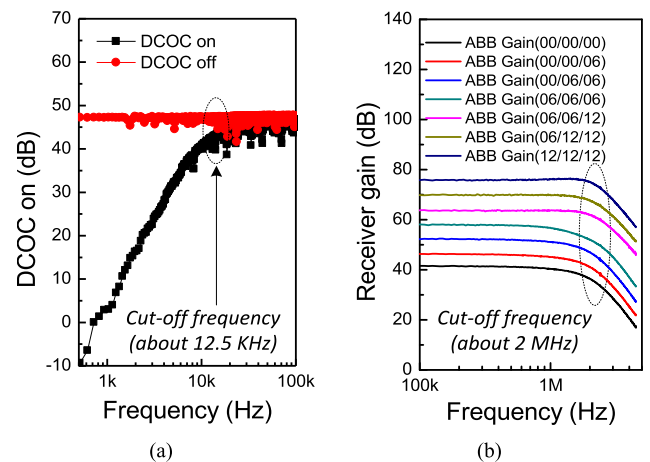


FIGURE 21. The measurement result of the frequency modulated wave form in time domain.



(a)

(b)

FIGURE 22. The measurement result of the receiver gain operating as a Doppler mode whether the DCOC is operated (a) or not (b).

that the FE gain is 32 dB and the second mixer gain is 10 dB without DCOC operation. Since the gain of ABB is adjustable from 0 to 36 dB in 6 dB steps, the range of the receiver gain is 42 dB to 78 dB. The measured cut-off frequency is the same as the result from the calculation and simulation.

Figure 23 shows the measurement results of the NF in Doppler radar whether the LO chopping technique is used or not. The NF performance varies from 3 to 5 dB in the region where the Doppler frequency exists. Since the SNR of the detected signal increases more than 3 dB, the false alarm rate (FAR) performance can be improved in the Doppler radar.

Figure 24(a) shows the measurement result of on-chip range compensation filter cut-off frequency using DCOC. As expected, a 40-dB slope appears at 1.85 kHz which is the cut-off frequency of the DCOC. Figure 24(b) shows the measured gain graph of receiver when operating as FMCW radar. Because the second mixer is not used, the gain of the receiver is measured as low as 10 dB compared to the Doppler mode. A loopback test was performed to verify the operation of the FMCW radar. The loopback cable length between the TX and the RX was set to 10 m. Fig. 25 shows a

TABLE 2. Comparison of ever reported researches.

Reference	This study	[11]	[16]	[18]	Unit	
Process	130 nm CMOS	130nm CMOS	130nm SiGe	180nm CMOS	nm	
Feature	Fully-integrated (LO+FE+ABB)	Only LO	(LO+FE+ABB+ADC)	(FE+PA ¹ +VCO)		
Radar function	Doppler FMCW	FMCW	FMCW	FMCW ²)	-	
Frequency range	9.7 ~ 12.3	9.7 ~ 12.3	8.2 ~ 8.25	8 ~ 9	10 ~ 10.5	GHz
Chirp bandwidth (Chirp time)	-	750 (0.8 ms)	50 (0.1 ms)	50 (N/A)	50 (N/A)	MHz
RMS Chirp error	-	±2.94	N/A	N/A	N/A	MHz
PLL loop bandwidth	500	500	500	100	N/A	kHz
Phase noise @1 MHz	-96.25	-98.85	-98.85	-114	-93	dBc/Hz
Receiver gain	40 ~ 76	32 ~ 68	N/A	10.7 ~ 44.7 ³)	-4.5 ³)	dB
Receiver NF	15 ~ 25	8 ~ 9	N/A	N/A	11.5	dB
Power	216	201.6	N/A	333 ⁴) / 326 ⁵)	350	mW
Area	7.68	5.04	5.04	8.75	8.58	mm ²

¹)Power amplifier; ²) Using external PLL and DDS; ³) Only FE gain; ⁴) TX mode; ⁵) RX mode;

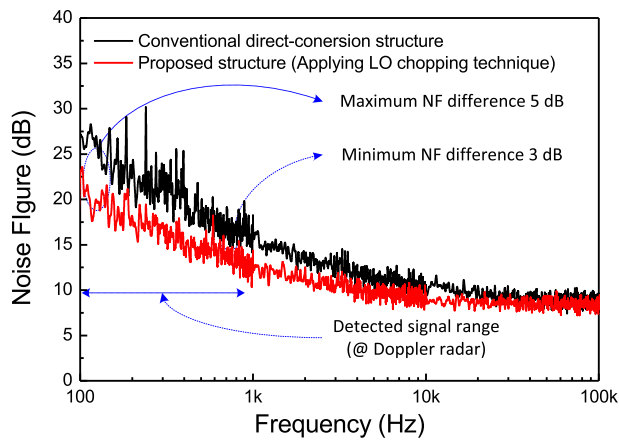


FIGURE 23. The measurement results of the NF in Doppler radar whether the LO chopping technique is used or not.

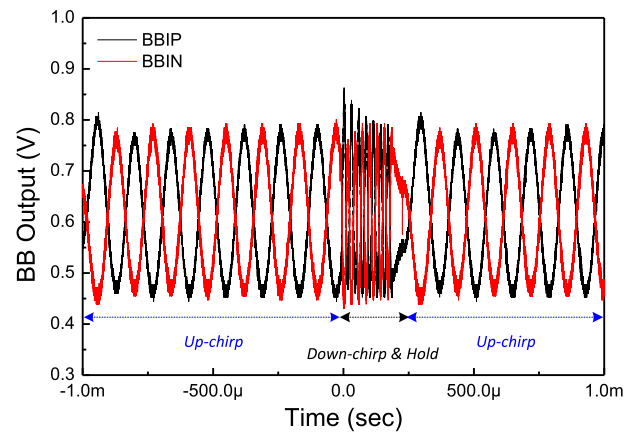


FIGURE 25. The measured output waveform of the ABB in time domain when operating as a FMCW radar.

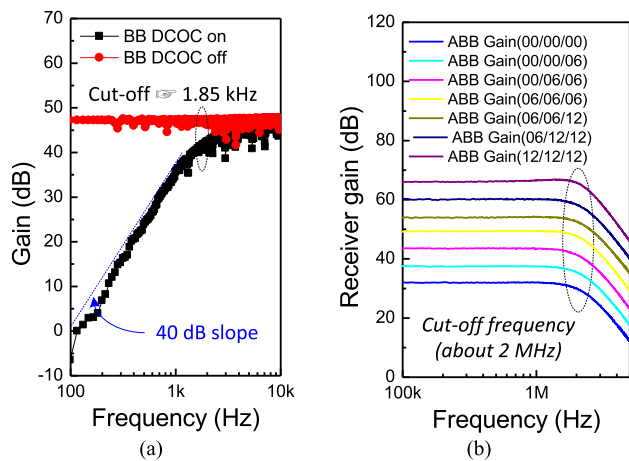


FIGURE 24. The measurement result of on-chip range compensation filter cut-off frequency using DCOC and receiver gain when operating as FMCW radar.

measured voltage waveform of the ABB output in the time domain, which is obtained using an oscilloscope with the up-chirp time of 1 ms and the down chirp and hold time

of 232 μsec. The differential output signals have a common mode of 600 mV due to the DCOC circuit.

The performance of the proposed structure is summarized and compared with other similar works in Table 2. As shown in this table, the proposed radar transceiver shows better performance in terms of power consumption, chirp bandwidth and chip size compared to the SiGe process [16].

V. CONCLUSION

In this paper, a fully-integrated dual-mode X-band radar transceiver using configurable RX and LO is proposed. The proposed LO is implemented by adding FSG blocks to the fractional-N PLL using a method that controls the division ratio of the PLL. The proposed LO can reduce power consumption and chip size compared to using DDS-based structures, and it is also easy to control dual-mode. The configurable RX can be changed to a structure suitable for Doppler radar or FMCW radar. In the Doppler radar, DC blocker can be removed, and NF performance is also improved by using an LO chopping technique. In FMCW radar, the on-chip range compensation filter is implemented

by using DCOC. The power consumption is 216 mW for Doppler radar and 201.6 mW for FMCW radar, respectively. The chip size of the proposed structure is 7.68 mm² including all pads. The proposed dual-mode X-band radar transceiver represents an excellent solution for numerous motion sensor applications.

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