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Effects of heat dissipation on unipolar resistance switching in Pt/NiO/Pt capacitors

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We fabricated Pt/NiO/Pt capacitor structures with various bottom electrode thicknesses t_{BE} and investigated their resistance switching behaviors. The capacitors with $t_{BE} \geq 50$ nm exhibited typical unipolar resistance memory switching, while those with $t_{BE} \leq 30$ nm showed threshold switching. This interesting phenomenon can be explained in terms of the temperature-dependent stability of conducting filaments. In particular, the thinner t_{BE} makes dissipation of Joule heat less efficient, so the filaments will be at a higher temperature and become less stable. This study demonstrates the importance of heat dissipation in resistance random access memory. © 2008 American Institute of Physics. [DOI: 10.1063/1.2924304]

Resistance switching phenomena, which are observed in numerous materials,[1] have recently regained a great deal of attention due to their potential application in nonvolatile memory devices called resistance random access memory (RRAM).[2–8] Achieving good scalability is an important issue for meeting the current demands for device miniaturization.[9] One of the important scalability issues is reducing the bottom electrode thickness t_{BE} to make the etching process easier.[10]

Many binary oxides such as NiO, TiO_2, and Fe_2O_3 exhibit unipolar resistance switching.[5–8] Although the mechanism is still somewhat ambiguous, it is widely accepted that unipolar resistance switching is due to the formation and rupture of conducting filamentary paths under external bias.[6,7,9,11,12] It is also generally assumed that the rupturing process of the conducting filaments may be closely related to Joule heating.[6,12] If this is true, we could control Joule-heating effects in unipolar resistance switching by changing the thermal transport properties of the RRAM device structure, which is typically made with metal/oxide/metal. In particular, t_{BE} could significantly affect the thermal heat dissipation process through the bottom electrode.

In this letter, we investigated resistance switching behaviors of Pt/NiO/Pt capacitor structures as a function of t_{BE}. Due to its finite size and low thermal convection through air, the top electrode is much less efficient in heat dissipation than the bottom electrode. We found that our capacitors with $t_{BE} \leq 30$ nm exhibited volatile resistance switching behaviors called threshold switching. On the other hand, all capacitors with $t_{BE} \geq 50$ nm exhibited typical unipolar memory switching behaviors. We explained this interesting t_{BE} dependence in terms of the thermal stability of conducting filamentary paths, which are closely related to heat dissipation through the bottom electrode. This result indicates that thermal heat dissipation through the electrodes is crucial for RRAM, just

as it is for phase change random access memory.[13]

We fabricated Pt/NiO/Pt capacitor structures by growing polycrystalline NiO films on $Pt/TiO_x/SiO_2/Si$ substrates. We used e-beam evaporation to deposit the Pt bottom electrode layers with a t_{BE} of 10–50 nm. For thicker Pt bottom electrodes with a t_{BE} of 50–200 nm, we used commercially available platinized silicon substrates (Inostek Inc., Seoul, Korea) that were grown by sputtering. The microstructure and electrical conductivity of sputtered Pt layers were found to be quite similar to those of evaporated Pt layers. Our atomic force microscopy showed that all of the Pt films have nearly the same root-mean-square roughness of about 1.2 nm. The thinnest Pt layer with $t_{BE} = 10$ nm had an electrical conductivity of $2.16 \times 10^6 \ \Omega^{-1} \text{m}^{-1}$ at 300 K, which is comparable to the bulk Pt value of $9.26 \times 10^6 \ \Omega^{-1} \text{m}^{-1}$.[14] We deposited Ni films on these substrates by using e-beam evaporation and oxidized them into NiO layers by using thermal oxidation at 450 °C at ambient air pressure for 1 h.[15] The NiO layers were approximately 60 nm thick. For the top electrodes, we deposited Au and Pt layers (30 and 10 nm thick, respectively) by using e-beam evaporation with a shadow mask. All of the Pt/NiO/Pt capacitors used in this study had an electrode area of $46 \times 46 \ \mu\text{m}^2$.

We investigated the resistance switching characteristics of our Pt/NiO/Pt capacitors by measuring the current-voltage (I-V) curves with a conventional two-probe measurement system (Agilent 4155C semiconductor parameter analyzer, Agilent Technologies, Santa Clara, CA). To avoid a complete dielectric breakdown, we used a compliance current to set a limit to the current flow.

Interestingly, we observed two types of unipolar resistance switching behaviors in our Pt/NiO/Pt capacitors: memory and threshold switchings. As shown in Fig. 1(a), a capacitor with $t_{BE} = 150$ nm has an I-V curve typical of resistance memory switching. When we increased V, the resistance changed to a low-resistance state (LRS) at the setting

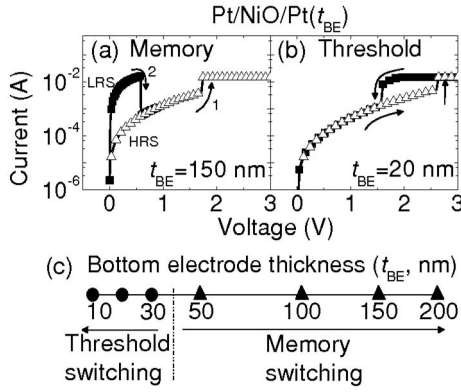a)Author to whom correspondence should be addressed. Electronic mail: twnoh@snu.ac.kr.

FIG. 1. Resistance switching behaviors of Pt/NiO(60 nm)/Pt capacitors with an area of 46×46 μm^2. (a) A capacitor with $t_{BE}=150$ nm shows typical unipolar resistance memory switching behavior, while (b) a capacitor with $t_{BE}=20$ nm shows threshold switching behavior. (c) Types of resistance switching behaviors in terms of the Pt bottom electrode thickness.

TABLE I. Parameter values of the Fourier heat equation for Pt, Au, Ni, NiO, SiO$_2$, and TiO$_2$.

Material	Density ρ (g/cm^3)	Specific heat C_p (J/g K)	Thermal conductivity k (W/cm K)
Pt	22	0.13	0.72
Au	19	0.13	3.2
Ni	8.9	0.44	0.91
NiO	6.7	0.59	0.35
SiO$_2$	2.2	0.74	0.014
TiO$_2$	4.2	0.69	0.13

voltage, which is marked with "1" in the figure. The capacitor was then in a LRS. When we increased V from zero again, it changed to a high-resistance state (HRS) at the resetting voltage, which is marked with "2." We repeated the *I-V* measurements up to 40 times. All of the *I-V* curves showed quite stable memory switchings with reasonable-sized threshold voltage fluctuations, consistent resistance values at both LRS and HRS, and long term stability. On the other hand, a capacitor with $t_{BE}=20$ nm had an *I-V* curve of typical threshold switching, as shown in Fig. 1(b).[5,16] Although this capacitor exhibited an interesting resistance change from the HRS to the LRS, it could not be maintained in the LRS. Therefore, it was not suitable for use as a nonvolatile memory device since it did not have bistable states without an external voltage.

We found that the resistance switching behavior systematically varied depending on the value of t_{BE}. As shown in Fig. 1(c), all of the capacitors with $t_{BE} \leq 30$ nm exhibited threshold switching behaviors, while all of the capacitors with $t_{BE} \geq 50$ nm exhibited resistance memory switching behaviors. This indicates that t_{BE} is a key parameter for controlling the type of resistance switching.

To clarify the origin of the t_{BE}-dependent change of the type of resistance switching, we considered three possibilities: the chemical stoichiometry of the NiO films, the structural and chemical property changes near the bottom electrode interface, and the heat dissipation effects. While most NiO films have resistance memory switching characteristics,[5,12,15,16] there have been several reports of threshold switching in relative Ni-deficient NiO films.[5,16] However, in our case, we deposited Ni films and oxide onto NiO layers under the same conditions. Therefore, a variation in chemical stoichiometry is not a plausible candidate to explain the change in the type of resistance switching illustrated in Fig. 1.

We also investigated cross-sectional images and depth profiles of our Pt/NiO/Pt capacitors by using a transmission electron microscope equipped for energy-dispersive x-ray spectroscopy, although we do not show the results here. We found that the structural properties near the interface between the bottom Pt electrode and the NiO layer do not significantly vary in terms of t_{BE}. In addition, solid-state diffusions of Ni, Ti, O, Pt, and Si ions were found to be rather small. If

such diffusions were significant, the chemical compositions of the top and bottom electrode interfaces would be different, and their junction-related parameters such as the Schottky barrier height would vary.[17] This would mean that the *I-V* characteristics would be asymmetric,[17] which is contrary to our symmetric *I-V* curves along the bias polarity in both samples. Therefore, the structural and chemical properties near the bottom electrode interface do not play an important role.

Joule-heating effects are widely considered to be important for the resetting process, i.e., the change from a LRS to a HRS. Some research has presented an argument based on the time scale of the resetting process. A typical reported value of the characteristic time for the resetting process is a few microseconds for capacitors that are a submicron or larger in size. This is much longer than the characteristic time for the change from a HRS to a LRS, which is typically about 10 ns.[6,9] A relatively long time scale is consistent with a slow thermal process. With a thinner t_{BE}, thermal dissipation through the bottom electrode will decrease so that conducting filaments inside the NiO capacitor can reach a higher temperature and more easily rupture. Therefore, if these Joule-heating effects are significant, they could affect the thermal stability of conducting filamentary channels.[18]

To confirm the t_{BE}-dependent thermal dissipation effects, we calculated a three-dimensional heat flow by solving the following Fourier equation by using finite element analysis[19]

$$\rho C_P \frac{\partial T}{\partial t} = k\nabla^2 T + Q, \tag{1}$$

where ρ, C_p, and k are the density (g/cm^3), specific heat (J/g K), and thermal conductivity (W/cm K), respectively, of the constituents. The parameter Q is the heat flux density (W/cm^3) supplied by the electric current through the conducting filaments. Table I contains the values of the constituents in our NiO capacitors.[14,20] Recently, we observed the formation and rupture of conducting channels by using a scanning probe microscope.[7] The reported size of a conducting channel is typically in the range of 5–70 nm.

Figure 2(a) shows a schematic diagram that we used in our calculations. For the sake of simplicity, we assumed that only one rectangular filament, $30 \times 30 \times 60$ nm^3, is formed inside the capacitor. The top and bottom of the capacitor are in contact with the air and Si substrates, respectively, and all components are assumed to be at a room temperature of 300 K. The resistance of the filament is 30–40 $\mu\Omega$ cm, and it is assumed to be under an external bias of 2 V. In our simulations, we used actual values for the dimensions of the Au/Pt top electrode, NiO, TiO$_2$ adhesion, and SiO$_2$ layers. We calculated two cases with t_{BE} values of 10 and 200 nm.
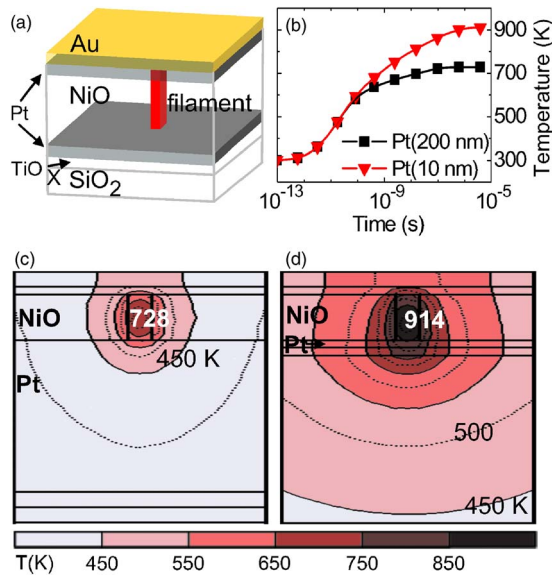
FIG. 2. (Color online) Results of a finite element analysis for thermal distributions inside a NiO capacitor with a conducting filament. (a) A schematic picture showing the sample geometry for Au(30 nm)/Pt(10 nm)/NiO(60 nm)/Pt(10 or 200 nm)/TiO$_x$(10 or 20 nm)/SiO$_2$(1000 or 300 nm) capacitors. A single conducting filament is assumed with dimensions of $30 \times 30 \times 60$ nm^3 located at the center of the capacitor. (b) Time-dependent temperature rise at the center of the filament after the external voltage is applied. Note that the temperature becomes saturated within about 1 μs. [(c) and (d)] Temperature contours for the cases with $t_{BE} = 200$ and 10 nm, respectively.

As shown in Fig. 2(b), the filament's temperature becomes saturated at a time scale of about 1 μs for both cases, which agrees with earlier experimental work.[6,9] Figures 2(c) and 2(d) show contour plots of the temperature gradients in selected cross-sectional areas near the conducting filament for a scale of 320×330 nm^2. The filament temperature for $t_{BE} = 10$ nm is about 910 K, which is approximately 200 K higher than that for $t_{BE} = 200$ nm. This result indicates that the conducting filament could be less thermally stable in a capacitor with a thinner t_{BE}.

Note that the thermal conductivity of SiO$_2$ (0.014 W/cm K) is about 50 times less than that of Pt (0.72 W/cm K). Therefore, the heat dissipation through the thinner bottom electrode should be much less efficient. Figures 3(a) and 3(b) show vector representations of heat flow, i.e., $-k\nabla T$, for the cases of $t_{BE} = 200$ nm and $t_{BE} = 10$ nm, respectively. In Fig. 3(a), the heat flow vectors inside the
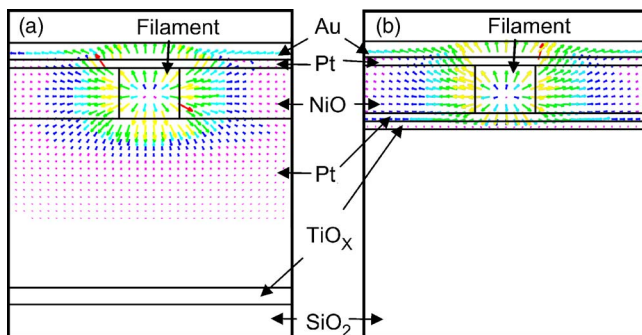
thicker bottom electrode are pointing in nearly every direction and remain significant even for the region about 100 nm below the NiO/Pt interface. On the other hand, in Fig. 3(b), the heat flow vectors inside the thinner bottom electrode are mostly confined to a very narrow region near the bottom electrode, indicating that heat dissipation occurs through the thin bottom electrode and is very inefficient. These simulation results suggest the importance of parameters that control the heat dissipation process in real RRAM devices such as t_{BE}.

In summary, we found that the bottom electrode thickness of Pt/NiO/Pt capacitors plays an important role in their resistance switching behaviors. Resistance memory switching phenomena become unstable and turn into threshold switching when there are thinner bottom electrodes. We explained these phenomena in terms of the thermal stability of the conducting filaments. This work demonstrates the importance of controlling heat dissipation in unipolar resistance memory switching and associated devices.

FIG. 3. (Color online) Vector representations of the heat flow, i.e., $-k\nabla T$, for cases with (a) $t_{BE} = 200$ nm and (b) $t_{BE} = 10$ nm.

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