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A 60 GHz CMOS I/Q Receiver for High-Speed Wireless Communication System

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Abstract: This paper presents a 60 GHz CMOS I/Q receiver for the high-speed wireless communication system. It consists of a low noise amplifier, single-to-differential (S2D) amplifier, passive mixer, buffer amplifier with passive I/Q generator, and wideband baseband amplifier (BBA) stage. The measured conversion gain of 51 dB is achieved. The baseband bandwidth of 300 MHz is achieved from 57 GHz to 60 GHz. The 90° tandem coupler was implemented for I/Q signal generation, which has a phase error of <7° and an amplitude imbalance of <2 dB from 55 to 62 GHz. The Marchand balun is used to convert the I/Q signal to the differential, which has a phase error of <4°. A 60 GHz CMOS I/Q receiver is designed and fabricated, using a commercial 40 nm CMOS bulk process. The size of the receiver is 2.02 × 1.45 mm^2, including the pads. The circuit is operated from a 0.9 V supply. The power consumption is 172 mW at maximum gain mode.

Keywords: 60 GHz; 802.11ad; WiGig; I/Q receiver; millimeter wave

Citation: Bhatta, A.; Baek, D.; Kim, J.-G. A 60 GHz CMOS I/Q Receiver for High-Speed Wireless Communication System. *Appl. Sci.* **2022**, *12*, 4468. https://doi.org/10.3390/app12094468

Academic Editor: Christos Bouras

Received: 25 March 2022
Accepted: 25 April 2022
Published: 28 April 2022

1. Introduction

The demand for millimeter-wave components is increasing because of the need for high data rates communication systems, such as 5G NR communication, millimeter- wave short range, IEEE 802.11ad, WiGig, and IEEE 802.11ay, which are capable of supporting wireless applications, such as full-HD video streaming, real-time data synchronization, and high-speed wireless links up to tens of billions of bits per second [1,2]. The 60 GHz is especially popular due to the wide available RF bandwidth [3,4]. In addition, CMOS technology progress makes it possible to develop mass production, highly integrated, and low-cost millimeter-wave ICs with moderate RF performance. Hence, CMOS is dominant in the market of millimeter-wave transceivers.

The I/Q receiver is one of the key building blocks in the 60 GHz wireless system. There are several challenges to designing CMOS I/Q receivers at 60 GHz, such as wide bandwidth, wide gain control range, and high I/Q signal accuracy. The performance of the I/Q receiver is dependent on the accuracy of the I/Q signal generator in the LO path. Therefore, it is necessary to make an I/Q generator with low phase and amplitude errors since an I/Q mismatch degrades the image rejection ratio in the receiver. To generate accurate I/Q signals, passive poly-phase filters, various quadrature couplers, and LC filters are introduced. However, 60 GHz is still too high [5,6]. Even though the RF bandwidth is wide at 60 GHz, the baseband amplifier limits the usable bandwidth, and, as a consequence, making a wideband baseband amplifier is a difficult task.

In this paper, a 60 GHz CMOS direct-conversion I/Q receiver with wide bandwidth and gain control range is presented for millimeter-wave high-speed wireless communication systems.

2. Design of 60 GHz CMOS I/Q Receiver

The 60 GHz I/Q receiver requires the wideband bandwidth, wide dynamic range, and the high accuracy I/Q signal to achieve a high image rejection ratio. The block diagram of

the proposed 60 GHz I/Q receiver is shown in Figure 1. It consists of a low noise amplifier (LNA), single-to-differential (S2D) amplifier, double-balanced passive mixer, LO buffer amplifier, quadrature generator (IQGEN), and baseband amplifier (BBA). The LNA is a single-ended design, with the first two stages being a common source amplifier with source degeneration to achieve an optimal noise figure (NF) so that it can amplify the RF signal around 60 GHz with low noise figure [7–11]. Since the mixer is double balanced and mixes in phase (I) and quadrature phase (Q) individually, the amplified RF signal from the LNA, which is a single-ended design, is converted to the differential form using an S2D amplifier. In an S2D amplifier, the single-ended RF signal is converted into the differential form using S2D balun. Balun, being a passive device, introduces some attenuation to the RF signal from the LNA, thus we need to compensate for the loss using the amplifier in the S2D stage. The RF signal from an S2D and local oscillator signal (LO signal) is mixed in the passive mixer. Since the mixer is passive, there is conversion loss in the mixing process, thus we need a LO buffer amplifier that ensures the LO signal has enough swing to switch on the passive mixer switches. For image rejection, the receiver is designed for I and Q mixing. The I and Q signals are generated before the LO buffer amplifier stage using the I/Q generator. The I/Q generator consists of a quadrature tandem coupler and balun. The quadrature tandem coupler generates the I and Q signal from the local oscillator input [12–14]. The I and Q signals are then converted to differential signals using a balun and fed to the LO buffer amplifier. The down-converted intermediate frequency (IF) baseband signal is amplified using BBA. The BBA consists of six stages of the amplifier to increase the signal level suitable for further processing for ADC and demodulation of the signal. The last stage is a buffer circuit to drive the external 50 Ω load of the base-band signal. Since all the amplifiers are gain controllable, based on the control bit, the receiver can operate in required gain states [15,16].

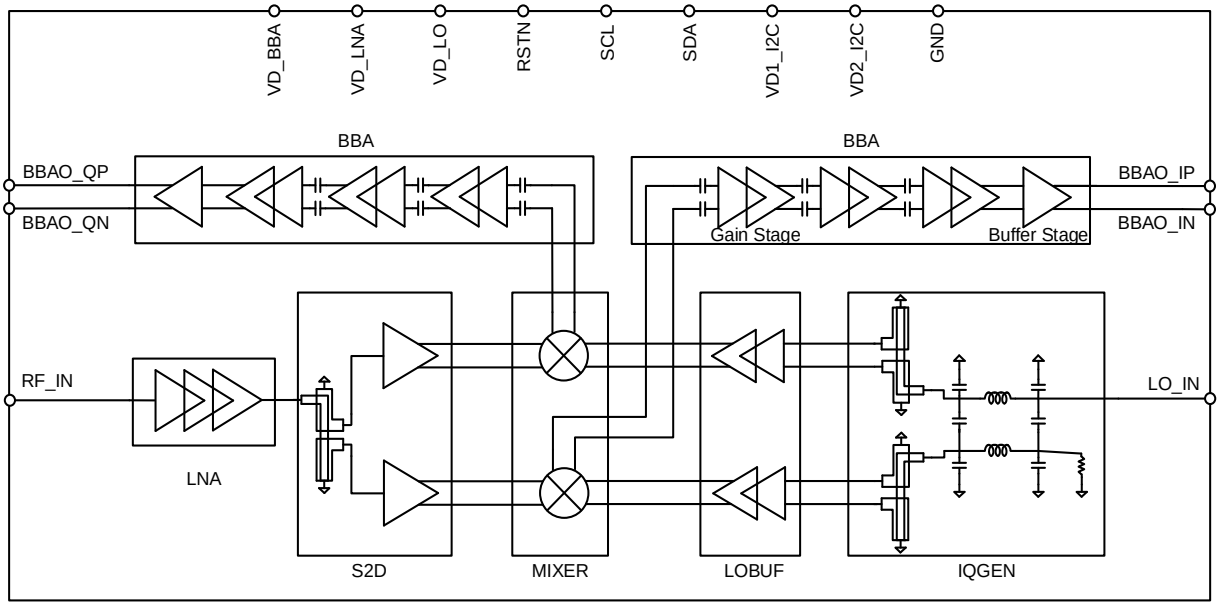


Figure 1. Block diagram of proposed 60 GHz CMOS I/Q receiver.

2.1. Design of 60 GHz Low Noise Amplifier

A 60 GHz receiver requires a low noise figure as well as high linearity. Therefore, a three-stage CS LNA with a low noise figure is proposed. Figure 2 shows the schematic of 60 GHz LNA. The single-ended structured LNA input is connected to the antenna. The inductive source degeneration technique (L_4, L_6) is used in the first and the second stages to achieve the low noise figure at 60 GHz. The common source amplifier structure is implemented without a source degeneration inductor in the third stage to improve the gain and linearity. The input matching network is formed by inductors L_1 and L_2 and

capacitor C_1. The shunt inductor (L_1) is implemented in the input matching network for ESD protection. The switched resistive feedback network is implemented to control the gain at the second and the third stage. The PMOS transistor switch is used in the feedback network so that the additional DC block capacitor is avoidable. Since the additional parasitic capacitance can be removed, it helps to achieve a 21 dB gain at 60 GHz. To control the gain of around 6 dB, the feedback resistors R_{f1} and R_{f2} are used, considering the on-resistance of PMOS. A custom cap metal-oxide-metal (MOM) capacitor is used with EM simulation to achieve an accurate frequency of 60 GHz. The shunt inductor (L_1) is implemented in the input matching network for ESD protection. The simulated gain of 21 dB and the noise figure of <5.5 dB are achieved at 57–62 GHz. The gain of the LNA is controllable from 15 dB to 21 dB at 57–62 GHz. The output impedance is matched to 50 Ω for driving two separate single-to-differential amplifiers. The parameter value of the components in the circuit is shown in Figure 2.

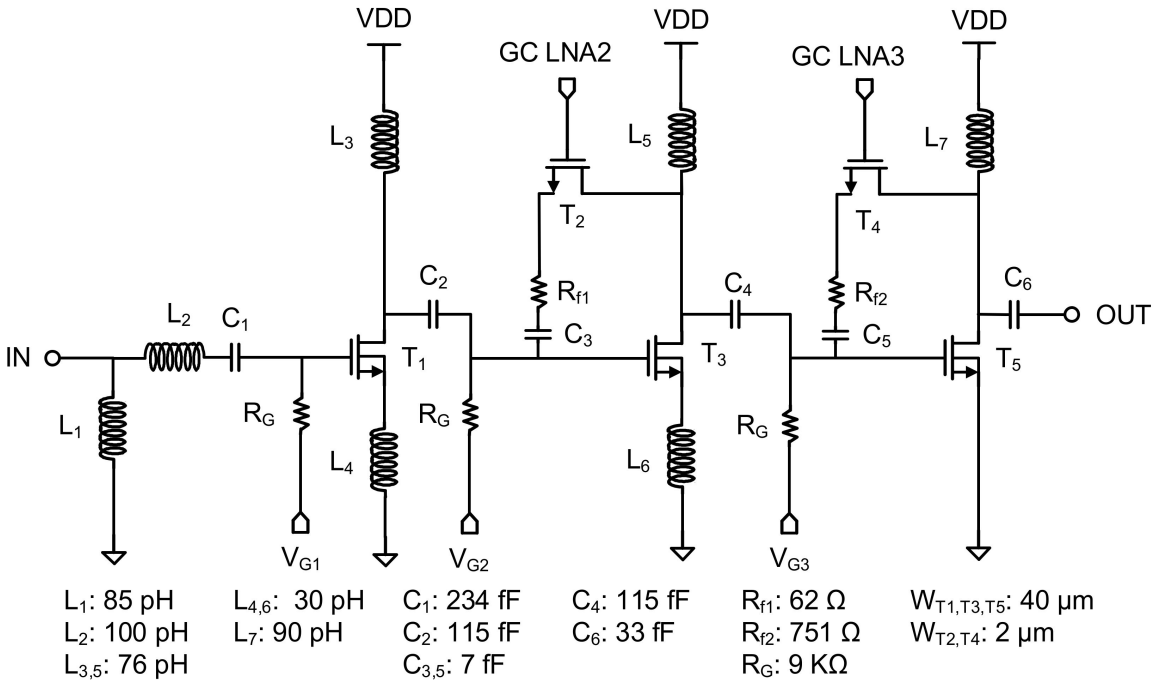


Figure 2. Schematic of 60 GHz low noise amplifier.

2.2. Design of 60 GHz Single-to-Differential Amplifier

The single-to-differential amplifier is designed to drive to the RF port of the double-balanced mixer because of the single-ended output at the LNA. The schematic of the 60 GHz single-to-differential amplifier is shown in Figure 3. It consists of a Marchand balun, a cascode amplifier with switched resistive feedback networks. The Marchand balun is used to generate the differential signal. The use of the capacitors in the balun makes the size of the balun compact. The input impedance of 100 Ω is chosen at the input of the Marchand balun because two balun ports for I/Q mixers are connected to the output of the single-ended LNA. The simulated phase and amplitude mismatches of balun are <1 degree and ~0.2 dB, respectively, at 57–62 GHz. The 2-bit resistive feedback gain control is used with the PMOS switch to increase the gain control range. The cascode amplifier with the resistive feedback is achieved with the gain control of 4 dB for the linearity. The transformers of XFM_1 and XFM_2 are used at input and output for matching, which results in making the accurate differential signal and the compact chip size. To improve the phase and the amplitude balance, the transformer with the shunt capacitor (C_3) is implemented at the load.

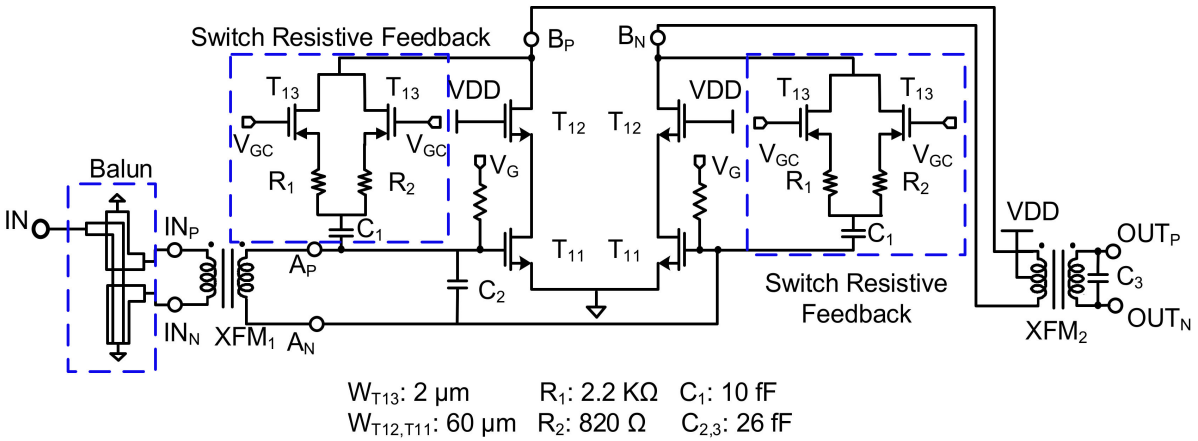


Figure 3. Schematic of 60 GHz single to differential amplifier.

2.3. Design of 60 GHz LO Buffer Amplifier

The LO buffer proposed in this work adopts a cascode structure. The schematic of the LO buffer amplifier is shown in Figure 4. It consists of 2 stages of cascode differential amplifier stages. The first stage amplifier has a gain control feedback network. The second stage has only a cascode amplifier to boost the gain of the first stage. The same switched resistive feedback in S2D is implemented to control the gain. The cascode topology is chosen to achieve the advantage of its higher gain and proper isolation of input and output ports which facilitates impedance matching. The transformer is considered to form the part of the matching network. The simulated gain of the 60 GHz LO buffer amplifier is 16 dB with a 4 dB gain control range.

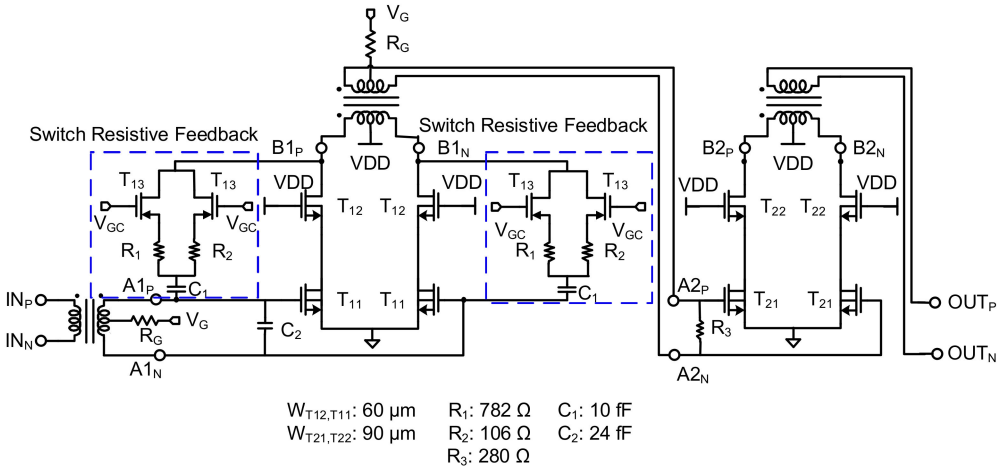


Figure 4. Schematic of 60 GHz LO buffer amplifier.

2.4. Design of 60 GHz I/Q Signal Generator

The double-balanced I/Q passive mixers are used in the receiver, and therefore, the I/Q signal generator should have a balun to convert single-ended signal to differential and a 90° tandem coupler to generate accurate I and Q signals as shown in Figure 5. The passive couplers with the reduced transmission lines are used in the 60 GHz differential I/Q signal generator to achieve the wideband and accurate performance in phase and amplitude with the compact size. The tandem coupler is used in the 90-degree coupler to achieve the compact size because it can be implemented with only two inductors and capacitors. The capacitively loaded microstrip line is used to reduce the size of the coupler. The capacitors of C_5 and C_6 are used to improve the phase and the amplitude mismatches in the coupler. The full EM simulation is performed to make high accurate phase and amplitude at 60 GHz.

The amplitude and the phase mismatches are 2 dB and <7° at 57–62 GHz. The size of the coupler is 0.1 × 0.43 mm^2. The Marchand balun with the broadside coupled transmission line structure is designed to enhance the coupled coefficient and balanced output. The capacitor C_7 is used for input matching, and capacitor C_8 is used for output port matching. The custom MIM capacitor is used, which has a high-quality factor at 60 GHz. These capacitors also provide phase compensation at respective ports.

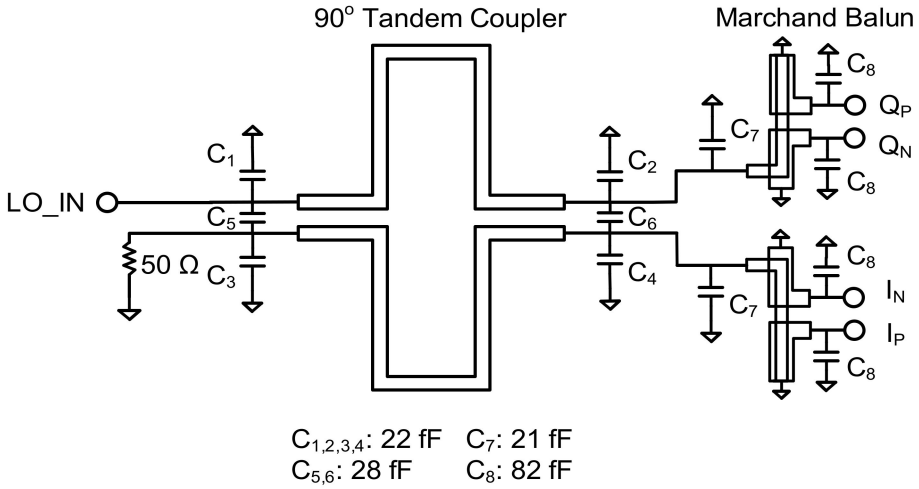


Figure 5. Schematic of 60 GHz passive I/Q generator.

2.5. Design of 60 GHz Passive Mixer and Base Band Amplifier (BBA) Circuit

The passive switching quad is implemented for the double-balanced mixer for the high linearity and low DC power consumption as shown in Figure 6. The passive mixer is realized with a transistor size of 40 µm total width is implemented to achieve high conversion gain at 60 GHz. The conversion gain is dependent on the gate bias and the vgs of 0.45 V is chosen for the high conversion gain; it can be digitally controllable. The capacitive loads are used to filter out the unwanted RF and LO signals. To achieve the wide bandwidth, the capacitors, including the loading capacitance of the baseband amplifier, are chosen.

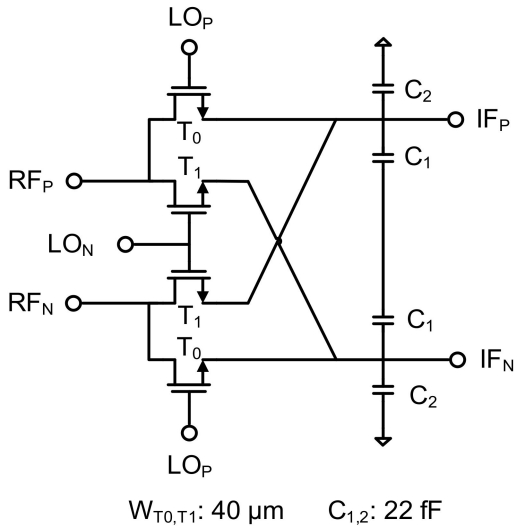


Figure 6. Schematic of 60 GHz double-balanced passive mixer.

The block diagram of BBA is shown in Figure 7a. It consists of six stages of an amplifier cascaded in series, and a DC block capacitor is placed after every two stages to prevent the DC offset. It is a 4-bit digital controlled wideband programmable gain control amplifier.

The structure is differential, and the gain depends on the load resistance R_L and the value of source degeneration resistance at each gain stage as shown in Figure 7b. The buffer circuit shown in Figure 7c drives the external 50 Ω load of the baseband signal. The simulated gain control range is around 60 dB, and the 3 dB baseband bandwidth is around 1 GHz. The parameter values of the components of the baseband amplifier circuit are shown in Figure 7.

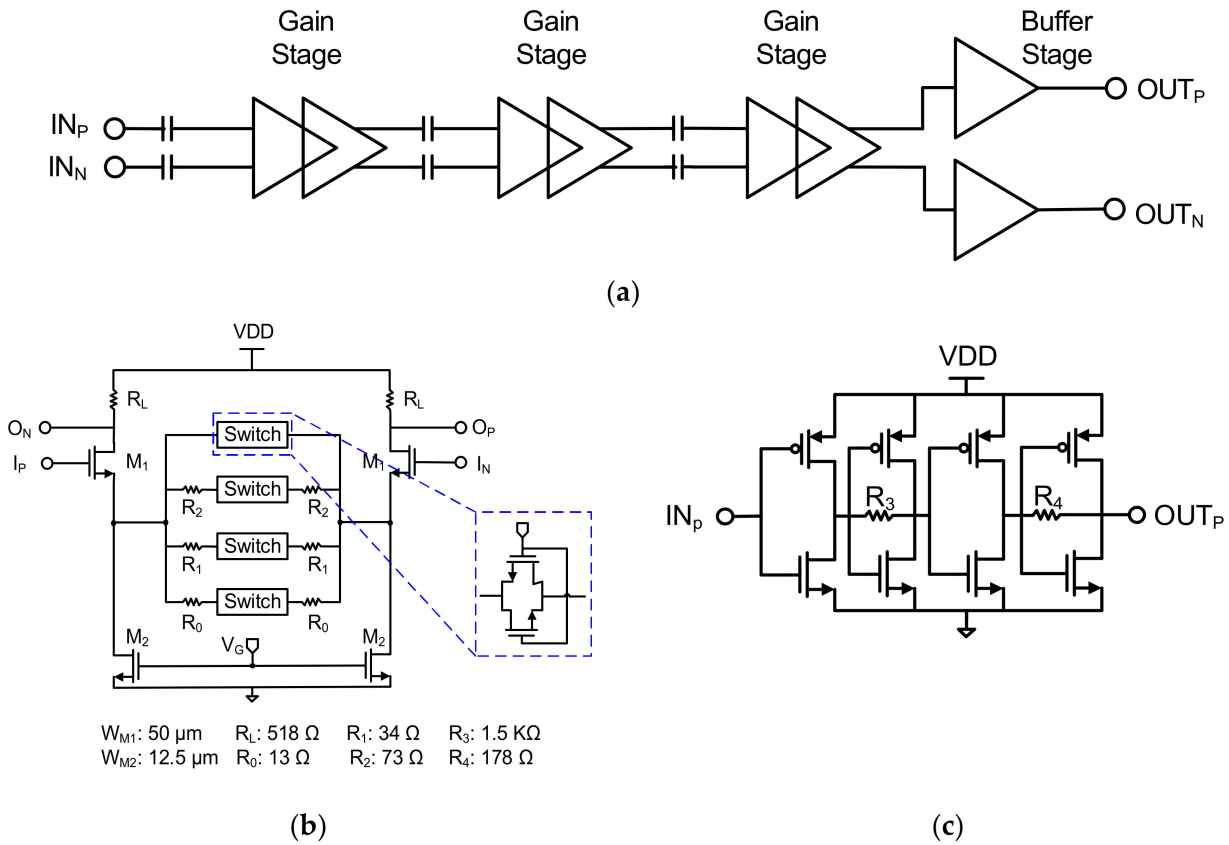


Figure 7. (**a**) Block diagram of 60 GHz baseband amplifier, (**b**) schematic of gain stage, (**c**) schematic of buffer stage of baseband amplifier.

3. Measurement Results

The chip microphotograph of the 60 GHz CMOS LNA is shown in Figure 8. The measured S-parameter results of the 3-stage LNA are shown in Figure 9. The gain of 13.5 dB is achieved in the frequency from 57 to 62 GHz. The input return loss is <10 dB, and the output return loss is <7 dB from 57 to 62 GHz. The 60 GHz LNA consumes a current of 25 mA with a supply of 0.9 V. The chip size of the LNA including the pads is 0.45 × 0.49 mm^2. The proposed 60 GHz I/Q receiver uses a 40 nm CMOS technology. Figure 10 shows the microphotograph of the proposed 60 GHz I/Q receiver. The chip size is 2.02 × 1.45 mm^2, including the pads. The measurements are performed on a high-frequency probe station with DC pads wire bonded to a PCB.

The measurement setup for the 60 GHz CMOS I/Q receiver using a spectrum analyzer is shown in Figure 11. The millimeter-wave source module is used to increase the frequency of the signal generator up to V-band. The LO signal generated from the vector network analyzer has also a limit on the frequency and power, thus the frequency quadrupler is used to extend the frequency up to the V-band and increase the output power to ~16 dBm. The IF outputs I_p is observed in the spectrum analyzer while other IF ports are terminated at 50 Ω. The I2C interface is used to control the 60 GHz I/Q receiver chip.

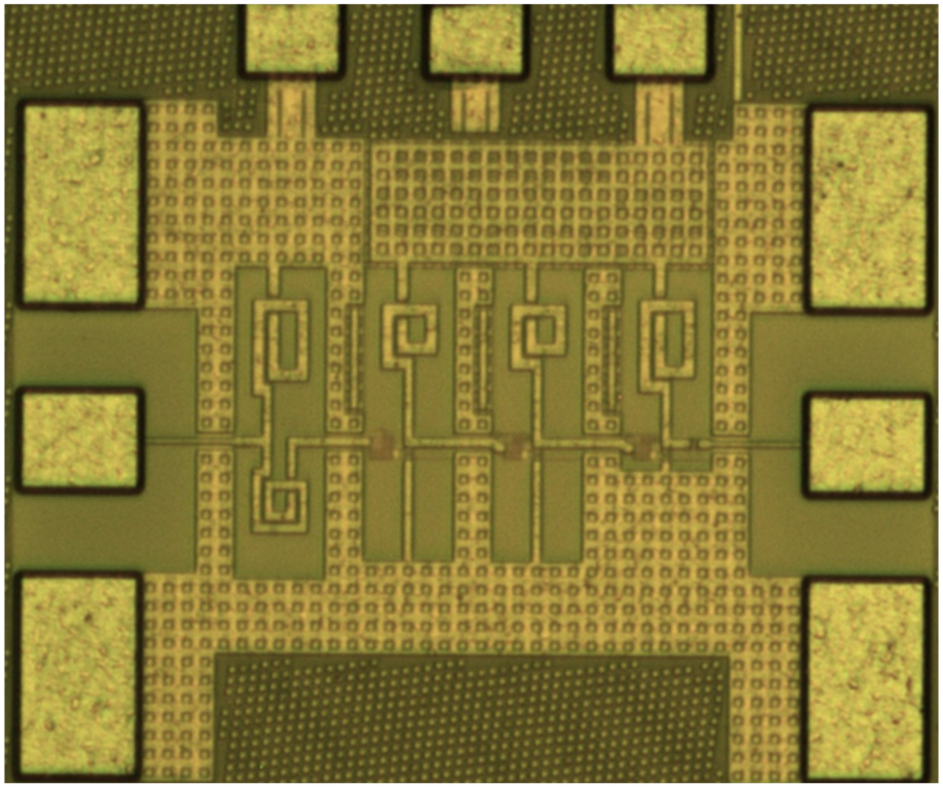


Figure 8. Chip microphotograph of 60 GHz CMOS LNA test pattern.

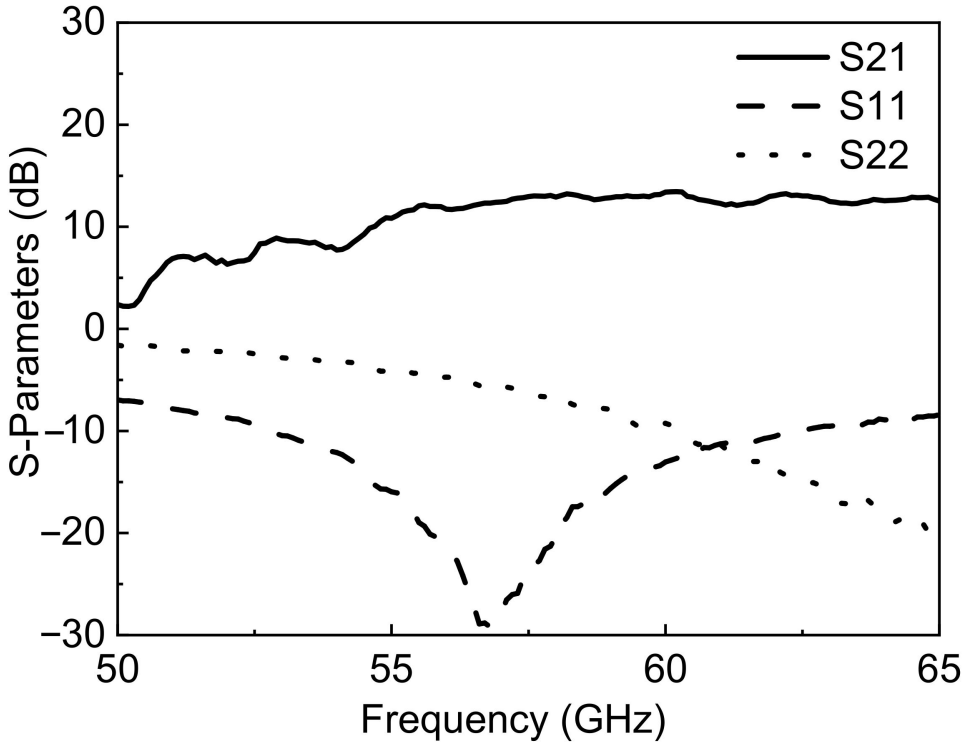


Figure 9. Measured S-parameters of the 60 GHz LNA test pattern.

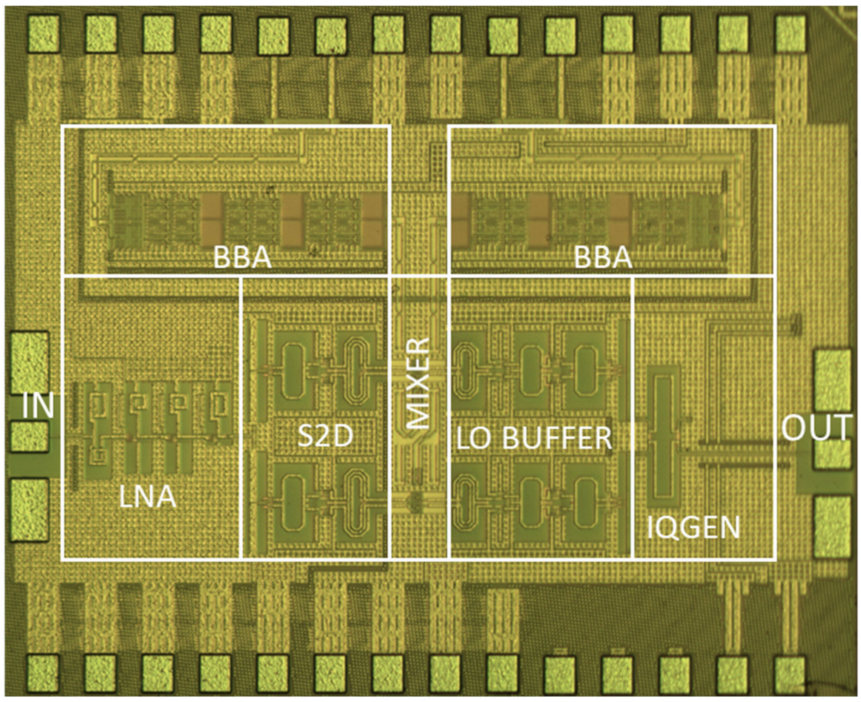


Figure 10. Chip microphotograph of 60 GHz CMOS I/Q receiver.

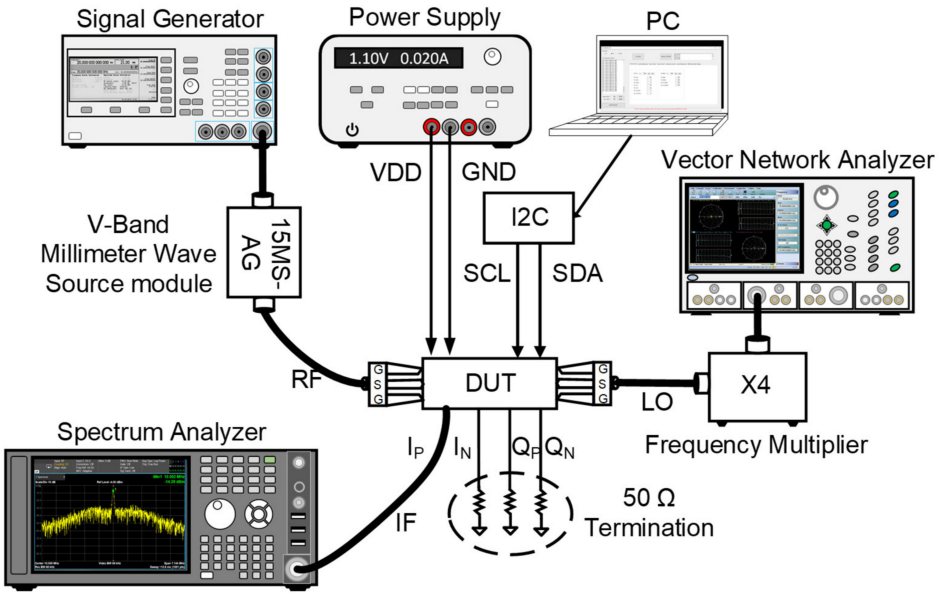
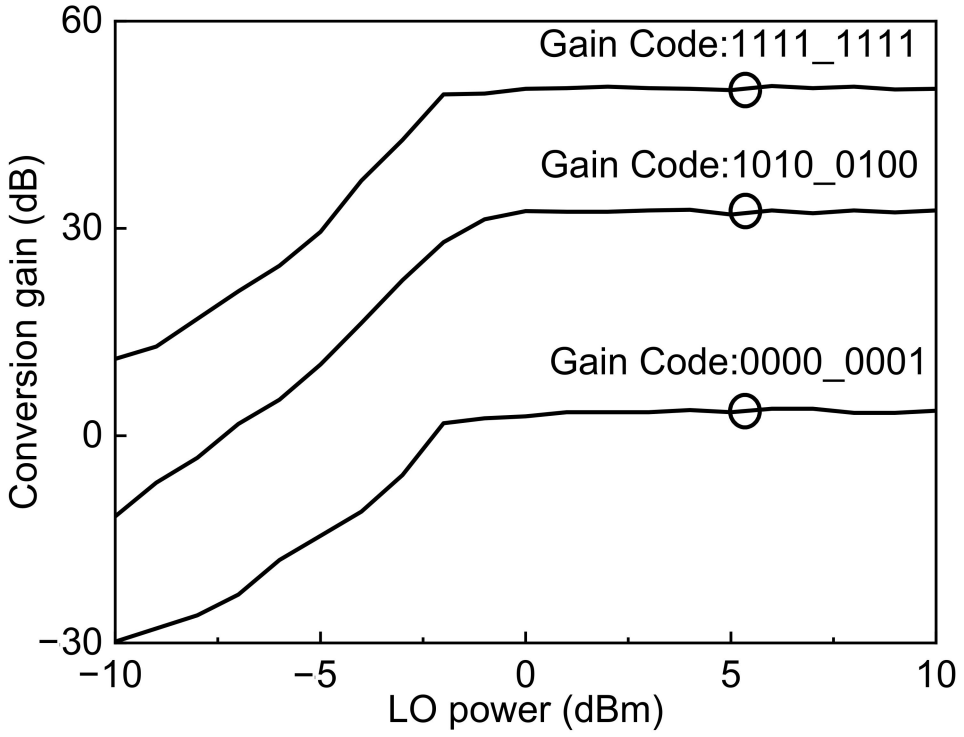


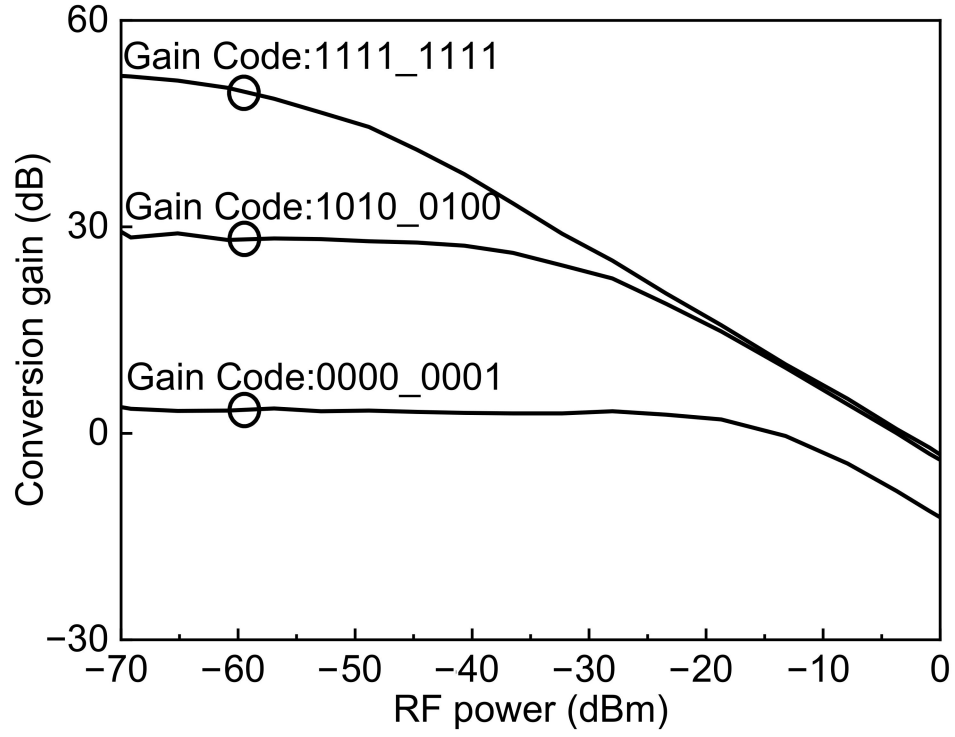
Figure 11. Measurement setup for 60 GHz CMOS I/Q receiver using spectrum analyzer.

Figure 12a plots the three different conversion gain states with the LO power varied from −10 to 10 dBm. The 8-bit gain control is implemented in the receiver, in which 2 bits from MSB are for LNA gain control, and the next 2 bits are for the S2D gain control, and the last 4 bits are for the baseband amplifier. The gain code of 1111_1111 is the highest gain state, and the gain code of 0000_0001 is the lowest gain state. As shown in Figure 12a, the conversion gain is saturated over the LO power of −2 dBm. The measured conversion gain is ~50 dB (Gain code: 1111_1111), ~30 dB (Gain code: 1010_0100), and ~3 dB (Gain code: 0000_0001). Similarly, Figure 12b shows the conversion gain versus RF power. The RF power is swept from −70 to 0 dBm, and the RF frequency is maintained at 60 GHz. Further, the LO power of 5 dBm is applied at 60 GHz. The conversion gains are ~51 dB (Gain code:

1111_1111), ~30 dB (Gain code: 1010_0100), and ~3 dB (Gain code: 0000_0001) at RF power of –70 dBm.



(**a**)



(**b**)

Figure 12. Measured (**a**) conversion gain versus LO power, (**b**) conversion gain versus RF power of 60 GHz CMOS I/Q receiver.

The conversion gain across frequency is measured by sweeping RF and LO together, keeping the IF fixed and superimposed as shown in Figure 13a. The conversion gain of

different IF ports versus RF Frequency is plotted. The RF frequency is varied from 57 to 61 GHz, maintaining the constant IF frequency of 10 MHz. The RF and the LO power of −61 dBm and 5 dBm respectively are applied. The peak gain is ~56 dB at 59 GHz. Figure 13b shows the conversion gain of the I/Q Rx receiver against the IF frequency at the LO frequency of 60 GHz. The measured conversion gains are ~50 dB (Gain code: 1111_1111), ~32 dB (Gain code: 1010_0100), and ~3 dB (Gain code: 0000_0001). The 3 dB baseband bandwidth is around 300 MHz at the highest gain state (Gain code: 1111_1111). The gain control range achieved is around 48 dB.

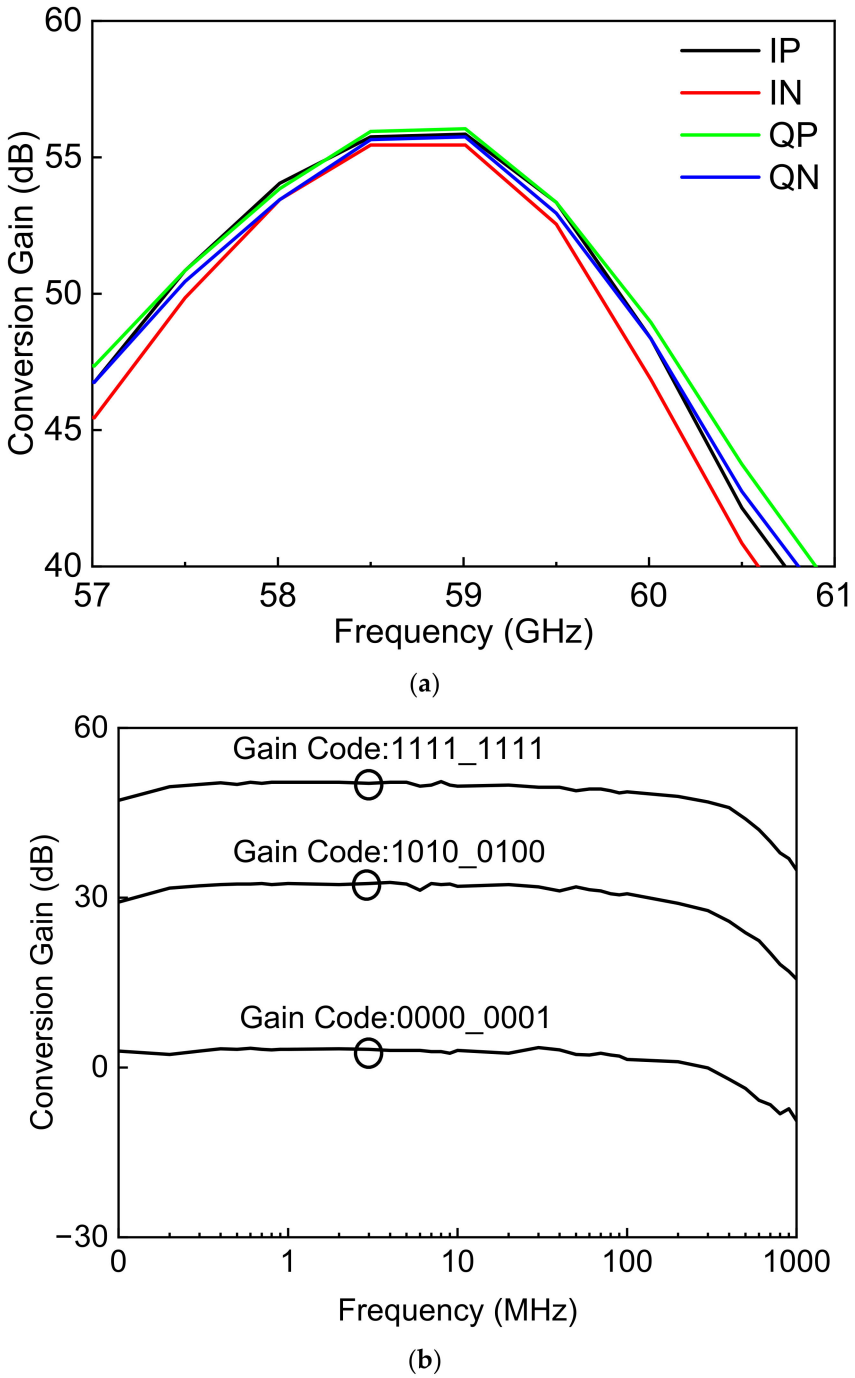


Figure 13. Measured (**a**) conversion gain versus RF frequencies at different IF ports (Gain code: 1111_1111), (**b**) conversion gain versus IF frequency.

The I/Q waveform measurement setup of the 60 GHz CMOS receiver is shown in Figure 14. The RF signal of 60 GHz is applied using the V-band source module to extend the frequency and power range. The LO signal of 60.01 GHz is applied from VNA using a frequency quadrupler to the LO port of the receiver. The DC voltage supply of 0.9 V is applied. The chip consumes a total current of 191 mA. The four IF outputs are connected to the four channels of the oscilloscope, and the output waveforms are observed. All the control bits of LNA, S2D, and BBA are kept in the highest gain state (Gain code: 1111_1111) to observe the I/Q baseband signal. Figure 15 shows the measured baseband output waveform at the highest gain state. The RF power is set at −30 dBm, and LO power is set to 5 dBm.

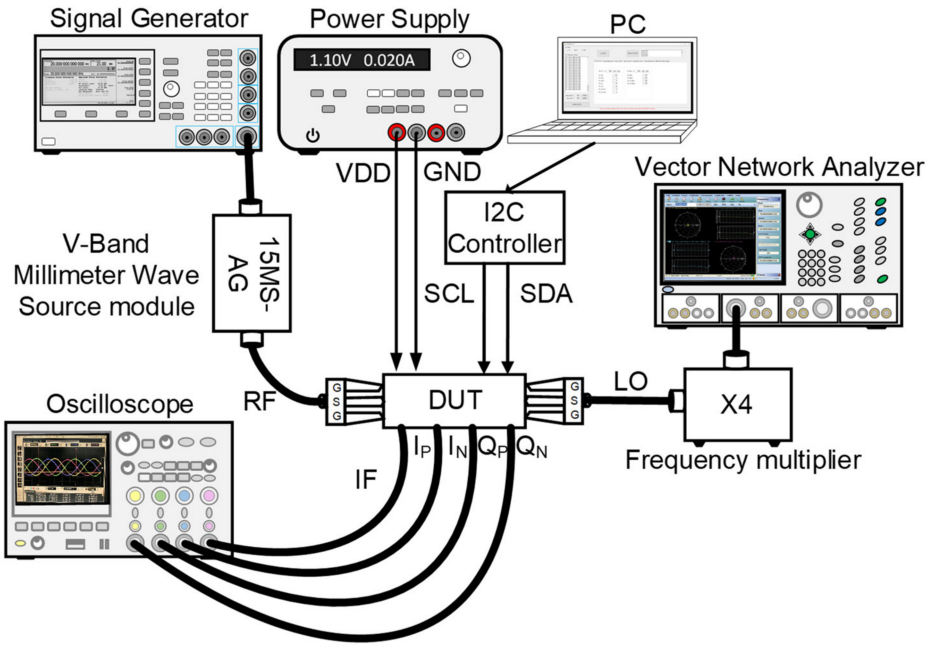


Figure 14. I/Q waveform measurement setup of 60 GHz CMOS I/Q receiver.

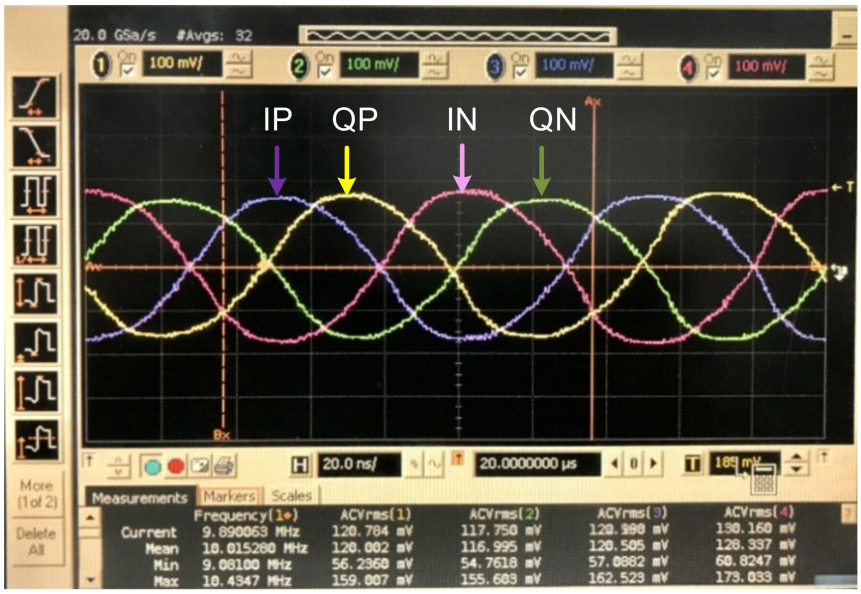


Figure 15. I/Q waveform measurement results at high gain mode of 60 GHz CMOS I/Q receiver.

The performance of the 60 GHz CMOS I/Q receiver is summarized in Table 1 along with the published design for comparison. A passive I/Q generator with a quadrature tandem coupler and Marchand balun is used with full EM simulation to generate an

accurate I/Q signal at 60 GHz. A transformer-based design technique is used in this work to generate accurate differential signals. As a result, the proposed 60 GHz I/Q receiver can also be implemented with compact chip size, improved conversion gain, and low power consumption at millimeter-wave frequency.

Table 1. Performance summary and comparison of 60 GHz I/Q receiver.

Ref.	This Work	JSSC [17]	JSSC [18]
Tech (CMOS)	40 nm	32 nm	65 nm
Freq. (GHz)	57–60	58–60	57–62
I/Q generation	Passive Tandem Coupler and Marchand Balun	Frequency Divider (Double Conversion)	Quadrature Injected Local Oscillator
Gain Range (dB)	3–51	15–54	30
Supply (V)	0.9	1	1.2
Power (mW)	172	247	220
Chip Size (mm^2)	2.8	10.2 [1]	1.25 [2]

[1] 4-Channel transceiver; [2] Only core area.

4. Conclusions

This paper presents a wideband 60 GHz I/Q receiver in bulk 40 nm CMOS technology. The passive I/Q generator with a tandem coupler and Marchand balun is implemented to generate the accurate I/Q signals at 60 GHz. To achieve the wide gain control range, the resistive feedback with the PMOS switch is implemented in the 60 GHz amplifiers. The receiver achieves a conversion gain of 51 dB at 60 GHz with a gain control range is nearly 48 dB. The 3 dB baseband bandwidth of 300 MHz is achieved from 57 GHz to 60 GHz. The I/Q receiver chip dissipates a 172 mW of power from a 0.9 V supply, and the chip size is $2.01 \times 1.45\ mm^2$. With these specifications, the proposed 60 GHz I/Q receiver with passive I/Q generation is well suited for a variety of high-speed wireless communication applications.

Author Contributions: Conceptualization, A.B. and J.-G.K.; methodology, A.B. and J.-G.K.; investigation, A.B. and J.-G.K.; writing—original draft preparation, A.B., D.B. and J.-G.K.; writing—review and editing, A.B. and J.-G.K.; supervision, J.-G.K.; project administration, D.B. and J.-G.K.; funding acquisition, J.-G.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No.2018-0-01663, Development of Communication Sensing Converged B5G Millimeter Wave System).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data can be obtained from the authors on request.

Conflicts of Interest: The authors declare no conflict of interest.

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