Detection and Identification Technique for Series and Parallel DC Arc Faults

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ABSTRACT This paper proposes a series and parallel DC arc detecting and identifying (SPADI) technique using the frequency features of the load current (I_L) and the load voltage (V_L). The frequency changes in V_L and I_L under the series and parallel arc are different. The parallel arc can only raise the high-frequency components of V_L. In contrast, the high-frequency components of I_L can be increased in both series and parallel arcs. However, the increasing frequency range is different. The high-frequency components of I_L generated by the series arc are concentrated in the 5 kHz to 40 kHz band. Meanwhile, the high-frequency components of I_L caused by the parallel arc are observed evenly in all frequency ranges. Inspired by these features, V_L's 5 kHz to 100 kHz components are used to sense the parallel arc in the proposed technique. In addition, the series arc is detected using the 5 kHz to 40 kHz and 50 kHz to 100 kHz bands of I_L. Experimental tests verified the proposed algorithm implemented at the digital signal processor (DSP). As a result of 160 repeated tests, the probabilities of detecting the series and parallel arc were 100 % and 96.25 %, respectively. Moreover, the probability of correctly identifying the arc type when detecting the arc was 100 %. Also, the average detection times of the series and parallel arc were 0.11 s and 0.16 s, respectively.

INDEX TERMS Parallel arc, series arc, fast Fourier transform, frequency characteristics.

NOMENCLATURE

V_I	Input voltage
V_L	Load voltage
I_L	Load current
I_{arc}	Arc current
R_r	Limiting resistance
V_{LV}	Voltage sensor output
V_{LC}	Current sensor output
f_{sw}	Inverter switching frequency
b_1	5 kHz to 40 kHz frequency bands
b_2	50 kHz to 100 kHz frequency bands
b_3	5 kHz to 100 kHz frequency bands
F_{avc1}	Average of b_1 of I_L
F_{avc2}	Average of b_2 of I_L
$F_c(k)$	kth frequency bin of the FFT results
Th_{avc1}	Threshold value for detecting the series arc
F_{avv}	Average of b_3 of V_L
Th_{avv}	Threshold value for detecting the parallel arc
i_a	Inverter a-phase current
DSP	Digital signal processor
FFT	Fast Fourier transform
PCB	Printed circuit board
GPIO0	General-purpose input-output 0 in DSP
GPIO1	General-purpose input-output 1 in DSP

I. INTRODUCTION

As a countermeasure against air pollution caused by fossil fuels, the use of renewable energy from photovoltaic (PV) systems is increasing. Since PV systems obtain energy from the sun, they must be installed outdoors. For this reason, PV systems are greatly influenced by the external environment. Insulation of electric wires composing PV systems may be destroyed by external factors such as natural disasters or damages caused by wild animals. A DC arc accident occurs between wires with damaged insulation. PV systems are more susceptible to such DC arc accidents because PV systems are composed of many PV modules where there are numerous connectors and cables [1]. Also, DC arc faults can occur in the energy storage system (ESS) [2].

DC arc faults are classified into series and parallel arcs [1]. An arc accident in conductors having the same voltage is called the series arc. In contrast, an arc accident in conductors having a different voltage is named the parallel arc. When the series and parallel arc occur, it is difficult to detect with a conventional circuit breaker because the series and parallel arcs do not make a sufficient current to trip the circuit breaker [1], [3]. Because DC arc faults can cause a fire that destroys electrical systems and hurts many people, DC arc accidents must be quickly detected and blocked. Several techniques have been proposed to detect such DC arc accidents.

Studies on DC arc accident detection have mainly focused on detecting series or parallel arcs alone. In series arc detection research, time features [4]–[6], frequency features [7], [8], hybrid features mixing time and frequency [9], [10], statistical features [2], [11], [12], and artificial intelligence (AI) [13], [14] were used to distinguish series arc accidents from normal situations. Similar to series arc studies, parallel arc studies were conducted using time and frequency features [15], [16]. However, relatively few studies have been undertaken on algorithms for reliably discriminating two arc accidents.

Because the series arc occurs in the existing current path, the series arc is eliminated by disconnecting the DC power source and load. On the other hand, since the parallel arc is generated through the newly created current path, it cannot be effectively removed by disconnecting the DC power source and load [17]. Since a particular blocking method must be applied for the parallel arc extinguishment, it is essential to distinguish what kind of an arc accident occurred when an arc accident is generated.

There are few studies to detect and discriminate series and parallel arcs [18], [19]. [18] proposed an algorithm to discriminate series and parallel arcs through the slope of the load current. However, the arc detection probability and the detection time of the method were not fully addressed. Also, if the arc accident is judged only by the slope of the load current, there is a risk of malfunction when the inverter is turned on or off. In [19], additional capacitors are installed to detect and identify the occurrence of series and parallel arcs. However, there are disadvantages that additional capacitors need to be installed, and the capacitor currents need to be monitored. Moreover, as [18], the algorithm's arc detection probability and detection time were not studied. Also, the algorithm was not implemented based on the digital signal processor (DSP). Therefore, developing an algorithm for detecting and discriminating series and parallel arcs with high reliability is needed.

This paper proposes the series and parallel arc detecting and identifying (SPADI) technique using the load voltage and current frequency characteristics. The proposed technique uses the frequency characteristics obtained from the load voltage and current, showing high arc detection and discrimination probability and fast detection speed. Repeated arc detection tests verified the performance of the proposed method.

This paper is mainly composed of five sections. Section I is the introduction. The time and frequency characteristics of series and parallel arcs are described in Section II. A description of the proposed technique is given in Section III. The experimental results of the proposed method are in Section IV. Finally, Section V is the conclusion.

II. CHARACTERISTICS OF SERIES AND PARALLEL DC ARC

The time and frequency domain analyses were done to devise an algorithm to catch the series and parallel arc. The series and parallel arc were generated with a 3-phase pulse-width modulation (PWM) inverter as a load. Then, the load voltage and current were collected.

Fig. 1 shows the experimental circuit diagrams and a picture of the experimental setup for the series and parallel
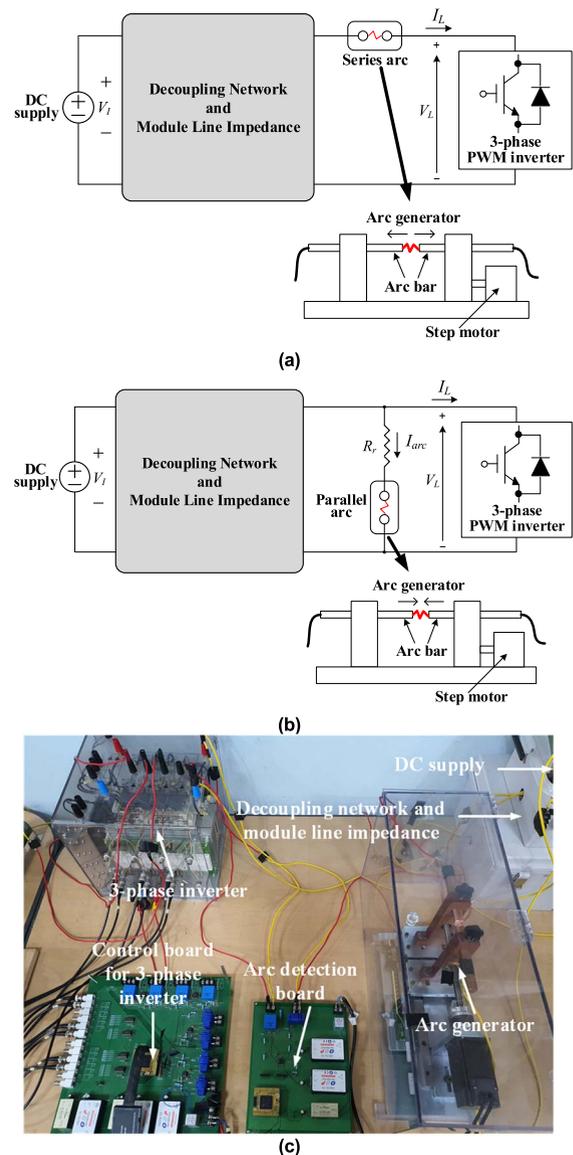

FIGURE 1. (a) Series arc generating circuit, (b) parallel arc generating circuit, (c) picture of arc generating circuit.

arc data acquisition. In Fig. 1, V_I means the input voltage. V_L represents the load voltage. I_L is the load current. In Fig. 1(b), I_{arc} denotes the arc current. R_r means the limiting resistance. The DC supply used in the experiment is KEYSIGHT N8741A. Also, the 3-phase PWM inverter is composed of SEMIKRON SKM50GB123D, and the rating is 20 kW. In addition, the inverter supplies power to a 3-phase load composed of resistors and inductors. The resistors and inductors used in each phase are 10 Ω and 10 mH, respectively. Moreover, the inverter was controlled by space vector modulation (SVM) with open-loop control. The arc generating circuit was manufactured by referring to UL1699B to imitate an actual arc generating system [20]. UL1699B is a regulation for a device that detects the series arc generated in a photovoltaic (PV) system. In UL1699B, a decoupling network and module line impedance are used to mimic the actual arc generating system. In this paper, the arc generating circuit was constructed using the decoupling network and module line impedance between the DC supply and the 3-phase PWM inverter [21]. Loss occurs due to the resistance in the decoupling network and module line impedance. To find out the degree of loss, the loss distributions were studied when I_L was 5 A and the inverter switching frequency was 5 kHz through an experiment. As a result, when the average power supplied by the DC supply was 1448.03 W, the power loss in the decoupling network was 23.13 W, and the power consumed in the module line impedance was 18.36 W. This means that the DC supply powers the inverter with an efficiency of 97.13 %. Series and parallel arcs were generated between the module line impedance and the load, as shown in Fig 1. Detailed configurations of the decoupling network and module line impedance are described in [21].

The parallel arc occurs when two points with different potentials are connected. If there is no resistance between two points of different potentials, a considerable current will flow, which can cause damage to the circuit. Therefore, for the protection of the circuit, a resistor is inserted in series with the parallel arc generator [16], [19]. Also, the parallel arc current is small enough not to trip the circuit breaker [3]. To imitate the parallel arc current, resistors of 300 Ω and 600 Ω were used for R_r.

Disconnecting a current-carrying arc generator creates the series arc. On the other hand, if arc rods with different potentials are placed close together, a parallel arc occurs. V_L and I_L under series and parallel arcs are collected by voltage and current sensors of the arc detector that will be implemented with DSP in the future. The reason for collecting data in this way is that the DSP's data to determine the arc are the output values of sensors, not the measured values of proves. The voltage sensor used for data collection is LEM LV25P, and the current sensor used is LEM LA55P. Fig. 2 describes the circuit diagram for collecting V_L and I_L.

In Fig. 2, V_{LV} describes the output of the voltage sensor, and V_{LC} is the output value of the current sensor. V_{LV} and V_{LC} were acquired with an oscilloscope using a Tektronix TPP0201 at a sampling rate of 250 kHz. The collected V_{LV}
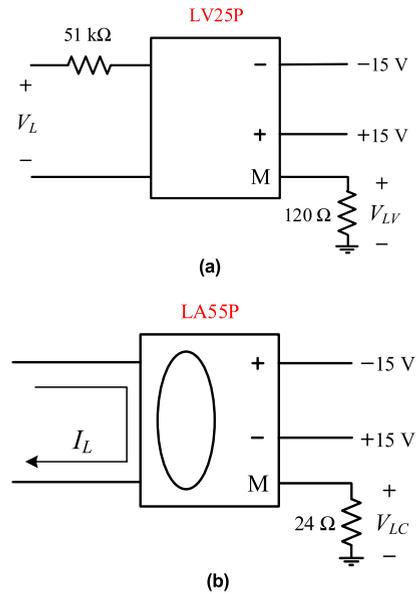

FIGURE 2. Circuit diagrams for measuring V_L and I_L (a) LV25P, (b) LA55P.

and V_{LC} were loaded into MATLAB and analyzed for the time and frequency features. TABLE 1 is a table summarizing the generation conditions of the series and parallel arcs. In TABLE 1, f_{sw} means the inverter switching frequency. In the series arc, I_L and I_{arc} arc are the same because the arc rod is connected in series with the load.

TABLE 1. Conditions of series and parallel arc.

	Series arc	Parallel arc
V_I	300 V	300 V
I_L	5 A, 8 A	5 A
I_{arc}	5 A, 8 A	0.5 A, 1 A
R_r	X	600 Ω at I_{arc} = 0.5 A 300 Ω at I_{arc} = 1 A
f_{sw}	5 kHz, 10 kHz, 15 kHz, 20 kHz	5 kHz, 10 kHz, 15 kHz, 20 kHz

A. SERIES AND PARALLEL ARC ANALYSIS IN TIME-DOMAIN

This section analyzes data obtained by the voltage and current sensors shown in Fig. 2 during series and parallel arcs in the time domain. For the convenience of analysis, V_{LV} and V_{LC} were converted into actual values of V_L and I_L, respectively.

Fig. 3 shows V_L and I_L in the series arc according to f_{sw} when I_L is 5 A. In Fig. 3, the series arc was created from 0 s. After the series arc, the series arc entered a transient state. At this time, V_L and I_L fluctuated severely. After the transient state, it entered a section where the series arc was stably maintained. It can be seen that the DC magnitude of V_L and I_L at this time slightly decreased compared to before the series arc. This is because when the series arc is
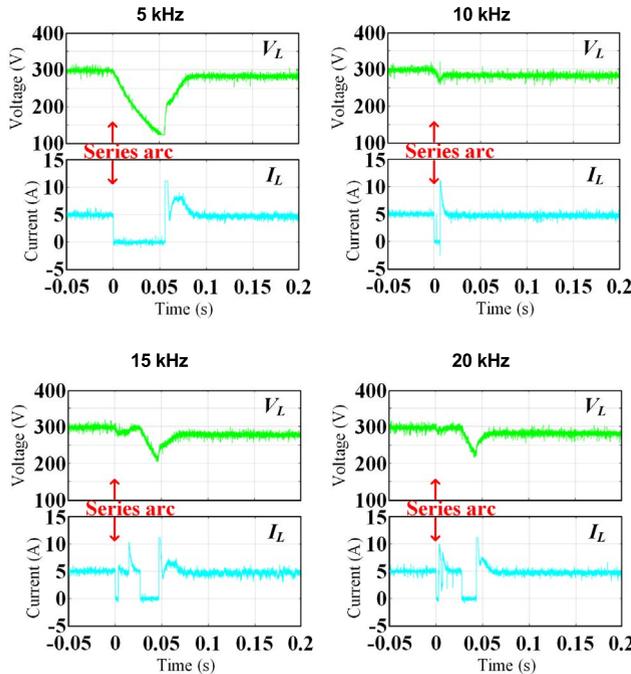
FIGURE 3. V_L and I_L before and after the series arc according to f_{sw} when I_L is 5 A.

created, a positive impedance is generated [1], [12], thereby reducing V_L and I_L. In addition, there was no change in the high-frequency components in V_L after the series arc.

Fig. 4 shows V_L and I_L in the series arc according to f_{sw} when I_L is 8 A. As in the case where I_L is 5 A, it can be
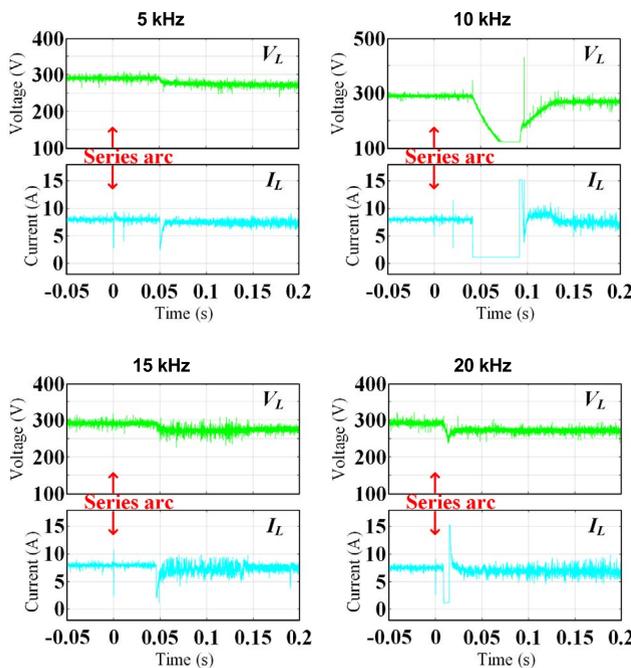

FIGURE 4. V_L and I_L before and after the series arc according to f_{sw} when I_L is 8 A.

seen that V_L and I_L fluctuated severely in the transient series arc. Moreover, in the stable series arc, the DC magnitudes of V_L and I_L slightly decreased compared to before the series arc. Meanwhile, the high-frequency components of V_L after the series arc slightly increased when f_{sw} is 10 kHz and 15 kHz. For I_L, the high-frequency components increased after series arcing at all switching frequencies. When comparing Fig. 3 and Fig. 4, the transient arc time in I_L of 8 A was shorter than that in I_L of 5 A, except for the case where f_{sw} was 10 kHz.

Fig. 5 represents V_L and I_L in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A. As shown in Fig. 5, the parallel arc that occurred at 0 s generated significant high-frequency components in V_L and I_L. In addition, unlike the series arc, the transient arc state and the steady arc state were not distinguished. Moreover, the reduction of DC magnitude of V_L and I_L was not observed after arcing.
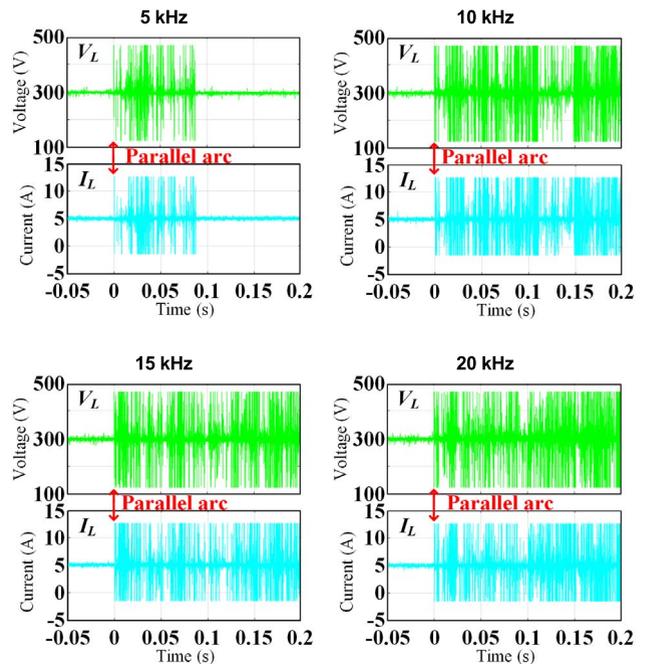

FIGURE 5. V_L and I_L before and after the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A.

Fig. 6 describes V_L and I_L in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A. The parallel arc made significant high-frequency components in V_L and I_L when I_L is 5 A and I_{arc} is 1 A. Similar to I_{arc} of 0.5 A, the transient and steady arc states were not identified. Also, the reduction of DC value of V_L and I_L was not seen after arcing. From a comparison of Fig. 5 and Fig. 6, the smaller I_{arc}, the larger the high-frequency components generated by the parallel arc.

B. SERIES AND PARALLEL ARC ANALYSIS IN FREQUENCY-DOMAIN

This section analyzes the series and parallel arc frequency properties using a fast Fourier transform (FFT). 1024 samples of V_L and I_L converted from V_{LV} and V_{LC} at a 250 kHz
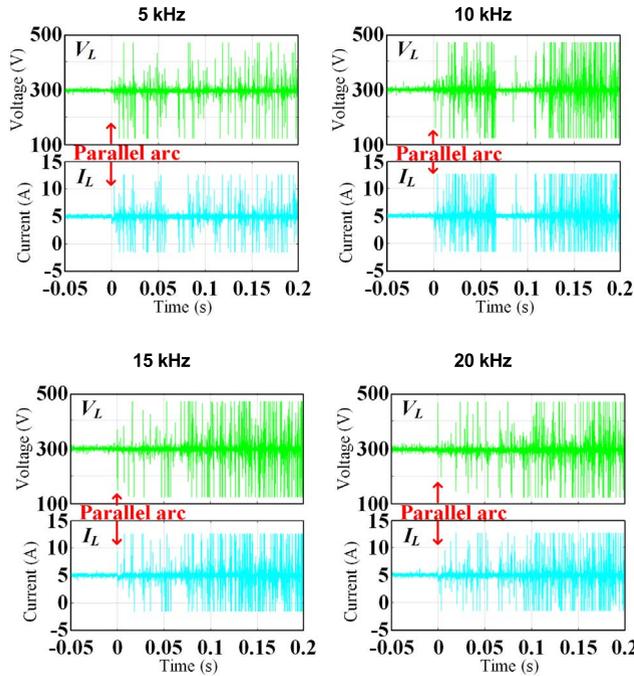
FIGURE 6. V_L and I_L before and after the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A.

FIGURE 7. FFT difference before and after the series arc according to f_{sw} when I_L is 5 A.

sampling rate made one FFT result. To check how the frequency changes before and after the series and parallel arc, the values obtained by subtracting the pre-arc FFT result from the post-arc FFT result were graphed. The post-arc FFT result used in this paper was an average of 10 FFT results after arcing to reduce the influence on the measurement error of the sensor. Similarly, for the pre-arc FFT result, an average of 10 FFT results before arcing was used.

Fig. 7 shows the FFT difference in the series arc according to f_{sw} when I_L is 5 A. Fig. 7 indicates that there was almost no FFT difference before and after series arcing for V_L regardless of f_{sw}. However, in the case of I_L, the 5 kHz to 40 kHz band rose significantly at all switching frequencies. In addition, there were few changes of I_L in the band above 50 kHz.

Fig. 8 represents the FFT difference in the series arc according to f_{sw} when I_L is 8 A. In Fig. 8, there was no high-frequency change in V_L at any switching frequency after the series arc, but the 5 kHz to 40 kHz band for I_L increased noticeably.

Fig. 9 represents the FFT difference in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A. Unlike the series arc, the parallel arc increased the high-frequency components of V_L and I_L together. In addition, the entire frequency band rose evenly.

Fig. 10 shows the FFT difference in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A. Compared to Fig. 9, the magnitude of the high-frequency components after the parallel arc when I_{arc} is 1 A was smaller than when I_{arc} is 0.5 A. Meanwhile, the entire frequency band increased evenly after the parallel arc.
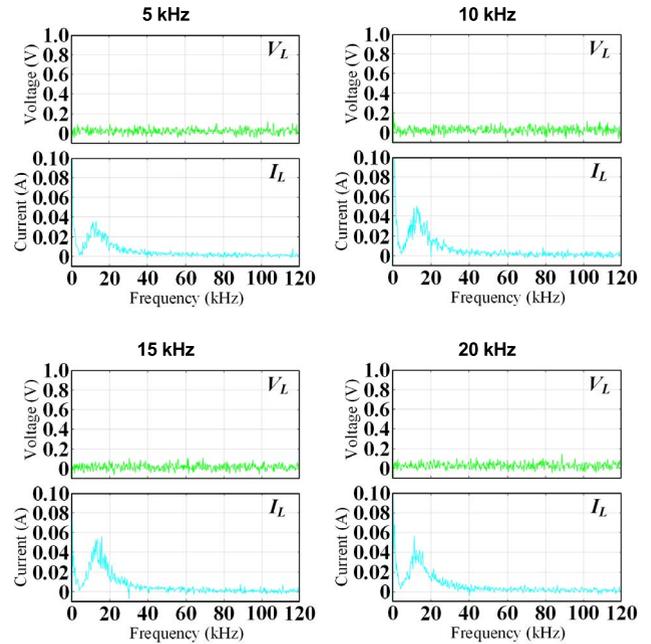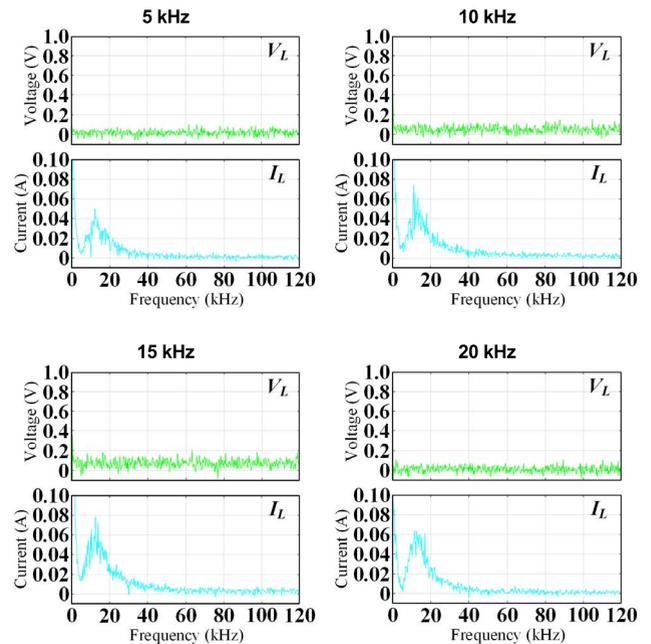

FIGURE 8. FFT difference before and after the series arc according to f_{sw} when I_L is 8 A.

When the parallel arc occurs, V_L and I_L fluctuate very significantly, as shown in Figs. 5 and 6. However, looking at the FFT result in Figs. 9 and 10, a value smaller than the observed voltage and current fluctuation in the time domain is calculated. The reason for this can be seen by magnifying waveforms. Fig. 11 shows time axis enlarged waveforms for V_L and I_L when the parallel arc occurs at I_L of 5 A, I_{arc} of 0.5 A, and f_{sw} of 5 kHz. In this paper, 1024 data collected
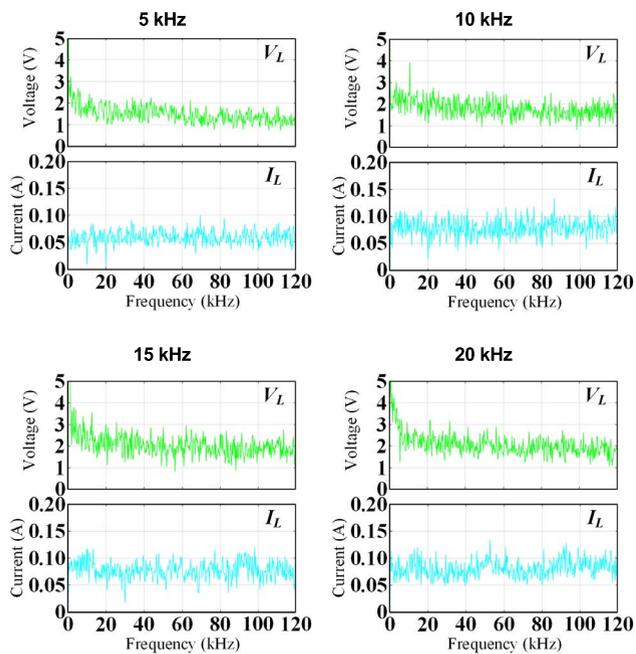
FIGURE 9. FFT difference before and after the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A.
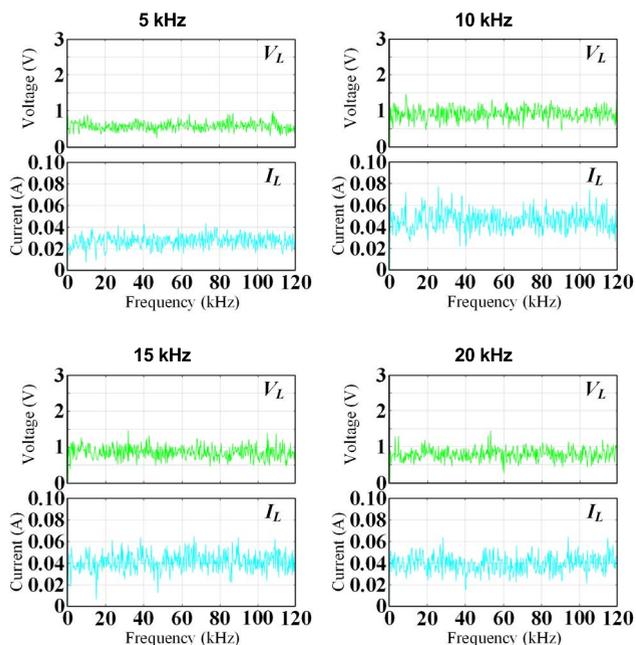

FIGURE 10. FFT difference before and after the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A.

at a 250 kHz rate are required to calculate one FFT result. That is, the time needed to calculate one FFT is about 4 ms. In the waveform of V_L for 4 ms shown in Fig. 11, significant high-frequency components are intermittently observed. Therefore, large values are not calculated in the FFT result. For the same reason, the FFT result of I_L does not show a significant value which can be observed in the time domain.
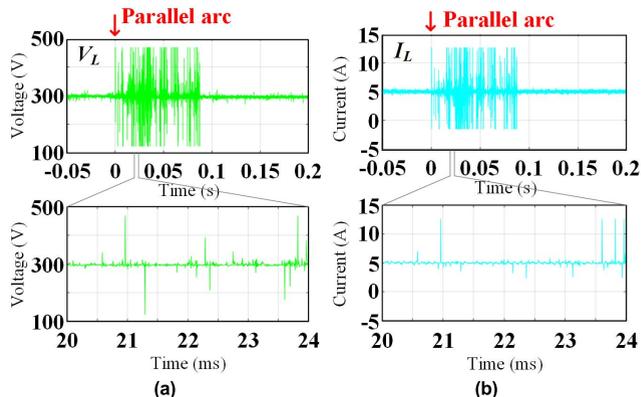

FIGURE 11. Time axis enlarged waveforms for V_L and I_L when the parallel arc occurs at I_L of 5 A, I_{arc} of 0.5 A, and f_{sw} of 5 kHz (a) V_L, (b) I_L.

TABLE 2. Frequency features of series and parallel arc.

	Series arc	Parallel arc
Load voltage	No change	Increase in 0 to 120 kHz
Load current	Increase in 5 kHz to 40 kHz	Increase in 0 to 120 kHz

TABLE 2 is a table summarizing the frequency features of the series and parallel arc.

There are distinct series and parallel arc features in the frequency domain. The proposed SPADI technique uses these properties to detect and identify the series and parallel arcs.

III. PROPOSED SPADI METHOD

The proposed method uses three types of frequency bands for the series and parallel arc detecting and identifying: 5 kHz to 40 kHz called b_1, 50 kHz to 100 kHz called b_2, and 5 kHz to 100 kHz called b_3. The b_1 and b_2 are utilized for the series arc detection. Also, b_3 is for parallel arc detection. F_{avc1} is the average of b_1 of I_L. In addition, F_{avc2} is the average of b_2 of I_L. F_{avc1} and F_{avc2} can be calculated by (1).

$$F_{avc1} = \frac{1}{144} \sum_{k=22}^{k=165} F_c(k),$$
$$F_{avc2} = \frac{1}{206} \sum_{k=206}^{k=411} F_c(k). \qquad (1)$$

In (1), $F_c(k)$ means a kth frequency bin of the FFT results. Because an FFT resolution is 244.14 Hz (=250000/1024), the 22nd, 165th, 206th, and 411th frequency bins represent 5.13 kHz, 40.04 kHz, 50.05 kHz, and 100.10 kHz, respectively. The proposed algorithm determines that the series arc occurs if (2) and (3) are satisfied.

$$F_{avc1} > Th_{avc1}. \qquad (2)$$
$$F_{avc1} > 3F_{avc2}. \qquad (3)$$

In (2), Th_{avc1} is a threshold value for detecting the series arc. Only the condition of (2) is sufficient to detect the series arc. However, since condition (2) can be satisfied even in the parallel arc, the series arc is judged by considering (3)

together in the proposed method. Under the series arc, F_{avc1} is greater than F_{avc2}. On the other hand, F_{avc1} and F_{avc2} are similar for the parallel arc. Therefore, condition (3) is suitable for identifying the series arc from the parallel arc.

The proposed technique uses F_{avv} to sense the parallel arc. F_{avv} is the average of b_3 of V_L. Equation (4) is a calculation method of F_{avv}.

$$F_{avv} = \frac{1}{390} \sum_{k=22}^{k=411} F_c(k). \tag{4}$$

$$F_{avv} > Th_{avv}. \tag{5}$$

Equation (5) is the condition used to determine the parallel arc. In (5), Th_{avv} is the threshold value of F_{avv}. Since the high-frequency components of V_L do not change in the series arc, the occurrence of the parallel arc can be judged only by condition (5).

To determine the generation of the series and parallel arc using equations (2), (3), and (5), first, measure I_L and V_L through the current and voltage sensor. To use the analysis results through the oscilloscope in the DSP, the data sampling speed of the DSP is set to be the same sampling rate of the oscilloscope at 250 kHz. Moreover, as in the previous analysis, one FFT result from the DSP is obtained using 1024 samples. After that, the FFT is performed using the measured current and voltage. For the FFT result of I_L, the filtering technique proposed in [7] is applied to remove the inverter switching noise. Then, F_{avc1}, F_{avc2}, and F_{avv} are calculated using the FFT results of I_L and V_L. The proposed technique detects the series arc if conditions (1) and (2) are satisfied 10 times in a row. In addition, if condition (3) is met 10 times consecutively, the proposed technique senses the parallel arc. It is judged that an arc is generated when the threshold value is exceeded 10 times in a row to prevent the proposed algorithm from malfunctioning in normal transient conditions such as inverter startup and inverter shutdown situations. Since 1024 samples collected at a 250 kHz sampling rate are required to obtain one FFT result, it takes about 4 ms to get one FFT result. Therefore, the minimum time required for this algorithm to detect and identify an arc accident is about 40 ms. The threshold values Th_{avc1} and Th_{avv} are set to 0.01 and 0.5, respectively, through trial and error. Th_{avc1} and Th_{avv} are values optimized for the circuit system used in this paper. If this proposed algorithm is applied to a system with different circuit parameters, it is necessary to change the threshold value. The flow chart of the proposed SPADI technique is represented in Fig. 12.

IV. EXPERIMENTAL RESULTS

A printed circuit board (PCB) was fabricated to verify the proposed SPADI method, as shown in Fig. 13. Fig. 13 (a) describes the circuit diagram of the PCB. Fig. 13 (b) is the photograph of the PCB. The current and voltage sensor used in the PCB are LEM LA55P and LEM LV25P, respectively. Also, the DSP in the PCB is TI TMS320F28335. To convert an analog signal to a digital signal, the sampling frequency must be greater than or equal to twice the frequency of the
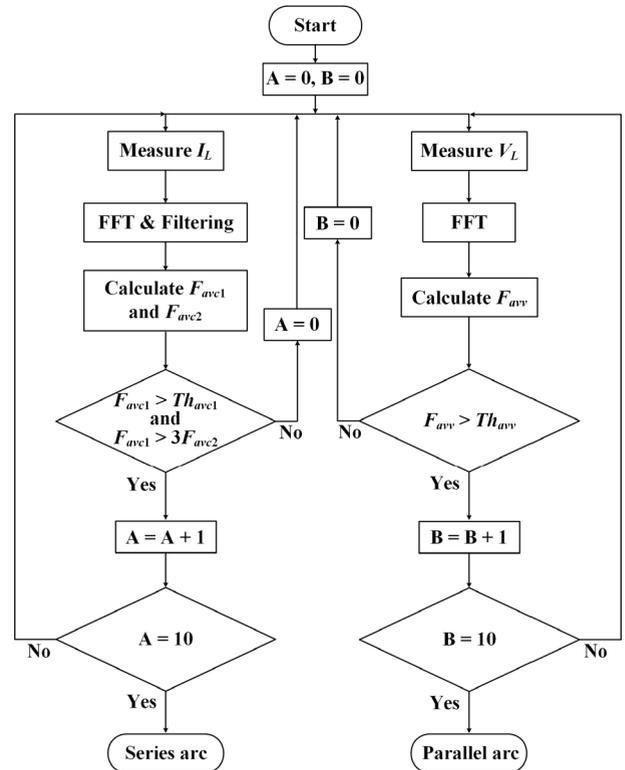

FIGURE 12. Flow chart explaining the proposed SPADI technique.

signal to be converted [7]. Since the proposed method deals with signals up to 100 kHz, data were collected at 250 kHz, including margin. Also, low-pass filters blocking frequencies above 100 kHz were used in the PCB.

Using the manufactured PCB, the performance of the proposed method was verified by repeated arc detection experiments under the arc generation conditions in TABLE 1. To check the operation of the proposed algorithm, the DSP GPIO0 is set to output 3.3 V when the DSP detects the series arc. In addition, the DSP GPIO1 is set to output 3.3 V when the DSP detects the parallel arc.

A. EXPERIMENT RESULTS OF THE PROPOSED METHOD

This section shows the arc detection experiment results when the PCB, as shown in Fig. 13, is connected to the DC arc generating circuit as shown in Fig. 1 under the conditions of TABLE 1. Each experimental result consists of a-phase inverter current (i_a) to check inverter operation, V_{arc} to confirm the arc generation, and GPIO0 and GPIO1 waveforms to show the arc judgment of the proposed technique.

Experimental results of the proposed SPADI technique in the series arc according to f_{sw} under I_L of 5 A are represented in Fig. 14. When the series arc is created, a positive impedance is generated [1], [12]. Therefore, V_{arc} was maintained at 0 V before the series arc and increased to a specific value after the series arc. As shown in Fig. 14, the peak value of i_a decreased after the series arc. In this paper, since the inverter is controlled in open-loop control, the peak value of
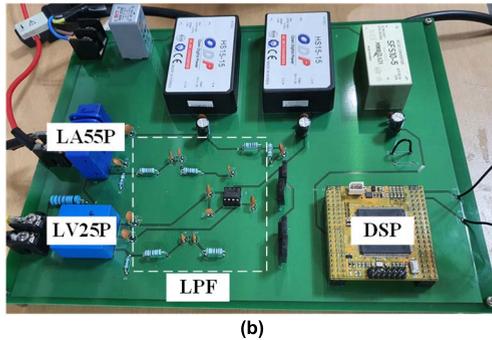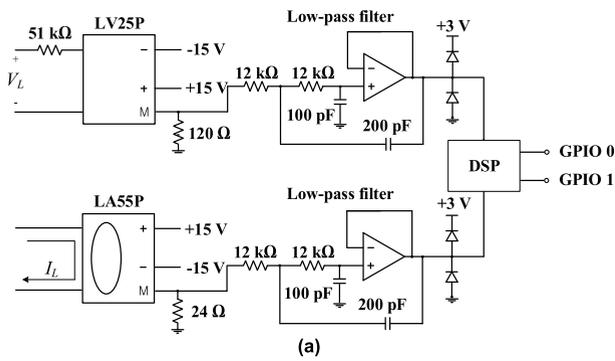
FIGURE 13. PCB for the proposed SPADI method (a) circuit diagram, (b) picture.

FIGURE 14. Experimental results of the proposed SPADI technique in the series arc according to f_{sw} when I_L is 5 A.

the inverter phase current decreases when the inverter input voltage called V_L in this paper decreases. When the series arc occurs, a specific DC voltage is applied across the series arc fault point, as shown in the V_{arc} waveform in Fig. 14. As a result, because of the reduction of V_L, the peak value of the inverter phase currents including i_a decreases. After the series arc, the DSP GPIO0 output changed from 0 V to 3.3 V within a short time in all switching frequency conditions. This means that the series arc was detected by the proposed SPADI method. In addition, since the DSP GPIO1 output was kept at 0 V, the proposed SPADI method did not detect the parallel arc.

Fig. 15 shows the experimental results of the proposed SPADI technique in the series arc according to f_{sw} under I_L of 8 A. As the results of Fig. 14, in all switching frequency conditions, the series arc was quickly detected by the proposed technique. In addition, a reduction in the a-phase inverter current peak value due to V_{arc} after the series arc was observed. The series arc detection time shown in Figs 14 and 15 is much less than the 2.5 s specified by UL1699B [20]. Therefore, Figs 14 and 15 demonstrate that the proposed technique detected the series arc quickly.

Fig. 16 shows the experimental results of the proposed SPADI technique in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A. The parallel arc is generated by placing arc rods where the voltage difference is 300 V close together. Therefore, V_{arc} was measured at 300 V before the arc occurred. When the parallel arc started, V_{arc} decreased rapidly, making many high-frequency components. Referring
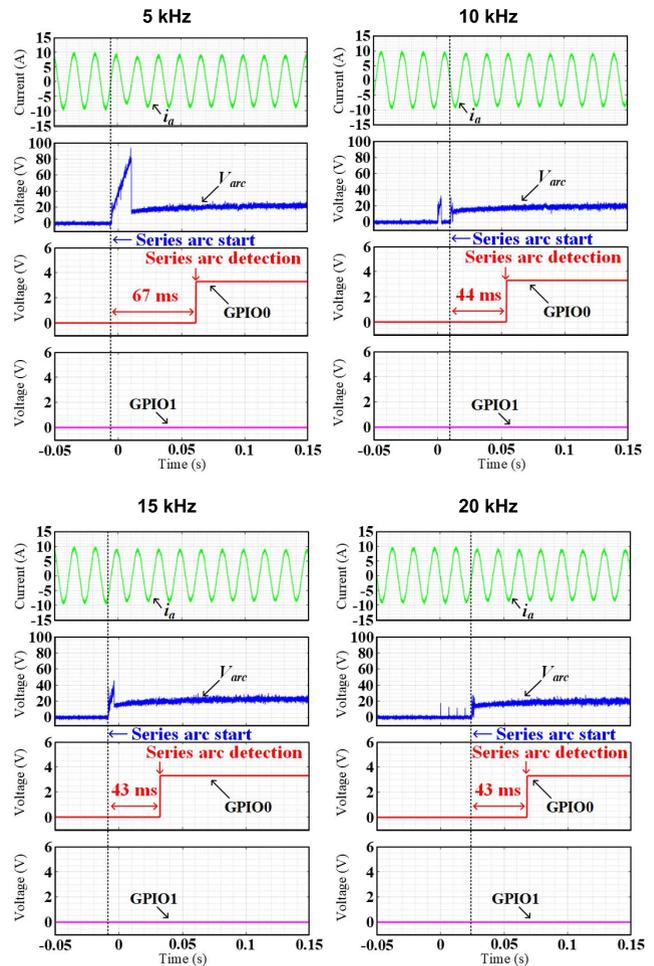
to Fig. 16, the parallel arc appeared at 0 s, and high-frequency components were observed in V_{arc}. After the parallel arc, the DSP GPIO1 output changed from 0 V to 3.3 V within a short time under all switching frequency conditions while maintaining the DSP GPIO0 output at 0 V. Therefore, the proposed SPADI method detected and discriminated the parallel arc quickly and accurately. On the other hand, since the parallel arc occurs in parallel with the load, the DC reduction phenomenon of V_L due to the parallel arc does not occur. Therefore, there is no reduction in the a-phase inverter current after parallel arcing.

Fig. 17 represents the experimental results of the proposed SPADI technique in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A. In Figs. 5, 6, 9, and 10, it was observed that when I_{arc} is large, the high-frequency components in V_L and I_L are less generated than when I_{arc} is small. This result can be explained by the high-frequency component of V_{arc} generated when parallel arcs occur. Comparing Figs. 16 and 17, it can be seen that when I_{arc} is small, more high-frequency components are generated in V_{arc}. Because the high-frequency components generated in
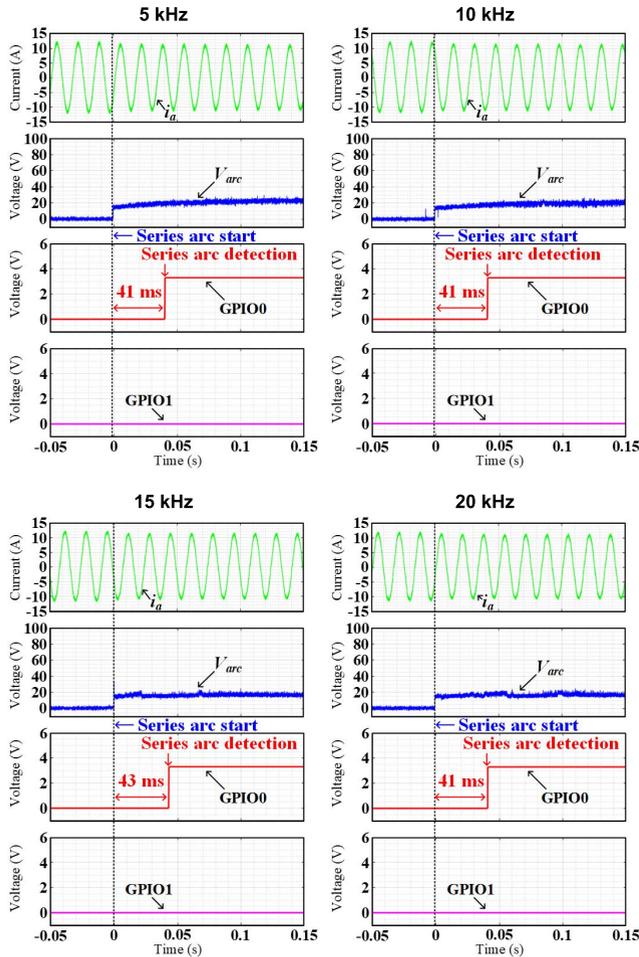
FIGURE 15. Experimental results of the proposed SPADI technique in the series arc according to f_{sw} when I_L is 8 A.

FIGURE 16. Experimental results of the SPADI technique in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 0.5 A.

V_{arc} are transferred to the load side, when I_{arc} is large, the high-frequency components in I_L and V_L are small. Fig. 17 indicates that parallel arcs are accurately detected with I_{arc} of 1 A, similar to the result of I_{arc} of 0.5 A. However, the detection time of the parallel arc under I_{arc} of 1 A is longer than that under I_{arc} of 0.5 A. This is because when I_{arc} is large, the high-frequency components in V_L are small.

The proposed SPADI technique detects and discriminates the series and parallel arc by using the high-frequency components of V_L and I_L. High-frequency components can occur not only in arcing but also in the normal transient states: the inverter startup, inverter shutdown, and load step change. A test was conducted to check whether the proposed SPADI technique does not malfunction under the normal transient states in Fig. 18. Figs. 18 (a) and (b) show the test results of the proposed SPADI method in the inverter startup and shutdown situations. It can be seen that the proposed technique did not malfunction when the inverter was turned on or off. Figs 18 (c) and (d) describe the test results of the proposed technique in situations where I_L changes rapidly. Even in these situations, the proposed technique did not malfunction.
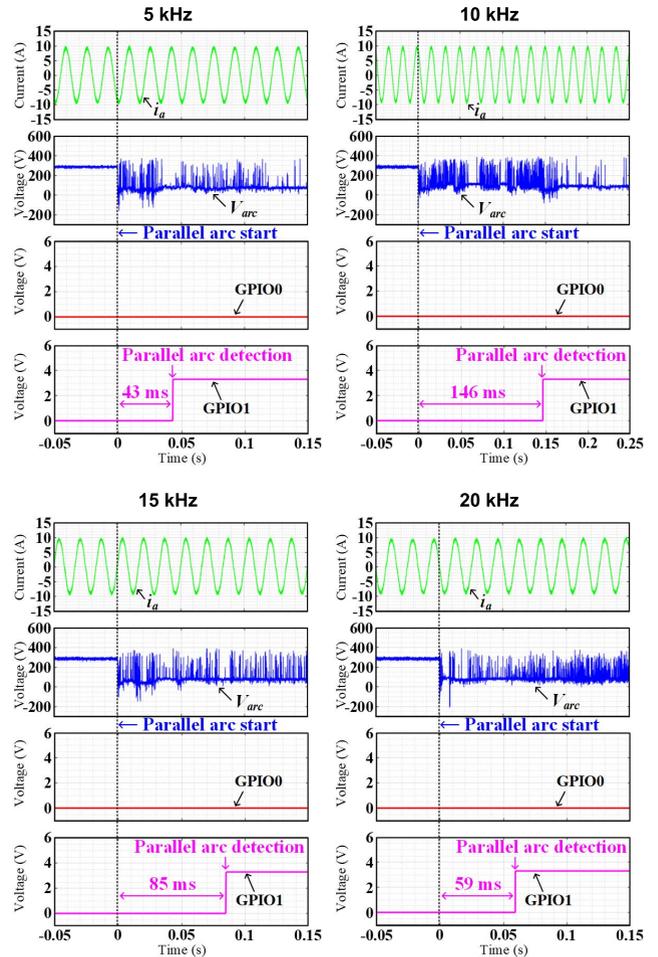
Therefore, the proposed method does not make the unwanted trip in the normal transient state.

B. REPEATED ARC TESTS OF THE PROPOSED METHOD

To verify the performance of the proposed technique, repeated arc tests were conducted. In the repeated test, each of the conditions in TABLE 1 was performed 10 times. Also, the arc detection probability, the arc detection time, and the arc identification probability of the proposed technique were examined.

Fig. 19 shows the arc detection probabilities of the proposed method obtained by repeated series and parallel arc tests. Fig. 19(a) demonstrates that the proposed technique detected the series arc with 100 % probability regardless of I_L and f_{sw}. Moreover, the average detection probability of the parallel arc was 96.25 %, where the proposed algorithm detected parallel arcs in 77 of 80 tests. The parallel arc was not detected in three attempts due to the lack of the high-frequency components made by the parallel arc. Even when parallel arcs occur, there are cases in which the high-frequency components are insufficiently generated because of the random and chaotic nature of the arc.
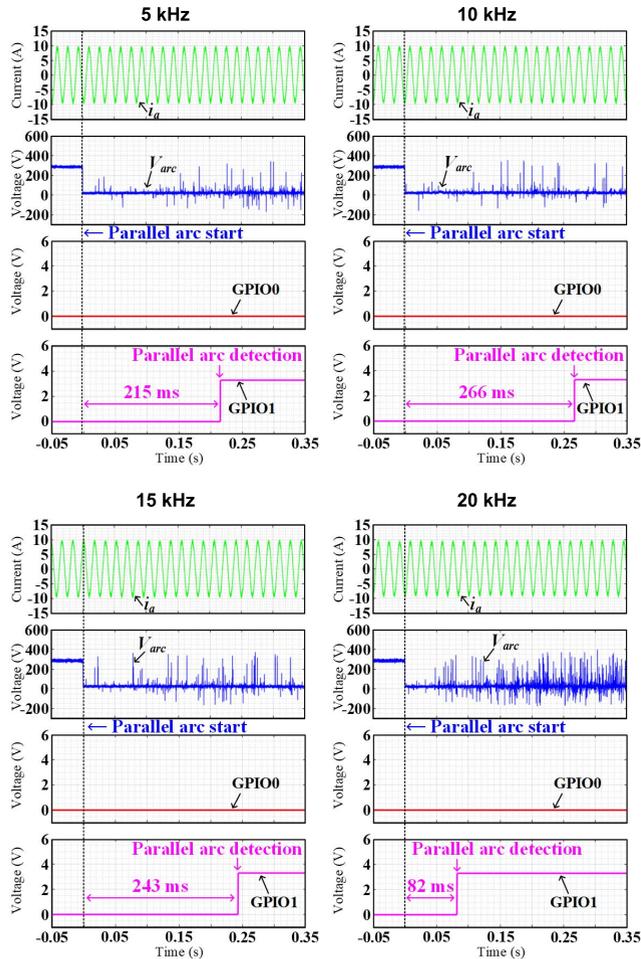
FIGURE 17. Experimental results of the proposed SPADI technique in the parallel arc according to f_{sw} when I_L is 5 A and I_{arc} is 1 A.

FIGURE 18. Experimental results of the proposed SPADI technique in the normal transient states (a) inverter startup, (b) inverter shutdown, (c) load step change (up), (d) load step change (down).

Meanwhile, the probability of identifying the correct arc type was 100 % when it was determined that the arc occurred.

Fig. 20 represents the average series arc detection times of the proposed method obtained from repetitive arc tests. Fig. 20 describes that the average series arc detection times were less than 0.15 s under all conditions except when I_L was 8 A and f_{sw} was 20 kHz. The average detection time for all conditions of the series arc was 0.11 s. When I_L was 8 A and f_{sw} was 20 kHz, the average arc detection time was 0.33 s which is less than the series arc detection time specified by UL1699B of 2.5 s [20]. The average series arc detection time under I_L of 8 A and f_{sw} of 20 kHz was significantly higher than in other conditions. This is because the series arc detection time was 1.7 s in one of ten repeated experiments.

Fig. 21 shows load currents for the fastest and slowest series arc detection time cases among 10 repeated tests conducted under I_L of 8 A and f_{sw} of 20 kHz. As demonstrated in Fig. 21(a), in the case with the shortest detection time, the high-frequency components significantly increased within a short time after the arc was generated. However, in the case with the slowest arc detection time in Fig. 21(b), the high-frequency components were not rapidly generated
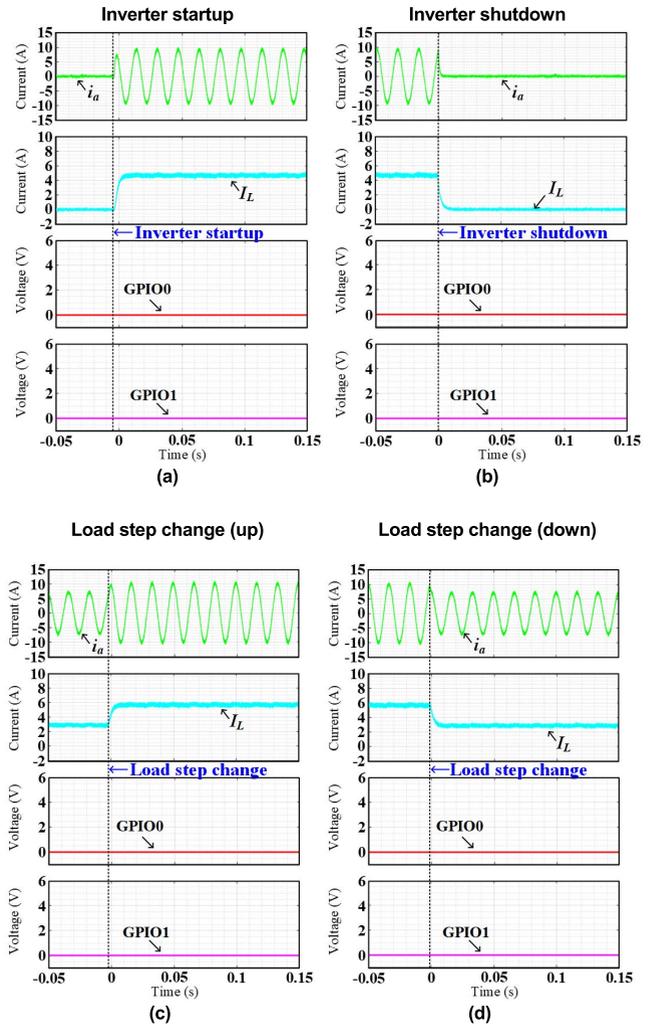
after arcing. The high-frequency components were sufficiently generated after 1.5 s, taking the slowest time to detect the series arc. Except for the attempt, the average series arc detection time with I_L of 8 A and f_{sw} of 20 kHz was 0.17 s.

Meanwhile, Fig. 20 indicates that the series arc detection time when I_L is 5 A was shorter than when I_L is 8 A. This is because when I_L is small (5 A), the transient arc time is long, resulting in a more prominent high-frequency component at the initial arc. Also, when I_L is 5 A, the series arc detection time was similar regardless of f_{sw}. However, when I_L is 8 A, the series arc detection time increased as f_{sw} increased. This phenomenon can be explained by the switching noise included in the frequency band used for the series arc detection. The frequency band used to detect the series arc in the proposed method is 5 kHz to 40 kHz. Depending on f_{sw}, the switching frequency and multiple components called switching noise may be included in this band.

Fig. 22 represents FFT results before arc generation according to f_{sw} when I_L is 8 A. As shown in Fig. 22, the
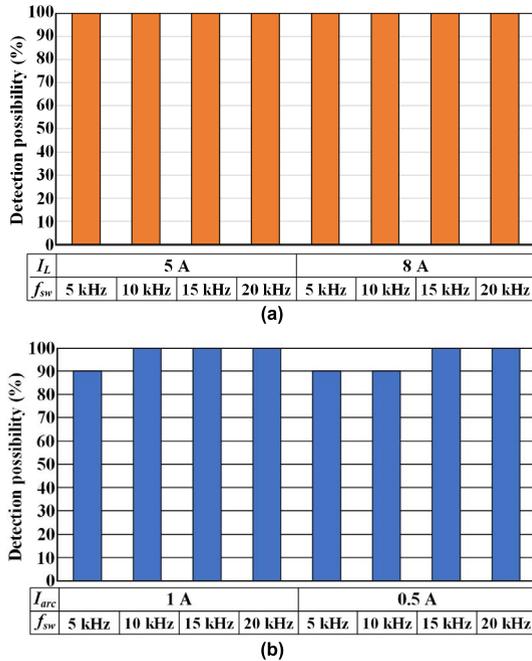
FIGURE 19. Arc detection probabilities of the proposed method obtained from repetitive arc tests (a) series arc, (b) parallel arc.
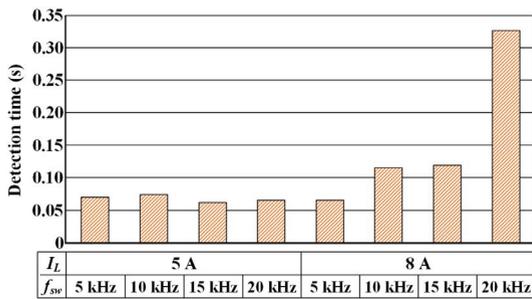

FIGURE 20. Average series arc detection times of the proposed method obtained from the repetitive arc.
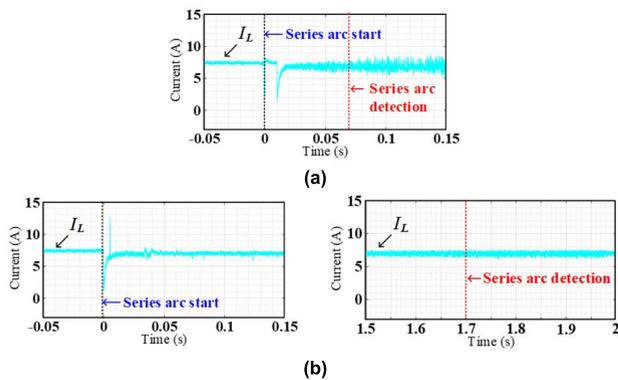

FIGURE 21. Load currents for the fastest and slowest series arc detection time cases among 10 repeated tests conducted under I_L of 8 A and f_{sw} of 20 kHz. (a) the shortest detection time case, (b) the slowest detection time case.

higher f_{sw}, the lower the switching noise included in the 5 kHz to 40 kHz band. Since the threshold value for detecting the
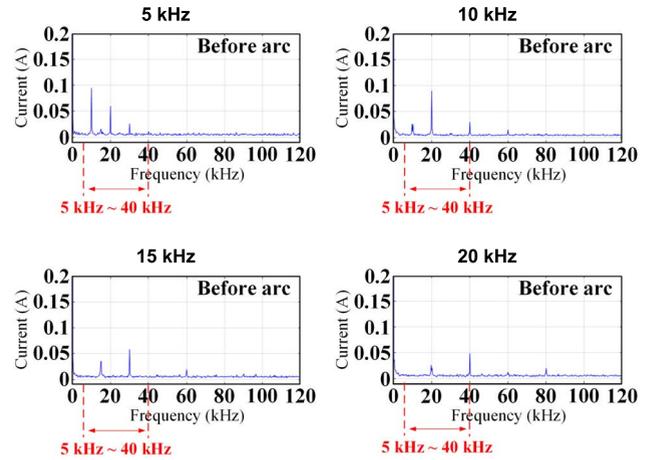

FIGURE 22. FFT results before arc generation according to f_{sw} when I_L is 8 A.
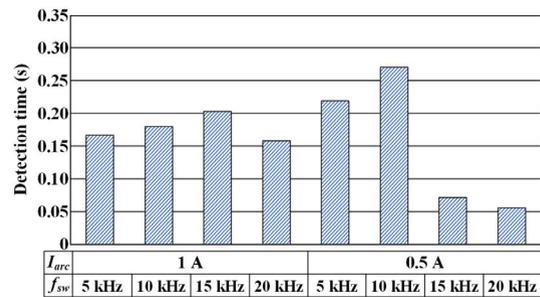

FIGURE 23. Average parallel arc detection times of the proposed method obtained from repetitive arc tests.

series arc is the same regardless of f_{sw}, even a relatively small increase in the high-frequency components under a low f_{sw} is judged to be the series arc. Therefore, as f_{sw} in I_L of 8 A increases, the detection time also increases.

Fig. 23 represents the average parallel arc detection times of the proposed method obtained from repetitive arc tests. As shown in Fig. 23, the parallel arc detection times were short as the series arc. For the parallel arc, the average detection time for all conditions was 0.16 s, which is very short as the series arc. The detection time of parallel arc was more significant when I_{arc} is 1 A than when I_{arc} is 0.5 A. This is because when I_{arc} is large, the high-frequency components generated in V_L are smaller than when I_{arc} is small. Consequently, Figs. 19, 20, and 23 demonstrate that the proposed technique can detect and identify series and parallel arcs quickly and accurately.

TABLE 3 compares the proposed technique with the existing techniques. TABLE 3 indicates that, unlike the conventional methods, the proposed method performances, such as the arc detection and discrimination probability and the arc detection time, were verified through repeated arc detection tests. As a result, the proposed method can secure high detection probability and short detection time. In addition, the proposed method did not malfunction in the normal transient state, as shown in Fig. 18. Moreover, it is confirmed that

TABLE 3. Comparisons between the conventional and proposed methods.

	Conventional method		Proposed method
	[18]	[19]	
Series arc detection probability	Not mention	Not mention	100 %
Parallel arc detection probability	Not mention	Not mention	96.25 %
Arc type identification probability	Not mention	Not mention	100 %
Series arc detection time	Not mention	Not mention	0.11 s
Parallel arc detection time	Not mention	Not mention	0.16 s
Ability to distinguish between the normal transient and arc conditions	No	Yes	Yes
DSP-based implementation	Yes	No	Yes

the proposed method is an algorithm that can be used in the actual electrical systems by implementing the proposed method based on DSP.

V. CONCLUSION

In this paper, the series and parallel arc detecting and identifying (SPADI) technique with high detection probability and fast detection speed was developed using the frequency characteristics of V_L and I_L. The performance of the proposed algorithm was verified through repeated arc detection tests. The algorithm of this paper has a limitation in that its performance was verified in a specific system. In future research, a DC arc detection algorithm applicable to various systems and high voltage and current ratings will be studied.

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