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RESEARCH ARTICLE

Per-Phase Switching Frequency Control Method to Extend Lifespan of Three-Phase Voltage Source Inverters

JAE-CHANG KIM AND SANGSHIN KWAK, (Member, IEEE)
School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea

Corresponding author: Sangshin Kwak (sskwak@cau.ac.kr)

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ABSTRACT This paper proposes a per-phase switching frequency control method to extend the lifespan of a three-phase voltage source inverter. The model predictive control that can intuitively deal with various control objectives is used in the proposed method. The cost function of the proposed technique consists of two terms. One is for current control, and another is for switching frequency control of each phase. Also, if necessary, a term for capacitor current RMS reduction can be added to the proposed cost function. The proposed technique reduces the switching loss of the most aged phase by reducing the number of switching operations. As a result, the reduced switching losses lower the junction temperature of the switching device. This extends the lifetime of the switching device. In addition, in the proposed technique, the capacitor current RMS, which can increase due to the per-phase switching frequency control, is effectively reduced by using the optional term for the capacitor current RMS reduction. The performances of the proposed method were verified through simulations and experiments.

INDEX TERMS Model predictive control, three-phase voltage source inverter, lifespan, switching frequency, DC-link capacitor, junction temperature.

NOMENCLATURE

T_j	Junction temperature.
MPC	Model predictive control.
VSI	Voltage source inverter.
T_{case}	Case temperature.
R	Load resistor.
L	Load inductor.
EMF	Electromotive force.
E_x	x-phase back EMF.
V_{dc}	Inverter input voltage.
C_{dc}	DC-link capacitor.
I_{dc}	Input source current.
I_{cap}	DC-link capacitor current.
I_{in}	Inverter input current.
I_{Lx}	x-phase load current.
V_{Lx}	x-phase load voltage.
T_s	Sampling period.
G_{iL}	Cost function for current control.
G_{sw}	Cost function for switching frequency control.
K_x	x-phase switching frequency control coefficient.
G_t	Proposed cost function.
M	Modulation index.
I_m	Maximum output current.
θ	Load angle.
G_{in}	Cost function for capacitor current RMS reduction.
P_{out}	Inverter output power.
I_{peak}	Peak load current.
G_{t_RMS}	Proposed cost function with capacitor current RMS reduction.
V_{cap}	Voltage across the DC-link capacitor.
P_{total}	Total loss of the device.
FTM	Foster thermal model.
PT_{con}	Conduction losses of the transistor.
PT_{sw}	Switching losses of the transistor.
PD_{con}	Conduction losses of the diode.
PD_{sw}	Switching losses of the diode.

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$T_{j(TX)}$	Transistor junction temperatures of SX.
$T_{j(DX)}$	Diode junction temperatures of SX.
N_f	Number of cycles at which the switch fails.
T_{on}	Heating time.
I_B	Current per bond wire.
V_c	Voltage rating.
D_b	Bond wire diameter.
ΔT_j	Junction temperature fluctuation.
T_{jmin}	Minimum junction temperature.
L	Capacitor lifetime.
L_o	Capacitor lifetime in the rated condition.
K_t	Temperature factor.
K_r	Ripple factor.
K_v	Voltage factor.
I_{capr}	Rated RMS of the capacitor.
I_{capn}	Normalized actual RMS of the capacitor current.

I. INTRODUCTION

Uses of power converters are increasing with the growth of renewable energy systems and eco-friendly transportation such as electric vehicles [1]. A power converter consists of various elements such as power devices, gate drivers, resistors, inductors, and capacitors. Among the different elements constituting the power conversion device, power devices are evaluated as the most fragile [2]. Therefore, since the converter lifespan is decided by the element with the shortest lifespan, the lifespan of the power devices is important.

The lifetime of power devices such as IGBTs is affected by the junction temperature (T_j) [3]. Various attempts have been made to reduce the average T_j or T_j fluctuations because the large average T_j or T_j fluctuations result in the short lifetime of switching devices. Variable switching frequency [3], [4], [5], [6], [7], discontinuous PWM (DPWM) [8], [9], [10], [11], reactive power [12], and switch redundances [13] were used to prolong the converter lifetime. Moreover, in the field of model predictive control (MPC) capable of fast dynamic operation and intuitive control, studies have been conducted to prolong the lifespan of the converter by adding a control objective for converter lifetime extension to the cost function [14], [15].

As explained earlier, the converter lifetime is decided by the shortest lifetime device. Therefore, to effectively extend the converter lifespan, it is necessary to reduce the T_j of the device with the shortest lifespan. However, the conventional converter life extension technique using the variable switching frequency is not effective because the switching frequency of all phases of the converter is changed at once without considering the aging state of each phase. As a result, the output quality of the converter changes dramatically with the application of the converter life extension techniques. If only the switching frequency of the aged phase is changed to improve the reliability of the converter, the variation in the converter output quality can be minimized and the desired lifespan extension performance can be secured. Meanwhile, the change in the converter switching pattern affects the DC-link capacitor [16]. Therefore, if the effects of modified switching patterns on capacitors are not considered, the changed switching patterns may adversely affect the lifespan of capacitors, easily broken elements along with power devices. However, in the existing converter life extension technique, the effects of the changed converter switching patterns to extend the converter lifespan on the DC-link capacitors were not analyzed. Also, countermeasures for accelerated capacitor aging were not established.

This article proposes a technique to extend the three-phase voltage source inverter (VSI) lifetime by changing the switching frequency of the most aging phase. To do this, MPC which can easily add the control objectives is used. The proposed method uses two control objectives to construct a cost function for the MPC. One is current control, and another is per-phase switching frequency control. Also, if necessary, an optional control objective for reducing capacitor current RMS can be added to the proposed cost function. This optional term of the proposed cost function is selectively used to prevent accelerating aging of the DC-link capacitor caused by the per-phase switching frequency control or to prolong the capacitor lifespan. The proposed technique lowers the T_j by reducing the switching loss of the most aged phase. This prolongs the inverter reliability. The proposed method was verified through simulations and experiments.

This article consists of six sections. First, Section I is an introduction. Section II shows the control method of the proposed technique and its simulation results. Section III analyzes the effect of the proposed approach on the capacitor current RMS and suggests countermeasures. Section III also demonstrates the capacitor current RMS reduction capability of the proposed method through simulations. Section IV displays the comparison with conventional and proposed methods. The experimental verifications for the proposed technique are in Section V. Section VI confirms the reduction effect of T_j, case temperature (T_{case}), and the capacitor current RMS by the proposed method with simulations and IR camera measurement results. Section VIII is the conclusion.

II. PROPOSED PER-PHASE SWITCHING FREQUENCY CONTROL METHOD

In this paper, the per-phase switching frequency is controlled using the MPC to extend the inverter lifespan. For this, the MPC in *abc* frame is utilized in the proposed method.

A. MODEL PREDICTIVE CONTROL IN ABC FRAME

A three-phase VSI with a three-phase motor as a load is displayed in Fig. 1. In Fig. 1, one phase of the three-phase motor is expressed as a resistor (R), an inductor (L), and a back electromotive force (EMF). e_a means a-phase back EMF. Also, the inverter input voltage is expressed as V_{dc}. C_{dc} stands for the DC-link capacitor. i_{dc}, i_{cap}, i_{in}, and i_{La} represent input source current, DC-link capacitor current, inverter input current, and a-phase load current, respectively. The six switches constituting the three-phase inverter are represented by S1, S2, S3, S4, S5, and S6. The proposed method

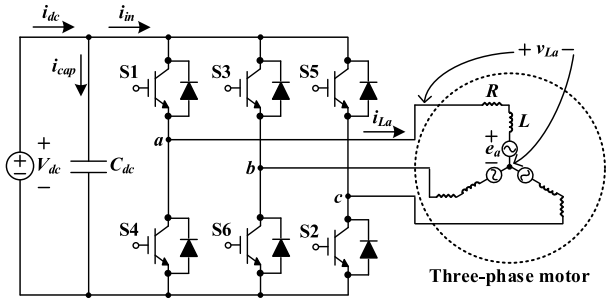


FIGURE 1. Three-phase VSI.

TABLE 1. Phase load voltages according to switching states.

Vector	S1	S3	S5	v_{La}	v_{Lb}	v_{Lc}
V_0	0	0	0	0	0	0
V_1	1	0	0	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
V_2	1	1	0	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$
V_3	0	1	0	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
V_4	0	1	1	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$
V_5	0	0	1	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$
V_6	1	0	1	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$
V_7	1	1	1	0	0	0

is designed to target inverters for motor drives. Therefore, no LC or LCL filters are installed as shown in Fig. 1. LC or LCL filters can be installed if grid-connected inverters are targeted.

Moreover, v_{La} means a-phase load voltage. The switching operation of the inverter changes the load voltage. TABLE 1 shows the load voltage of each phase according to switching states. In TABLE 1, v_{Lb} and v_{Lc} mean b- and c-phase load voltages, respectively. In addition, $\boldsymbol{V_0}$ to $\boldsymbol{V_7}$ represent the load voltage vectors expressed in the $\alpha\beta$ frame.

The phase load voltages can be expressed as (1).

$$\begin{aligned} v_{La} &= i_{La}R + L\frac{di_{La}}{dt} + e_a, \\ v_{Lb} &= i_{Lb}R + L\frac{di_{Lb}}{dt} + e_b, \\ v_{Lc} &= i_{Lc}R + L\frac{di_{Lc}}{dt} + e_c. \end{aligned} \tag{1}$$

In (1), i_{Lb} and i_{Lc} mean the load currents of the b- and c-phase, respectively. Also, e_b and e_c represent back EMFs of the b- and c-phase, respectively.

Using Euler approximation, the load voltage can be represented in the discrete time as (2).

$$\begin{aligned} v_{La}(k) &= i_{La}(k)R + L\frac{i_{La}(k+1) - i_{La}(k)}{T_s} + e_a(k), \\ v_{Lb}(k) &= i_{Lb}(k)R + L\frac{i_{Lb}(k+1) - i_{Lb}(k)}{T_s} + e_b(k), \\ v_{Lc}(k) &= i_{Lc}(k)R + L\frac{i_{Lc}(k+1) - i_{Lc}(k)}{T_s} + e_c(k). \end{aligned} \tag{2}$$

In (2), T_s denotes the sampling period. When (2) is rearranged for the $(k+1)^{\text{th}}$ predicted load current, (3) is obtained. The superscript P stands for the predicted value.

$$\begin{aligned} i^p_{La}(k+1) &= \frac{T_s}{L}(v_{La}(k) - e_a(k)) + \left(1 - \frac{T_sR}{L}\right) i_{La}(k), \\ i^p_{Lb}(k+1) &= \frac{T_s}{L}(v_{Lb}(k) - e_b(k)) + \left(1 - \frac{T_sR}{L}\right) i_{Lb}(k), \\ i^p_{Lc}(k+1) &= \frac{T_s}{L}(v_{Lc}(k) - e_c(k)) + \left(1 - \frac{T_sR}{L}\right) i_{Lc}(k). \end{aligned} \tag{3}$$

Meanwhile, the $(k+1)^{\text{th}}$ reference of the load current can be expressed as (4) using Lagrange extrapolation [17]. In (4), the superscript * means the reference value.

$$\begin{aligned} i^*_{La}(k+1) &= 3i^*_{La}(k) - 3i^*_{La}(k-1) + i^*_{La}(k-2), \\ i^*_{Lb}(k+1) &= 3i^*_{Lb}(k) - 3i^*_{Lb}(k-1) + i^*_{Lb}(k-2), \\ i^*_{Lc}(k+1) &= 3i^*_{Lc}(k) - 3i^*_{Lc}(k-1) + i^*_{Lc}(k-2). \end{aligned} \tag{4}$$

The cost function for the current control, called g_{iL}, is expressed as (5).

$$\begin{aligned} g_{iL} = &\left|i^*_{La}(k+1) - i^p_{La}(k+1)\right| + \left|i^*_{Lb}(k+1) - i^p_{Lb}(k+1)\right| \\ &+ \left|i^*_{Lc}(k+1) - i^p_{Lc}(k+1)\right|. \end{aligned} \tag{5}$$

In the MPC, the voltage source inverter is controlled using the switching state that makes g_{iL} the smallest.

B. PROPOSED PER-PHASE SWITCHING FREQUENCY CONTROL METHOD

The switching frequency of the most aged phase is controlled in the proposed approach to extend the inverter lifespan effectively. To this end, a cost function, called g_{sw}, which can change the switching frequency of each phase, is developed as (6).

$$\begin{aligned} g_{sw} = &k_a\left|S1(k) - S1^p(k+1)\right| + k_b\left|S3(k) - S3^p(k+1)\right| \\ &+ k_c\left|S5(k) - S5^p(k+1)\right|. \end{aligned} \tag{6}$$

In (6), S1(k), S3(k), and S5(k) represent k^{th} S1, S3, and S5 switching states, respectively. Also, S1^p($k+1$), S3^p($k+1$), and S5^p($k+1$) are the $(k+1)^{\text{th}}$ predicted switching states of S1, S3, and S5, respectively. k_a, k_b, and k_c are switching frequency control coefficients that control the number of switching of the a-, b-, and c-phase, respectively. Since the switches of one phase in the voltage source inverter operate complementarily, a cost function for controlling the number of switches can be constructed using only three upper switches. By increasing k_a, k_b, and k_c, the switching frequency of each phase can be reduced.

Meanwhile, as shown in TABLE 2, the three-phase VSI has two zero vectors that make the load voltage 0. If only one zero vector is used, there is no thermal balance between the upper and lower switches. Therefore, the proposed method includes only one zero vector in the switching state candidate group for choosing the optimal switching state at every sampling

TABLE 2. Parameters used in the simulation.

Parameter	Value
V_{dc}	200 V
C_{dc}	680 μF
R	10 Ω
L	10 mH
Sampling frequency	20 kHz
Magnitude of reference load current	5 A

period. In addition, as for the zero vector included in the candidate group, $\boldsymbol{V_0}$ and $\boldsymbol{V_7}$ are alternately selected for every sampling period so that two types of zero vectors are evenly selected.

$$g_t = g_{iL} + g_{sw}. \tag{7}$$

In (7), g_t denotes the proposed cost function. The proposed cost function is created by adding (5) and (6). Through this, it is possible to control the load current and the number of switching of each phase. To diminish the switching frequency of the most aged phase, the switching frequency control coefficient of the most aged phase is set to a positive number, and the coefficients of the other two phases are set to 0. Moreover, if the switching frequency control coefficient of each phase is appropriately adjusted, the switching frequency of all phases can be properly regulated. Through this, the aging degree of the three-phase can be adequately managed.

Before applying the proposed technique to the most aged phase, it is necessary to know the aging degree of switching devices. Various methods to know the aging degree of switching devices have been proposed through recent research. As the switches age, the on-resistance increases due to bond wire crack and bond wire lift-off [18]. Also, the turn-on time and gate leakage current rise [19], [20]. Moreover, in the case of SiC MOSFET, the voltage between the drain and source also changes [21], [22]. Therefore, the aging degree of the switching devices is estimated using these aging indicators: on-resistance, turn-on time, gate leakage current, drain and source voltage, etc. A detailed method for determining the degree of aging is not covered because it is beyond the scope of this paper.

C. SIMULATION RESULTS OF THE PROPOSED TECHNIQUE

The effectiveness of the proposed approach was confirmed by simulations. The simulation tool used in this paper is PSIM. The three-phase VSI shown in Fig. 1 was implemented as a simulation. In addition, assuming that the back EMF is 0, a three-phase *R-L* load was utilized for the inverter load. The parameters used in the simulation are summarized in TABLE 3.

The simulation waveforms of the proposed technique are displayed in Fig. 2. Waveforms of Fig. 2(a) are obtained under the full switching condition in which the number of switching is not reduced by setting k_a, k_b, and k_c in (6) to 0. In Fig. 2(a), the signal waveforms of the three-phase upper switches are displayed. Fig. 2(a) demonstrates that since it is a full switching condition, the number of switching of three-phase is similar. Also, RMS of i_{cap} is 1.974 A.

TABLE 3. Parameters used for comparison with conventional methods.

Parameter	Value
V_{dc}	1500 V
C_{dc}	680 μF
R	20 Ω
L	10 mH
(Average) switching frequency	4 kHz
Magnitude of reference load current	30 A

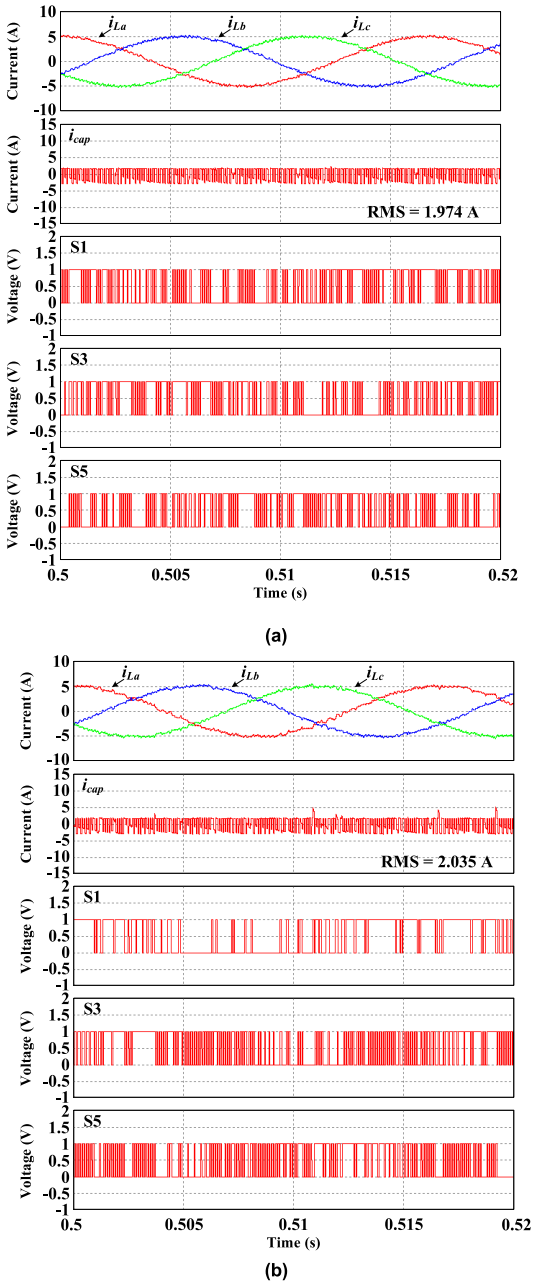


FIGURE 2. Simulation waveforms of the proposed per-phase switching frequency control method (a) full switching (b) half switching of the a-phase leg.

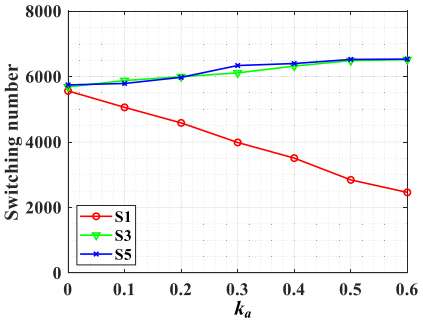


FIGURE 3. Switching numbers of upper switches according to k_a.

Fig. 2(b) represents the simulation results in which the number of a-phase switching is reduced by about half, assuming that the a-phase leg is the most aged. To reduce the a-phase switching frequency, the k_a was set to 0.6 and both k_b and k_c were set to 0. Fig. 2(b) shows that the number of switching of a-phase is noticeably reduced compared to Fig. 2(a). Also, there is no significant change in the switching frequency of the b- and c-phase. Meanwhile, in the case of the load current, the quality of the a-phase load current is lowered because the a-phase switching frequency is reduced. Also, the ripple of i_{cap} rises slightly. RMS of i_{cap} is 2.035 A.

Fig. 3 shows the number of switching operations of upper switches according to k_a in the proposed technique. In Fig. 3, both k_b and k_c are set to 0. To obtain the results of Fig. 3, the switching waveforms during 1 s are used. Fig. 3 indicates that the number of switching of a-phase decreases as k_a increases. Also, the number of switching of the remaining phases increases slightly.

Figs. 2 and 3 indicate that the proposed technique can lower the most aged phase switching frequency. This reduction in the switching frequency can diminish the switching loss, thereby reducing T_j. In addition, the quality of the load current slightly deteriorates due to the decrease in the number of switching. Meanwhile, the i_{cap} waveform in Fig. 2(b) demonstrates that the ripple of the i_{cap} slightly rises when the number of a-phase switching is reduced. Since the increased capacitor ripple by the proposed technique shortens the capacitor lifespan, more detailed research and countermeasures are needed. Therefore, in the next section, the effects of the proposed technique on i_{cap} are dealt with in detail, and countermeasures are suggested.

III. EFFECTS OF THE PROPOSED METHOD ON DC-LINK CAPACITOR CURRENT AND CAPACITOR CURRENT RMS REDUCTION METHOD

A. EFFECTS OF THE PROPOSED METHOD ON DC-LINK CAPACITOR CURRENT

Section II indicates that the RMS of i_{cap} increases in the proposed per-phase switching frequency control. This phenomenon becomes more severe as the inverter load angle increases. Fig. 4 represents the simulation waveforms when the load angle is large. In the simulation of Fig. 4, the load

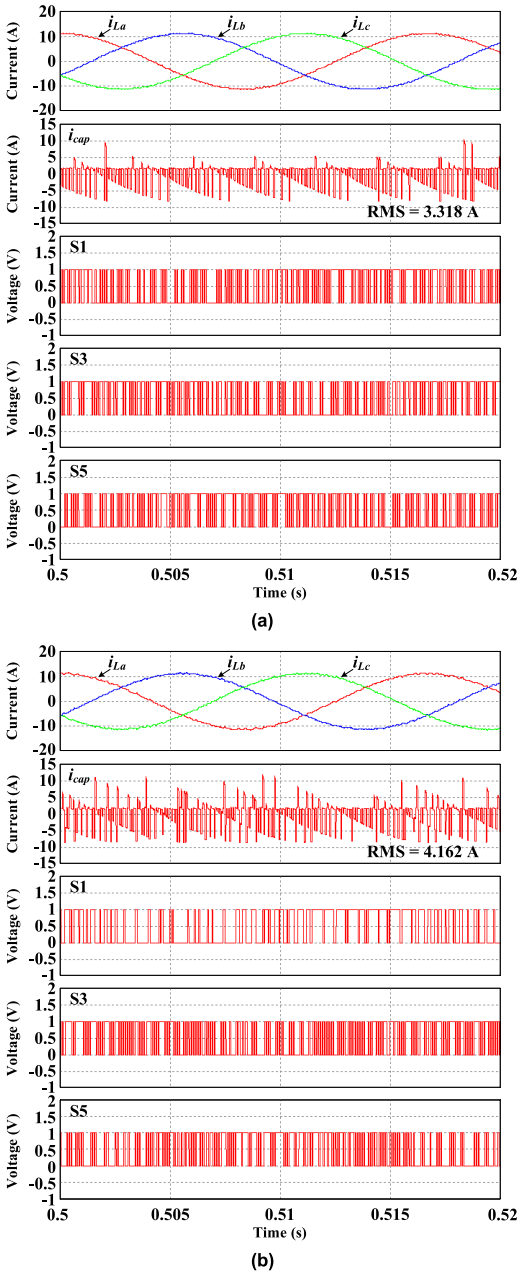


FIGURE 4. Simulation waveforms of the proposed per-phase switching frequency technique in the large load angle (a) full switching (b) half switching of the a-phase leg.

resistance was changed to 2 Ω to increase the load angle. The reference value of the load current was modified to 11.18 A to set the output power equal to Fig. 2. In addition, the rest of the conditions were the same as in TABLE 2. Note that the load angle is 21° for Fig. 2 and 62 ° for Fig. 4.

Fig. 4(a) shows the simulation results without reducing the number of switching by setting k_a, k_b, and k_c to 0. Also, Fig. 4(b) shows simulation results in which the a-phase switching frequency is reduced by half by setting k_a to 0.6 and k_b and k_c to 0. The comparison of Figs. 4(a) and (b) demonstrates that the ripple of i_{cap} increases significantly under the

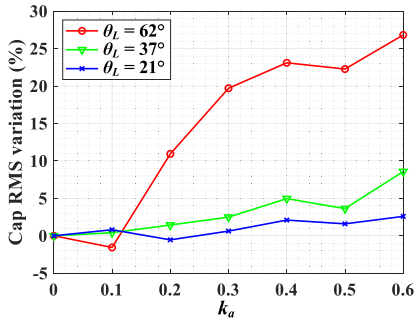


FIGURE 5. Capacitor current RMS variation according to k_a change.

half switching condition. Due to the rise of ripple, the RMS of i_{cap} increases from 3.318 A to 4.162 A in Fig. 4. Also, comparing Fig. 2(b) and Fig. 4(b) demonstrates that the ripple of i_{cap} rises significantly under a large load angle condition when the switching frequency is reduced by almost half.

Fig. 5 shows the change rate of i_{cap} RMS by k_a variations under various load angles. The result in Fig. 5 is obtained when k_b and k_c are set to 0. When the load angle is small, the increase in i_{cap} RMS according to the rise of k_a is not large. However, in the large load angle, i_{cap} RMS dramatically increases. Therefore, there is a need to solve the i_{cap} RMS rise problem that occurs when the proposed technique is used in the condition of the large load angle.

B. CAPACITOR CURRENT RMS REDUCTION METHOD

Reducing the RMS of the inverter input current decreases the ripple of the i_{cap}, resulting in the reduction of the i_{cap} RMS. The i_{cap} RMS can be expressed as (8) [16].

$$\text{RMS of } i_{cap} = \sqrt{(\text{RMSof} i_{in})^2 - (\text{average of } i_{dc})^2}. \quad (8)$$

Moreover, the average of i_{dc} can be expressed by (9) [16].

$$\text{Average of } i_{dc} = 0.75 m I_m \cos\theta. \quad (9)$$

In (9), m, I_m and θ mean modulation index, maximum output current, and load angle, respectively. Equation (9) indicates that the average of i_{dc} is constant at a steady state. Therefore, to reduce the i_{cap} RMS, the i_{in} RMS should be reduced. The i_{in} RMS can be reduced by diminishing the ripple of i_{in} [16].

In order to reduce the i_{cap} RMS in the conventional MPC, the following term (10) is added to the cost function [23]. The purpose of (10) is to reduce the i_{in} RMS and ultimately reduce the i_{cap} RMS.

$$g_{in} = k_{in} \left| i^*_{in}(k+1) - i^p_{in}(k+1) \right|. \quad (10)$$

In (10), g_{in} means the term for i_{cap} RMS reduction. Adding g_{in} to the cost function makes the i^p_{in} follow the i^*_{in}. i^*_{in} in (10) is set as the average current of i_{in}. Minimizing g_{in} reduces the i_{in} ripple because i_{in} tracks the average of i_{in}. As a result, the i_{cap} RMS is diminished. In (10), k_{in} is a coefficient that can control the RMS reduction ability. As k_{in} increases, i_{cap} RMS reduction ability increases. In [23], the i^*_{in} was calculated using the output power and V_{dc} as (11).

$$P_{out} = 3\left(\frac{i^*_{peak}}{\sqrt{2}}\right)^2 R = 1.5 (i^*_{peak})^2 R,$$
$$i^*_{in}(k+1) = \frac{P_{out}}{V_{dc}} = \frac{1.5 R (i^*_{peak})^2}{V_{dc}}. \quad (11)$$

In (11), P_{out} is the inverter output power, and i^*_{peak} represents the peak reference load current. The calculation method such as (11) has a disadvantage in that i^*_{in} cannot be accurately calculated unless the R is accurately known. To overcome this problem, this paper proposes new i^*_{in} calculation method as shown in (12).

$$i^*_{in}(k+1) = \frac{1}{M} \sum_{k-M+1}^{k} i^*_{in}(n). \quad (12)$$

As shown in (12), in this paper, the moving average of i^*_{in} of the previous step is used to calculate the $(k+1)^{\text{th}} i^*_{in}$. In (12), M represents the number of i^*_{in} used for the moving average. Also, $i^*_{in}(n)$ means the reference of the n^{th} inverter input current. $i^*_{in}(n)$ can be calculated as in (13) using the n^{th} inverter switching state and the reference load current.

$$i^*_{in}(n) = \text{S1}(n)\, i^*_{La}(n) + \text{S3}(n)\, i^*_{Lb}(n) + \text{S5}(n)\, i^*_{Lc}(n).$$
$$(\text{If } S1(n) = S3(n) = S5(n) = 1, \text{ then, } i^*_{in}(n) = 0.) \quad (13)$$

In (13), S1(n), S3(n), and S5(n) represent the n^{th} state of S1, S3, and S5, respectively. Also, $i^*_{La}(n)$, $i^*_{Lb}(n)$, and $i^*_{Lb}(n)$ are the n^{th} reference load current of a-, b-, and c-phase, respectively. Consequently, $i^*_{in}(k+1)$ can be calculated using the three-phase reference load current and the switching state through (12) and (13).

Meanwhile, (14) shows a calculation method of $i^p_{in}(k+1)$ in (10).

$$i^p_{in}(k+1) = \text{S1}^p(k+1)\, i^p_{La}(k+1) + \text{S3}^p(k+1)\, i^p_{Lb}(k+1) + \text{S5}^p(k+1)\, i^p_{Lc}(k+1).$$
$$(\text{If S1}^p(k+1) = \text{S3}^p(k+1) = \text{S5}^p(k+1) = 1, \text{ then, } i^p_{in}(k+1) = 0.) \quad (14)$$

In (14), S1$^p(k+1)$, S3$^p(k+1)$, and S5$^p(k+1)$ are the $(k+1)^{\text{th}}$ predictive state of S1, S3, and S5, respectively. Equation (14) represents that the predicted inverter input current can be calculated from the predicted load current and the predicted switching state. As a result, the g_{in} of (10) can be calculated through (12) to (14).

Equation (15) shows the cost function of the proposed technique with the i_{cap} RMS mitigation capability. This cost function is created by adding (10) to (7).

$$g_{t\_RMS} = g_{iL} + g_{sw} + g_{in}. \quad (15)$$

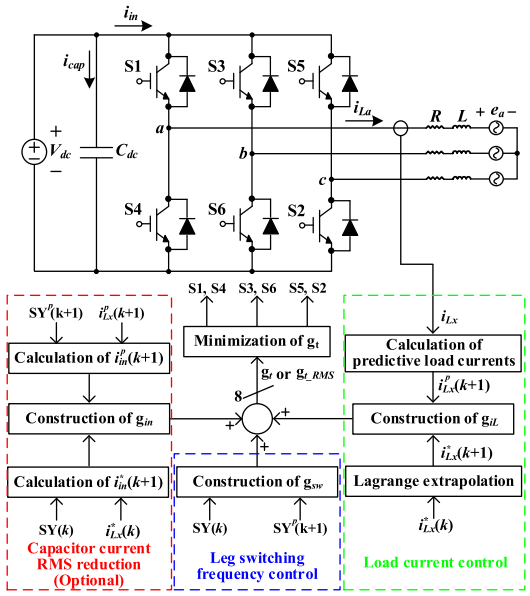


FIGURE 6. Flow chart of the proposed method.

Fig. 6 represents the flow chart of the proposed technique. In Fig. 6, i_{Lx}, $i^*_{Lx}(k)$, $i^*_{Lx}(k+1)$, and $i^p_{Lx}(k+1)$ represent three-phase values. For example, i_{Lx} means i_{La}, i_{Lb}, and i_{Lc}. Also, $\mathrm{SY}^p(k+1)$ represents $\mathrm{S1}^p(k+1)$, $\mathrm{S3}^p(k+1)$, and $\mathrm{S5}^p(k+1)$. The g_{in} for reducing RMS of i_{cap} in Fig. 6 is optionally used when it is needed to reduce RMS of i_{cap}. In order to select the optimal switching state through the cost function g_t or g_{t_RMS}, the cost function results in all switching states are calculated. Since there are a total of eight switching states of the three-phase inverter, the eight cost function results can be obtained according to the switching states. Among the eight cost function results, the smallest cost function result is selected and used for inverter control.

Generally, in the MPC, the coefficients of various control objectives constituting the cost function are determined through trial and error rather than a deterministic method. In this paper, coefficients such as k_a, k_b, k_c, and k_{in} were determined through trial and error, which is a general method for setting coefficients.

C. SIMULATION RESULTS OF THE PROPOSED METHOD WITH CAPACITOR CURRENT RMS REDUCTION

Simulation waveforms were obtained to confirm the i_{cap} RMS reduction technique. The k_{in} used in the simulation is 0.1.

Fig. 7 represents the simulation waveforms applying a-phase half switching and the i_{cap} RMS reduction. Fig. 7(a) is the simulation results under the small load angle condition. Also, Fig. 7(b) displays the simulation waveforms under the large load angle condition. Comparisons of Figs. 2, 4, and 7 indicate that the ripple of the i_{cap} is significantly reduced thanks to the i_{cap} RMS reduction technique under a-phase half switching condition. Due to the reduction of ripple, the

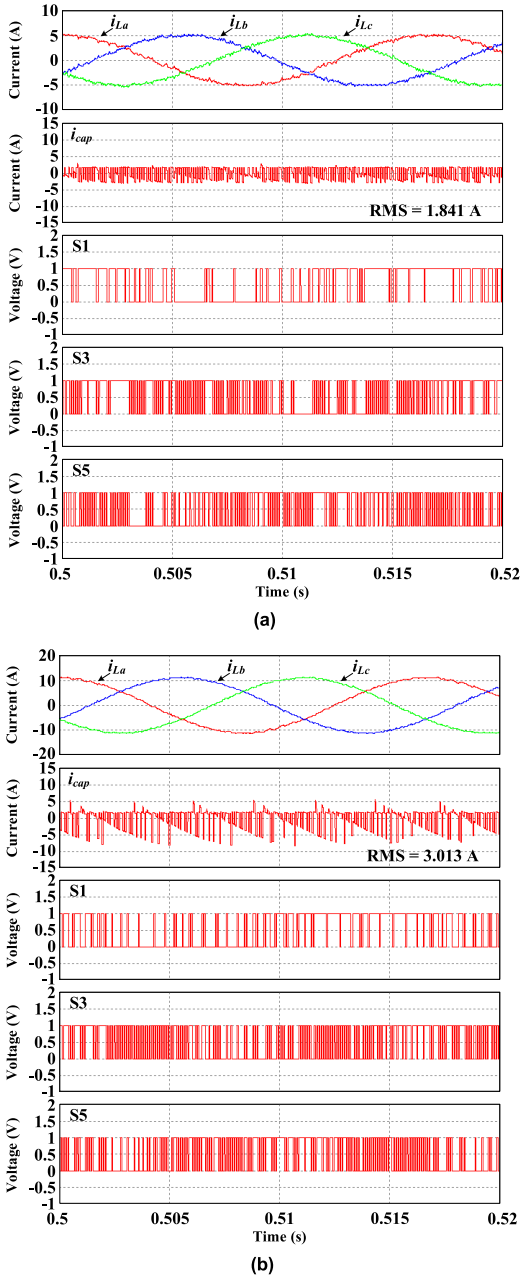


FIGURE 7. Simulation results of proposed method with capacitor current RMS reduction (a) load angle = 21 ° (Fig. 2) (b) load angle = 62 °(Fig. 4).

RMS of i_{cap} decreases from 2.035 A to 1.841 A at low load angle (Fig. 2) and from 4.162 A to 3.013 A at high load angle (Fig. 4). Therefore, it is possible to prevent the acceleration of capacitor aging using the i_{cap} RMS reduction method.

Fig. 8 shows the trend of the average output current THD and the capacitor current RMS according to the change in k_{in}. Fig. 8 represents the results obtained by simulation using the conditions in TABLE 2. As k_{in} increases, the average output current THD increases because the weight for load current control becomes relatively small. In addition, due to

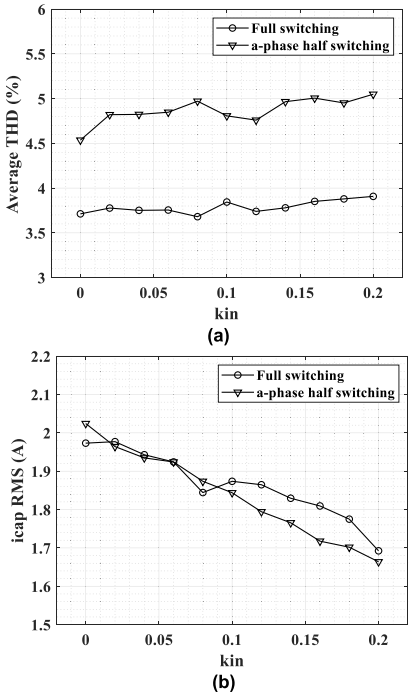


FIGURE 8. Average output current THD and capacitor current RMS as a function of k_{in} (a) average load current THD (b) capacitor current RMS.

the increase in k_{in}, the weight for reducing capacitor current RMS increases, so the capacitor current RMS decreases.

D. AVERAGE OUTPUT CURRENT THD AND CAPACITOR CURRENT RMS ACCORDING TO DC-LINK CAPACITANCE

The inverter output current THD and capacitor current RMS according to the DC-link capacitance size were examined. Fig. 9 is the simulation result when the DC-link capacitance is 100 μF. Fig. 9(a) is the result under the full switching condition without reducing the number of switching of three phases, and Fig. 9(b) is the result of reducing the number of a-phase switching by about half. In addition, Fig. 9(c) is the result of reducing the number of a-phase switching by half and reducing the RMS of DC-link capacitor current. From Fig. 9, it can be confirmed that the proposed technique can reduce the number of switching of one-phase even at low DC-link capacitance with little voltage stabilizing effect and can also reduce DC-link capacitor current RMS.

Fig. 10 is the simulation result when the DC-link capacitance is 700 μF. Figs. 10(a), (b), and (c) are the results of the full switching condition without reducing the number of switching of three phases, the a-phase half switching condition, and the a-phase half switching with capacitor current RMS reduction condition, respectively. Fig. 10 indicates that the one-phase switching reduction capability and capacitor RMS reduction capability of the proposed technique can be confirmed even under the condition of high DC-link capacitance.

Fig. 11 shows the average load current THD and capacitor current RMS according to the DC-link capacitance.

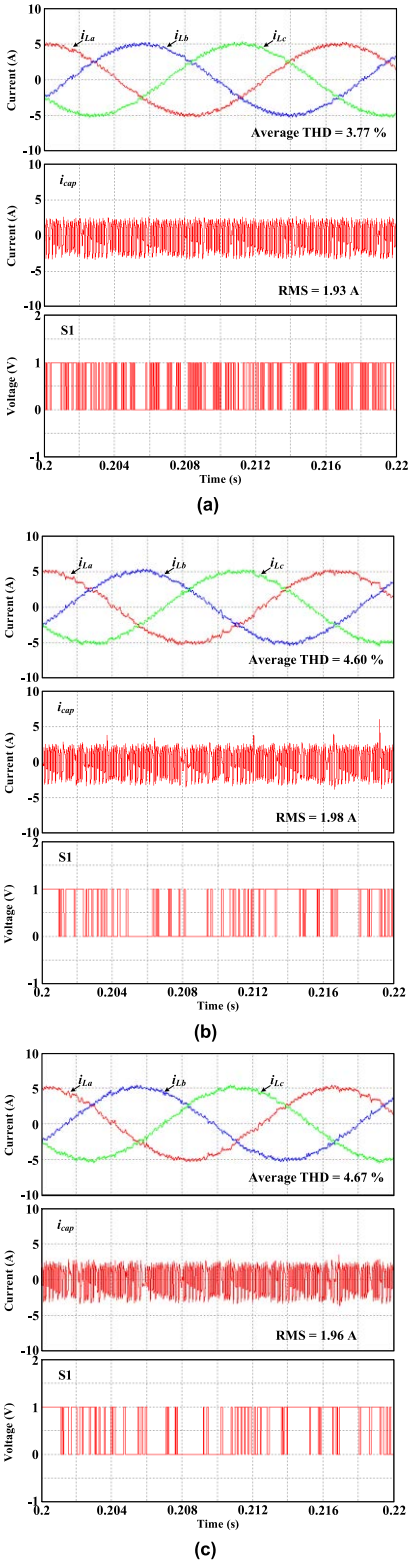


FIGURE 9. Simulation results when DC-link capacitance is 100 μF (a) full switching (b) half switching (c) half switching with capacitor current RMS reduction.

Fig. 11(a) shows the average THD of the three-phase load current, and Fig. 11(b) represents the capacitor current RMS. As shown in Fig. 11(a), the average load current THD hardly

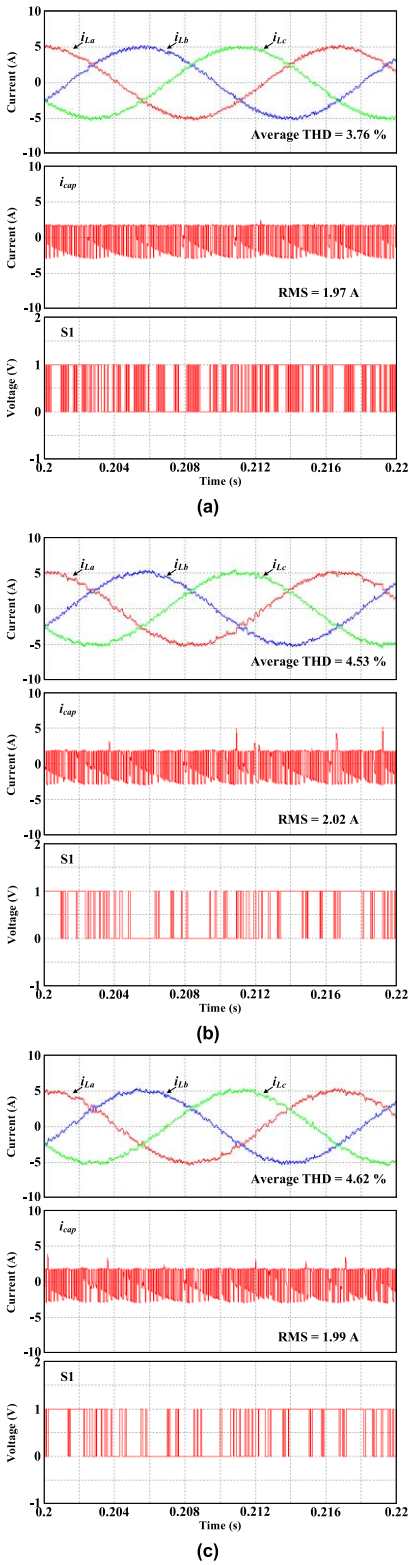


FIGURE 10. Simulation results when DC-link capacitance is 700 μF (a) full switching (b) half switching (c) half switching with capacitor current RMS reduction.

changes according to the DC-link capacitance. However, when a-phase switching is reduced by half, the THD in half switching condition becomes larger than in the full switching condition because the number of switching is reduced. Meanwhile, Fig. 11(b) shows that the capacitor current RMS slightly increases as the capacitance increases. The rise in capacitor current RMS due to the increase in capacitance can be mitigated by using the capacitor current RMS reduction capability of the proposed technique.

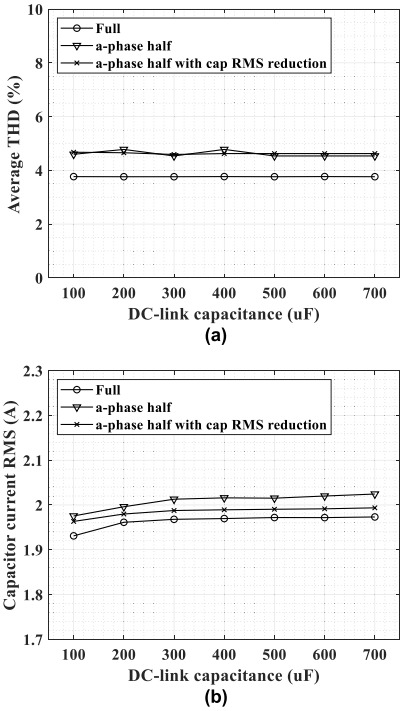


FIGURE 11. Average load current THD and capacitor current RMS according to DC-link capacitance (a) average THD of load current (b) capacitor current RMS.

E. EFFECTS OF REDUCING DC-LINK CAPACITOR CURRENT RMS ON DC-LINK CAPACITOR VOLTAGE

Simulations were conducted to check the capacitor voltage quality according to the change in capacitor current RMS. The capacitor voltage quality observed in the simulation is peak-to-peak value. To take a good look at the peak-to-peak value, 100 μF of DC-link capacitance was used. Moreover, the remaining parameters are the same as TABLE 2.

Fig. 12 shows before and after applying the capacitor current RMS reduction technique without reducing the number of switching. In Fig. 12, v_{cap} means the voltage across the DC-link capacitor. Fig. 12(a) is the result before applying the capacitor current RMS reduction method. Also, Fig. 12(b) is the result when the capacitor current RMS reduction method is applied to reduce the capacitor current RMS by about 17 %. The comparison of Figs. 12(a) and (b) indicates that the peak-to-peak of the capacitor voltage hardly changes in the full switching condition even when the capacitor current RMS is reduced.

Fig. 13 shows the capacitor current and voltage simulation results before and after applying the capacitor current RMS reduction technique under the condition that the number of

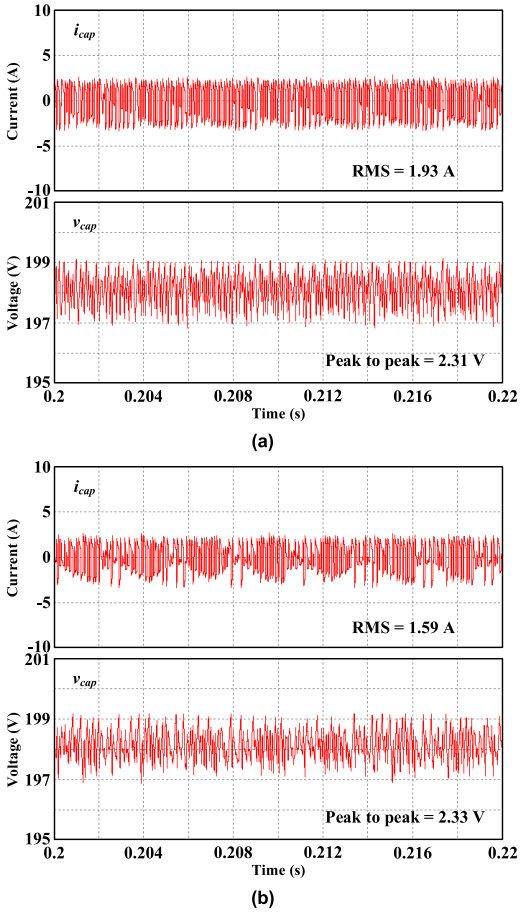


FIGURE 12. Capacitor current and capacitor voltage waveforms under full switching condition (a) full switching (b) full switching with capacitor current RMS reduction.

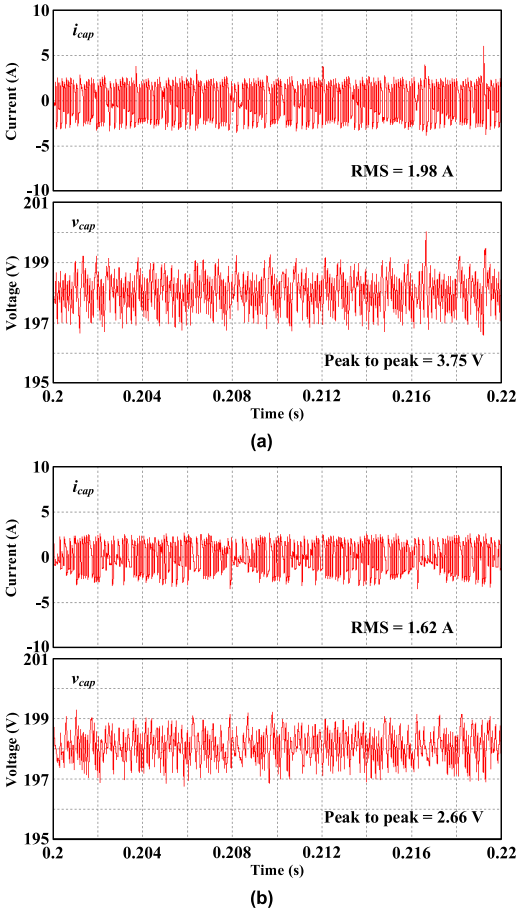


FIGURE 13. Capacitor current and capacitor voltage waveforms under half switching condition (a) only half switching (b) half switching with capacitor current RMS reduction.

a-phase switching is reduced by about half. Fig. 13(a) is the result before applying the capacitor current RMS reduction technique. In addition, Fig. 13(b) shows the result when the capacitor current RMS is reduced by about 17 % by applying the capacitor current RMS reduction technique. By comparing Fig. 12(a) and Fig 13(a), it can be seen that the capacitor voltage peak-to-peak value rises when the number of *a*-phase switching number is reduced by half. Also, by comparing Fig. 13(a) and Fig. 13(b), it can be confirmed that both the capacitor current RMS and the capacitor voltage peak-to-peak value decrease when the capacitor current RMS reduction technique is applied in half switching operation.

Fig. 14 shows the change in capacitor voltage peak-to-peak value according to the capacitor current RMS reduction. Fig. 14 represents that the capacitor voltage peak-to-peak value does not change significantly when only the capacitor current RMS reduction technique is applied. However, when applied with the one-phase switching frequency reduction by half, the capacitor voltage peak-to-peak value decreases. Therefore, in the half switching condition, the proposed capacitor current RMS reduction technique improves not only the capacitor current RMS but also the capacitor voltage quality.

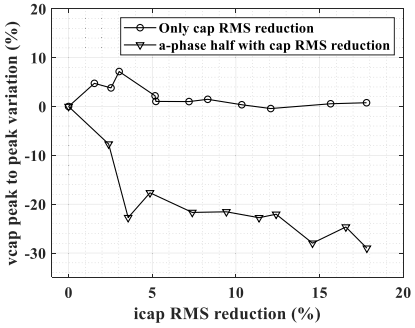


FIGURE 14. Capacitor voltage peak-to-peak variations according to capacitor current RMS reduction.

IV. COMPARISON WITH CONVENTIONAL AND PROPOSED METHOD

The lifespan of the converter is determined by the most aged device. Therefore, the conventional converter lifetime extension technique by reducing the switching frequency of

all phases and the proposed converter lifetime extension technique by reducing the switching frequency of the most aged phase have similar reliability improvement capabilities. The converter lifetime extension technique using variable switching frequency reduces the switching frequency, so the output quality deteriorates. However, since the proposed method reduces the switching frequency of one phase other than three phases, it is possible to alleviate the deterioration of output quality due to the reduction of the switching frequency compared to the existing method. To compare the proposed method with the existing method, the simulations were conducted under the conditions shown in TABLE 3. Also, the existing techniques used for comparison are space vector PWM (SVPWM) and DPWM-based variable switching frequency technique [10].

Fig. 15 shows the simulation results of SVPWM-based variable switching frequency. In this conventional technique, the reliability of the converter is improved by adjusting the switching frequency of the SVPWM. Fig. 15(a) represents the simulation result without reducing the switching frequency. Also, Fig. 15(b) describes the simulation result when the switching frequency is reduced to two-thirds of the initial value. The comparison of Figs 15(a) and (b) indicates that the output current THD greatly increases from 3.59 % to 5.39 % due to the reduction in the number of switching. Moreover, the capacitor current RMS is almost unchanged.

Fig. 16 shows the simulation results of the DPWM-based variable switching frequency technique. In [10], a DPWM-based variable switching frequency technique was implemented three-phase parallel inverters. Unlike [10], since this paper is not for a parallel structure, the switching frequency is varied by applying DPWM to one inverter. Fig. 16(a) shows the result when the clamping angle is 0 degrees. In other words, the switching frequency is not reduced. Fig. 16(b) represents the result of maximally reducing the switching frequency by setting the clamping angle to 60 degrees. In this condition, the switching frequency is reduced by 33 %. The comparison of Figs 16(a) and (b) demonstrates that the output current THD deteriorates rapidly after switching reduction. Meanwhile, the capacitor current RMS hardly changes, as in Fig. 15.

Fig. 17 shows the simulation results of the proposed technique. The proposed technique used in Fig. 17 did not use the capacitor current RMS reduction technique. Fig. 17(a) is before the reduction of the switching. Also, Fig. 17(b) represents the result of reducing the *a*-phase switching frequency by about 33 %. The comparison of Figs 17(a) and (b) indicates that the output current THD slightly increases from 4.61 % to 4.89 % after the switching frequency is reduced. Moreover, the capacitor current RMS is almost unchanged. The output current THD and capacitor current RMS variations according to the switching frequency reduction are summarized in Fig. 18.

Fig. 18 shows the output current THD and the capacitor current RMS variations according to the switching number reduction. As shown in Fig. 18, as the number of switching

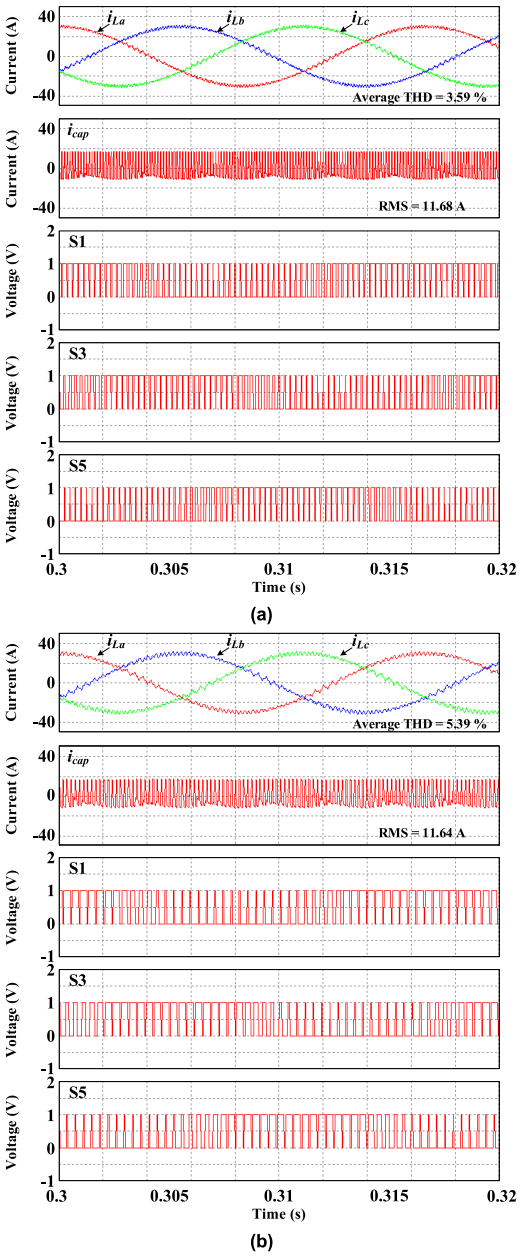


FIGURE 15. Simulation results of SVPWM-based variable switching frequency (a) full switching (b) 33 % reduction in the number of all phase switching.

increases, the output current THD of the conventional technique increases significantly. However, since the proposed technique only reduces the number of one-phase switching, the amount of THD increase is smaller than that of the existing technique even if the number of switching is reduced. On the other hand, the change in capacitor current RMS according to the switching frequency reduction is the same as the existing and proposed methods. Therefore, the proposed method has the advantage of improving the output current quality while having similar reliability to the existing method.

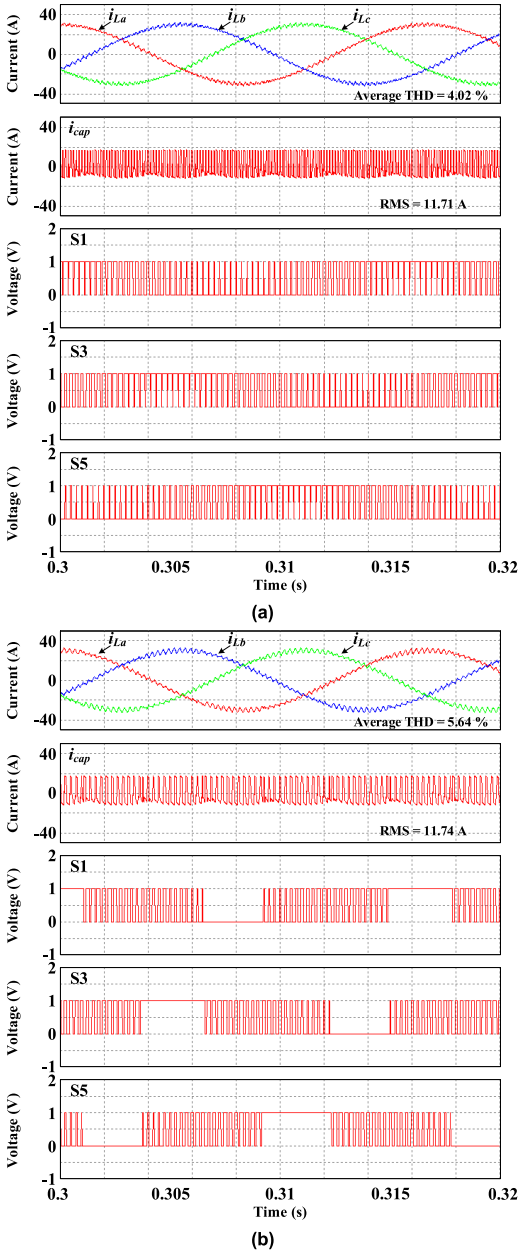


FIGURE 16. Simulation results of DPWM-based variable switching frequency technique (a) full switching (b) 33 % reduction in the number of all phase switching.

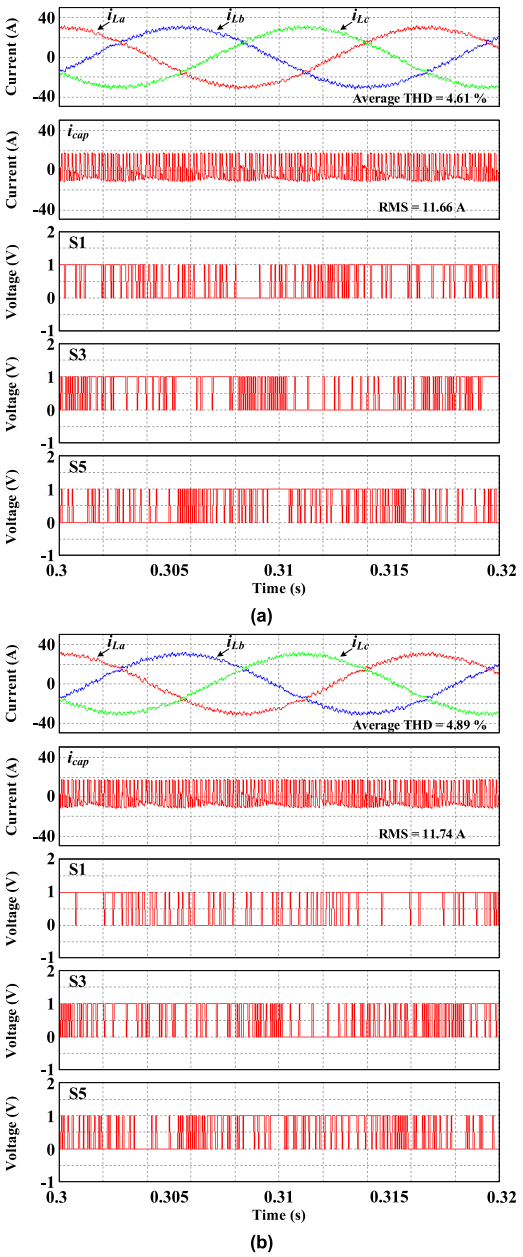


FIGURE 17. Simulation results of the proposed technique (a) full switching (b) 33 % reduction in the number of a-phase switching.

V. EXPERIMENT RESULTS

Experimental verifications for the proposed approach were carried out in this section. Fig. 19 represents a picture of the experimental setup.

The proposed technique was tested using a three-phase *R-L* load. Experimental conditions are the same as in TABLE 2. In addition, TMS320F28335 is used as the digital signal processor for the experimental verifications. Moreover, the switching device used is IXA37IF1200HJ. The gate driver used to drive the IXA37IF1200HJ is a SKHI22BR.

The experimental waveforms of the proposed technique when the i_{cap} RMS reduction technique is not applied (i.e., $k_{in} = 0$) are displayed in Fig. 20. The experimental results under the full switching condition are in Fig. 20(a). Also, Fig. 20(b) represents the experimental results when k_a is set to 0.2 and k_b and k_c are set to 0 in order to reduce the a-phase switching frequency by about half. Fig. 20 demonstrates that a-phase switching frequency is noticeably reduced when k_a is set to 0.2.

Fig. 21 represents the experimental waveforms of the proposed technique when the i_{cap} RMS reduction technique is applied (i.e., $k_{in} = 0.1$). Fig. 21(a) is the experimental results under the full switching condition. Moreover, Fig. 21(b) shows the experimental waveforms when k_a is set to 0.4 and k_b and k_c are set to 0 reducing the a-phase switching frequency by about half. The value of k_a required to reduce the

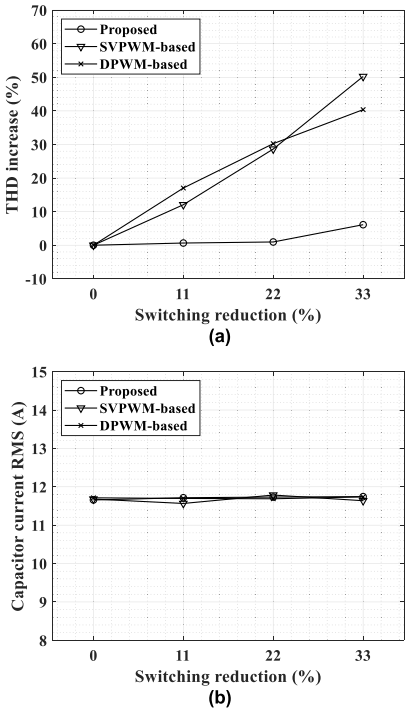


FIGURE 18. Output current THD and capacitor current RMS variations according to the switching number reduction (a) THD variation (b) capacitor current RMS.

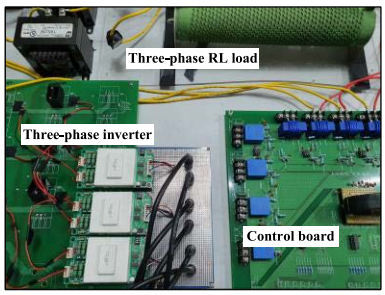


FIGURE 19. Picture of the experiment setup.

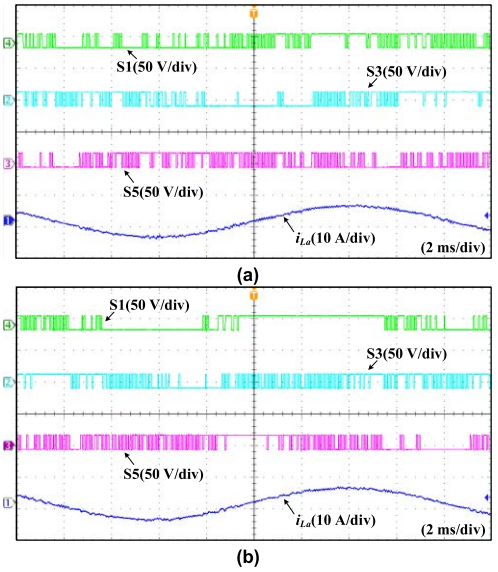


FIGURE 20. Experiment results of proposed method in $k_{in} = 0$ (a) full switching ($k_a = k_b = k_c = 0$) (b) half switching ($k_a = 0.2$, $k_b = k_c = 0$).

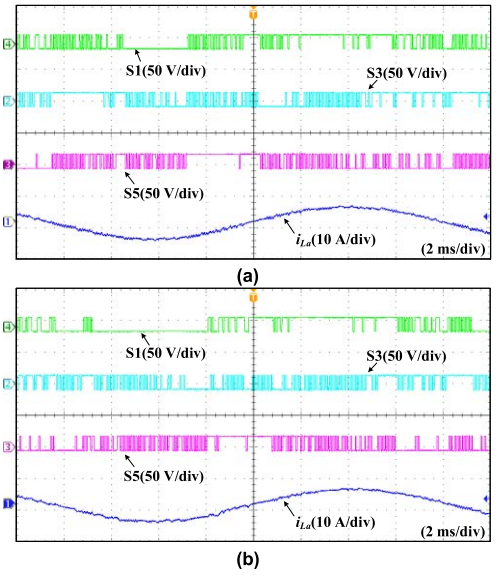


FIGURE 21. Experiment results of proposed method in $k_{in} = 0.1$ (a) full switching ($k_a = k_b = k_c = 0$) (b) half switching ($k_a = 0.4$, $k_b = k_c = 0$).

number of switching by half is different from Fig. 20, where the i_{cap} RMS reduction technique is not applied, because the cost function has changed due to the adding g_{in} to the cost function. As in Fig. 20, Fig. 21 confirms that the number of a-phase switching can be reduced using the k_a even if the i_{cap} RMS reduction technique is used.

Fig. 22 shows the number of switching of three-phase upper switches according to k_a obtained from the experiments. To measure the number of switching, the switching waveforms for 100 ms were acquired with an oscilloscope. Fig. 22(a) shows the results when the i_{cap} RMS reduction technique is not applied. Also, Fig. 22(b) represents the results when the i_{cap} RMS reduction technique is used. In each condition, both k_b and k_c were set to 0. Fig. 22 represents that the number of switching of a-phase decreases as k_a increases regardless of the application of the i_{cap} RMS reduction technique. In addition, the number of switching of b- and c-phase increased slightly. On the other hand, when the i_{cap} RMS reduction technique was applied, the reduction in the number of a-phase switching according to k_a was smaller than when the i_{cap} RMS reduction technique was not applied. Therefore, when k_{in} is 0.1, k_a must be set to 0.4 to reduce the number of a-phase switching by about half.

The experimental waveforms of the proposed approach including i_{cap} waveforms when the switching frequency is not reduced (i.e., $k_a = k_b = k_c = 0$) are in Fig. 23. Fig. 23(a) is before the application of the i_{cap} RMS reduction technique, and Fig. 23(b) is the experimental results after the application of the i_{cap} RMS reduction technique. The

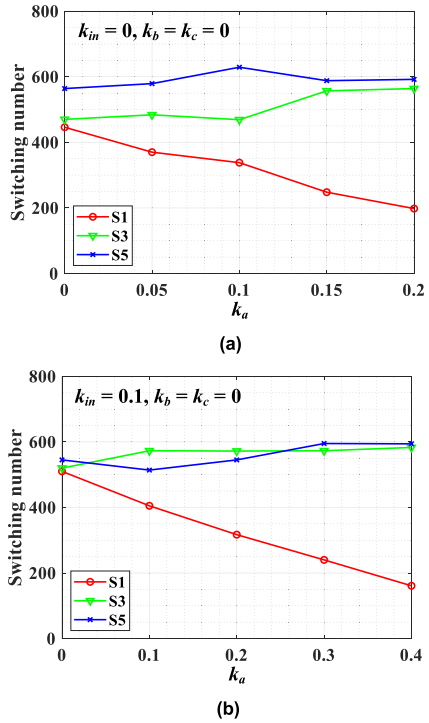


FIGURE 22. Switching numbers of the three-phase upper switches obtained by the experiment according to k_a (a) without capacitor current RMS reduction ($k_{in} = 0$) (b) with capacitor current RMS reduction ($k_{in} = 0.1$).

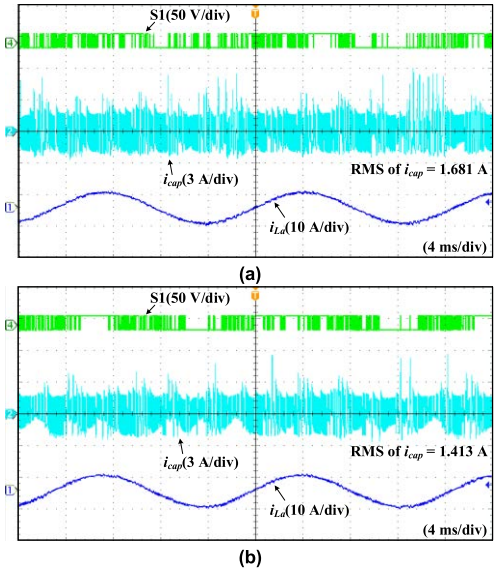


FIGURE 23. Experiment results of proposed method showing i_{cap} when full switching condition (a) without capacitor current RMS reduction ($k_{in} = 0$) (b) with capacitor current RMS reduction ($k_{in} = 0.1$).

comparison between Figs. 23(a) and (b) demonstrates that the ripple of i_{cap} is reduced when setting k_{in} to 0.1. Due to the reduction of ripple, the RMS of i_{cap} decreased from 1.681 A to 1.413 A.

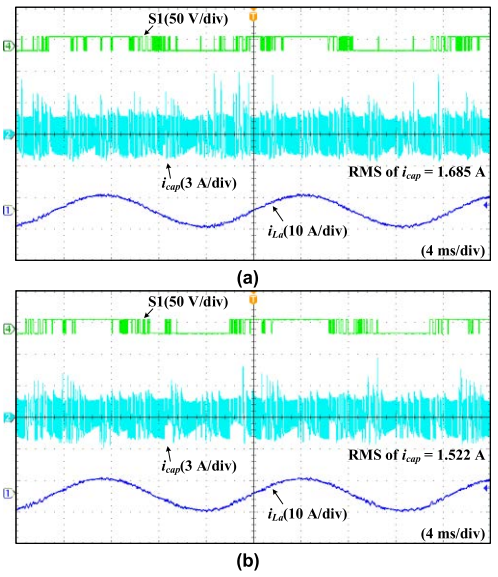


FIGURE 24. Experiment results of the proposed method showing i_{cap} when half switching condition (a) without capacitor current RMS reduction ($k_{in} = 0$) (b) with capacitor current RMS reduction ($k_{in} = 0.1$).

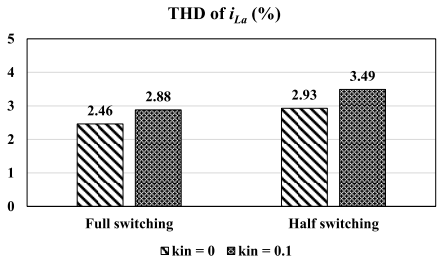


FIGURE 25. Total harmonic distortion of i_{La} obtained from experiment results.

The experimental results of the proposed technique including i_{cap} waveforms under the a-phase half switching condition are shown in Fig. 24. Fig. 24(a) is the results without the i_{cap} RMS mitigation technique, and Fig. 24(b) is the results including the i_{cap} RMS mitigation technique. To reduce the a-phase switching frequency, k_a used in Fig. 24(a) and (b) is 0.2 and 0.4, respectively. Also, k_b and k_c are both set to 0. Fig. 24 demonstrates that even when the number of switching is reduced by half, the i_{cap} ripple is reduced thanks to the application of the i_{cap} RMS reduction technique. After RMS reduction method, RMS of i_{cap} decreases from 1.685 A to 1.522 A. Figs. 23 and 24 show that the i_{cap} RMS reduction method effectively reduces the i_{cap} RMS regardless of the application of the switching frequency control technique.

Fig. 25 is a graph summarizing the total harmonic distortion (THD) of i_{La} obtained from the experimental results. Fig. 25 demonstrates that if the number of switching is halved using the proposed technique, the THD is slightly increased. Moreover, Fig. 25 indicates that the proposed technique can diminish the a-phase switching frequency while minimizing the deterioration of the quality of the load current because the THD increased by about 0.5% even though the number of

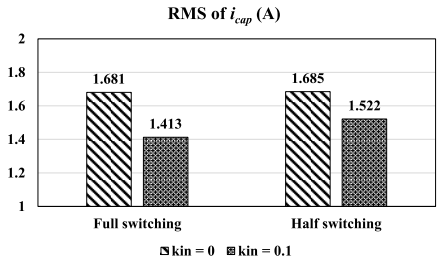


FIGURE 26. RMS of i_{cap} obtained from experiment results.

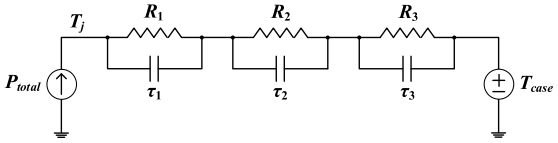


FIGURE 27. Description of FTM.

switching of a-phase was reduced by half under the condition of k_{in} is 0. Meanwhile, THD slightly rises even when i_{cap} RMS is decreased by setting k_{in} to 0.1. In addition, in the case of applying both one phase half switching and i_{cap} RMS reduction in the proposed technique, THD increased the most. THD is the largest in this condition because there are three control objectives (load current, phase switching frequency, and inverter input current) that should be considered to determine the optimal switching state.

Fig. 26 shows i_{cap} RMS according to the operating conditions of the proposed technique obtained from the experimental results. Fig. 26 shows that even if the number of switching is halved, i_{cap} RMS does not increase significantly. This is because the load angle used in the experiment is small. Meanwhile, i_{cap} RMS is effectively reduced in both full switching and a-phase half switching conditions when k_{in} is 0.1.

The experimental results reviewed above indicate that the number of switching of the most aged phase can be effectively reduced using the proposed technique. Also, the i_{cap} RMS reduction technique performed effectively regardless of whether the number of switching was reduced or not. The following section checks how effectively the proposed method reduces the T_j of the switch, and also examines the capacitor lifetime increased by the i_{cap} RMS reduction technique.

VI. JUNCTION TEMPERATURE AND CAPACITOR LIFETIME VARIATIONS BY PROPOSED METHOD

A. JUNCTION TEMPERATURE VARIATIONS BY THE PROPOSED METHOD

This subsection looks at T_j which is changed by the proposed technique. T_j can be calculated using the Foster thermal model (FTM) [5]. Fig. 27 shows the Foster thermal model.

As shown in Fig. 27, the input of the FTM is the total loss of the device to estimate T_j. P_{total} in Fig. 27 means total loss. R_1, R_2, R_3, τ_1, τ_2, and τ_3 are parameters of the FTM and can be calculated through the thermal impedance in the device's

TABLE 4. FTM parameters.

	R_1 (K/W)	R_2 (K/W)	R_3 (K/W)	τ_1 (s)	τ_2 (s)	τ_3 (s)
Transistor	0.3031	0.1333	0.2038	0.03550	0.08788	0.003656
Diode	0.2990	0.5827	0.3161	0.08948	0.02524	0.002302

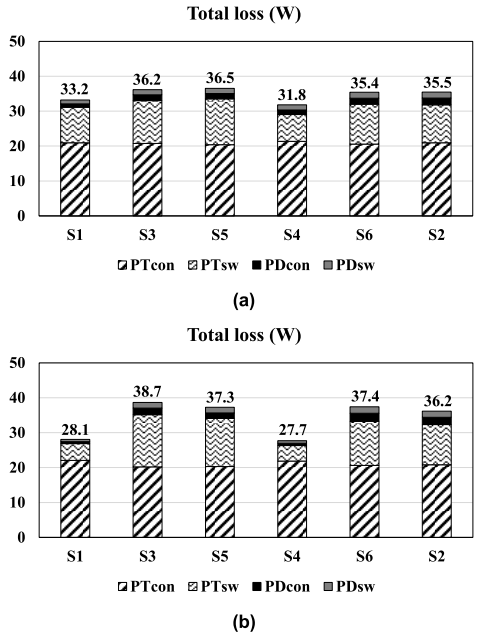


FIGURE 28. Total loss of switches obtained by the simulation (a) Full switching condition (b) half switching condition.

datasheet. The FTM parameters of the transistor and diode of the IXA37IF1200HJ used in this paper are in TABLE 4.

The total loss of each device was calculated through the simulation. Fig. 28 shows the calculated loss of switches when the three-phase VSI with an output power of 48 kW is driven with the proposed technique. Fig. 28(a) is the loss obtained from the full switching operation that does not reduce the number of switching of all phases, and Fig. 28(b) is the loss obtained when the a-phase switching frequency is reduced by half, assuming that a-phase is the most aged phase. In Fig. 28, PT_{con} and PT_{sw} mean the conduction and switching losses of the transistor, respectively. Also, PD_{con} and PD_{sw} refer to the conduction and switching losses of the diode.

Fig. 28 demonstrates that the switching losses of switches S1 and S4 in a-phase decreased by reducing the a-phase switching frequency by the proposed technique. Also, the conduction loss of S1 and S4 slightly increased with half switching condition. However, the total loss of S1 and S4 decreased because the switching loss reduction was large. Meanwhile, the total loss of the remaining phases increased slightly in half switching condition. This is because there is little change in conduction loss, but a slight increase in switching loss due to the rise in the number of switching. The fact that the number of switching of other phases increases

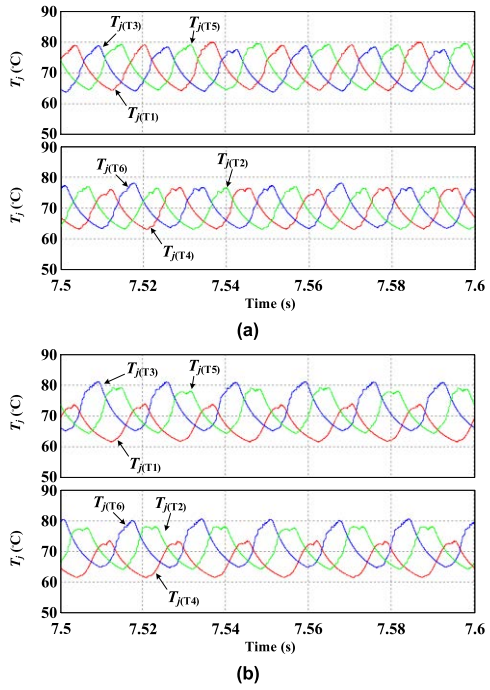


FIGURE 29. Transistor junction temperatures obtained by FTM (a) Full switching condition (b) half switching condition.

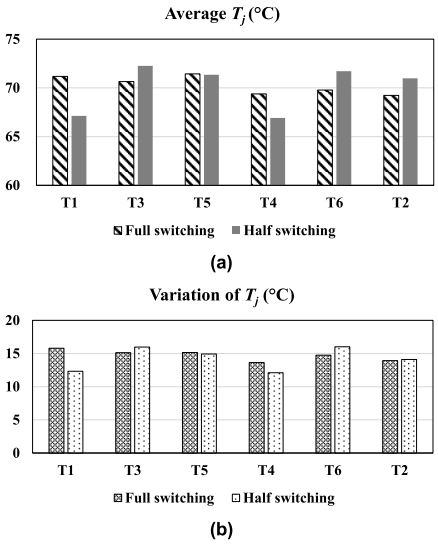


FIGURE 30. Average and variations of transistor junction temperatures in full and half switching conditions (a) average junction temperature (b) junction temperature variation.

when the a-phase switching frequency is reduced can also be confirmed from the experimental results in Fig. 22.

Fig. 28 (a) and (b) indicates that the total loss of the upper switch of a-phase, S1, was reduced by about 5.2 W due to halving the number of switching of a-phase. Also, the total loss of the lower switch of a-phase, S4, was reduced by about 4.1 W after half switching. The rest of the switches increased from 0.7 W to 2.5 W. Since the decrease in the total loss of a-phase considered the most aged phase is greater than the increase in the loss of the remaining phases, the proposed method can extend the overall life of the inverter.

T_j was calculated using the FTM parameters in TABLE 4 and the total loss of switches in Fig. 28. Fig. 29 shows the simulation results of T_j of the transistor obtained using the FTM. The simulation results in Fig. 29 were obtained under the operating conditions shown in Fig. 28 where the total loss was calculated.

Fig. 29 shows the T_j obtained using the FTM when the three-phase VSI is driven using the proposed technique. T_{case} was assumed to be 50 °C. In Fig. 29, $T_{j(T1)}$, $T_{j(T2)}$, $T_{j(T3)}$, $T_{j(T4)}$, $T_{j(T5)}$, and $T_{j(T6)}$ are the transistor junction temperatures of S1, S2, S3, S4, S5, and S6, respectively. Fig. 29(a) is the results under the full switching condition in which the number of switching of all phases is not reduced, and Fig. 29(b) is the results when the number of switching of a-phase is reduced by about half. Fig. 29(a) represents that the T_j of the transistors of all phases is almost balanced in the full switching condition. Meanwhile, in Fig. 29(b), the average and fluctuation of T_j of the transistors of S1 and S4 decreased. Also, the average and fluctuation of T_j of the remaining switches increased slightly.

Fig. 30 is the results of graphing the T_j change in Fig. 29. In Fig. 30, T1, T2, T3, T4, T5, and T6 represent the transistors of S1, S2, S3, S4, S5, and S6, respectively. Fig. 30(a) shows the average change in T_j for each switch, and Fig. 30(b) shows the variation change in T_j for each switch. Fig. 30(a) indicates that the average T_j of the a-phase transistor decreased under the a-phase half switching condition. T1 and T4 decreased by about 4.1 °C, and 2.5 °C, respectively. On the other hand, the rest of the transistors except T5 rose by about 1.6 to 1.9 °C. This is because as the switching loss of a-phase decreases, the switching loss of the remaining phases increases.

Even in the amount of fluctuation in Fig. 30(b), T_j fluctuation in a-phase decreased in half switching condition. In the case of T1, the T_j variation decreased by 3.5 °C and in the case of T4 by 1.5 °C. The remaining transistors except T5 increased by 0.2 to 1.3 °C due to an increase in switching loss.

Fig. 31 shows the diode T_j obtained using the FTM when the inverter is driven by the proposed technique. Fig. 31(a) is the results of the full switching condition, and Fig. 31(b) is the results of the half switching condition, reducing the a-phase switching frequency by half. Similar to the trend of T_j of the transistor, the average value and variation of T_j of the a-phase diodes decreases. Also, for the diodes of the phases without reducing switching, the average and fluctuation of T_j increase due to a rise in the total loss.

Fig. 32 is the results of graphing the diode T_j change in Fig. 31. In Fig. 32, D1, D2, D3, D4, D5, and D6 represent the diodes of S1, S2, S3, S4, S5, and S6, respectively. Fig. 32(a) shows the average change in T_j for each switch diode, and Fig. 32(b) shows the variation change in T_j for each switch

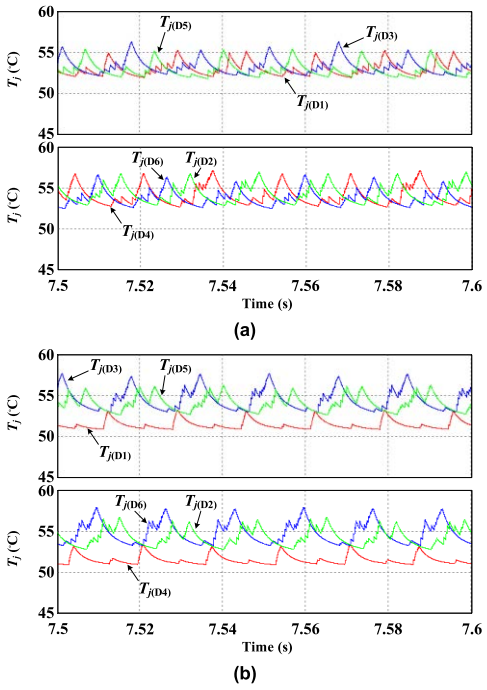


FIGURE 31. Diode junction temperatures obtained by FTM (a) Full switching condition (b) half switching condition.

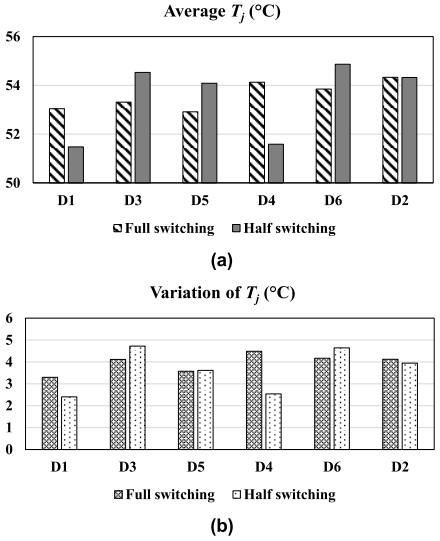


FIGURE 32. Average and variations of diode junction temperatures in full and half switching conditions (a) average junction temperature (b) junction temperature variation.

diode. Fig. 32(a) indicates that the average diode T_j of D1 and D4 was reduced by 1.6 and 2.5 °C, respectively, by the half switching operation of the proposed technique. In addition, the T_j variation of the diodes in *b*- and *c*-phase except D2 rose by about 1 to 1.2 °C. The average T_j of D2 was almost the same as the full switching condition.

Meanwhile, Fig. 32(b) shows that the variation of T_j of the *a*-phase diode is also reduced by the half switching operation

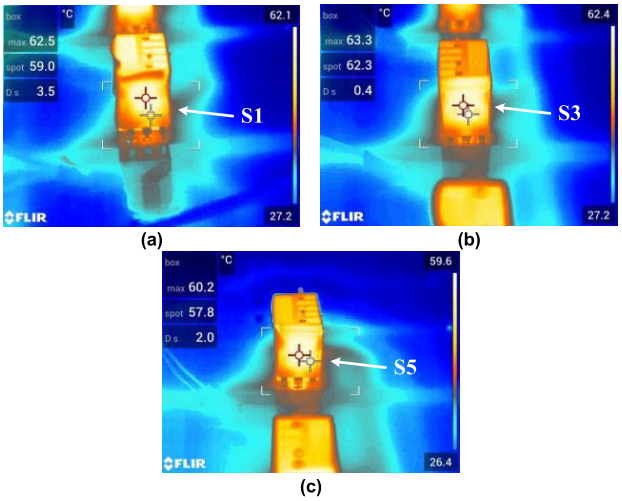


FIGURE 33. Case temperature of upper switches in the full switching condition (a) S1 (b) S3 (c) S5.

of the proposed technique. For D1, it decreased by about 0.9 °C, and in the case of D4 by about 1.9 °C. For the rest of the diodes except D2, it increased from about 0 to 0.6 °C. The T_j variation of D2 was slightly reduced by about 0.2 °C.

Figs 29 to 32 demonstrate that the average and variation of T_j of the *a*-phase transistors and diodes decreased when the *a*-phase switching frequency was reduced through the proposed method. Meanwhile, the average value and variation of T_j of the *b*-and *c*-phase transistors and diodes rose. Based on these results, the proposed technique can reduce the aging rate of the most aged phase and slightly increase the aging rate of the remaining phases, thereby extending the overall lifespan of the inverter.

To experimentally verify the proposed inverter lifetime extension method, the T_{case} of the switches was checked with an IR camera.

Fig. 33 shows the T_{case} measurement results when the proposed technique operates without reducing the number of switching of all phases. T_{case} measurement results only show the results of upper switches. T_{case} measurement results of lower switches are in Fig. 35. Fig. 33 represents that since the switching frequency of all phases is not reduced, there is no significant difference in the T_{case} of S1, S3, and S5.

Fig. 34 shows the T_{case} measurement results applying the half switching operation of the proposed method. Fig. 34 indicates that the T_{case} of S1 is noticeably lower than that of S3 and S5 because the number of switching operations of *a*-phase is halved.

Fig. 35 is the results of comparing the T_{case} of Figs. 33 and 34. Fig. 35 demonstrates that the T_{case} of the *a*-phase was reduced by about 7 °C due to the *a*-phase half-switching operation. In addition, T_{case} in the remaining phases increased to about 1 °C.

Through the change in T_j obtained from the FTM and T_{case} measured by the IR camera experimentally, it can be confirmed that the proposed method can effectively lower the

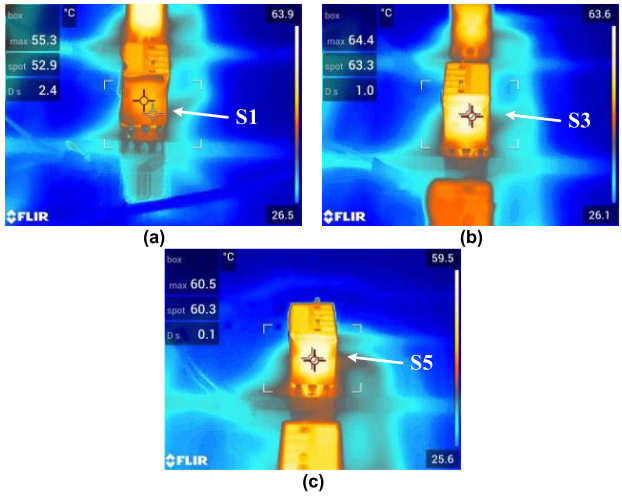


FIGURE 34. Case temperature of upper switches in the half switching condition (a) S1 (b) S3 (c) S5.

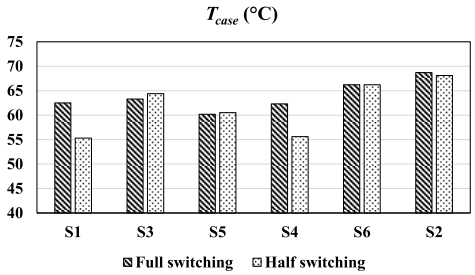


FIGURE 35. Case temperature comparisons of full switching and half switching conditions.

T_j and T_{case} of the most aged phase. These results suggest that the proposed technique can effectively extend the lifespan of the most aged phases.

B. LIFETIME EXTENSION ANALYSIS USING CIPS 08 MODEL

Switching device reliability is determined by various parameters, including junction temperature. The proposed technique reduces the loss by reducing the number of switching of the power device. The reduced loss suppresses the rise of the junction temperature, thereby increasing the lifetime of the power device. The lifetime of the power device is expressed as (16), which is the CIPS 08 model [24].

$$N_f = A\Delta T_j^{\beta_1} e^{\frac{\beta_2}{T_{jmin}+273}} t_{on}^{\beta_3} i_B^{\beta_4} V_C^{\beta_5} d_b^{\beta_6}. \tag{16}$$

In (16), N_f means the number of cycles at which the switch fails. Also, t_{on}, i_B, V_c, and d_b mean heating time, current per bond wire, voltage rating, and bond wire diameter, respectively. In addition, ΔT_j and T_{jmin} denote the junction temperature fluctuation and the minimum junction temperature, respectively. The remaining parameters are summarized in TABLE 5.

In order to investigate the increase in the lifetime of the a-phase switch according to the decrease in the number of switching, the change in the junction temperature was examined by periodically changing the output power. The output power was changed from 48 kW to 3 kW at a frequency of 0.3 Hz.

TABLE 5. Parameters in CIPS 08 model (16).

Parameter	Value
A	$9.3 * 10^{14}$
β_1	-4.416
β_2	1285
β_3	-0.463
β_4	-0.716
β_5	-0.761
β_6	-0.5

Equation (16) can be divided into terms related to the junction temperature and terms unrelated to the junction temperature. Equation (17) represents terms related to the junction temperature, and Equation (18) represents terms unrelated to the junction temperature.

$$D_T = \Delta T_j^{\beta_1} e^{\frac{\beta_2}{T_{jmin}+273}}. \tag{17}$$

$$ID_T = A t_{on}^{\beta_3} i_B^{\beta_4} V_C^{\beta_5} d_b^{\beta_6}. \tag{18}$$

The ID_T is determined by the type of the switching device. However, the D_T depends on the junction temperature. Therefore, by calculating the D_T, the variation in the lifetime of the switching device can be obtained.

Fig. 36 shows the junction temperature of T1 and T4 according to the output power change. The junction temperature in Fig. 36 is calculated using the switching device loss and Foster thermal model described in this paper. T1 and T4 in Fig. 36 refer to the transistors of S1 and S4, respectively. Fig. 36(a) is the result of not reducing the switching, and Fig. 36(b) is the result under the condition that the number of a-phase switching is reduced by about half. By comparing Figs. 36(a) and 36(b), it can be confirmed that the fluctuation in the transistor junction temperature of S1 and S4 can be reduced by diminishing the number of a-phase switching.

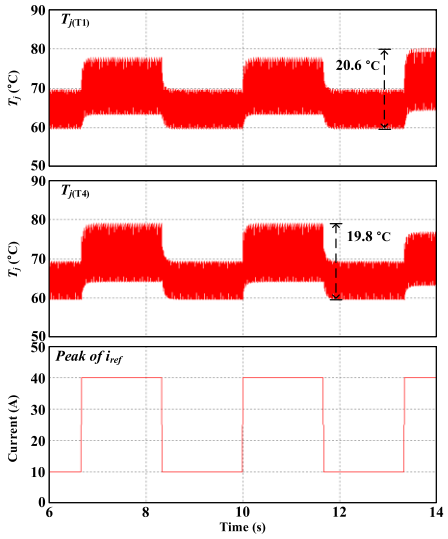
Fig. 37 shows the amount of life extension of T1 and T4 according to the a-phase switching frequency reduction. Fig. 37 indicates that the lifetime of T1 and T4 increases as the a-phase switching frequency reduction increases. Figs. 36 and 37 show that the proposed technique can reduce the fluctuation of the junction temperature of the transistor, thereby extending the lifetime of the transistor.

C. CAPACITOR LIFETIME VARIATIONS BY THE PROPOSED METHOD

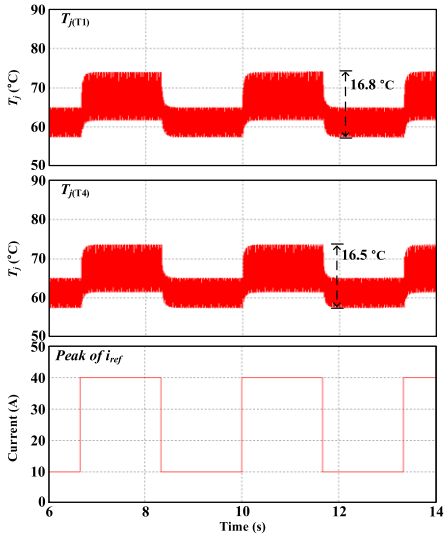
The lifetime of a capacitor is generally determined by three parameters as follows (19) [25], [26].

$$L = L_o k_t k_r k_v. \tag{19}$$

In (19), L is the capacitor lifetime, and L_o is the capacitor lifetime in the rated condition. Also, k_t, k_r, and k_v mean the temperature, ripple, and voltage factors that affect the



(a)



(b)

FIGURE 36. Junction temperature of T1 and T4 according to output power change (a) full switching (b) half switching.

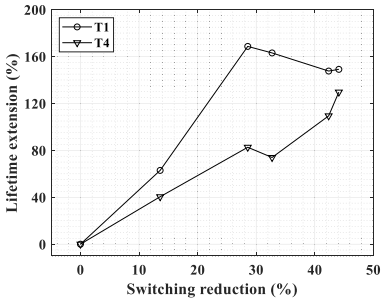


FIGURE 37. The amount of life extension of T1 and T4 according to the a-phase switching frequency reduction.

capacitor lifespan, respectively. Since the proposed method decreases i_{cap} RMS, only k_r is examined. k_r can be expressed as the following (20) [26].

$$k_r = 2^{(1-(i_{capn}/i_{capr})^2)}. \tag{20}$$

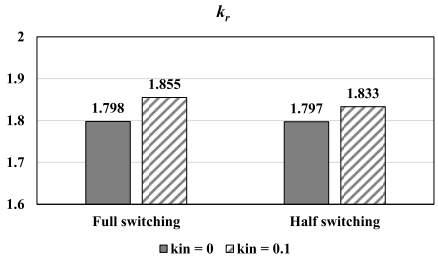


FIGURE 38. Capacitor ripple factors obtained from experimental results.

TABLE 6. Ripple coefficients of DC-link capacitor.

50 Hz	120 Hz	300 Hz	1 kHz	10 kHz	100 kHz
0.77	1.00	1.16	1.30	1.41	1.43

In (20), i_{capr} is the rated RMS of the capacitor current. Also, i_{capn} is the actual RMS of the capacitor current normalized by the ripple coefficient. Since the characteristics of capacitors vary according to the frequency, the measured i_{cap} RMS should be normalized with the ripple coefficient for calculating k_r. TABLE 6 shows the ripple coefficient of the capacitor used in the experiment of this paper.

Since the three-phase inverter in this paper is controlled with a sampling frequency of 20 kHz, 1.41 is used as the ripple coefficient. Fig. 38 shows k_r obtained using i_{cap} RMS of Fig. 26 and (20).

The calculated k_r is greater than 1 because the RMS of the capacitor current obtained in the experiment is smaller than the rated value. Note that the rated current RMS of the capacitor used is 3.04 A. In the case of full switching condition, k_r increased by about 3.2% after using the i_{cap} RMS reduction technique. Also, in the case of the half switching condition, k_r increased by about 2.0% after using the i_{cap} RMS reduction technique. Therefore, when the other factors such as k_t and k_v are the same, the lifespan of the capacitor can be increased by 2 to 3.2 % by the proposed method. If k_{in} is further increased, the RMS of the i_{cap} can be further reduced and the lifespan of the capacitor can be further increased. However, in this case, the THD of the load current becomes even worse, so the designer must carefully consider which performance should be prioritized.

VII. CONCLUSION

In this paper, the per-phase switching frequency control technique was proposed. For this purpose, MPC was used, which is easy to add control purposes. The cost function for the MPC was constructed by combining the term for current control and the term for controlling the switching frequency. In addition, in order to prevent accelerated aging of the DC-link capacitor, which is the weakest element along with the power devices in the power converter, a term for reducing the capacitor current RMS, which can be selectively used, is added to the cost function. The proposed technique reduces the number of switching times of the most aged phase,

thereby reducing the T_j of that phase. The ability to control the switching frequency and the T_j of the proposed technique was confirmed through simulations and experiments. Moreover, the capacitor current RMS reduction capability of the proposed technique was also verified through simulations and experiments.

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