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Impacts of SiC-MOSFET Gate Oxide Degradation on Three-Phase Voltage and Current Source Inverters

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Abstract: In this paper, the performance variations of SiC MOSFET-based voltage and current source inverters under gate oxide degradation are studied. It is confirmed that the turn-on and turn-off delays of SiC MOSFETs change significantly by high electric field stress, which accelerates the gate oxide degradation. Variations in the turn-on and turn-off delays of switching devices extend or reduce the duty error of voltage source inverters and current source inverters. The performance variations of the voltage and current source inverter due to the duty error changes caused by the gate oxide degradation are analyzed through simulations. As a result, the gate oxide degradation worsens the performance of the voltage source inverter. Furthermore, the negative gate oxide degradation, which lowers the threshold voltage, decreases the performance of the current source inverter.

Keywords: turn-on delay; turn-off delay; gate oxide degradation; silicon carbide MOSFET; high electric field stress; voltage source inverter; current source inverter

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1. Introduction

Along with gallium nitride (GaN) field effect transistor (FET), silicon carbide (SiC) metal-oxide-semiconductor field (MOSFET), a wide bandgap (WBG) device, is attracting attention as a next-generation power switching device due to its high efficiency and power density [1,2]. In particular, SiC MOSFET is increasingly used in systems close to human life, such as electric vehicles [3]. As a result, the reliability of SiC MOSFET is becoming more important.

A gate oxide degradation is a major aging phenomenon that affects the reliability of SiC MOSFET along with a package degradation [4]. The package degradation is caused by thermomechanical stress caused by temperature change [5]. If the package degradation continues, phenomena, such as bond wire crack and lift-off, occur, leading to a switching device failure [6,7]. Meanwhile, SiC MOSFET has a thin gate oxide layer, so electrons can be injected into the oxide layer by the Fowler–Nordheim tunneling current. Moreover, there are more interface trapped charges on the SiC/SiO_2 interface than Si MOSFET [8,9]. In particular, the interface trapped charge reduces the effective channel-carrier mobility and changes the threshold voltage (V_{th}). The reduced effective channel-carrier mobility eventually increases the on-resistance (R_{on}) of the switch. The shift direction of the V_{th} is determined by the sum of the oxide trapped charge and the interface trapped charge. These charges are changed more significantly by the gate oxide degradation. An increase in V_{th} causes an increase in conduction losses. Moreover, a decrease in V_{th} increases the risk of the switch being turned on undesirably [10,11]. If the gate oxide degradation continues, the gate insulation is eventually destroyed, and the control ability of the gate to switch is lost [12].

The gate oxide degradation is accelerated under high electric field (HEF) stress or high-temperature stress [13]. HEF stress is divided into positive HEF (PHEF) stress applying a positive voltage to the gate, and negative HEF (NHEF) stress using a negative

voltage. Characteristic changes during the gate oxide degradation of SiC MOSFETs have been studied through muchresearch [8,10,13–17], and Table 1 summarizes the previous research about the characteristics of SiC MOSFETs under gate oxide degradation. In Table 1, characteristics covered by the study were marked with an O, and properties not investigated by the analysis were marked with an X. Furthermore, the characteristics measured when the switching state is fixed are defined as stationary properties, and the properties measured when the switching state changes are defined as transient properties. The stationary properties are V_{th}, R_{on}, gate–drain capacitance (C_{gd}), gate–source capacitance (C_{gs}), and body diode forward voltage (V_{sd}). Moreover, the transient properties are Miller plateau voltage (V_m), Miller plateau time (T_m), gate charge time (T_{gc}), turn-on delay (T_{don}), and turn-off delay (T_{doff}).

Table 1. Summary of previous research about characteristics of SIC MOSFETs under gate oxide degradation.

Reference	Types of HEF		Stationary Properties				Transient Properties				
	PHEF	NHEF	V_{th}	R_{on}	C_{gs}, C_{gd}	V_{sd}	V_m	T_m	T_{gc}	T_{don}	T_{doff}
[8]	O	O	O	O	O	X	X	X	X	X	X
[10]	O	O	O	X	X	O	X	X	X	X	X
[13]	O	X	O	X	X	X	O	X	X	O	X
[14]	O	O	O	X	X	X	X	X	X	X	X
[15]	O	O	O	X	X	X	X	X	X	X	X
[16]	O	O	O	X	X	X	X	X	O	X	X
[17]	O	X	O	X	X	X	O	O	X	X	X

As shown in Table 1, previous studies dealt with the SiC MOSFET's stationary properties under gate oxide degradation. However, research about transient characteristics of SiC MOSFET has not been conducted much. Especially, except for T_{don} in [13], no studies on T_{don} and T_{doff} under gate oxide degradation were conducted in previous studies. T_{don} and T_{doff} can impact the performance of voltage and current source converters. The voltage source converter has a dead time to prevent a short circuit accident when one leg's switches are turned on simultaneously [18]. The dead time causes a duty error in the voltage vector. In addition to the dead time, T_{don} and T_{doff} introduce duty errors. These duty errors change the output quality of the voltage source converter. Furthermore, an overlap time is required in the current source converter to prevent an overvoltage of the DC link inductor from occurring when all upper or lower switches are turned off simultaneously [19]. Like the voltage source converter, the overlap time, T_{don}, and T_{doff} generate the duty errors in the current vector, resulting in changes in the output quality of the current source converter. Therefore, studies on changes in T_{don} and T_{doff} under gate oxide degradation are necessary.

In this paper, the changes of T_{don} and T_{doff} of SiC MOSFET in the gate oxide degradation are examined. In addition, the effects of T_{don} and T_{doff} variations caused by the gate oxide degradation on the performance of voltage and current source inverters are studied.

The structure of this paper is as follows. Section 1 is the introduction. Section 2 analyzes the effects of V_{th} on R_{on}, T_{don}, and T_{doff}. Section 3 describes HEF stress to accelerate the gate oxide degradation. Section 4 compares V_{th} and R_{on} changes of SiC MOSFET under HEF stress with those of Si-based devices. Section 5 compares the changes in T_{don} and T_{doff} of SiC MOSFET under HEF stress with those of Si-based devices. In Section 6, the performance variations of voltage and current source inverters according to the duty error changes due to the gate oxide degradation are examined by the simulation. Section 7 is the conclusion.

2. Effects of Threshold Voltage Variation on On-Resistance, Turn-On Delay and Turn-Off Delay

2.1. Gate Oxide Degradation

Gate oxide degradation is aging occurring in the gate oxide layer. Furthermore, it is one of the major degradations of MOSFETs, like package degradation. As the gate oxide degradation progresses, there is a change in V_{th}, and this change can be explained by the oxide trapped charge and the interface trapped charge in the gate oxide layer. Figure 1 is a structure of the MOSFET and the gate oxide layer.

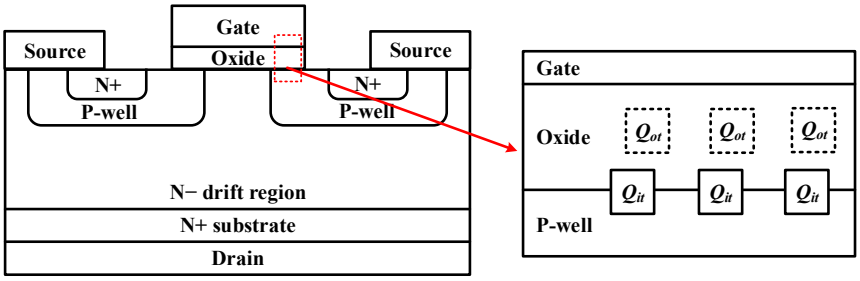


Figure 1. Structure of the MOSFET and the gate oxide layer.

In Figure 1, Q_{ot} denotes the oxide trapped charge, and Q_{it} means the interface trapped charge. By the gate oxide degradation, Q_{ot} is generated inside the oxide layer, and Q_{it} is generated on the surface of the oxide layer. V_{th} can be expressed as (1) using Q_{ot} and Q_{it} [20]:

$$V_{th} = V_{th0} + \frac{Q_{it} - Q_{ot}}{C_{ox}}, Q_{it} = qN_{it},\ Q_{ot} = qN_{ot} \tag{1}$$

In (1), V_{th0} means V_{th} in a fresh condition where the gate oxide degradation does not proceed. C_{ox} represents the gate oxide capacitance per unit area. Furthermore, q stands for the electric charge. Moreover, N_{it} and N_{ot} mean the interface trap density and the oxide trap density, respectively. When the gate oxide degradation proceeds, Q_{it} and Q_{ot} are generated. V_{th} increases or decreases depending on which charge is more generated relatively. As seen from (1), when Q_{it} occurs relatively significantly, V_{th} rises. On the other hand, when Q_{ot} is relatively large, V_{th} decreases. The gate oxide degradation is accelerated by HEF stress. In general, in PHEF stress where a positive voltage is applied to the gate voltage, Q_{it} is generated significantly to increase V_{th}. Meanwhile, in NHEF stress where a negative voltage is applied to the gate voltage, Q_{ot} is generated relatively significantly, and V_{th} decreases.

2.2. On-Resistance Variation Caused by Threshold Voltage

R_{on} can be subdivided into several types of resistances as follows (2) [8]:

$$R_{on} = R_{ch} + R_A + R_{JFET} + R_D + R_{sub} \tag{2}$$

In (2), R_{ch} is the channel resistance, R_A is the accumulation resistance, R_{JFET} is the JFET region resistance, R_d is the drift region resistance, and R_{sub} is the substrate resistance. In the case of SiC MOSFETs, among the five resistance types, R_{ch} is the most dominant [8]. R_{ch} can be expressed as (3) [8]:

$$R_{ch} \approx \frac{L_{ch}}{W_{ch}\mu C_{ox} V_{over}},\ V_{over} = V_{gs} - V_{th} \tag{3}$$

In (3), L_{ch} means the channel length, and W_{ch} represents the channel width. In addition, μ and V_{over} represent the channel mobility and the overdrive voltage, respectively. V_{over} is expressed as the difference between the gate–source voltage (V_{gs}) and V_{th}. As seen from (3), the variation of V_{over} changes R_{ch}. Therefore, when V_{th} changes, R_{ch} also changes. When

V_{th} increases, V_{over} decreases, and R_{ch} increases. When V_{th} decreases, V_{over} increases, and R_{ch} decreases. As a result, R_{on} increases when V_{th} increases, and R_{on} decreases when V_{th} decreases.

2.3. Turn-On Delay Variation Caused by Threshhold Voltage

A definition of T_{don} is the time from when V_{gs} starts to rise to when the drain–source current (I_{ds}) starts to increase [21]. V_{th} is related to T_{don} because V_{th} is the voltage at which I_{ds} starts flowing through the switch. Figure 2 shows V_{gs} and I_{ds} waveforms when the switch is turned on.

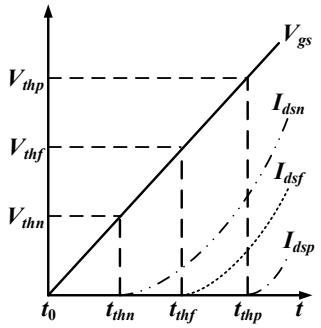


Figure 2. Waveforms of V_{gs} and I_{ds} in a turn-on state.

In Figure 2, t_0 means the time when V_{gs} starts to increase to turn on the switch. In addition, t_{thf} indicates the time when I_{ds} in the fresh condition begin to rise. t_{thn} and t_{thp} denote a time at which I_{ds} start to grow when V_{th} is negatively shifted and positively shifted, respectively. V_{th} and I_{ds} in the fresh condition are expressed as V_{thf} and I_{dsf}, respectively. Furthermore, V_{th} and I_{ds} in the negative V_{th} shift are described as V_{thn} and I_{dsn}, respectively. Moreover, V_{th} and I_{ds} in the positive V_{th} shift are denoted as V_{thp} and I_{dsp}, respectively. As shown in Figure 2, I_{ds} starts to flow when V_{gs} becomes greater than V_{th}. T_{don} of the fresh state, the negative V_{th} shift, and the positive V_{th} shift can be expressed by (4), respectively:

$$T_{donf} = t_{thf} - t_o, T_{donn} = t_{thn} - t_o, T_{donp} = t_{thp} - t_o \tag{4}$$

T_{donf}, T_{donn}, and T_{donp} in (4) mean T_{don} in fresh condition, negative V_{th} shift, and positive V_{th} shift, respectively. As shown in Figure 2, comparisons of T_{donf}, T_{donn}, and T_{donp} are expressed as (5). Therefore, as V_{th} increases, T_{don} increases:

$$T_{donn} < T_{donf} < T_{donp} \tag{5}$$

2.4. Turn-Off Delay Caused by Threshold Voltage

A definition of T_{doff} is the time from when V_{gs} starts to decrease to when the drain–source voltage (V_{ds}) begins to grow [22]. The point at which V_{ds} increases in the off transition is when V_{gs} enters V_m [22]. Therefore, the change in T_{doff} can be explained by V_m. The relationship between V_m and V_{th} can be expressed by (6) [20]:

$$V_m = V_{th} + \sqrt{\frac{I_{ds}L_{ch}}{\mu C_{ox}W_{ch}}} \tag{6}$$

Partial differentiation of (6) with respect to N_{ot} and N_{it} gives the following (7) [20]:

$$\frac{\partial V_m}{\partial N_{it}} = \frac{\partial V_{th}}{\partial N_{it}} - \frac{\mu^{-1.5}}{2}\sqrt{\frac{I_{ds}L_{ch}}{C_{ox}W_{ch}}}\frac{\partial \mu}{\partial N_{it}} \approx \frac{\partial V_{th}}{\partial N_{it}} > 0, \tag{7}$$

$$\frac{\partial V_m}{\partial N_{ot}} = \frac{\partial V_{th}}{\partial N_{ot}} - \frac{\mu^{-1.5}}{2}\sqrt{\frac{I_{ds}L_{ch}}{C_{ox}W_{ch}}}\frac{\partial \mu}{\partial N_{ot}} \approx \frac{\partial V_{th}}{\partial N_{ot}} < 0.$$

From (7), it can be seen that an increase in V_{th} increases V_m and vice versa. Figure 3 shows the relationship between the change in V_m and T_{doff}.

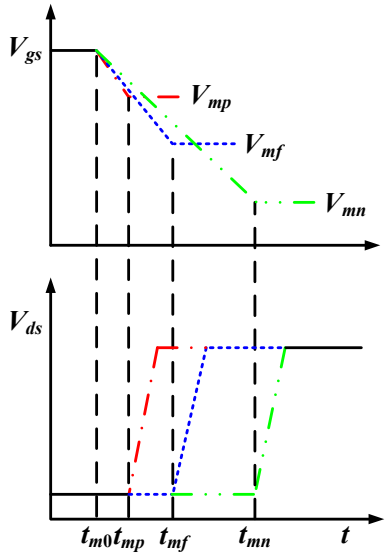


Figure 3. Turn-off waveform of V_{gs} and V_{ds} according to a variation of V_m.

In Figure 3, V_{mp}, V_{mf}, and V_{mn} mean V_m in positive V_{th} shift, fresh state, and negative V_{th} shift, respectively. In addition, t_{mp}, t_{mf}, and t_{mn} indicate a time when V_{ds} increases in positive V_{th} shift, fresh state, and negative V_{th} shift, respectively. t_{m0} is the point at which V_{gs} begins to decrease to turn off the switch. Figure 3 indicates that the time at which V_{ds} increases is faster as V_m increases. Therefore, as V_m increases, T_{doff} decreases and vice versa. T_{doff} can be expressed as (8):

$$T_{doffp} = t_{mf} - t_{m0},\ T_{doffp} = t_{mp} - t_{m0}, T_{doffn} = t_{mn} - t_{m0} \tag{8}$$

In (8), T_{doffp}, T_{doffp}, and T_{doffn} denote T_{doff} in a positive V_{th} shift, fresh state, and negative V_{th} shift, respectively. The magnitudes of T_{doffp}, T_{doffp}, and T_{doffn} can be expressed as (9):

$$T_{doffp} < T_{doffp} < T_{doffn} \tag{9}$$

3. High Electric Field Stress

As shown in Figure 4, The HEF stress circuit was constructed to accelerate the gate oxide degradation. The fabricated circuit was configured to apply HEF stress to five devices simultaneously. The drain and source or collector and emitter of the switching device were shorted to be connected to the ground. A resistor of 200 Ω was inserted to alleviate the overshoot of the gate current when HEF stress was applied to the gate side [8]. HEF stress was applied for 3600 s at room temperature, and the switching devices were disconnected from the HEF stress circuit every 900 s to measure V_{th}, R_{on}, T_{don}, and T_{doff} of the switching devices. The gate bias value used for HEF stress should be the proper value for accelerating the gate oxide degradation and preventing the gate insulation destruction. For this, 50 V was used as the gate bias value in PHEF. In the case of NHEF, the gate bias value was set to −38 V. In this paper, characteristics, such as V_{th}, R_{on}, T_{don}, and T_{doff}, were compared by applying HEF stress under the same conditions to various Si-based devices as well as SiC MOSFET. The reason for this comparison is to confirm that SiC MOSFET is more susceptible to the gate oxide degradation compared to other Si-based devices. The Si-based devices

used for comparison are Si IGBT, Si MOSFET, and Si IGBT with SiC diode. Information on the switching devices used for characteristic comparison is given in Table 2.

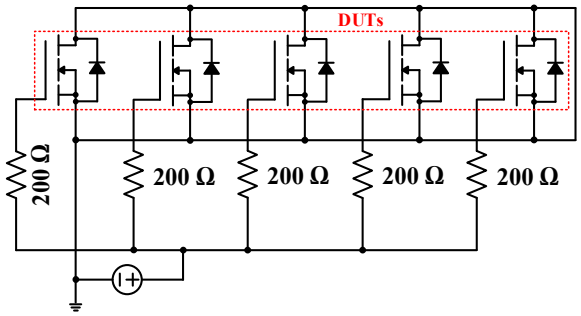


Figure 4. HEF stress circuit.

Table 2. Datasheet values of switching devices used in this paper.

	Si IGBT		Si MOSFET		Si IGBT (Hybrid)		SiC MOSFET	
	Values	**Conditions**	**Values**	**Conditions**	**Values**	**Conditions**	**Values**	**Conditions**
Part number	RGT60TS65DGC11		NTHL110N65S3F		IXGH30N60C3C1		SCT3080AL	
Voltage	650 V		650 V		600 V		650 V	
Current	30 A	T_c = 100 °C	19.5 A	T_c = 100 °C	30 A	T_c = 110 °C	21 A	T_c = 100 °C
V_{th}	6 V	V_{ce} = 5 V I_{ce} = 21 mA	3~5 V	$V_{gs} = V_{ds}$ I_{ds} = 0.74 mA	3~5.5 V	$V_{ge} = V_{ce}$ I_{ce} = 0.25 mA	2.7~5.6 V	V_{ds} = 10 V I_{ds} = 5 mA
R_{on}	55 mΩ	V_{ge} = 15 V, I_{ce} = 30 A	98 mΩ	V_{gs} = 10 V, I_{ds} = 15 A	130 mΩ	V_{ge} = 15 V, I_{ce} = 20 A	80 mΩ	V_{gs} = 18 V, I_{ds} = 10 A, T_c = 25 °C
T_{don}	29 ns	V_{cc} = 400 V I_{ce} = 30 A V_{ge} = 15 V R_G = 10 Ω	29 ns	V_{dd} = 400 V I_{ds} = 15 A V_{gs} = 10 V R_G = 4.7 Ω	17 ns	V_{cc} = 300 V I_{ce} = 20 A V_{ge} = 15 V R_G = 5 Ω	16 ns	V_{dd} = 300 V I_{ds} = 10 A V_{gs} = 18 V/0 V R_L = 30 Ω R_G = 0 Ω
T_{doff}	100 ns		61 ns		42 ns		27 ns	

The maximum gate voltages of Si IGBT, Si MOSFET, Si IGBT with SiC diode, and SiC MOSFET, as seen from the datasheet, are −30/+30 V, −30/+30 V, −20/+20 V, and −4/+22 V, respectively. Therefore, it can be inferred from the datasheet that the SiC MOSFET is most vulnerable to the large gate voltage. This paper experimentally checks a low-rated gate voltage of SiC MOSFET by applying the same voltage stress to four types of switching devices and examines a change of electrical characteristics caused by the gate oxide degradation.

4. Investigation of Threshold Voltage and On-Resistance under High Electric Field Stress

This paper investigated V_{th} and R_{on} according to HEF stress. The V_{th} and R_{on} measurement circuits were configured as shown in Figure 5.

Figure 5 shows the case of Si MOSFET and SiC MOSFET. In the case of Si IGBT and Si IGBT with SiC diode, V_{gs} and I_{ds} correspond to gate–emitter voltage (V_{ge}) and collector–emitter current (I_{ce}), respectively. Figure 5a shows the V_{th} measurement circuit.A device under test (DUT) is connected to measure V_{th}, as shown in Figure 5a.Then, the magnitude of V_{gs} is gradually raised from 0 V until I_{ds} is 1 mA. V_{gs}, when I_{ds} becomes 1 mA, is V_{th} [14].

As shown in Table 2, I_{ds} (or I_{ce}) used to measure V_{th} is very small for Si MOSFET and Si IGBT with SiC diode. These values are very small to measure with an oscilloscope. Therefore, I_{ds} (or I_{ce}) of 1 mA that can be measured with a small error is selected, and V_{th} is measured with 1 mA for all four devices.

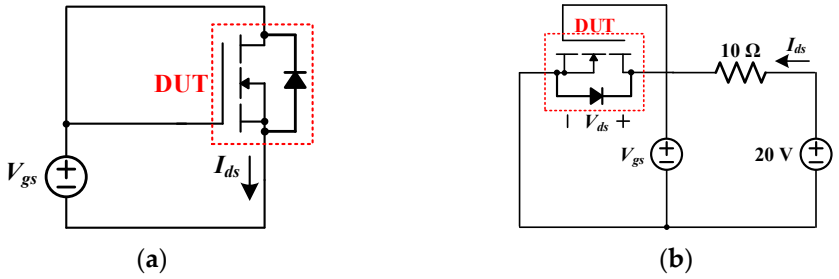


Figure 5. Measurement circuits (**a**) V_{th} (**b**) R_{on}.

Figure 5b represents the R_{on} measurement circuit. To measure R_{on}, the voltage used to measure R_{on} in the datasheet of each device is applied to V_{gs}. That is, V_{gs} for R_{on} measurement is 15 V for Si IGBT, 10 V for Si MOSFET, 15 V for Si IGBT with SiC diode, and 18 V for SiC MOSFET. Then, I_{ds} and V_{ds} when the switch is fully on are measured with an oscilloscope to eliminate the effect of parasitic components. Meanwhile, R_{on} varies with respect to the junction temperature.In order to reduce the variation caused by the junction temperature change, the temperature rise of the switch is minimized by applying I_{ds} (about 2 A) which is much smaller than the rated value of the switch for a short time (about 40 ms). R_{on} is calculated using the measured V_{ds} and I_{ds} as (10):

$$R_{on} = V_{ds}/I_{ds} \tag{10}$$

The measured device characteristics are expressed as the rate of change concerning the initial value as (11):

$$\text{Variation (\%)} = (P_{aging} - P_{fresh})/P_{fresh} \cdot 100 \tag{11}$$

In (11), P_{aging} represents a characteristic of the aging device. Moreover, P_{fresh} is a property of the fresh device. In Figure 6, the rules are established to distinguish the devices used in this paper.

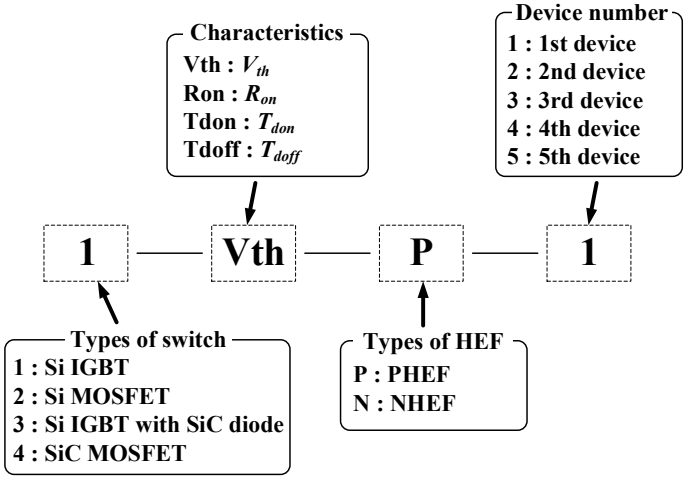


Figure 6. Device naming rule in this paper.

Figure 6 shows the device naming rule used in this paper. A device's name is divided into four parts. The first part indicates the type of switching device. As shown in Figure 6,

a number is assigned to each switch type. The second part shows the measured device property. The third part is the type of HEF, and the last part means the device number. The example of Figure 6, 1-Vth-P-1, refers to the first switch among the five switches where PHEF stress is applied to the Si IGBT for the V_{th} measurement.

4.1. Threshold Voltage Variation under HEF Stress

Figure 7 is the V_{th} variations in PHEF stress according to the types of the switching device. In Figure 7, Si IGBT with SiC diode is named Si IGBT (hybrid). Figure 7a,b demonstrate that V_{th} of Si IGBT and Si MOSFET had little change under PHEF stress. For Si IGBT with SiC diode, as shown in Figure 7c, the average value of V_{th} increased by about 3% compared to the initial value. Figure 7d shows the V_{th} of SiC MOSFET according to PHEF stress time. In the case of SiC MOSFET, V_{th} rapidly increases after PHEF stress. After 900 s PHEF stress, the average variation of V_{th} exceeded 100%. Moreover, the average variation of V_{th} was 166% when PHEF stress was finished. Consequently, under PHEF stress, the SiC MOSFET's V_{th} variation is more significant than Si-based devices. The V_{th} increment in SiC MOSFET indicates that Q_{it} occurs relatively more than Q_{ot}.

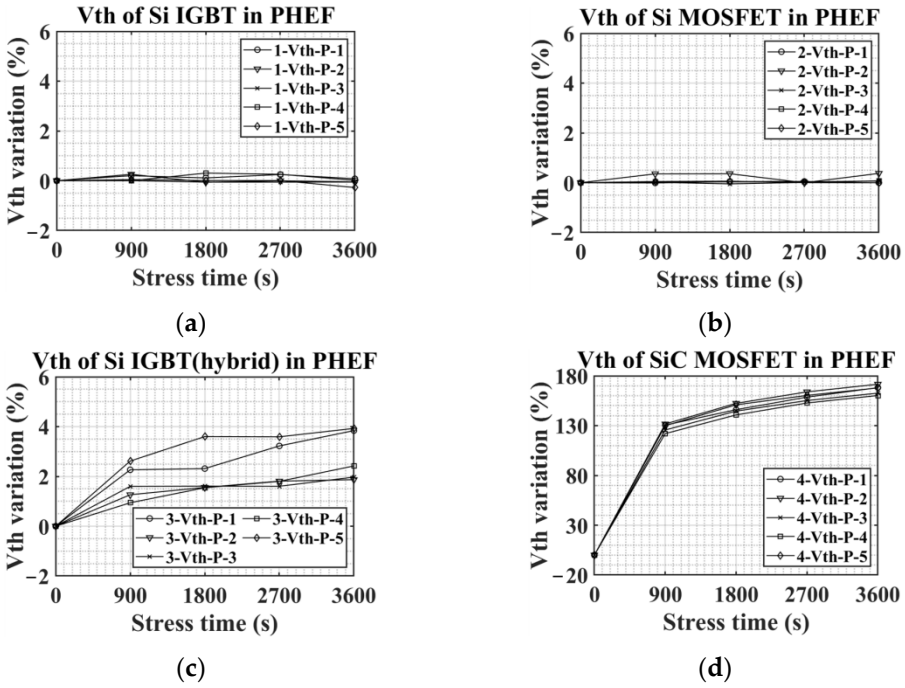


Figure 7. V_{th} variations in PHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

A small level change in V_{th} without a noticeable increase or decrease trend can be regarded as a measurement error by the experimental equipment. Therefore, the V_{th} change of Si IGBT and Si MOSFET in Figure 7 can be considered as the measurement error. On the other hand, since Si IGBT with SiC diode and SiC MOSFET has a marked increase in V_{th}, even though considering the measurement error, V_{th} variations in Si IGBT with SiC diode and SiC MOSFET can be referred to as a permanent shift in V_{th}.

Figure 8 shows V_{th} variations in NHEF stress according to the types of the switching device. As demonstrated from Figure 8a, in the case of Si IGBT, there were few changes in V_{th} after NHEF stress. The average V_{th} variations of Si MOSFET and Si IGBT with SiC diode after 3600 s NHEF stress were −0.6% and −0.4%, respectively. For SiC MOSFET, the amount of V_{th} reduction was more significant than that of other types of switching devices. When the NHEP stress time was 900 s, averagely, V_{th} decreased by about 51% compared to the initial value, and when the stress was finished, V_{th} decreased by about 69%. The V_{th} reduction in SiC MOSFET means that Q_{ot} occurs more than Q_{it}.

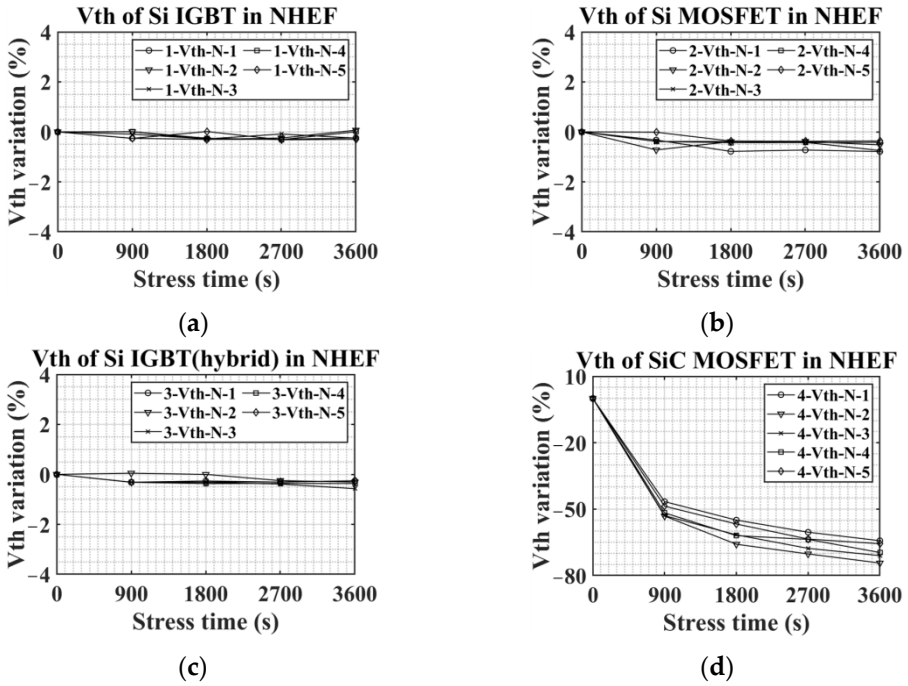


Figure 8. V_{th} variations in NHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

Figure 8 indicates that, in NHEF stress, SiC MOSFET experiences considerable V_{th} reduction. This means that SiC MOSFETs have a greater risk of being switched on when they should be switched off than other types of switching devices. Therefore, SiC MOSFETs are more vulnerable to NHEF stress than Si-based devices.

4.2. On-Resistance Variation under HEF Stress

Figure 9 shows the changes of R_{on} in PHEF stress according to the switching device. For Si IGBT, shown in Figure 9a, R_{on} increased by about 1.3% compared to the initial value when the stress was finished. Furthermore, as shown in Figure 9b, the average R_{on} variation of Si MOSFET was about 0.3% after PHEF stress. For Si IGBT with SiC diode depicted in Figure 9c, four out of five DUTs showed little change, but 3-Ron-P-1 had a reduction tendency of R_{on}. From this, it can be seen that in the case of the Si-based device, the change in R_{on} according to PHEF stress is not significant. However, R_{on} of SiC MOSFET increased rapidly as PHEF stress progressed, as shown in Figure 9d. After the first 900 s of the stress, R_{on} increased by about 55% on average, and at the end of the stress, R_{on} rose to about 100% compared to the initial value. As shown in Figure 7d, V_{th} of SiC MOSFET in PHEF stress rose, resulting in the reduction of V_{over} in (3). As explained earlier, R_{on} of SiC MOSFET is greatly affected by R_{ch}. Therefore, due to the decrement of V_{over}, R_{on} rose. Similar to the V_{th} trends in Figure 7, the rate of change of SiC MOSFET was the largest in R_{on}. These results indicate that the SiC MOSFET's conduction loss can be larger than other Si-based devices in the positive gate oxide degradation that raises V_{th}.

Figure 10 shows the changes of R_{on} in NHEF stress according to the switching device. Figure 10a–c describe that R_{on} of Si IGBT, Si MOSFET, and Si IGBT with SiC diode had no trend according to NHEF stress. R_{on} of Si IGBT had the variation within about 6% depending on the stress. In the case of Si MOSFET, a device with an increase in R_{on}, a device with a decrease in R_{on}, and a device with few changes in R_{on} appear. R_{on} of Si IGBT (hybrid) had the slightest change according to NHEF stress. Meanwhile, Figure 10d demonstrates that SiC MOSFETs had a reduction trend of R_{on} according to NHEF stress. At the end of the stress, the variation in R_{on} of 4-Ron-N-1 was about −6%, and the variation in R_{on} of 4-Ron-N-5 was about 18%.

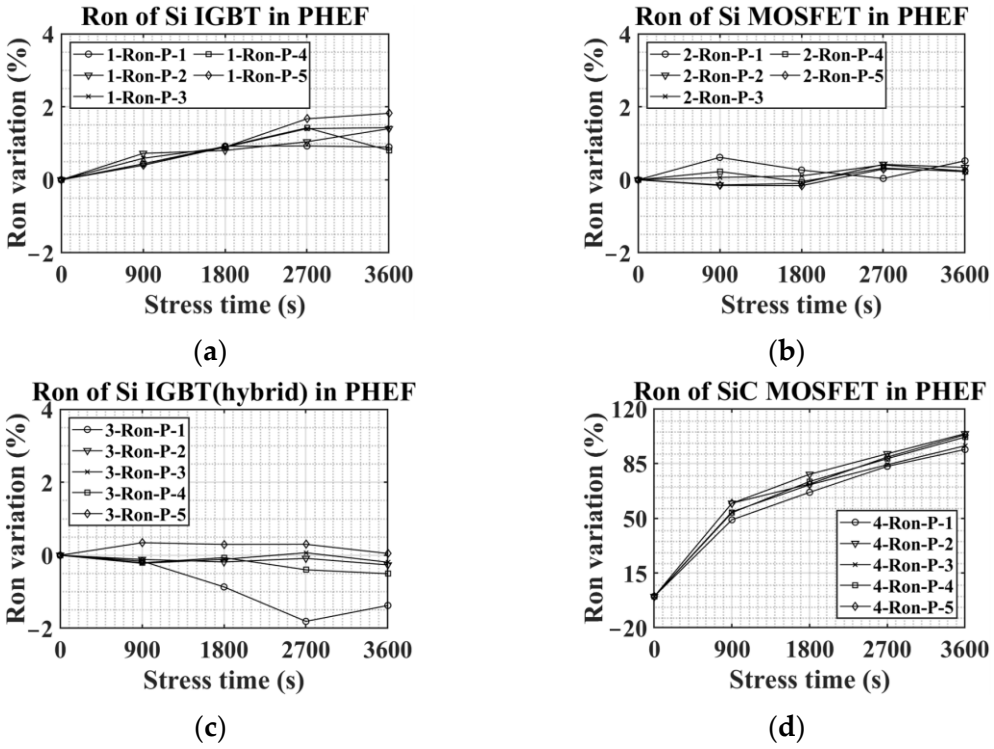


Figure 9. R_{on} variations in PHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

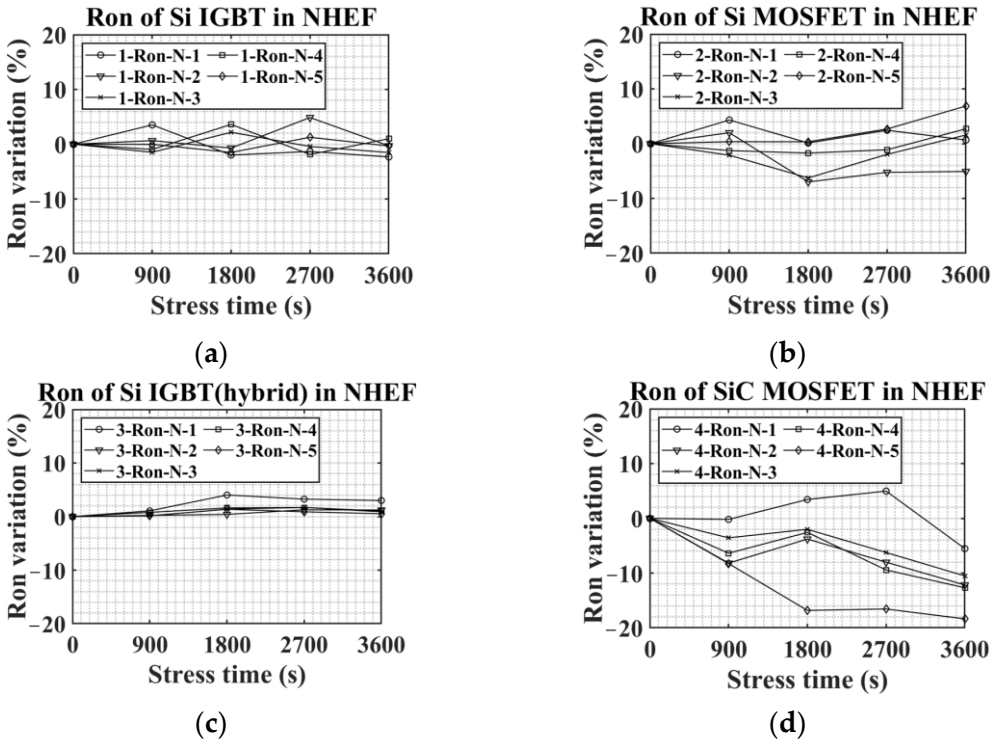


Figure 10. R_{on} variations in NHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

The R_{on} reduction of SiC MOSFET in the NHEF stress can be explained by the V_{th} change. As shown in Figure 8d, V_{th} of SiC MOSFET decreases in NHEF stress. This V_{th} reduction raises V_{over} in (3). As a result, R_{on} decreases.

5. Turn-On and Turn-Off Delay under High Electric Field Stress

Figure 11 represents a double pulse test circuit (DPTC) used to measure T_{don} and T_{doff}. Figure 11 shows the DPTC used to measure the T_{don} and T_{doff} of the switching devices. A gate driver named SKHI22BR was used in this paper. The gate driver driving pulse in the DPTC was generated through a digital signal processor (DSP). The DSP used in this paper is TI TMS320F28335. Furthermore, UP-3005T was used for DC supply. Figure 11a is the circuit diagram for measuring T_{don} and T_{doff}. DUT is located at the bottom, as shown in Figure 11a. A large gate driver resistor was used to easily observe T_{don} and T_{doff} characteristics [17,21]. The gate driver resistor R_g for T_{don} and T_{doff} is 485 Ω.

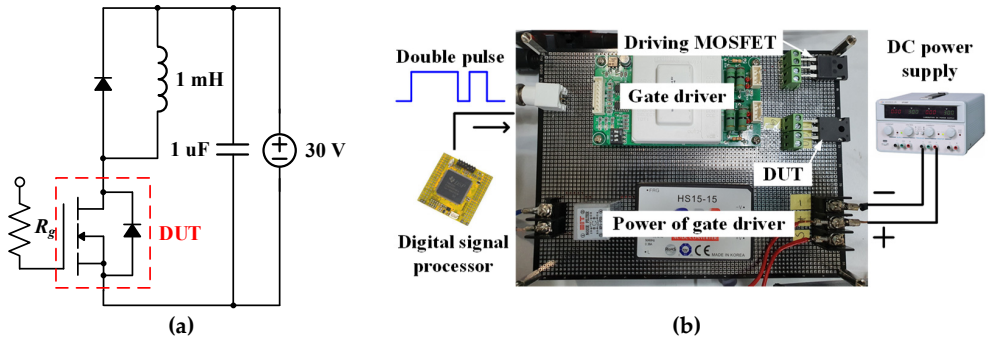


Figure 11. DPTC (**a**) circuit diagram, and (**b**) picture of DPTC.

5.1. Turn-On Delay Variation under HEF Stress

Figure 12 shows some of the results of the T_{don} experiment in PHEF stress. T_{don} in the fresh state and T_{don} after 3600 s of PHEF stress are displayed together. As shown in Figure 12, in the case of Si-based devices, the difference between before and after PHEF stress is not observed. However, as demonstrated from Figure 12d, T_{don} of 4-Tdon-P-4, which is SiC MOSFET before the stress was about 232 ns, but T_{don} measured after the stress was about 414.4 ns. Therefore, the T_{don} of 4-Tdon-P-4 had an increase of about 79% compared to the initial value. A change in T_{don} can be explained by V_{th} variation. As shown in Figure 12, the V_{th} of Si-based devices hardly changed after PHEF stress. However, in the case of SiC MOSFET, V_{th} grew significantly after PHEF stress. Therefore, the rise of V_{th} raised T_{don}.

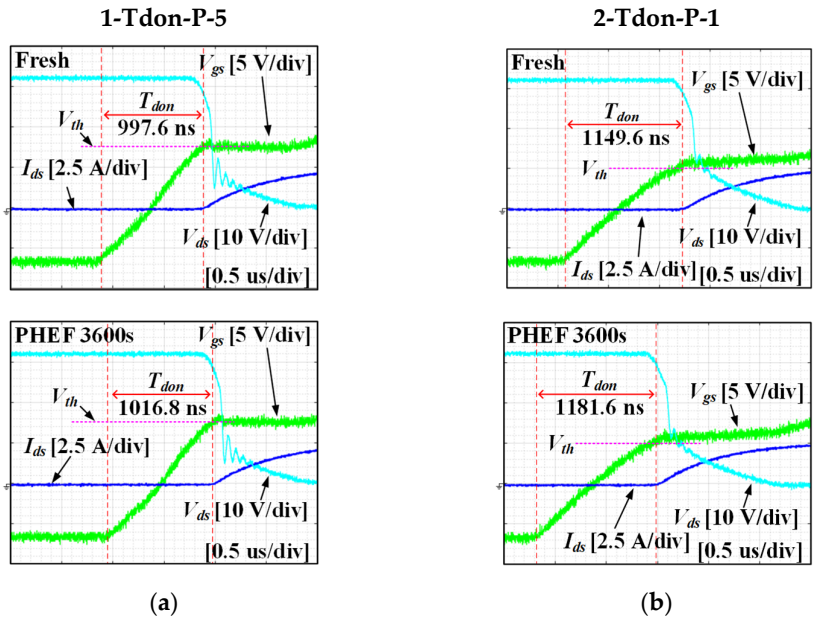


Figure 12. *Cont.*

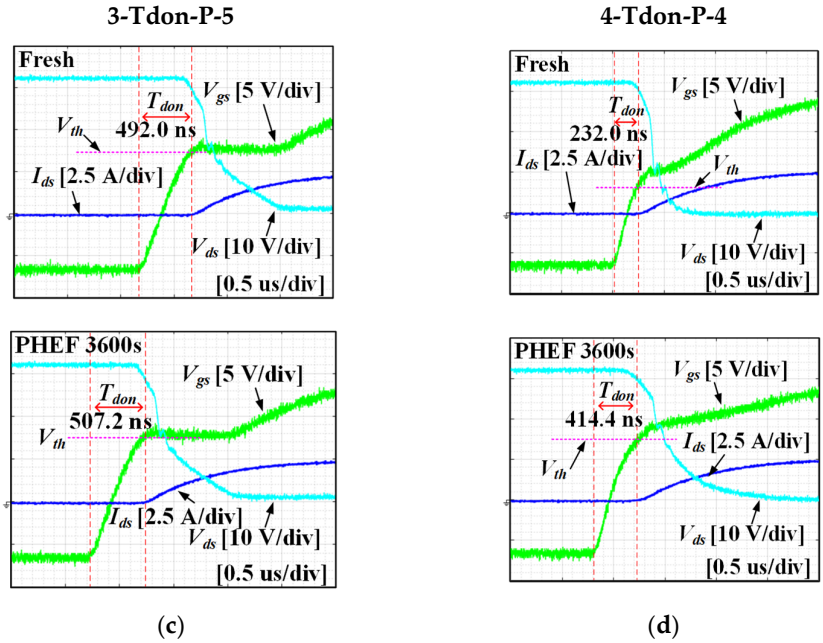


Figure 12. Turn on waveforms in PHEF stress: (**a**) 1-Tdon-P-1, (**b**) 2-Tdon-P-2, (**c**) 3-Tdon-P-1, and (**d**) 4-Tdon-P-4.

Figure 13 shows all of the results of the T_{don} experiment in PHEF stress according to the type of the switching device. Figure 13a–c indicate that there is no significant increase or decrease in T_{don} according to PHEF stress for Si-based devices. However, in the case of SiC MOSFETs, an increasing trend of T_{don} was observed in PHEF stress, similar to V_{th} in Figure 7d. At 900 s of PHEF stress, T_{don} rose sharply and continued to increase. In particular, 4-Tdon-P-4 had a very large variation of about 80% in T_{don} compared to the fresh condition after 3600 s of PHEF stress. Other SiC MOSFETs increased by 40% to 50% compared to the initial value. Based on Figures 12 and 13, it can be seen that SiC MOSFETs have a more considerable T_{don} increment during PHEF stress compared to Si-based devices.

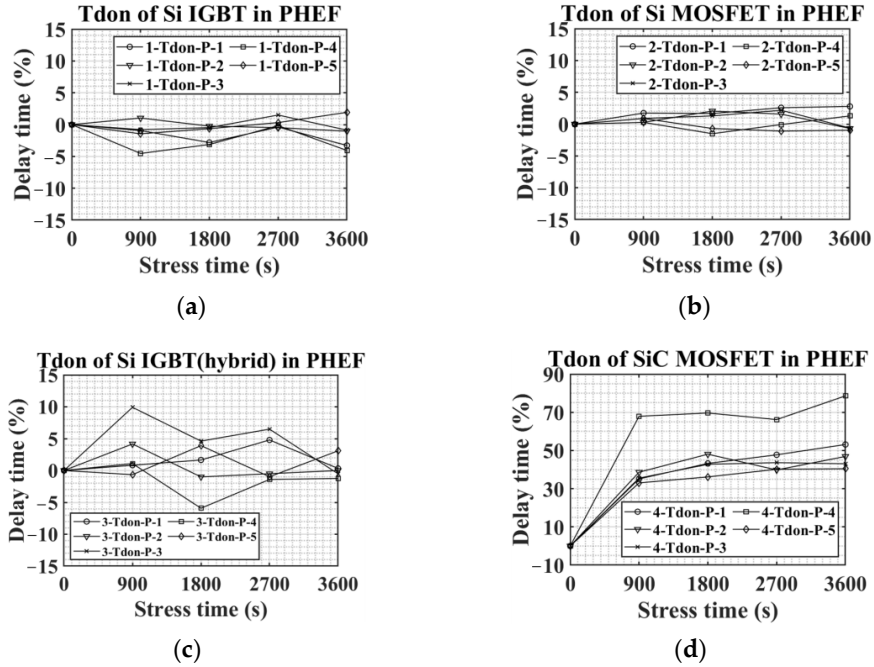


Figure 13. T_{don} variations in PHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

Figure 14represents some of the results of the T_{don} experiment in NHEF stress. Figure 14 shows that no significant change in T_{don} was observed for Si-based devices under NHEF stress. However, the T_{don} of 4-Tdon-N-2 was reduced after NHEF stress. T_{don} of 4-Tdon-N-2 in the fresh condition was 293.6 ns. Moreover, 4-Tdon-N-2 after NHEF stress was 248 ns. Therefore, the T_{don} variation of 4-Tdon-N-2 was −16%. This change is opposite to the trend in the PHEF stress of SiC MOSFET. T_{don} of 4-Tdon-N-2, a SiC MOSFET, was reduced because V_{th} decreased after NHEF stress.

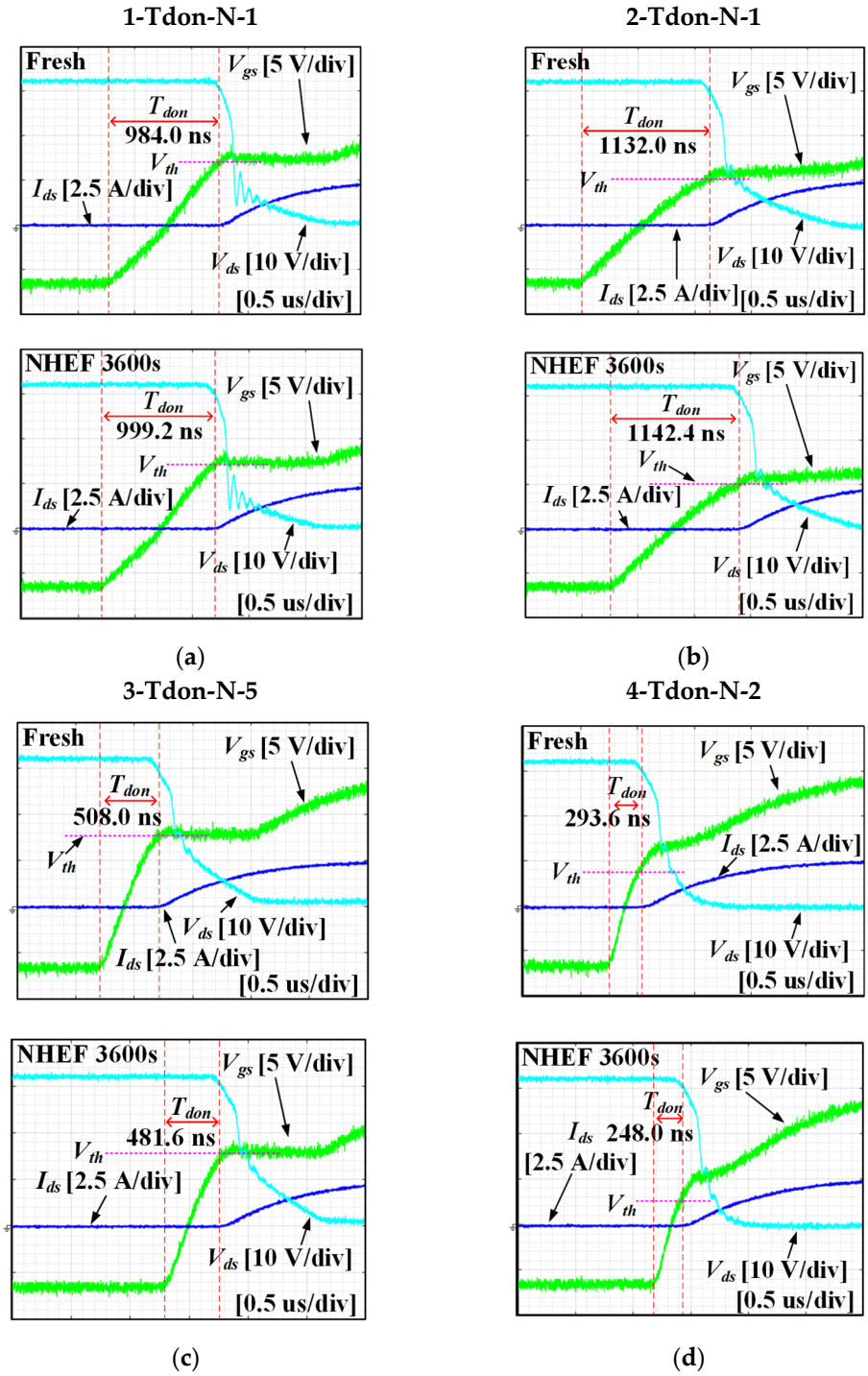


Figure 14. Turn on waveforms in NHEF stress: (**a**) 1-Tdon-P-1, (**b**) 2-Tdon-P-2, (**c**) 3-Tdon-P-1, and (**d**) 4-Tdon-P-4.

Figure 15 shows all the results of the T_{don} experiment in NHEF stress. Figure 15a–c describe that there was no significant change in T_{don} of Si IGBT, Si MOSFET, and Si IGBT with SiC diode under NHEF stress. However, in SiC MOSET, Figure 15d shows that T_{don} decreased as the NHEF stress progressed. After 3600 s of NHEF stress, the average T_{don} of the five SiC MOSFETs decreased by about 13% compared to the initial value. The T_{don} of SiC MOSFET decreases with the NHEF stress due to the reduction of V_{th}. As shown in Figure 2, T_{don} is reduced as V_{th} decreases. Figure 8d shows that V_{th} of SiC MOSFET decreased after NHEF stress. Therefore, the T_{don} of SiC MOSFET is reduced under NHEF stress.

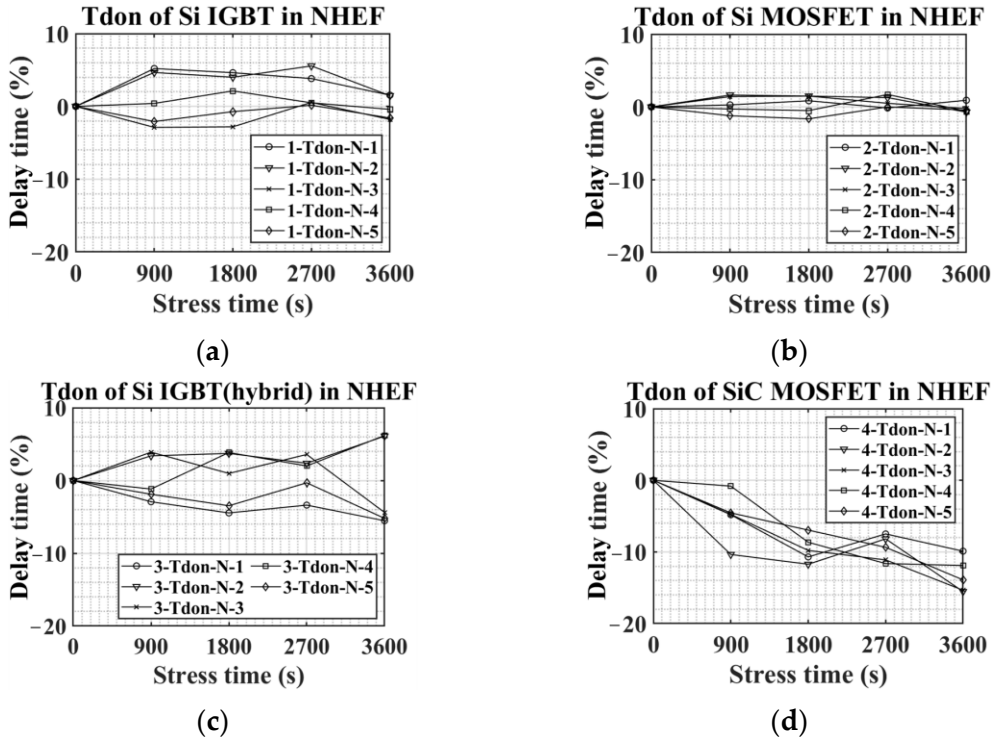


Figure 15. T_{don} variations in NHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

5.2. Turn-Off Delay Variation under HEF Stress

Figure 16 shows some of the results of the T_{doff} experiment in PHEF stress. As shown in Figure 16, in the case of 1-Tdoff-P-1, 2-Tdoff-P-2, and 3-Tdoff-P-1, the difference between before and after PHEF stress was not clear. However, T_{doff} of 4-Tdoff-P-4, as shown in Figure 16d, decreased sharply after PHEF stress. The T_{doff} variation of 4-Tdoff-P-4 was −42%. This reduction in T_{doff} can be explained by a change in V_m. Looking at the change in V_m before and after PHEF stress shown in Figure 16d, it can be seen that V_m increased after PHEF stress. Therefore, the T_{doff} of the SiC MOSFET, 4-Tdoff-P-4, is reduced.

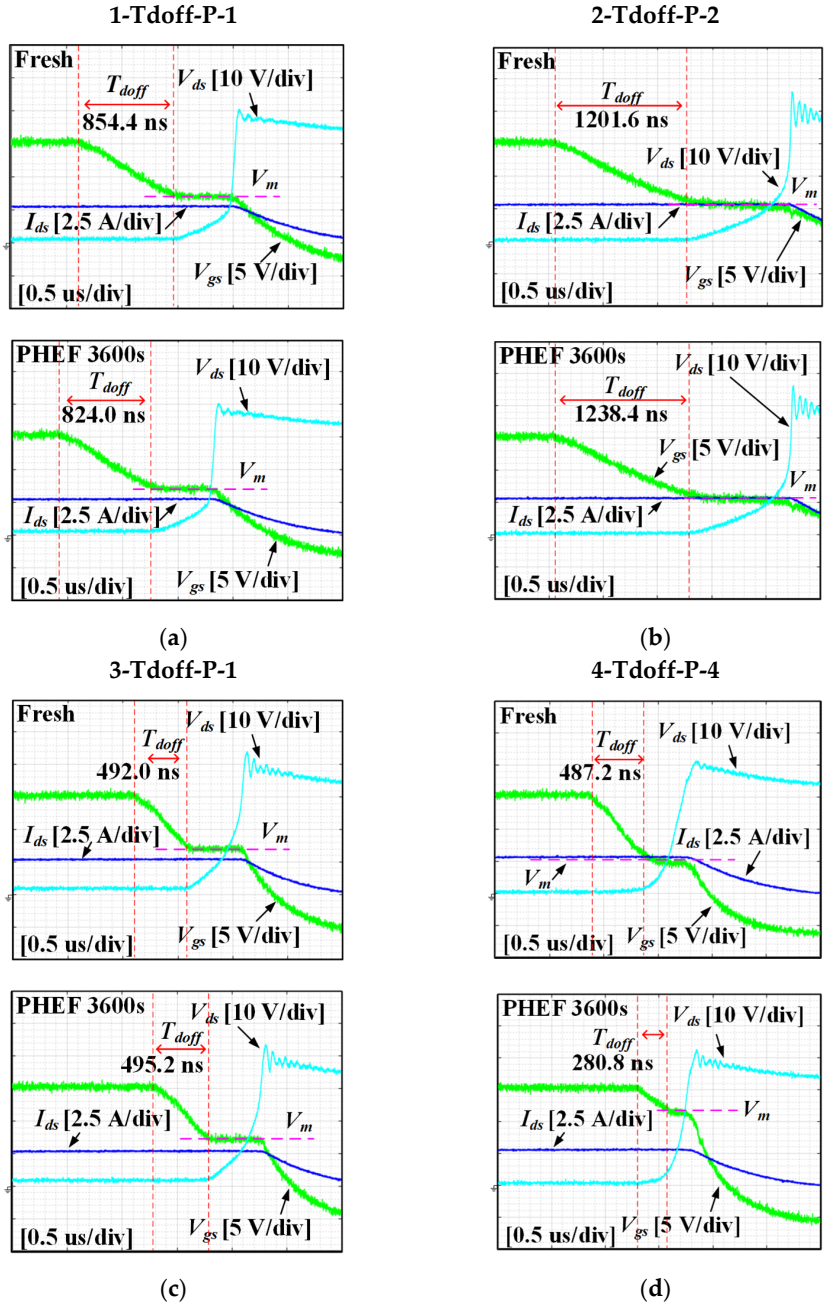


Figure 16. Turn off waveforms in PHEF stress: (**a**) 1-Tdoff-P-1, (**b**) 2-Tdoff-P-2, (**c**) 3-Tdoff-P-1, and (**d**) 4-Tdoff-P-4.

Figure 17 is all the results of the T_{doff} experiment in PHEF stress. For Si IGBT, Si MOSFET, and Si IGBT with SiC diode, Figure 17a–c demonstrate that there was no clear trend of increase or decrease in T_{doff} in PHEF stress. However, in the case of SiC MOSFETs, T_{doff} decreased steadily and sharply under PHEF stress. The average T_{doff} variation of SiC MOSFET after 3600 s of PHEF stress was −46%. In PHEF stress, as shown in Figure 7d, V_{th} increases. In addition, Equation (7) indicates that when V_{th} increases, V_m also increases. The rise of V_m decreases T_{doff}, as illustrated in Figure 3. Therefore, under PHEF stress, the T_{doff} of SiC MOSFET is reduced, as shown in Figure 17d. Consequently, the T_{doff} of SiC MOSFET is significantly reduced under PHEF stress compared to other Si-based devices. Figure 18 is some of the results of the T_{doff} experiment in NHEF stress. Figure 18a–c indicate that Si-based devices did not have much change in T_{doff} in NHEF stress. However, T_{doff} of 4-Tdoff-P-4 had a noticeable difference. T_{doff} of 4-Tdoff-P-4 in the fresh condition

was 452.0 ns. Moreover, the T_{doff} of 4-Tdoff-P-4 after 3600 s of PHEF stress was 560.8 ns. Therefore, the T_{doff} variation of 4-Tdoff-P-4 was 24%. Figure 18d demonstrates that V_m decreased after NHEF stress. As shown in Figure 3, decreasing V_m raises T_{doff}. Therefore, the T_{doff} of 4-Tdoff-P-4 increased.

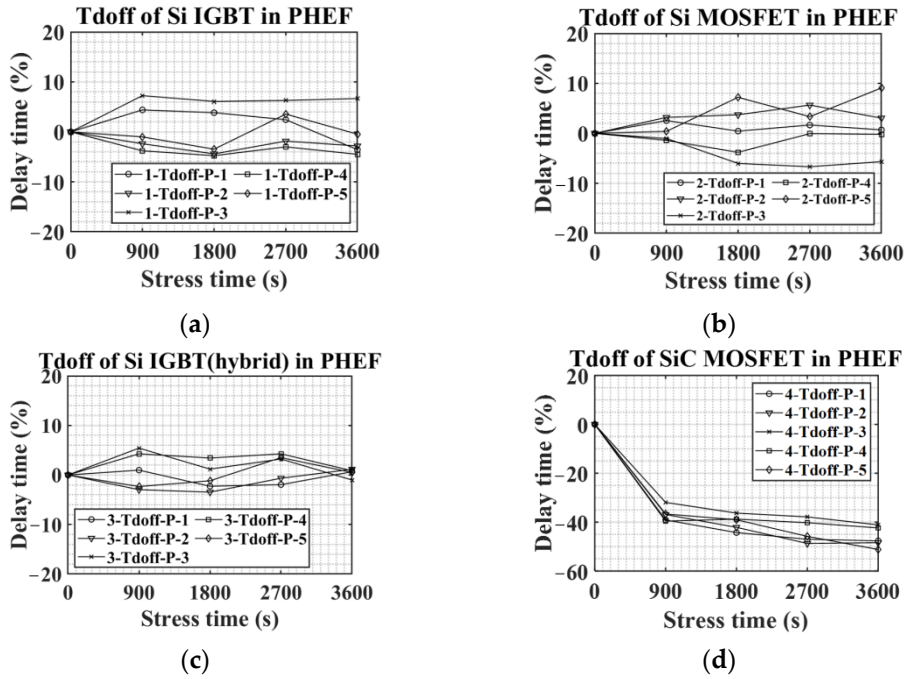


Figure 17. T_{doff} variations in PHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

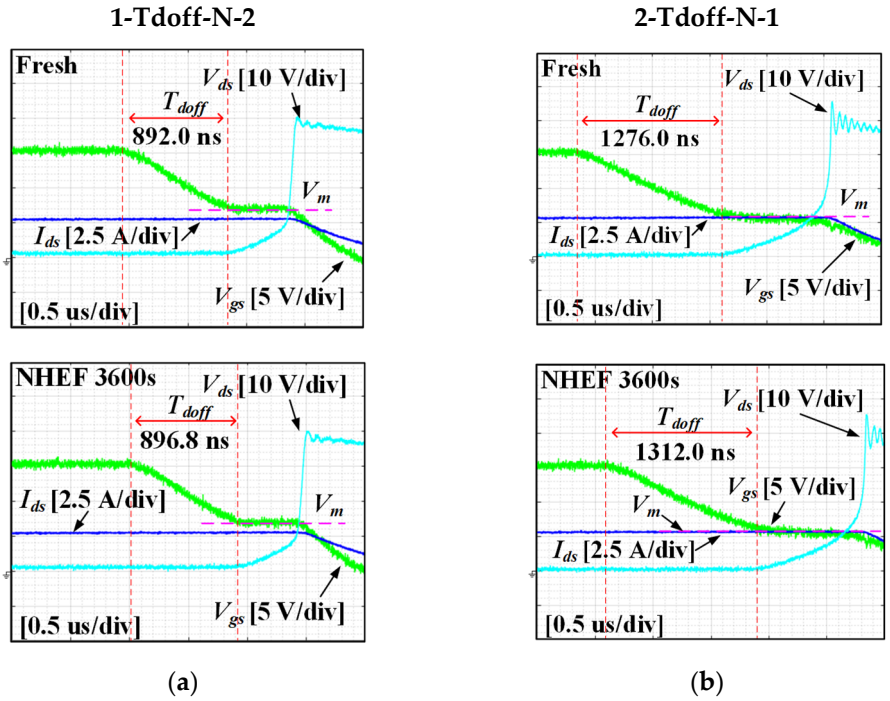


Figure 18. *Cont.*

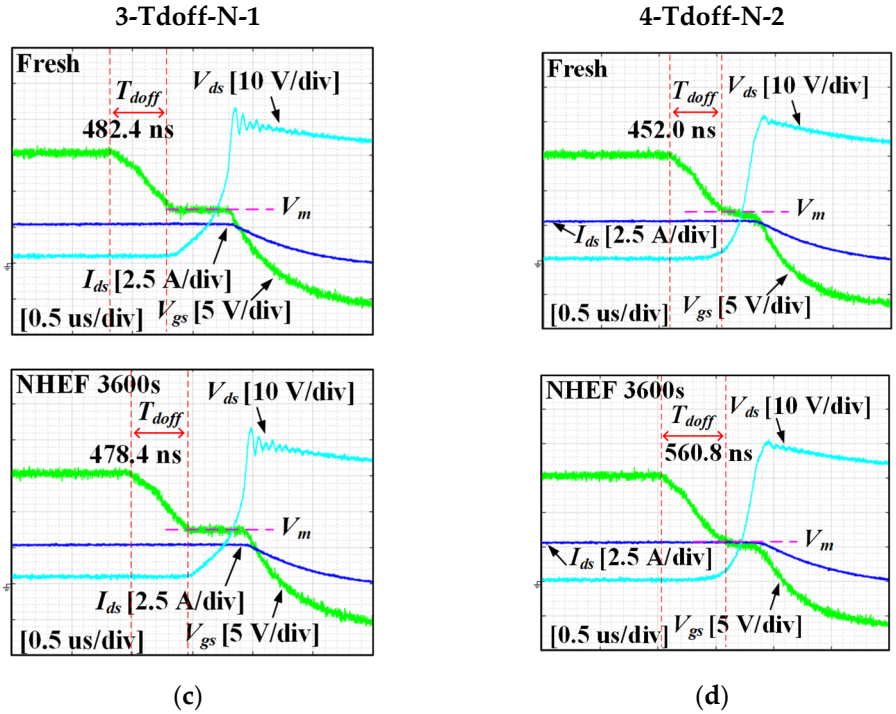
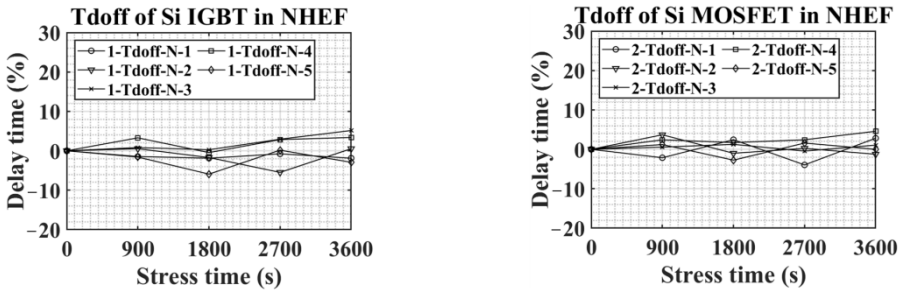


Figure 18. Turn off waveforms in NHEF stress: (**a**) 1-Tdoff-P-1, (**b**) 2-Tdoff-P-2, (**c**) 3-Tdoff-P-1, and (**d**) 4-Tdoff-P-4.

Figure 19 represents all the results of the T_{doff} experiment in NHEF stress. For Si-based devices, no clear trend was observed in NHEF stress. However, as shown in Figure 19d, the T_{doff} of SiC MOSFETs increased as the NHEF stress continued. The average T_{doff} of SiC MOSFETs after 3600 s of PHEF stress was 24%. In particular, 4-Tdoff-N-3 showed a significant change as T_{doff} increased by about 33% compared to the initial value. It was mentioned in the previous discussion that the decrement of V_{th} raises T_{doff}. Figure 8d demonstrates that V_{th} decreases with NHEF stress. Therefore, T_{doff} rises in NHEF stress. Table 3 summarizes changes in V_{th}, R_{on}, T_{don}, and T_{doff} under HEF stress according to switch types. The values in Table 3 are results obtained after 3600 s of HEF stress. Table 3 demonstrates that V_{th}, R_{on}, T_{don}, and T_{doff} variations of SiC MOSFET are larger than those of Si-based devices.



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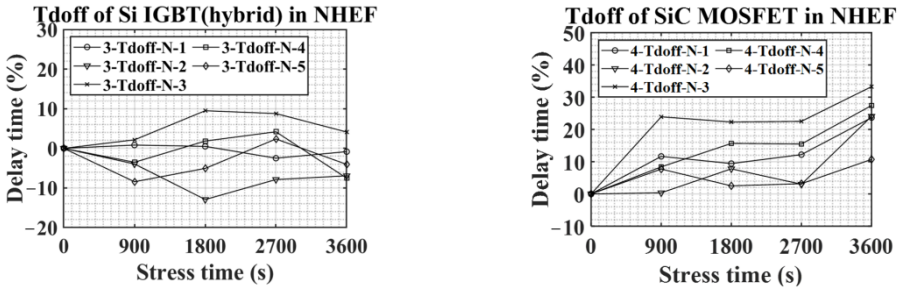


(**c**) (**d**)

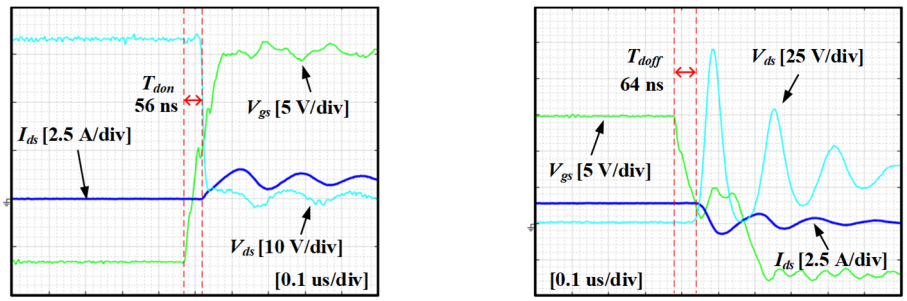
Figure 19. T_{doff} variations in NHEF stress: (**a**) Si IGBT, (**b**) Si MOSFET, (**c**) Si IGBT with SiC diode, and (**d**) SiC MOSFET.

Table 3. Threshold voltage, on-resistance, turn-on delay, and turn-off delay variations according to switch types under HEF stress.

		Si IGBT	Si MOSFET	Si IGBT with SiCDiode	SiC MOSFET
V_{th}	PHEF	0%	0%	3%	166%
	NHEF	0%	−1%	0%	−69%
R_{on}	PHEF	1%	0%	0%	100%
	NHEF	−1%	1%	1%	−12%
T_{don}	PHEF	−1%	0%	0%	52%
	NHEF	0%	0%	−1%	−13%
T_{doff}	PHEF	−1%	1%	0%	−46%
	NHEF	1%	1%	−3%	24%

6. Performance of Voltage and Current Source Inverter with Duty Error Changes

The previous experimental results demonstrate that T_{don} and T_{doff} change after HEF stress. In other words, it means that the duty error of the converter changes as the gate oxide degradation progresses. This section analyzes the effects of duty error change according to HEF stress on the performance of voltage source and current source inverter. In the characteristic analysis according to HEF stress, a large gate resistance was used to sensitively observe changes in T_{don} and T_{doff}. T_{don} and T_{doff} of SiC MOSFET using a practical gate resistance of 15 Ω are shown in Figure 20.



(**a**) (**b**)

Figure 20. Turn-on and turn-off waveforms when R_g = 15 Ω: (**a**) turn-on, and (**b**) turn-off.

Figure 20 shows the turn-on and turn-off waveforms when R_g is 15 Ω. As shown in Figure 20, a smaller R_g results in shorter T_{don} and T_{doff} because V_{gs} changes faster. However, since V_{th}, which is a parameter that determines T_{don} and T_{doff}, is the same regardless of R_g, the ratio of the change in T_{don} and T_{doff} according to V_{th} variation is similar even if R_g is

different. Therefore, the rate of change of T_{don} and T_{doff} according to the HEF stress time obtained in this paper is applicable even when R_g is 15 Ω. As shown in Figure 20, when R_g is 15 Ω, T_{don} is 56 ns, and T_{doff} is 64 ns. In order to calculate the change of duty error according to the HEF stress time, it is necessary to know the rate of change of T_{don} and T_{doff} according to the stress time. As shown in Figures 13d, 15d, 17d and 19d, $T_{don,}$ and T_{doff} in each condition were obtained using five devices. Using the average value of the five devices, the rate of change of T_{don} and T_{doff} in PHEF and NHEF stress can be calculated. Figure 21 shows the rate of change of T_{don} and T_{doff} obtained by average values of results in Figures 13d, 15d, 17d and 19d. In Figure 21, $Rate_{don}$ represents the change rate of T_{don} according to stress time, and $Rate_{doff}$ means the change rate of T_{doff} according to stress time.

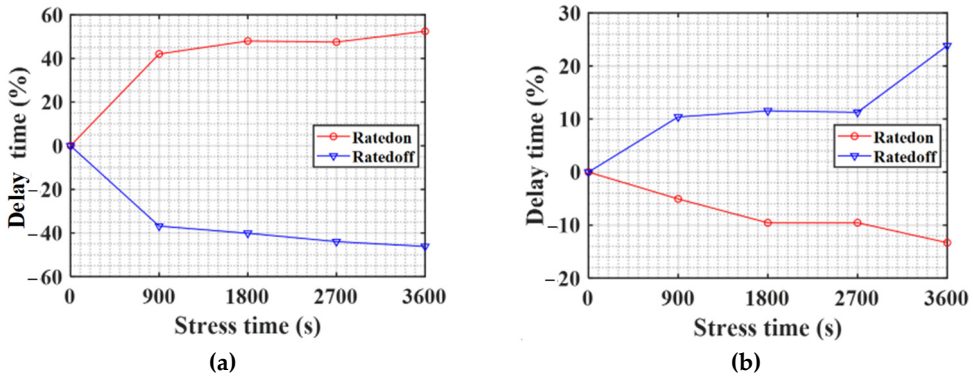


Figure 21. $Rate_{don}$ and $Rate_{doff}$ according to the stress time in PHEF and NHEF stress: (**a**) PHEF stress, and (**b**) NHEF stress.

6.1. Performance Variation of Grid-Connected Voltage Source Inverter with Duty Error Change Due to Gate Oxide Degradation

This section examines the performance variation of the grid-connected voltage source inverter according to the duty error change due to the gate oxide degradation. Figure 22 shows a typical grid-connected voltage source inverter.

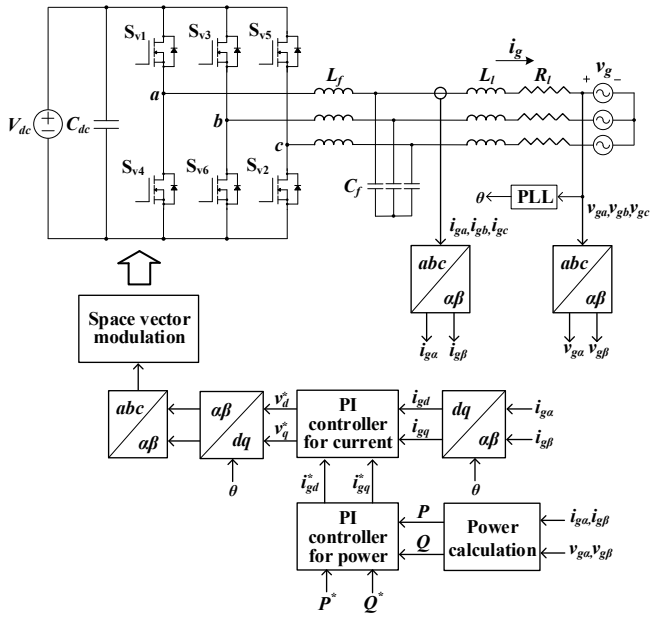


Figure 22. Grid-connected voltage source inverter.

In general, a grid-connected voltage source inverter is controlled with a current alone or a current and power simultaneously [23]. Figure 22 shows a grid-connected voltage

source inverter with both current and power controls. In Figure 22, S_{v1}, S_{v2}, S_{v3}, S_{v4}, S_{v5}, and S_{v6} mean the switches of the voltage source inverter. In addition, V_{dc} is the inverter input voltage, and C_{dc} is the inverter input capacitor. R_l and L_l are line resistance and line inductance, respectively. Moreover, L_f and C_f mean the inductance and capacitance of the LC filter of the inverter output, respectively. V_g indicates the grid voltage, and i_g represents the grid current. The voltage source inverter in Figure 22 simultaneously controls the grid current and instantaneous power. For the inverter control, first, the three-phase grid voltage and grid current are converted using *abc* to $\alpha\beta$ transformation. The *abc* to $\alpha\beta$ transformation is as (12). In (12), i_{ga}, i_{gb}, and i_{gb} are *a*-phase, *b*-phase, and *c*-phase grid current, respectively. Moreover, v_{ga}, v_{gb}, and v_{gb} are *a*-phase, *b*-phase, and *c*-phase grid voltages, respectively:

$$\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}, \quad \begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} \tag{12}$$

Using the α and β values of the three-phase grid voltage and current converted by (12), the instantaneous active power (P) and reactive power (Q) are calculated as in (13):

$$P = 1.5\left(v_{g\alpha}i_{g\alpha} + v_{g\beta}i_{g\beta}\right),\ Q = 1.5\left(v_{g\beta}i_{g\alpha} - v_{g\alpha}i_{g\beta}\right) \tag{13}$$

The instantaneous reactive power must be controlled to zero for the unity power factor control. Therefore, the reference of the instantaneous reactive power, denoted by Q^*, is set to zero. Moreover, the reference of the instantaneous active power is applied as a desired value. In Figure 22, P^* means the reference of the instantaneous active power. The instantaneous power calculated by (13) and its reference value are inputs to the PI controller for the power control.

Figure 23 shows the PI controller for the power control. The PI controller for the active power control generates an output value by amplifying and integrating the difference between P* and P, as shown in Figure 23. The output value of the active power becomes i_{gd}^*. Similarly, for the reactive power control, the output value, i_{gq}^*, is generated by amplifying and integrating the difference between Q* and Q. i_{gd}^* and i_{gq}^* mean the reference value of the d and q value of the grid current. K_{pp}, K_{ip}, K_{pq}, and K_{iq} in Figure 23 represent coefficients used in the PI controller for the power control.

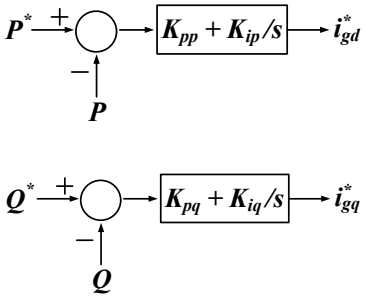


Figure 23. PI controller for power control.

Meanwhile, for the grid current control, the d and q values of the grid current are required. By (14), the d and q values of the grid current are obtained:

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix}\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} \tag{14}$$

In (14), θ is the phase of the grid voltage and is calculated through a phase-locked loop (PLL). The grid current reference values, which are the output of the PI controller for the power control, and the d and q values of the grid current from (14) are applied as the inputs of the PI controller for the grid current control.

Figure 24 shows the PI controller for the grid current control. As shown in Figure 24, to control the d value of the grid current, the output of the PI controller is generated by amplifying and integrating the difference between the reference value and the actual value of i_{gd}. The output of the PI controller controlling i_{gd} is v_d^*, which is the d value of the voltage source inverter control signal. Similarly, to control the q value of the grid current, the output v_q^* is generated by amplifying and integrating the difference between the reference value and the actual value of i_{gq}. v_q^* means the q value of the voltage source inverter control signal. The reference values of i_{gd} and i_{gq}, which are expressed as i_{gd}^* and i_{gq}^* are the output of the PI controller for the power control, shown in Figure 23. K_{pgd}, K_{igd}, K_{pgq}, and K_{igq} in Figure 24 mean coefficients used in the PI controller for the grid current control.

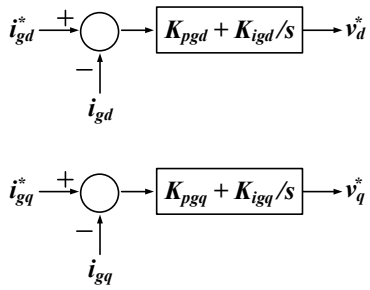


Figure 24. PI controller for grid current control.

v_d^* and v_q^* undergoes dq to $\alpha\beta$ conversion and $\alpha\beta$ to abc conversion, resulting in v_a^*, v_b^*, and v_c^*.The switching signals of the voltage source inverter are generated using space vector modulation [24]. The space vector modulation is implemented using an offset voltage, as shown in Figure 25 [25].

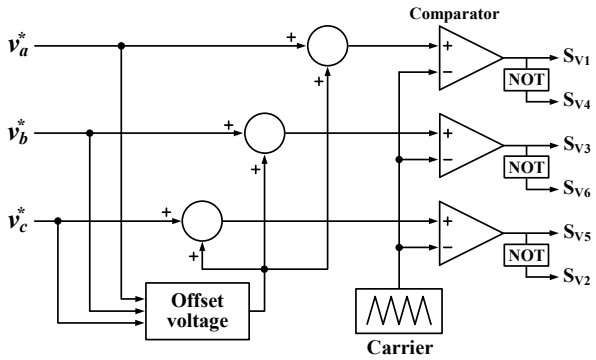


Figure 25. Space vector modulation using the offset voltage.

Figure 25 shows the space vector modulation using the offset voltage. v_a^*, v_b^*, and v_c^* in Figure 25 are the inverter control signal of a-phase, b-phase, and c-phase, respectively.v_a^*, v_b^*, and v_c^* are obtained from dq to $\alpha\beta$ conversion and $\alpha\beta$ to abc conversion of v_d^* and v_q^*. The offset voltage is calculated as follows (15):

$$v_{off} = -0.5 \cdot (V_{max} + V_{min}) \tag{15}$$

In (15), v_{off} means the offset voltage for the space vector modulation. Moreover, the largest of v_a^*, v_b^*, and v_c^* becomes V_{max} and the smallest becomes V_{min}. Switching signals are generated by comparing the carrier with the values obtained by adding the offset voltage to v_a^*, v_b^*, and v_c^*. Note that the switching frequency of the inverter is determined by the

frequency of the carrier. In the voltage source inverter, the switches of one leg operate complementarily. Since a huge current can flow at the moment when all the switches of one leg of the voltage source inverter are on, the dead-time is set to make all switches of one leg be off when the switching state changes. In addition, the duty of the switch is changed by T_{don} and T_{doff}. Figure 26 shows gating signals and the *a*-phase pole voltage considering the dead time, T_{don}, and T_{doff} of S_{v1} and S_{v4} which are the *a*-phase switches of the grid-connected voltage source inverter in Figure 22.

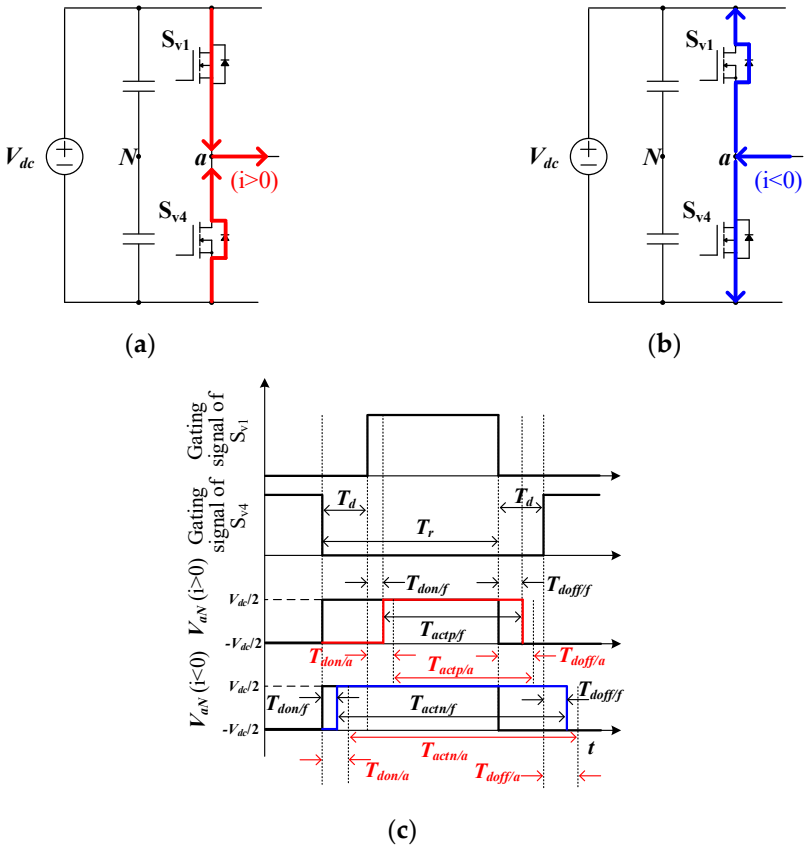


Figure 26. Current path and gating signals of S_{v1} and S_{v4} considering dead time, T_{don}, and T_{doff}. (**a**) current path in $i > 0$ (**b**) current path in $i < 0$ (**c**) gating signals of S_{v1} and S_{v4}.

In Figure 26, T_d means the dead time. Furthermore, V_{aN} is the a-phase pole voltage. T_r is the ideal dwelling time of V_{aN}. $T_{actp/f}$ is the dwelling time of V_{aN} considering T_d, T_{don}, and T_{doff} when the switching devices are fresh and the pole current (i) is positive. In addition, $T_{actn/f}$ is the dwelling time of V_{aN} considering T_d, T_{don}, and T_{doff} when the switching devices are fresh and the pole current is negative. $T_{don/a}$ and $T_{doff/a}$ denote turn-on delay and turn-off delay in aged condition, respectively. Moreover, $T_{actp/a}$ is the dwelling time of V_{aN} considering T_d, T_{don}, and T_{doff} when the switching devices are aging and the pole current is positive. In addition, $T_{actn/a}$ is the dwelling time of V_{aN} considering T_d, T_{don}, and T_{doff} when the switching devices are aging, and the pole current is negative. Figure 26a,b show the current path according to the pole current direction. Figure 26a,b demonstrate that the dwell time of V_{aN} changes, as shown in Figure 26c, because the path through which the current flows varies according to the sign of the pole current [26]. Equation (16) represents $T_{actp/f}$ and $T_{actn/f}$:

$$\begin{aligned} T_{actp/f} &= T_r - T_d - T_{don/f} + T_{doff/f}, \\ T_{actn/f} &= T_r + T_d - T_{don/f} + T_{doff/f} \end{aligned} \tag{16}$$

Equation (16) becomes as (17) when aging is considered:

$$\begin{aligned} T_{actp/a} &= T_r - T_d - T_{don/a} + T_{doff/a}, \\ T_{actn/a} &= T_r + T_d - T_{don/a} + T_{doff/a}. \end{aligned} \tag{17}$$

$T_{don/a}$ and $T_{doff/a}$ in (17) can be calculated through (18):

$$\begin{aligned} T_{don/a} &= T_{don/f}(1 + 0.01Rate_{don}), \\ T_{doff/a} &= T_{doff/f}(1 + 0.01Rate_{doff}) \end{aligned} \tag{18}$$

In (18), $Rate_{don}$ and $Rate_{doff}$ can be obtained from Figure 21. Meanwhile, the duty error due to aging can be calculated as (19) using (17) and the voltage source inverter switching frequency (F_{swv}):

$$\begin{aligned} D_{epv} &= \left(T_{actp/a} - T_r\right)F_{swv} = \left(-T_d - T_{don/a} + T_{doff/a}\right)F_{swv}, \\ D_{env} &= (T_{actn/a} - T_r)F_{swv} = \left(+T_d - T_{don/a} + T_{doff/a}\right)F_{swv}. \end{aligned} \tag{19}$$

In (19), D_{epv} means the duty error of the voltage source inverter due to the gate oxide degradation when the pole current is positive. D_{env} also represents the duty error of the voltage source inverter due to the gate oxide degradation when the pole current is negative. Figure 27 shows the duty error of the voltage source inverter according to the aging stress time.

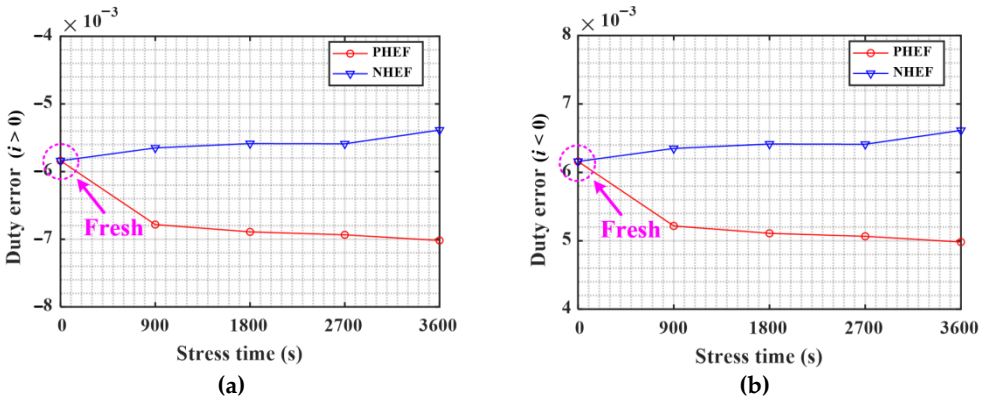


Figure 27. Duty error according to stress time (**a**) $i > 0$, and (**b**) $i < 0$.

Figure 27a shows the duty error according to the stress time when the pole current is positive. When the pole current is positive, the duty error increases at PHEF stress and decreases at NHEF stress. Figure 27b shows the duty error according to the stress time when the pole current is negative. When the pole current is negative, the duty error at PHEF stress decreases and the duty error at NHEF stress increases. In this chapter, the effects of the change in the duty error due to the gate oxide degradation on the output of the grid-connected inverter are analyzed through simulation. The parameters of the inverter used in the simulation are summarized in Table 4.

Figure 28 shows the simulation results of the grid-connected voltage source inverter according to HEF stress. Figure 28a–c are simulation results when using the duty error calculated from the fresh condition, PHEF stress during 3600 s, and NHEF stress during 3600 s, respectively. Figure 28 demonstrates that the THD of the grid current is the highest when the NHEF stress is applied for 3600 s. In addition, the peak-to-peak value of P is the largest in the case of PHEF stress. Moreover, the peak-to-peak value of Q is the largest in the case of NHEF stress.

Table 4. Parameters of grid-connected voltage source inverter.

Parameters	Value
V_{dc}	700 V
C_{dc}	550 uF
L_f	3 mH
C_f	20 uF
R_l	0.2 Ω
L_l	0.15 mH
V_g	311.13 V
Switching frequency	20 kHz
T_{dp}	0.3 us
P^*	3 kW
Q^*	0

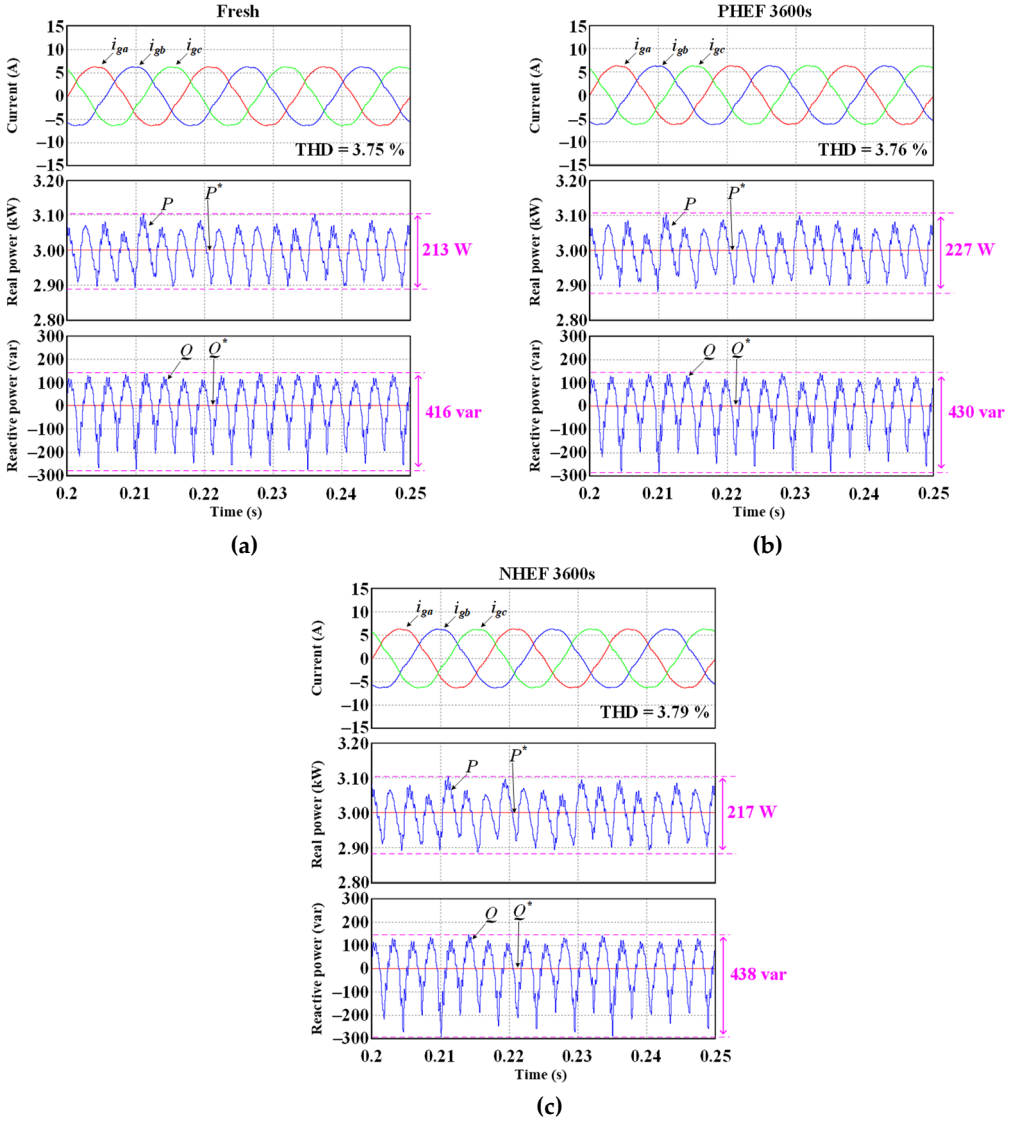


Figure 28. Simulation results of the grid-connected voltage source inverter according to HEF stress: (**a**) fresh condition, (**b**) PHEF stress during 3600 s, and (**c**) NHEF stress during 3600 s.

Figure 29 showsgraphs summarizing the THD of the grid current and the peak-to-peak values of the instantaneous power according to the stress time. Figure 29 indicates that as the gate oxide degradation progresses, the quality of the grid current and the reference tracking ability of the voltage source inverter deteriorates.

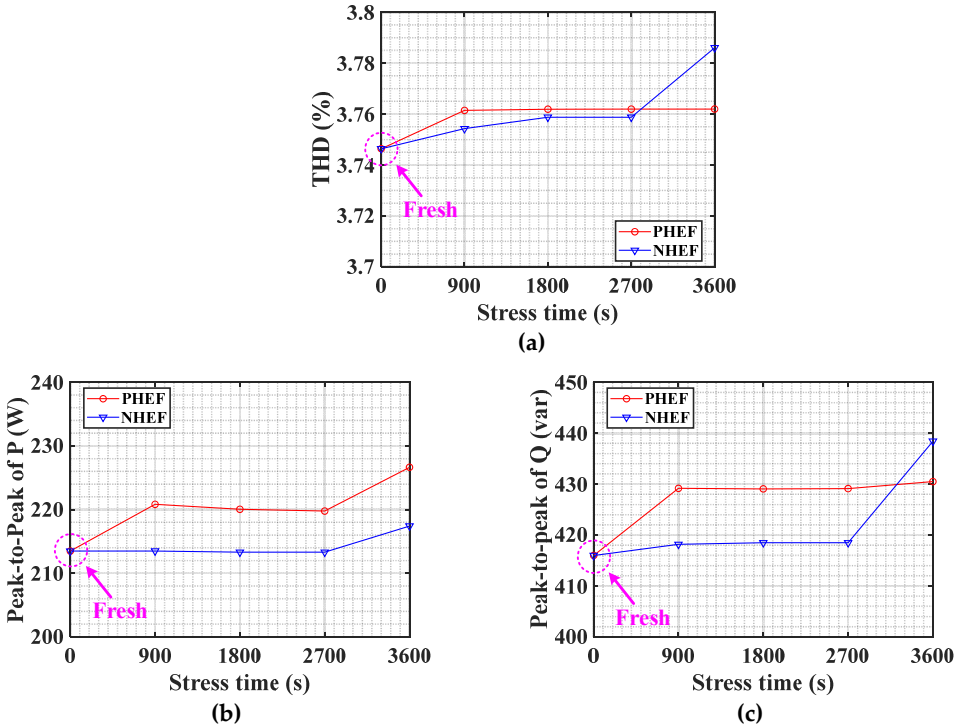
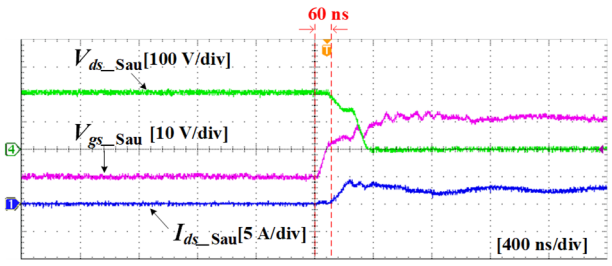


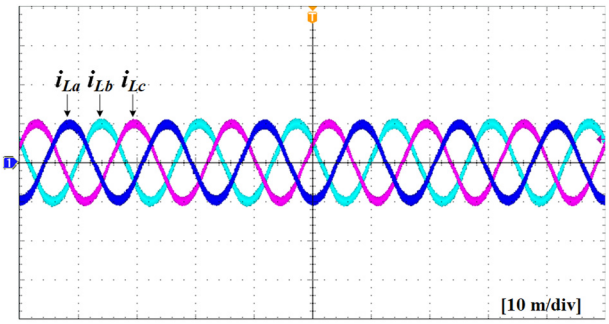
Figure 29. Performance change of voltage source inverter under HEF stress time: (**a**) THD, (**b**) peak-to-peak value of P, and(**c**) peak-to-peak value of Q.

Figure 30 shows experiment waveforms of a three-phase voltage source inverter with RL load. A-phase of the inverter in Figure 30 was composed of SiC MOSFETs aged with PHEF stress. In addition, the remaining phases were composed of fresh SiC MOSFETs. Figure 30a represents the waveforms when the upper switch of a-phase is turned on. In Figure 30a, V_{ds_Sau} means the V_{ds} of the upper switch of a-phase. Furthermore, V_{gs_Sau} represents the V_{gs} of the upper switch of a-phase. Moreover, I_{ds_Sau} is the I_{ds} of the upper switch of a-phase. Figure 30a shows that the turn-on delay of the a-phase upper switch is 60 ns. Figure 30b is the three-phase current waveform of the inverter. In Figure 30b, i_{La}, i_{Lb}, and i_{Lc} represent the a-phase, b-phase, and c-phase inverter currents, respectively. Figure 30b demonstrates that the shape of the waveform hardly changes even when a-phase is aged.Therefore, Figure 30b shows that the aging degree of the inverter cannot be monitored by the load current shape.



(**a**)

Figure 30. *Cont.*



(**b**)

Figure 30. Experiment waveforms of three-phase voltage source inverter with RL load: (**a**) turn-on waveform of aged *a*-phase upper switch, and (**b**) three-phase load current with aged *a*-phase.

6.2. Performance Variation of Current Source Inverter with Duty Error Change Due to Gate Oxide Degradation

This section examines the performance variation of the current source inverter (CSI) according to the duty error change due to the gate oxide degradation. Figure 31 shows a three-phase CSI.

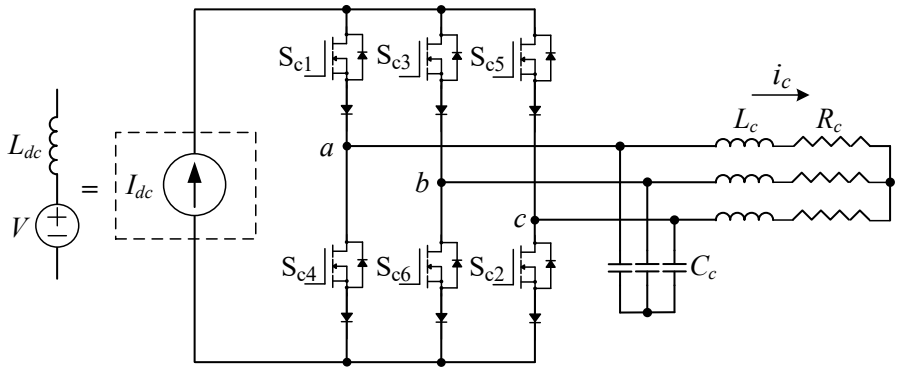


Figure 31. Three-phase CSI.

In Figure 31, S_{c1}, S_{c2}, S_{c3}, S_{c4}, S_{c5}, and S_{c6} represent the switches of the CSI. Additionally, R_c and L_c are the load resistor and inductor, respectively. Moreover, i_c means the output current of the current source inverter. I_{dc} is the input DC current supplied by the current source which can be expressed as a voltage source (V) and an inductor (L_{dc}) connected in series. L_{dc} represents the DC link inductor. C_c is the output capacitor required to drive the current source inverter. The current source inverter is usually controlled by space vector modulation [27].

In the CSI, I_{dc} on the input side must flow without interruption. If the path through which I_{dc} can flow disappears, an overvoltage is induced in L_{dc}. The voltage induced by the variation of I_{dc} is expressed by (20). In (20), V_{Ldc} denotes a voltage induced in L_{dc}. Therefore, in the current source inverter, the overvoltage in L_{dc} is prevented by setting the overlap time when the switching state changes:

$$V_{Ldc} = L_{dc}\frac{dI_{dc}}{dt} \tag{20}$$

Figure 32 represents the gating signals of the CSI in Figure 30.

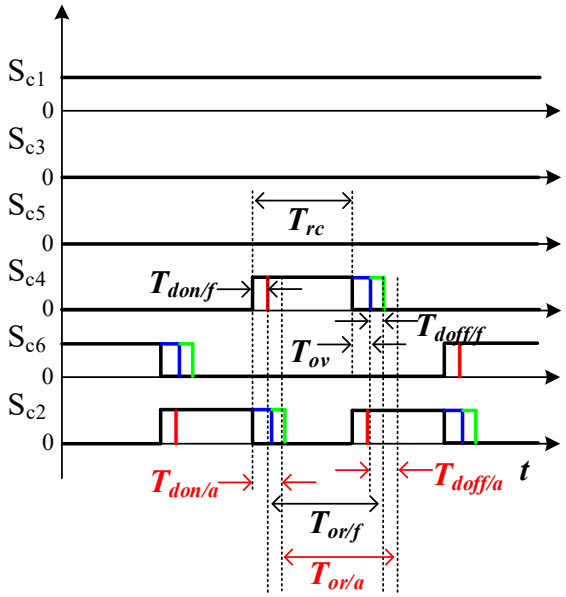


Figure 32. Gating signals of CSI.

In Figure 32, T_{ov} means the overlap-time set in advance when outputting the switching signals. In addition, $T_{or/f}$ means the dwelling time of the switching signal considering T_{ov}, T_{don}, and T_{doff} in the fresh state. Moreover, $T_{or/a}$ represents the dwelling time of the switching signal considering T_{ov}, T_{don}, and T_{doff} in the aged state. T_{rc} indicates the dwelling time of the switching signal under ideal conditions. $T_{or/f}$ and $T_{or/a}$ are calculated through (21):

$$\begin{aligned} T_{or/f} &= T_{rc} + T_{ov} - T_{don/f} + T_{doff/f}, \\ T_{or/a} &= T_{rc} + T_{ov} - T_{don/a} + T_{doff/a} \end{aligned} \tag{21}$$

$T_{don/a}$ and $T_{doff/a}$ in (21) are calculated by (18). From (21), the duty error of the CSI when it is aged can be obtained as (22):

$$D_{ec} = (T_{or/a} - T_{rc})F_{swc} = \left(T_{ov} - T_{don/a} + T_{doff/a}\right)F_{swc} \tag{22}$$

In (22), D_{ec} means the duty error of the CSI according to aging. Moreover, F_{swc} represents the switching frequency of the CSI. Figure 33 shows the duty error of the CSI according to the HEF stress time. As shown in Figure 33, the duty error decreases under PHEF stress and increases under NHEF stress.

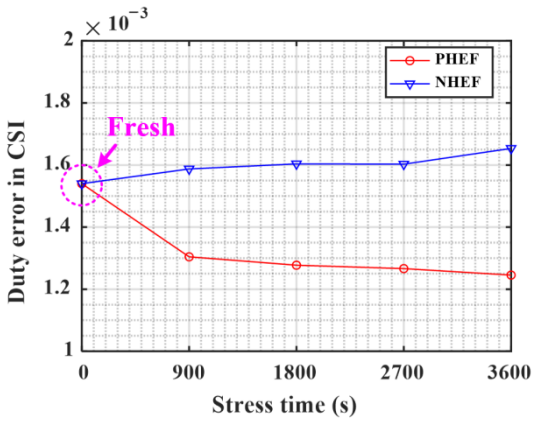


Figure 33. Duty error in CSI according to HEF stress time.

A simulation was conducted to find out the effect of the change in duty error due to the gate oxide degradation on the CSI output current THD. Using the simulation, the THD of the output current of the CSI according to the duty error is examined. The CSI is controlled through space vector modulation, and open-loop control is performed. The parameters of the CSI used in the simulation are shown in Table 5.

Table 5. Parameters of CSI.

Parameters	Value
I_{dc}	10 A
R_c	10 Ω
L_c	1 mH
C_f	20 uF
Switching frequency	5 kHz
T_{ov}	0.3 us
Modulation index	0.2

Figure 34 shows the simulation results of the CSI according to HEF stress. i_{ca}, i_{cb}, and i_{cc} in Figure 34 represent the *a*, *b*, and *c*-phase output currents of the CSI, respectively. Figure 34 demonstrates that simulation results at PHEF stress have the smallest THD of the output current. In addition, the output current quality at NHEF stress is the worst.

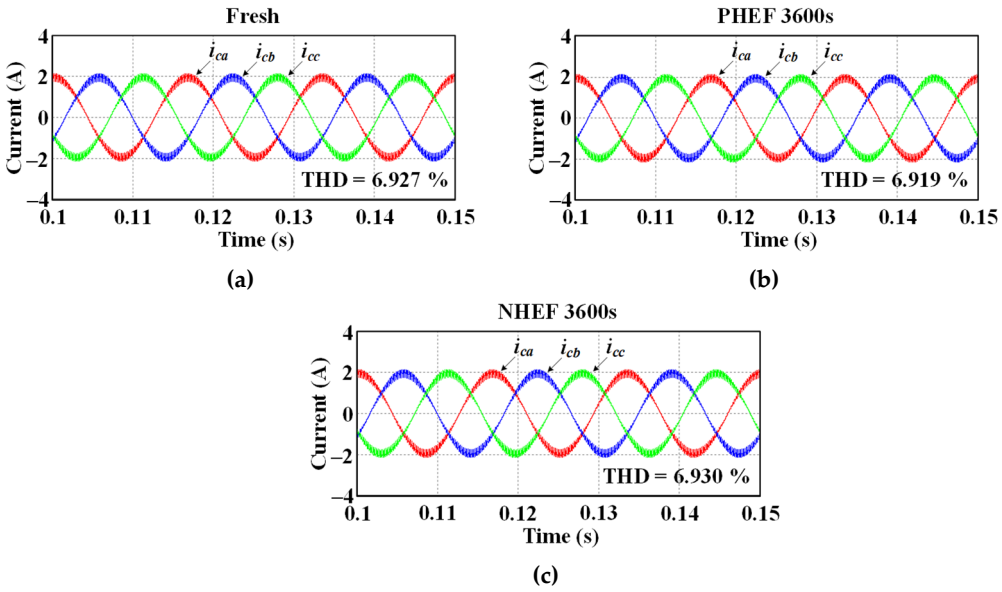


Figure 34. Simulation results of the CSI according to HEF stress: (**a**) fresh condition, (**b**) PHEF stress during 3600 s, and (**c**) NHEF stress during 3600 s.

Figure 35 summarizes the average of the three-phase output current of the CSI according to the stress time. Figure 35 shows that in the case of PHEF stress, where the duty error decreases with the stress time, the THD of the three-phase output current is reduced as the stress time increases. However, in the case of NHEF stress, the THD of the output current slightly increases because the duty error rises with the stress time.

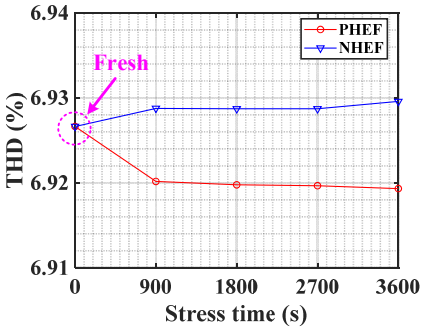


Figure 35. THD of the output current of the CSI according to HEF stress.

7. Conclusions

This paper conducted studies on the changes in T_{don} and T_{doff} of SiC MOSFETs due to the gate oxide degradation. In addition, the performance variations of voltage and current source inverters due to changes in T_{don} and T_{doff} were examined. As a result, it was confirmed that T_{don} and T_{doff} of SiC MOSFETs significantly changed compared to other Si-based devices under the gate oxide degradation. In addition, variations in T_{don} and T_{doff} due to the gate oxide degradation worsened the output performance of the voltage source inverter. Moreover, changes in T_{don} and T_{doff} due to the negative gate oxide degradation reducing V_{th} declined the output performance of the current source inverter. These results indicate that the output performances of the SiC MOSFET-based voltage and current source inverter deteriorate under gate oxide degradation.

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References

1. Zhang, C.; Liu, S.; Li, S.; Ma, Y.; Lu, W.; Huang, J.; Sun, W.; Yang, Z.; Zhu, Y.; Ni, L. Investigation on the Degradation Mechanism for GaN Cascode Device Under Repetitive Hard-Switching Stress. *IEEE Trans. Power Electron.* **2021**, *37*, 6009–6017. [CrossRef]
2. Hazra, S.; Madhusoodhanan, S.; Moghaddam, G.K.; Hatua, K.; Bhattacharya, S. Design considerations and performance evaluation of 1200-V 100-A SiC MOSFET-based two-level voltage source converter. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4257–4268. [CrossRef]
3. Jahns, T.M.; Sarlioglu, B. The incredible shrinking motor drive: Accelerating the transition to integrated motor drives. *IEEE Power Electron. Mag.* **2020**, *7*, 18–27. [CrossRef]
4. Pu, S.; Yang, F.; Vankatalapati, B.T.; Akin, B. Aging mechanisms and accelerated lifetime tests for SiC MOSFETs: An overview. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 1232–1254. [CrossRef]
5. Ugur, E.; Xu, C.; Yang, F.; Pu, S.; Akin, B. A new complete condition monitoring method for SiC power MOSFETs. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1654–1664. [CrossRef]
6. Luo, H.; Iannuzzo, F.; Baker, N.; Blaabjerg, F.; Li, W.; He, X. Study of current density influence on bond wire degradation rate in SiC MOSFET modules. *IEEE J. Emerg. Sel. Topics Power Electron.* **2020**, *8*, 1622–1632. [CrossRef]
7. Baba, S.; Gieraltowski, A.; Jasinski, M.; Blaabjerg, F.; Bahman, A.S.; Zelechowski, M. Active power cycling test bench for SiC power MOSFETs—Principles, design, and implementation. *IEEE Trans. Power Electron.* **2021**, *36*, 2661–2675. [CrossRef]
8. Farhadi, M.; Yang, F.; Pu, S.; Vankayalapati, B.T.; Akin, B. Temperature-independent gate-oxide degradation monitoring of SiC MOSFETs based on junction capacitances. *IEEE Trans. Power Electron.* **2021**, *36*, 8308–8324. [CrossRef]
9. Lelis, A.J.; Habersat, D.; Green, R.; Ogunniyi, A.; Gurfinkel, M.; Suehle, J.; Goldsman, N. Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements. *IEEE Trans. Electron. Devices* **2008**, *55*, 1835–1840. [CrossRef]
10. Xin, J.; Du, M.; Ouyang, Z.; Wei, K. Online monitoring for threshold voltage of SiC MOSFET considering the coupling impact on BTI and junction temperature. *IEEE Trans. Electron. Devices* **2021**, *68*, 1–6. [CrossRef]

11. Aichinger, T.; Rescher, G.; Pobegen, G. Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs. *Microelectron. Rel.* **2018**, *80*, 68–78. [CrossRef]
12. Ye, X.; Chen, C.; Wang, Y.; Zhai, G.; Vachtsevanos, G.J. Online condition monitoring of power MOSFET gate oxide degradation based on miller platform voltage. *IEEE Trans. Power Electron.* **2017**, *32*, 4776–4784. [CrossRef]
13. Jensen, W.R.; Foster, S.N. Online detection of MOSFET gate oxide degradation in a three-phase inverter-drive application. *IEEE Trans. Transp. Electrif.* **2021**, *7*, 50–57. [CrossRef]
14. Yang, L.; Castellazzi, A. High temperature gate-bias and reverse-bias tests on SiC MOSFETs. *Microelecton. Rel.* **2013**, *53*, 1771–1773. [CrossRef]
15. Gonzalez, J.O.; Wu, R.; Jahdi, S.; Alatise, O. Performance and reliability review of 650 V and 900 V silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs. *IEEE Trans. Ind. Electron.* **2020**, *67*, 7375–7385. [CrossRef]
16. Xie, M.; Sun, P.; Wang, K.; Luo, Q.; Du, X. Online Gate-Oxide Degradation Monitoring of Planar SiC MOSFETs Based on Gate Charge Time. *IEEE Trans. Power Electron.* **2022**, *37*, 7333–7343. [CrossRef]
17. Karki, U.; Gonzalez-Santini, N.S.; Peng, F.Z. Effect of gate-oxide degradation on electrical parameters of silicon carbide MOSFETs. *IEEE Trans. Electron. Devices* **2020**, *67*, 2544–2552. [CrossRef]
18. Zhang, L.; Yuan, X.; Zhang, J.; Wu, X.; Zhang, Y.; Wei, C. Modeling and implementation of optimal asymmetric variable dead-time setting for SiC MOSFET-based three-phase two-level inverters. *IEEE Trans. Power Electron.* **2019**, *34*, 11645–11660. [CrossRef]
19. Liu, P.; Wang, Z.; Xu, Y.; Xiao, H.; Li, Y. Optimal overlap-time distribution of space vector modulation for current-source rectifier. *IEEE Trans. Ind. Electron.* **2021**, *68*, 4586–4597. [CrossRef]
20. Karki, U.; Peng, F.Z. Effect of gate oxide degradation on electrical parameters of power MOSFETs. *IEEE Trans. Power Electron.* **2018**, *33*, 10764–10773. [CrossRef]
21. Yang, F.; Pu, S.; Xu, C.; Akin, B. Turn-on delay based real-time junction temperature measurement for SiC MOSFETs with aging compensation. *IEEE Trans. Power Electron.* **2021**, *36*, 1280–1294. [CrossRef]
22. Zhang, Z.; Dyer, J.; Wu, X.; Wang, F.; Costinett, D.; Tolbert, L.M.; Blalock, B.J. Online junction temperature monitoring using intelligent gate drive for SiC power devices. *IEEE Trans. Power Electron.* **2019**, *34*, 7922–7932. [CrossRef]
23. Wen, B.; Boroyevich, D.; Burgos, R.; Mattavelli, P.; Shen, Z. Analysis of D-Q small-signal impedance of grid-tied inverters. *IEEE Trans. Power Electron.* **2016**, *31*, 675–687. [CrossRef]
24. Wu, B.; Narimani, M. *High-Power Converters and AC Drives*; IEEE Press: Piscataway, NJ, USA, 2006.
25. Blasko, V. Analysis of a hybrid PWM based on modified space-vector and triangle-comparison method. *IEEE Trans. Ind. Appl.* **1997**, *33*, 756–764. [CrossRef]
26. Shen, Z.; Jiang, D. Dead-time effect compensation method based on current ripple prediction for voltage-source inverters. *IEEE Trans. Power Electron.* **2019**, *34*, 971–983. [CrossRef]
27. Kim, J.; Kwak, S. Direct power control method with minimum reactive power reference for three-phase AC-to-DC matrix rectifiers using space vector modulation. *IEEE Access* **2019**, *7*, 67515–67525. [CrossRef]