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A Ku-Band Bi-Directional Transmit and Receive IC in 0.13 μm CMOS Technology

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Abstract: This paper presents a Ku-band transmit and receive IC in 0.13 μm CMOS technology for mobile satellite communication beamforming systems. A Ku-band transmit and receive IC is composed of a bi-directional amplifier, a 6-bit phase shifter, and a 6-bit digital step attenuator. The precise trimming bits are implemented in the phase shifter (2.8°) and digital step attenuator (0.5 and 1 dB) for the amplitude and phase error correction. The phase variation range of the phase shifter is 360° with a phase resolution of 5.625°. The attenuation range of 31.5 dB with an amplitude resolution of 0.5 dB is achieved. The gain of 2~5 dB and the input/output return losses of >10 dB are achieved from 12 to 16 GHz. The chip size is 2.5 × 1.5 mm^2 including bonding pads. The DC power consumption is 216 mW.

Keywords: Ku-band transmit and receive IC; phased array antenna; CMOS

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1. Introduction

A Ku-band transmit and receive IC is one of the key components in active phased array antennas for Ku-band satellite communications [1,2]. The silicon technology in phased array antennas is receiving attention because it allows for low size, weight, power, and cost (SWAP-C) implementation [3]. Separate phase shifters and gain control circuits for transmit and receive operations are typically used to implement the transmit and receive IC for the phased array antenna [4]. However, it occupies a large chip area and results in high manufacturing costs. The chip size can be decreased significantly using bi-directional topology, sharing the Tx and Rx chains with phase shifters and attenuators [5–7]. One disadvantage of the bi-directional topology is that it results in an additional loss of two SPDT switches. A Ku-band transmit and receive IC is composed of a switchless bi-directional amplifier to reduce the losses caused by two SPDT switches. The previous paper composed each test circuit for a phased array antenna in the X band to verify the proposed topology [5–7]. Many research groups have already published phase shifters with various circuit topologies [8–12]. The vector sum or the switched filter phase shifter circuit topologies are popularly used. A compact size with decent gain, precise phase control, and wide bandwidth can be achieved in the vector sum phase shifter. However, it has relatively poor linearity and only operates unidirectionally. It also consumes DC current, whereas the switched filter phase shifter can provide high linearity with nearly zero DC power consumption. It operates bidirectionally due to the passive circuit. The digital step attenuator is necessary to control the antenna sidelobe level. The amplitude errors among the elements in the phased array antenna can be compensated.

In this paper, a transmit and receive IC for a Ku-band phased array antenna is presented with 0.13 μm CMOS technology.

2. Design of Ku-Band Bi-Directional Transmit and Receive IC

Figure 1 shows a block diagram of a Ku-band bi-directional CMOS transmit and receive IC. The transmit and receive IC is composed of a bi-directional amplifier, a 6-bit phase shifter, and a 6-bit digital step attenuator. The phase shifter and attenuator are composed of DPDT switches. Since the series transistors in the switches determine the insertion losses of the phase shifter or the attenuator, the number of the cascaded series transistors should be reduced. The phase shifter or the attenuator with DPDT switches can reduce the number of the series transistors compared to the control circuits only with SPDT switches, which results in improving the insertion loss. In this design, the phase shifter and the attenuator are split with bi-directional amplifiers to improve linearity. A serial peripheral interface (SPI) is implemented to control the state registers of the phase and attenuation, and a low dropout (LDO) voltage regulator is also integrated to provide the stable DC bias.

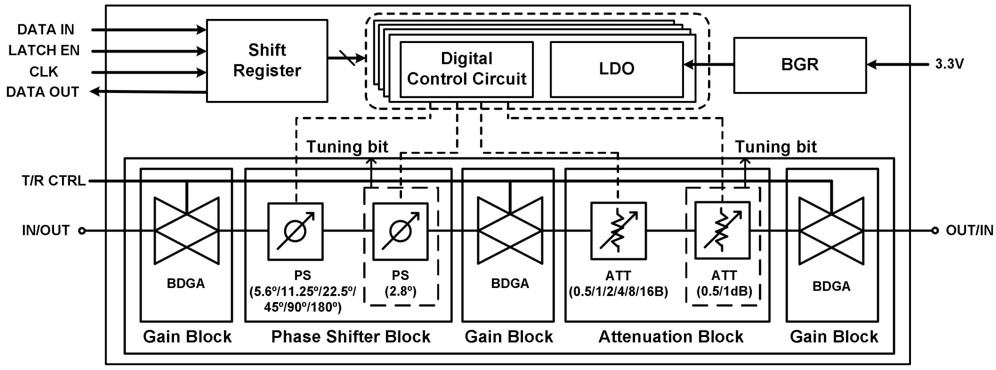


Figure 1. Block diagram of the Ku-band CMOS transmit and receive IC.

2.1. Ku-Band 6-Bit Phase Shifter

Figure 2 shows the circuit block diagram of a Ku-band 6-bit phase shifter with DPDT switches. The DPDT switch with a series–shunt circuit is designed to provide high port-to-port isolation. Figure 3 shows the schematic of the SPDT and DPDT switches. The DPDT switch is implemented with four 16-finger 64 µm series transistors (T_1–T_4) and four 8-finger 40 µm shunt transistors (T_5–T_8). The series inductors (L_1) of 260 pH improve the input and the output return losses. The filter type phase shifting circuits are implemented in Figure 4. In the 11.25° and 22.5° phase states, BPF and LPF networks are used. Since a large shunt inductance is necessary to implement 11.25° and 22.5° phase states, the BPF with small series inductance is used to reduce the chip size. In the 45° and 90° phase states, HPF and LPF networks are used. To provide the wideband operation, two stages of HPF and LPF networks are used in the180° phase state. Table 1 summarizes the design parameters of the switched filter phase shifter. The 5.625° phase state and the 2.8° phase tuning bit are implemented with the switched LPF in Figure 5. The body floating technique is used in the switches to reduce the silicon substrate leakage. Vertically stacked spiral inductors are used to reduce the chip size. All the passive devices such as inductors, MIM capacitors, and interconnection lines were designed using the electromagnetic simulator.

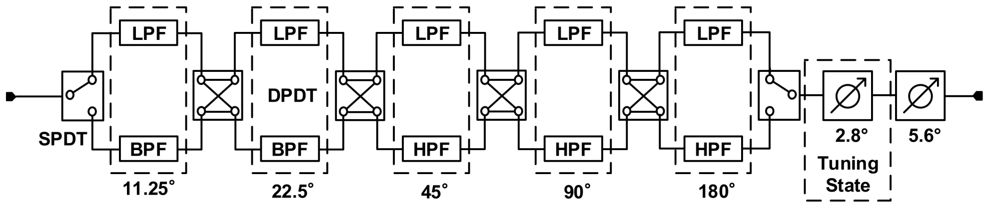
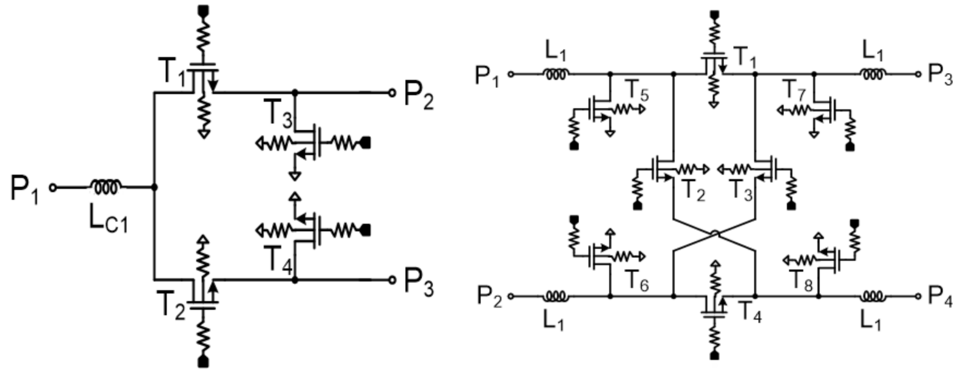
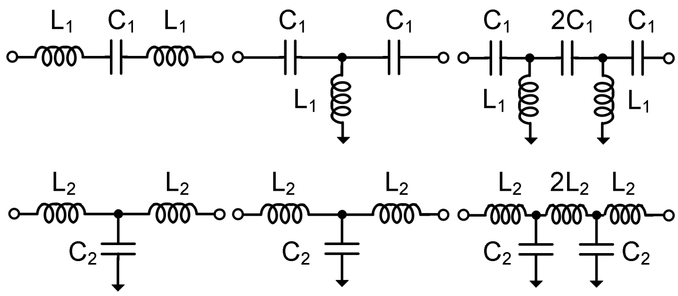


Figure 2. Block diagram of the Ku-band 6-bit phase shifter.



(a) (b)

Figure 3. Schematics of (**a**) the SPDT switch, and (**b**) the DPDT switch.



(**a**) (**b**) (**c**)

Figure 4. Schematics of the phase shifting elements of (**a**) 11.25° and 22.5°, (**b**) 45° and 90°, (**c**) 180°.

Table 1. Design parameters of the phase shifting filter networks.

Parameter		11.25°	22.5°	45°	90°	180°
HPF (BPF)	L_1 (pH)	177	221	1420	898	915
	C_2 (pF)	1.2	0.57	2.1	0.62	0.62
LPF	L_2 (pH)	156	229	176	287	287
	C_2 (fF)	74	118	102	146	146

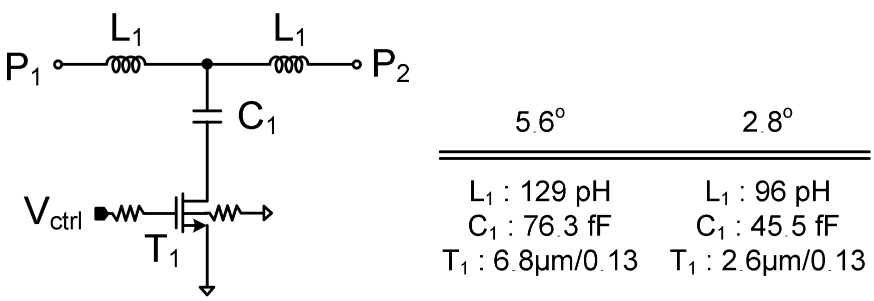


Figure 5. Schematic of the phase shifting elements of 5.6° and 2.8°.

2.2. Ku-Band 6-Bit Digital Step Attenuator

The block diagram of the Ku-band 6-bit digital step attenuator is shown in Figure 6. The attenuator is designed with T-type resistive networks. The attenuation steps of 2, 4, 8, and 16 dB are controlled by steering the signal paths between the reference paths and the T-shape resistive network path using the DPDT switches. The 0.5 and 1 dB attenuation states are designed with a switched shunt resistor to reduce the insertion loss and chip size. Additionally, the 0.5 and 1 dB attenuation states are designed as tuning bits to compensate for the amplitude error. The attenuation variation range is 31.5 dB with an attenuation resolution of 0.5 dB.

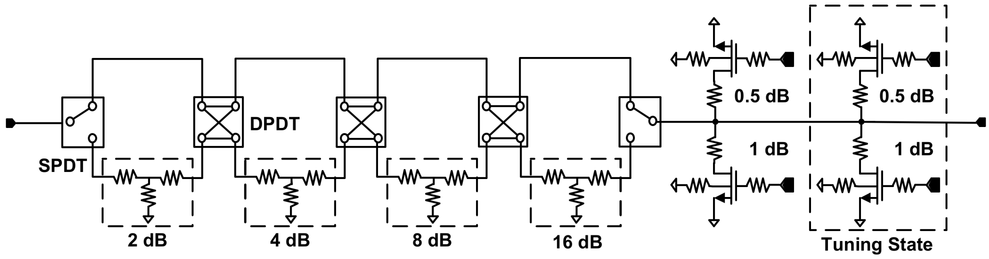


Figure 6. Block diagram of the Ku-band 6-bit digital step attenuator.

2.3. Switchless Bi-Directional Amplifier

The bi-directional amplifier in the transmit and receive IC for the phased array antenna is generally implemented with two SPDT switches, an LNA, and a PA. Two SPDT switches for the bi-directional operation result in an additional loss and a larger chip size. Figure 7 shows the schematic of the proposed bi-directional amplifier. The switchless bi-directional amplifier is composed of a paired two-stage distributed cascode amplifier. Since the transmit and receive switching operation is provided by switching the cascode transistors in the proposed amplifier, the small size can be achieved by removing the two transmit and receive SPDT switches. In the receive operation from P_1 to P_2, the transistors of M1/M5 and M2/M6 are in ON states and the transistors of M3/M7 and M4/M8 are in OFF states. Therefore, it works equivalently as a distributed amplifier. The transmit operation is vice versa. Generally, the insertion losses in the control circuits have a negative slope versus the frequencies, and so the amplifier is designed to have a positive gain slope. Flat overall gain performance can be achieved in the Ku-band transmit and receive IC. The symmetric layout was performed for identical operational characteristics in the transmit and receive operation modes.

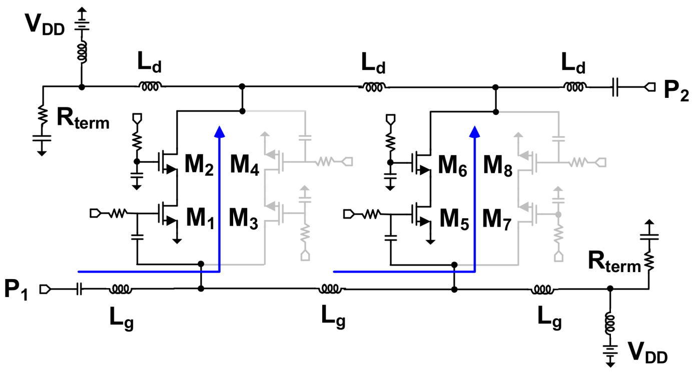


Figure 7. Schematic of the switchless bi-directional amplifier (operation mode: P_1->P_2).

3. Experiment Results

The Ku-band transmit and receive IC is fabricated in 0.13 µm CMOS technology and the chip size is 2.5 × 1.5 mm^2 including bonding pads. The microphotograph of the Ku-band CMOS transmit and receive IC is shown in Figure 8. The measurement setup of the Ku-band CMOS transmit and receive IC is shown in Figure 9. The S-parameter measurement is performed using a PNA-X network analyzer. The short, open, load, and thru (SOLT) calibration was performed with the on-wafer probe station. The power characteristics are measured with the signal source and the spectrum analyzer. Figure 10 shows the measured gain of the reference state. The gain is 2~5 dB at 12–16 GHz. The input and output return losses are >10 dB at 12–16 GHz as shown in Figure 11. Figure 12 shows the measured phase characteristics in all phase states. A phase variation range of 360° with a phase resolution of 5.625° is achieved. Figure 13 shows the measured attenuation characteristics in all attenuation states, and an attenuation range of 31.5 dB with an attenuation resolution of 0.5 dB is achieved at 12–16 GHz. As shown in Figure 14, the measured root mean square amplitude error is <0.3 dB and the root mean square phase error is <4° at 12–16 GHz when varying the phase states. Figure 15 shows that the measured root mean square amplitude error is <0.4 dB and the root mean square phase error is <3° at 12–16 GHz when varying the attenuator states. Figure 16 shows the measured power characteristics. The saturated output power is ~2 dBm at 14 GHz. A performance comparison of the previously published silicon-based transmit and receive ICs is summarized in Table 2.

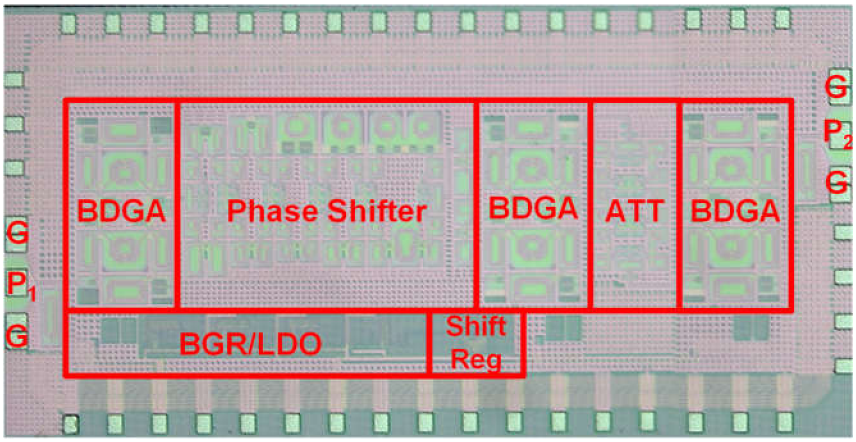


Figure 8. Microphotograph of the Ku-band CMOS transmit and receive IC.

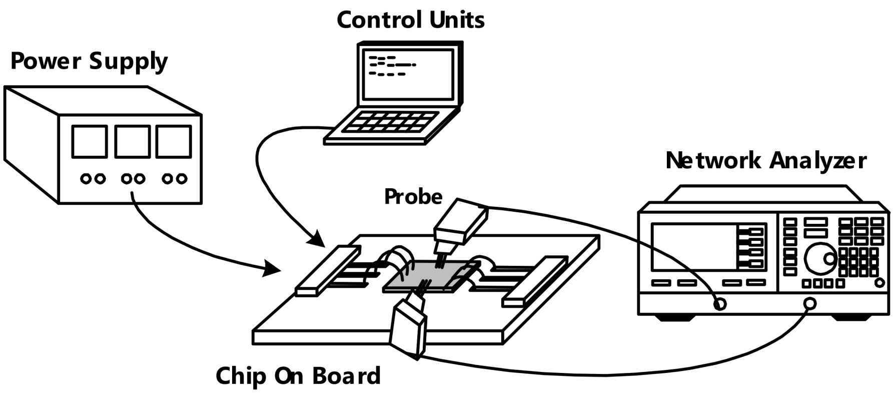


Figure 9. Measurement setup of the Ku-band CMOS transmit and receive IC.

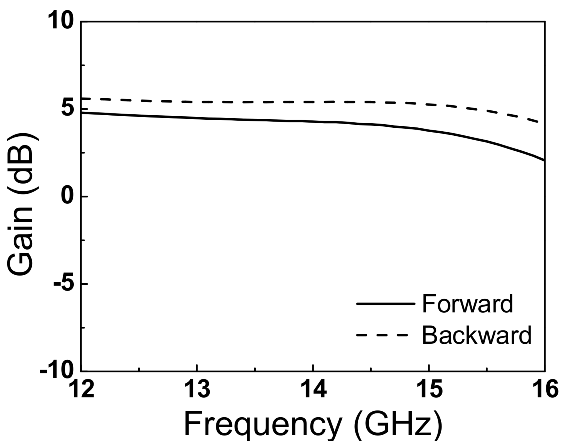


Figure 10. Measured gain of the Ku-band CMOS transmit and receive IC.

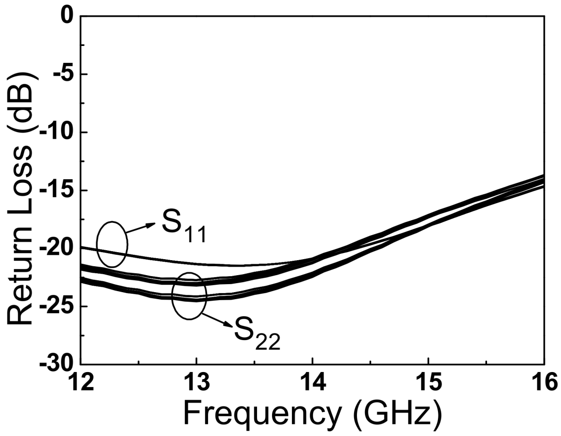


Figure 11. Measured return losses of the Ku-band CMOS transmit and receive IC.

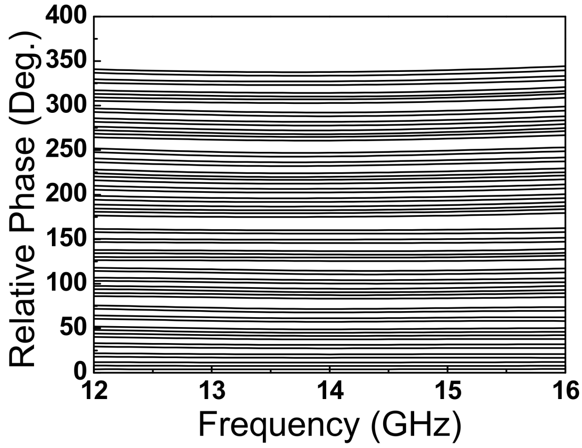


Figure 12. Measured phase characteristics of the Ku-band CMOS transmit and receive.

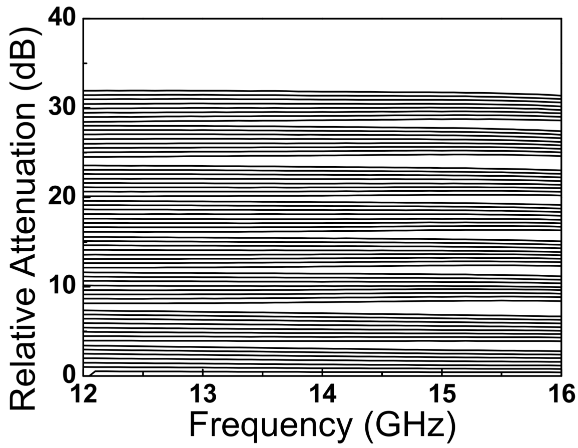


Figure 13. Measured attenuation characteristics of the Ku-band CMOS transmit and receive.

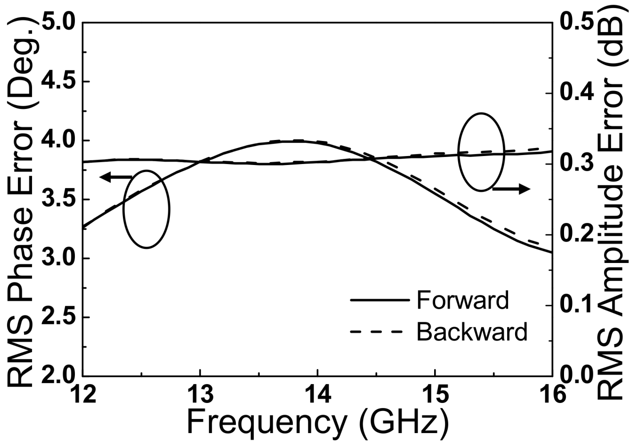


Figure 14. Measured root mean square phase and amplitude errors of the phase shifter.

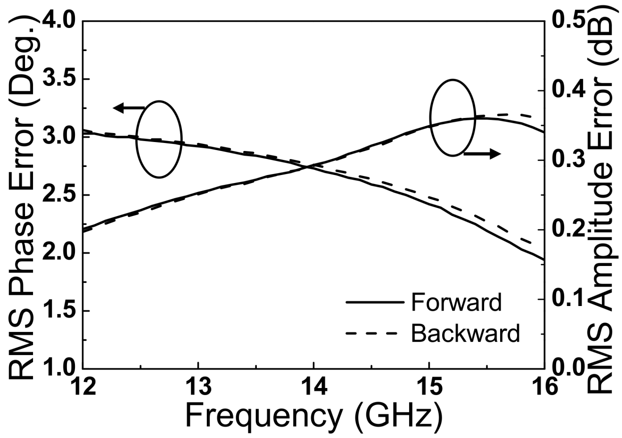


Figure 15. Measured RMS phase and amplitude errors of the attenuator.

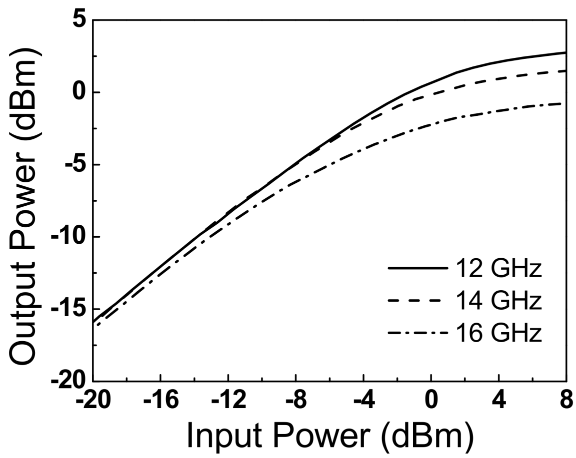


Figure 16. Measured output power of the Ku-band CMOS transmit and receive IC in Tx operation.

Table 2. Performance comparison of the relevant silicon-based transmit and receive IC.

Reference	[4]	[6]	[7]	This Work
Frequency (GHz)	8–16	8–10.5	8–10.5	12–16
Technology	SiGe 0.18 µm	CMOS 0.13 µm	CMOS 65 nm	CMOS 0.13 µm
Rx/Tx Gain (dB)	10~16/15~21	3.5/3.5	3.7/3.7	2~5/2~5
Phase shifter range/step (Deg.)	360/2.8	360/5.625	360/5.625	360/5.625
Gain control range/step (dB)	31/0.5	31.5/1	31.5/0.5	31.5/0.5
RMS Phase Error (Deg.)	2.8	4.3	4	4
RMS Phase Error (Deg.)	0.3	0.3	0.5	0.5
Psat (dBm)	13	9.5	10	2 @ 14 GHz
Rx/Tx Power consumption (mW)	215/280	150/150	170/170	216/216
Chip size (mm^2)	16	1.19	9.56	3.75

4. Conclusions

This paper presents a Ku-band CMOS transmit and receive IC in 0.13 µm CMOS technology, which is the key part of the phased array antenna for mobile satellite communication beamforming systems. It is proposed to enable the bi-directional amplifier without switches to compensate for the gain, phase shifting for beam steering, and attenuating for weighting technique to reduce the side lobe level. The maximum phase shift range of 360° with a phase resolution of 5.625° and the maximum attenuation range of 31.5 dB with an attenuation resolution of 0.5 dB is achieved. The measured gain is 2~5 dB and the input and output return losses are >10 dB at 12–16 GHz. The saturated output power is −2 dBm at 14 GHz. The chip size is 2.5 × 1.5 mm^2 including bonding pads. The total power consumption is 216 mW. The proposed Ku-band CMOS transmit and receive IC will enable the low SWAP-C Ku-band satellite communication and radar system.

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