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Injection-Locked Frequency Divider Topology and Design Techniques for Wide Locking-Range and High-Order Division

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ABSTRACT An injection-locked frequency divider topology for wide locking-range and high-order division is presented. Based on the theoretical analysis of the locking-range and injection locking characteristic, we propose locking-range enhancement techniques and high-order dividing topology. Fabricated in a 0.18-μm BiCMOS process, three test circuits are designed with only a standard CMOS, aiming at input frequency ranges of 7.8, 11.1, and 11.7 GHz. The 7.8-GHz divide-by-2 ILFD consumes 2.9 mW with a locking range of 692 MHz operated from a 1.5 V supply. The optimized dual injection method improves the locking range by a factor of 10. The 11.1-GHz divide-by-3 ILFD employs an even-harmonic phase tuning technique and the proposed technique improves the locking range by 25%. The core of the 11.1-GHz ILFD consumes 6.15 mW from a 1.8 V supply. For the 11.7-GHz divide-by-3 ILFD, a self-injection technique is proposed that utilizes harmonic conversion and self-injection to improve phase-noise, locking-range, and input sensitivity simultaneously. By employing harmonic tuning and self-injection, odd-order division is enabled with 47.8% enhancement in the locking-range and 15.7-dBc/Hz reduction in phase noise.

INDEX TERMS Injection-locking, frequency divider, self-injection, locking-range, phase noise, sensitivity.

I. INTRODUCTION

Frequency divider is an essential building block in wireless and wireline communications such as frequency synthesis, local oscillator signal generation, and quadrature signal generation. Several types of frequency dividers have been presented in the literature and they can be largely categorized into the digital divider, regenerative divider, and injection-locked frequency divider (ILFD). The digital divider is based on the flip-flop logic circuits, and has the disadvantages of high power consumption due to the complete charging and discharging of capacitances during each cycle [1]. While the regenerative divider is capable of high frequency operation, it has a relatively high power consumption. ILFD offers low power consumption due to the tuned nature of its circuits, its locking-range (operating BW) is narrow, hindering its widespread use.

The conventional ILFD based on the tail injection and the direct injection is illustrated in Fig. 1. ILFD based on the tail injection shown in Fig. 1(a) suffers from low injection efficiency due to the large input capacitance of the current source transistor [1], [2]. To improve the injection efficiency as well as the input locking-range, the direct injection method is proposed as shown in Fig. 1(b) [3], [4].

Several attempts have been made to improve the locking range even further [4]–[6] including voltage injection, current injection, or both. These efforts strive to increase the injection efficiency, subsequently enhancing the locking range.

The division ratio of the conventional ILFD is favorable for the even-order injection-locking due to the circuit implementation. The mixing operation with conventional ILFD topologies is dependent on the cross-coupled differential pair and metal-oxide semiconductor (MOS) transistor switch over the out-of-phase differential nodes for the tail injection method and direct injection method, respectively. The mixing function with these mechanisms has an odd symmetry and thus it only generates odd-order mixing products corresponding to the even frequency division ratios [7]. Series injection and parallel injection

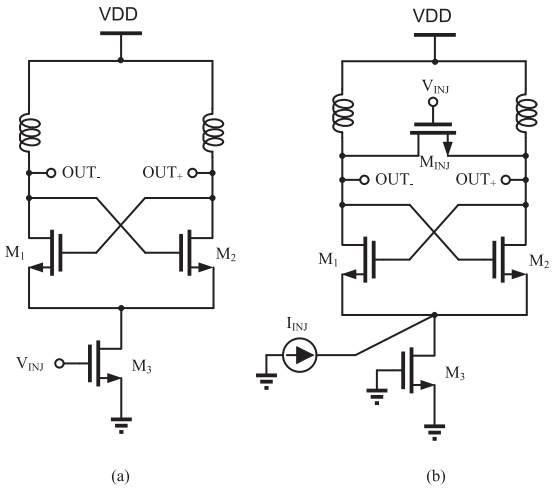

FIGURE 1. Conventional ILFD: (a) tail injection method. (b) direct injection method.

have been developed to enable an odd-order division ratio, typically divide-by-3 [7], [8]. The series injection method relies on stacked transistors and is therefore not favorable for low supply operation. Parallel injection, on the other hand, needs extra DC current, jeopardizing the power efficiency.

In this paper, we present ILFD topologies with locking range enhancement techniques and high-order division ratios. The dependence of the Quality factor (Q), i_{OSC}, and i_{INJ} on the active-device bias condition is utilized to improve the locking range. The phase tuning method for even-harmonics is proposed to enable divide-by-3 operation with enhanced locking-range. The self-injection technique along with an odd-to-even mode harmonic converter is employed for simultaneous improvement of the locking range, phase noise, and input sensitivity.

This paper is organized as follows. Section II describes the proposed techniques to improve the injection locking-range and to enable odd-order division. Design and implementation details are given in Section III. Section IV provides the measurement results of three ILFD designs employing the techniques illustrated in Section II. Concluding remarks are given in Section V.

II. PROPOSED TECHNIQUES

Fig. 2 shows the block diagram and phase relationship of the ILFD. Based on the block diagram shown in Fig. 2(a), the i_{INJ} component at the frequency ω_{INJ} (radian/s) is mixed with Nth harmonics of the output signal (i_{OSC}). Only the components at the vicinity of the bandpass filter (BPF) center frequency remain, and remaining components are thus suppressed by the selectivity of BPF. Assuming the BPF is centered at the difference frequency of i_{INJ} and the Nth harmonic of i_{OSC}, the operating condition of the ILFD can be expressed as

$$\omega_o = \omega_{INJ} - N \cdot \omega_o \Rightarrow \omega_o = \frac{\omega_{INJ}}{N+1}. \quad (1)$$

Since the Nth harmonic component is generated from either the non-linearity of the device or the conversion gain

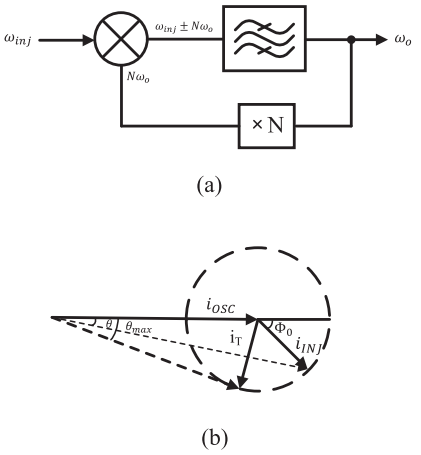

FIGURE 2. (a) Block diagram of harmonic ILFD. (b) phase diagram of injection-locked oscillator/divider.

of the square-wave mixing operation, the Nth harmonic component weakens as N increases. Although not shown in Fig. 2(a), injection efficiency is also limited due to the various parasitic components through the injection path. The locking-range is then limited further as the operating frequency of ILFD increases.

A. DUAL-INJECTION METHOD WITH OPTIMIZED Q AND i_{OSC}

The locking range of ILFD was derived analytically in [9]–[11] and can be expressed as

$$\omega_L = \omega_o - \omega_{inj} = \frac{\omega_o}{2Q} \cdot \frac{i_{INJ}}{\sqrt{i_{OSC}^2 - i_{INJ}^2}} = \frac{\omega_o}{2Q} \cdot \frac{i_{INJ}}{i_T}. \quad (2)$$

Deduced from Eq. (2), the locking range of ILFD can be increased by minimizing Q of the LC tank, minimizing i_T, and maximizing the injection current (i_{INJ}), assuming $i_{OSC} \gg i_{INJ}$.

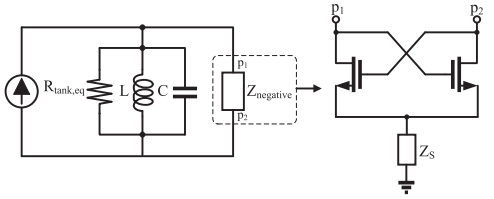

FIGURE 3. Equivalent circuit of the resonator with negative resistance due to cross-coupled transistors.

Fig. 3 shows the equivalent circuit of the resonator circuit with the negative resistance due to the cross-coupled differential pair. The cross-coupled differential pair provides negative resistance ($-2/g_m$) and can compensate for the energy loss component of the LC tank. Although the negative resistance model due to the cross-coupled differential pair is sufficient to predict the oscillation frequency and condition of the oscillator, it can be shown that equivalent impedance at high frequency is not simply $-2/g_m$, but is $-2/g_m - 2Z_s$ due to the shunted capacitive parasitics (C_P) at the common-source

node [12]. The parasitic capacitor at the common-source node is converted to a negative capacitor, effectively becoming an inductor. Equivalent inductance and its quality factor due to the cross-coupled pair is analytically derived as [12]

$$L_E = \frac{1}{C_P\omega_o^2},\ Q_E = \frac{g_m^2}{4C_P^2\omega_o^2}. \tag{3}$$

This impedance transformation behavior affects the loaded quality factor (Q_L) of the ILFD from the following relationship [13].

$$\frac{1}{Q_L} = \frac{1}{Q_E} + \frac{1}{Q}. \tag{4}$$

Then, the loaded quality factor of the ILFD which is dependent on the bias condition can be utilized to adjust the loaded quality factor and locking-range accordingly.

In our work, the loaded quality factor is adjusted by tuning the supply level (V_{DD}). The detrimental effect on the phase noise due to the reduced supply is not significant in ILFD since phase noise is largely dependent on the phase noise of the injection source. The external quality factor (Q_E) with the supply dependency can be expressed as

$$Q_E = \frac{g_m^2}{4C_P^2\omega_o^2} = \frac{\left[\mu C_{ox}\left(\frac{V_{DD}}{2} - V_{th}\right)\right]^2}{4C_P^2\omega_o^2}. \tag{5}$$

The gate-source voltage (V_{GS}) of the cross coupled pair is assumed to be set at $V_{DD}/2$ with the complementary MOS (CMOS) implementation of the ILFD core (see Fig. 6).

B. EVEN HARMONIC PHASE TUNING

Based on the locking-range of ILFD shown in Eq. (2), in most of the locking-range enhancement efforts in the literature, attempts were made to improve the injection efficiency and the locking-range accordingly. To the best of our knowledge, no efforts have been made to alter the phase relationship between i_{INJ} and i_{OSC}.

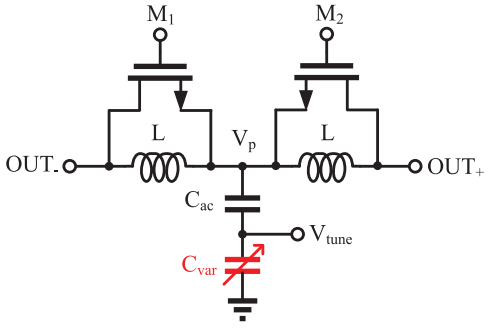

FIGURE 4. Phase tuner with T-network.

We employ the phase tuner to align the phase towards an optimized angle for the locking-range when the resultant current (i_T) and i_{INJ} are orthogonal manifested from the phase diagram of the ILFD shown in Fig. 2(b). Fig. 4 shows the phase tuner that is utilized in our work. Phase tuner configured in the T-network along with the differential injection effectively functions as an odd-to-even harmonic converter, the detailed explanation of which is given in Section II-C. Assuming $C_{ac} \gg C_{var}$, the ABCD matrix for the network in Fig. 4 can be written as

$$\begin{bmatrix} 1 - LC_{var}\omega^2 & j\omega L\left(1 - LC_{var}\omega^2\right) + j\omega L \\ j\omega C_{var} & 1 - LC_{var}\omega^2 \end{bmatrix}. \tag{6}$$

The equivalent ABCD matrix for a transmission line of characteristic impedance Z_o and phase shift ϕ is as follows [13]

$$\begin{bmatrix} cos\phi & jZ_o sin\phi \\ jY_o sin\phi & cos\phi \end{bmatrix}. \tag{7}$$

If we equate the two matrices, we can derive the phase of the tuner as

$$\phi = \frac{1}{2} sin^{-1}\left(C\omega Z_o\right). \tag{8}$$

Eq. (8) shows that the varactor capacitance is utilized to alter the phase of T-network and then improve the locking-range accordingly.

C. SELF-INJECTION WITH ODD-TO-EVEN HARMONIC CONVERTER

The conventional ILFD topology shown in Fig. 1 is suitable for an even-order division ratio (most prevalently divide-by-2) due to the odd symmetry of the cross-coupled differential pair. Several efforts have been made to develop a divide-by-3 ILFD [7], [14]–[16]. However, all of the previous approaches utilized the spurious harmonic components in the mixing process and they exhibited an even smaller locking-range than the divide-by-2 ILFD.

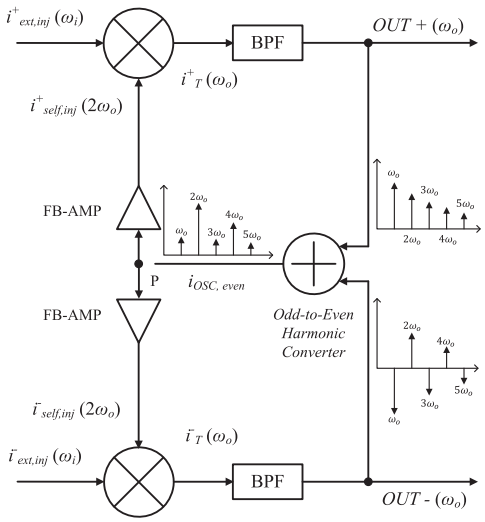

FIGURE 5. Block diagram of the divide-by-3 ILFD utilizing self-injection with odd-to-even harmonic converter.

Fig. 5 shows the block diagram of the divide-by-3 with self-injection and an odd-to-even harmonic converter. The odd-to-even harmonic converter is the same as the T-network with differential injection shown in Fig. 4. Instead of the

varactor, fixed capacitance is used for the T-network. The two differential output signals with identical amplitude and frequency but with the phase difference of 180 degrees, can be represented in phasor as [17]

$$V_{out+}(t) = a_1 e^{j\omega_o t} + a_2 e^{j2\omega_o t} + a_3 e^{j3\omega_o t} + \cdots . \quad (9)$$

$$V_{out-}(t) = a_1 e^{j(\omega_o t+\pi)} + a_2 e^{j(2\omega_o t+\pi)} + a_3 e^{j(3\omega_o t+\pi)} + \cdots . \quad (10)$$

The signal at the common-node (V_p) can then be expressed as

$$V_p(t) = 2a_2 e^{j2\omega_o t} + 2a_4 e^{j4\omega_o t} + \cdots . \quad (11)$$

Only even order harmonics remain and the tuned amplifier at $2 \cdot \omega_o$ amplifies only the 2nd order terms to enable divide-by-3 operation. Due to the BPF action of the LC resonator, only the difference of the external injection signal at $3 \cdot \omega_o$ and self-injected signal at $2 \cdot \omega_o$ survives and injection-locking at undesired harmonics is prevented.

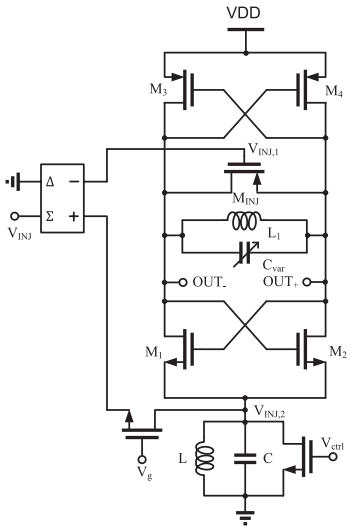

FIGURE 6. Schematic of the 7.8-GHz divide-by-2 ILFD.

III. CIRCUIT DESIGNS

Three ILFDs are realized in a 0.18-μm BiCMOS process to prove the validity of the proposed techniques described in Section II. Fig. 6 shows the 7.8-GHz divide-by-2 ILFD employing dual injection with optimized Q and i_{OSC}. A quadrature hybrid off-chip is used to generate two out-of-phase injection signals ($V_{INJ,1}$, $V_{INJ,2}$). Injection through a MOS switch (M_{INJ}) similar to the injection described in [4] is effectively a voltage direct injection, whose effective current is $i_{INJ,1}$.

Additional injection ($i_{INJ,2}$) applied to the common-source of the NMOS cross-coupled pair is in the current domain and is then added to the output current ($i_{INJ,1} + i_{OSC}$). The LC tank at the common-source of the NMOS cross-coupled pair is resonating at twice the resonance frequency of the LC tank at the output of ILFD. Due to the dual injection approach,

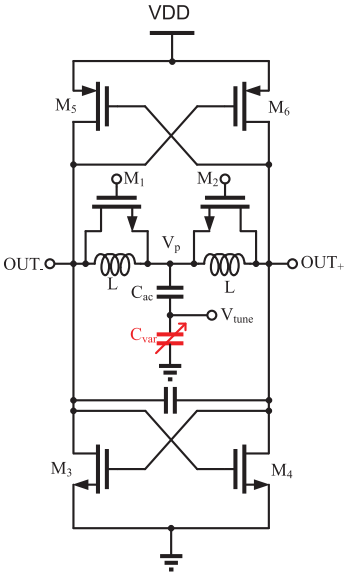

FIGURE 7. Schematic of the 11.1-GHz divide-by-3 ILFD.

the locking-range of the proposed ILFD is expressed as

$$\omega_L = \omega_o - \omega_{inj} \approx \frac{\omega_o}{2Q_L} \cdot \frac{i_{INJ,1} + i_{INJ,2}}{i_{OSC}}, \quad (12)$$

where Q_L is the loaded quality factor given in Eq. (4).

Divide-by-3 ILFD with phase tuner is shown in Fig. 7. Similar to Fig. 6, the proposed divide-by-3 employs CMOS implementation with better current efficiency and pseudo-differential architecture supporting low supply. The proposed phase tuner in this design functions as an odd-to-even harmonic converter for the divide-by-3 operation and the phase tuner in order to rotate i_{INJ} towards the maximum locking-range.

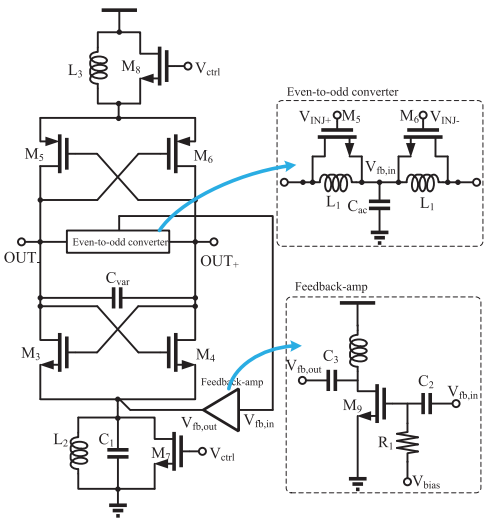

FIGURE 8. Schematic of the 11.7-GHz divide-by-3 ILFD.

Another divide-by-3 ILFD in Fig. 8 aiming at 11.7-GHz input frequency employs the T-network for odd-to-even harmonic conversion and self-injection technique to improve

locking-range, phase noise, and input sensitivity. An external signal at $3 \cdot \omega_o$ is applied using the direct injection method with MOS resistor switch (M_5, M_6). Odd-to-even harmonic conversion through the T-network emphasizes the second harmonics of the differential output signals. The second-harmonic component is further amplified through the feedback amplifier, of which the feedback signal is modulated by the power supply. We employ CMOS implementation for a differential cross-coupled pair. The LC tank resonates at $2 \cdot \omega_o$ to provide high impedance to the differential pair functioning as a current source at the desired frequency range.

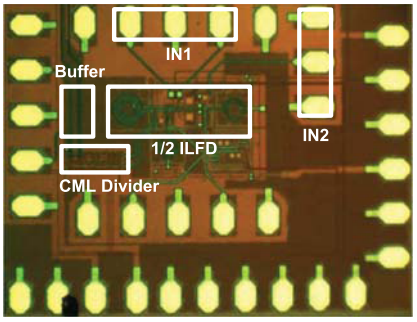

FIGURE 9. 7.8GHz divide-by-2 ILFD test chip photograph.

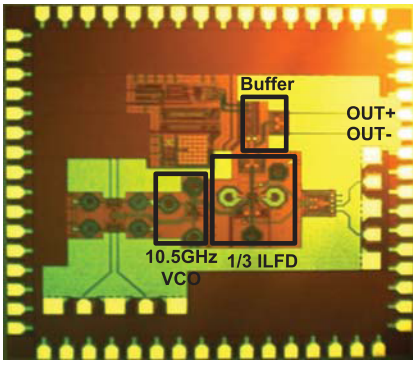

FIGURE 10. 11.1GHz divide-by-3 ILFD test chip photograph.

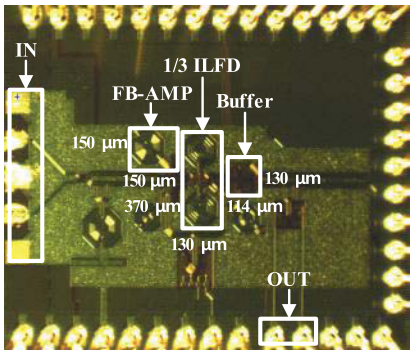

FIGURE 11. 11.7GHz divide-by-3 ILFD test chip photograph.

IV. MEASUREMENT RESULTS

The proposed ILFD topologies are realized in the Jazz 0.18-μm BiCMOS process and the photographs of three test chips are shown in Fig. 9, 10, 11. The core size of each ILFD

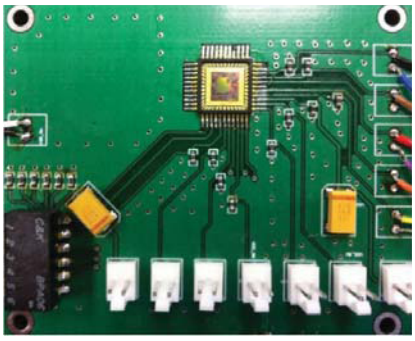

FIGURE 12. 7.8GHz divide-by-2 ILFD test chip packaged and mounted on FR-4 board.

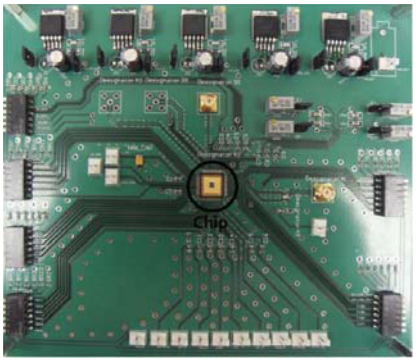

FIGURE 13. 11.1GHz divide-by-3 ILFD test chip packaged and mounted on FR-4 board.

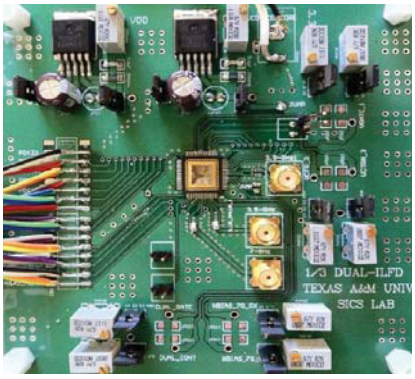

FIGURE 14. 11.7GHz divide-by-3 ILFD test chip packaged and mounted on FR-4 board.

is 0.156, 0.25, and 0.048-mm^2, respectively. Encapsulated test chips are mounted on FR-4 board for on-wafer probing test as shown in Fig. 12, 13, 14. All chips are encapsulated in a quad flat no leads (QFN) package to connect the DC pads and outputs. The external injection signal (HP83620A signal generator) is applied by on-wafer probing for the 7.8-GHz divide-by-2 and the 11.7-GHz divide-by-3. The 11.1-GHz divide-by-3 receives an injection signal from the integrated VCO, whose output power was measured separately. The output spectrum is measured using HP8692L spectrum analyzer.

The measurement result of the divide-by-2 ILFD locking-range is shown in Fig. 15. Note that the measurement is performed after the additional current-mode logic (CML)

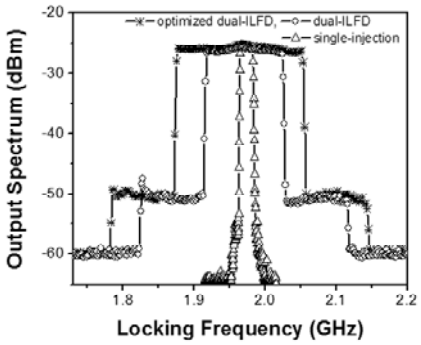

FIGURE 15. Measured locking-range ($P_{inj} = 10dBm$) of the 7.8-GHz divide-by-2 ILFD.

divider on-chip and, output frequency is thus divided by 4 compared to the input injection signal. Effectiveness of the proposed scheme is manifested by three different measurements: single-injection, dual-injection, and optimized dual-injection. The locking ranges for these cases are 70, 502, and 692-MHz, respectively. The dual-injection with optimized Q and i_{OSC} is 890% and 38% better, respectively, than that of the singe-injection and dual-injection without optimization. The simulation result also shows the similar trends in which the locking ranges for the aforementioned three different cases are 80, 450, and 677-MHz, respectively.

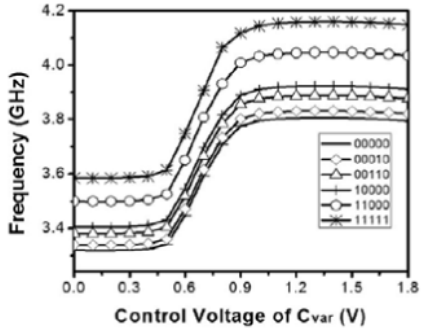

FIGURE 16. Measured locking-range ($P_{inj} = -18dBm$) of the 11.1-GHz divide-by-3 ILFD.

Fig. 16 shows the measured locking-range of the 11.1-GHz divide-by-3 as a function of the varactor capacitor (C_{var}) control voltage and 5-bit digital-control. An input injection signal is applied on-chip from the integrated VCO, whose output power was measured on-wafer (50Ω reference) as -18dBm. An output frequency locking range from 3.21 to 4.18-GHz is achieved with low injection power of -18dBm supplied from the integrated VCO, and the locking range is 26.2% accordingly. Note that a much wider locking range can be achieved with a stronger input injection signal, but this work focuses on the technique of the phase tuner to improve the locking-range with a small injection power of -18dBm from the on-chip VCO. Fig. 17 shows the locking range for two different tuning voltages ($V_{tune} = -1.6V$, $V_{tune} = -0.6V$). The locking range is 12MHz without phase tuning ($V_{tune} = -1.6V$).

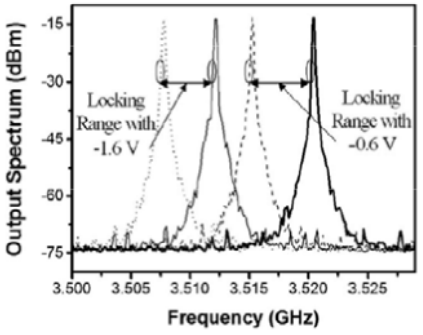

FIGURE 17. Measured output spectrum ($P_{inj} = -18dBm$) with non-optimal ($V_{tune} = -1.6V$) and optimal ($V_{tune} = -0.6V$) phase tuning voltage of the 11.1-GHz divide-by-3 ILFD.

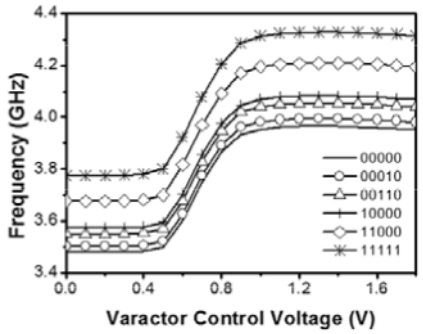

FIGURE 18. Measured locking-range ($P_{inj} = -12dBm$) of the 11.7-GHz divide-by-3 ILFD.

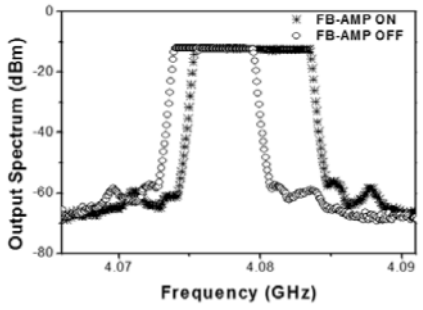

FIGURE 19. Measured locking-range ($P_{inj} = -12dBm$) with feedback path on and off of the 11.7-GHz divide-by-3 ILFD.

With optimal phase tuning voltage ($V_{tune} = -0.6V$), the locking range reaches 15MHz representing an 25% improvement. Simulation results show 28% improvements in the locking range with optimal tuning voltage of $V_{tune} = -0.75V$. Using different capacitor array settings and control voltages, the 11.7-GHz divide-by-3 ILFD achieves an output frequency locking-range from 3.47 to 4.313 GHz as shown in Fig. 18. Corresponding input frequency locking range is from 10.41 to 12.94 GHz, representing a locking-range of 21.7%. Fig. 19 shows the effect of the self-injection path by comparing the output locking range with the feedback path on and off under fixed capacitor array settings and varactor capacitor control voltage.

The measured performance of the fabricated ILFDs is summarized in Table 1. Recently published works with LC

TABLE 1. Comparison to recently published works.

	Technology	Division Ratio	Supply Voltage [V]	Power* [mW]	Inj. Power [dBm]	Lock Range [GHz]	Lock Range [%]	Area [mm^2]
[4]	$0.13\mu m$ CMOS	2	1.5	23 (N.A.)	7	14.2-17.3	9.8	0.23
[5]	$0.18\mu m$ CMOS	2	1.4	N.A. (2.8)	3	53.7-58.6†	8.72	0.38
[6]	$90nm$ CMOS	2	0.8	N.A. (0.8)	5	35.7-54.9	42.38	0.385
[7]	$0.18\mu m$ CMOS	3	1.8	45.27 (4.6)	4	16.11-18.3	12.72	0.81
[14]	$90nm$ CMOS	3	1	N.A. (4)	0	19.52-23.8	19.8	0.6
[15]	$0.18\mu m$ CMOS	3	1.8	N.A. (12.51)	5	4.85-5.7	16.1	0.64
[18]	$0.18\mu m$ CMOS	3	0.9	17.8 (8.28)	0	21.7-24.9	13.7	0.137 (active)
This work [19] (f_{in} = 7.8-GHz)	**0.18μm BiCMOS**	**2**	**1.5**	**4.4 (2.9)**	**10**	**7.51-8.2**	**8.8**	**0.156 (active)**
This work [20] (f_{in} = 11.1-GHz)	**0.18μm BiCMOS**	**3**	**1.8**	**10.6 (6.15)**	**-18**	**9.63-12.54**	**26.2**	**0.25 (active)**
This work [21] (f_{in} = 11.7-GHz)	**0.18μm BiCMOS**	**3**	**1.8**	**18.2 (6.5)**	**-12**	**10.41-12.94**	**21.7**	**0.048 (active)**

* Total power consumption (ILFD core power consumption)
† Estimated from the Fig. 8 in [5]

type ILFDs are compared with the proposed structure. The divide-by-2 ILFD in [6] shows much wider locking range than our divide-by-2 and the other references. In [5], [6], dual-injection method is applied with the same circuit topology and similar operating (center) frequency. However, the work in [6] shows much wider locking range and it is attributed to more advanced process node. With 90nm CMOS process in [6], self-oscillation behavior of the ILFD is much wider at similar injection power and the locking-range is much wider as well. The divide-by-3 from our works shows similar or wider locking-range than the others with much smaller injection power ($P_{inj} < -10$ dBm). Note that, although our work is fabricated in a 0.18-μm BiCMOS process, the tested circuits are designed with only a CMOS device. The proposed schemes benefit from a wide locking-range under high-order division ratios with low power consumption.

V. CONCLUSIONS

Wide locking-range and high-order division schemes for an LC injection-locked frequency divider are presented. The concept is verified with three fully integrated ILFD designs fabricated in a 0.18-μm BiCMOS process. The measurement results in terms of the locking-range, phase-noise, and input sensitivity as well as good correlation between the simulation and measurement results clearly verify the circuit implementation and the validity of the proposed techniques. The 7.8-GHz divide-by-2 ILFD performs a wide locking-range, employing dual injection with the simultaneous optimization of the loaded Q and bias condition, and consumes only 2.9mW from a 1.5-V supply. It is proposed that the two divide-by-3 ILFDs operate at input frequencies of 11.1 and 11.7 GHz input frequency, respectively. The 11.1-GHz ILFD proposes an odd-to-even harmonic converter implemented with the T-network and phase tuner embodied within the T-network. The odd-to-even harmonic converter enables divide-by-3 and higher odd-order division, and the phase tuner rotates i_{INJ} towards the maximum locking-range condition. The other divide-by-3 further ILFD improves the locking range and phase noise simultaneously by self-injecting the signal with the supply modulated feedback amplifier. The proposed techniques rely on various fundamental parameters determining the locking-range of the injection-locked oscillator in addition to the injection-efficiency enhancement efforts. A divide-by-3 and higher odd order division scheme does not rely on the spurious harmonic component in their regeneration process and thus exhibits a wider locking range than in previous efforts.

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