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A Fast Loss Model for Cascode GaN-FETs and Real-Time Degradation-Sensitive Control of Solid-State Transformers

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Abstract: This paper proposes a novel, degradation-sensitive, adaptive SST controller for cascode GaN-FETs. Unlike in traditional transformers, a semiconductor switch's degradation and failure can compromise its robustness and integrity. It is vital to continuously monitor a switch's health condition to adapt it to mission-critical applications. The current state-of-the-art degradation monitoring methods for power electronics systems are computationally intensive, have limited capacity to accurately identify the severity of degradation, and can be challenging to implement in real time. These methods primarily focus on conducting accelerated life testing (ALT) of individual switches and are not typically implemented for online monitoring. The proposed controller uses accelerated life testing (ALT)-based switch degradation mapping for degradation severity assessment. This controller intelligently derates the SST to (1) ensure robust operation over the SST's lifetime and (2) achieve the optimal degradation-sensitive function. Additionally, a fast behavioral switch loss model for cascode GaN-FETs is used. This proposed fast model estimates the loss accurately without proprietary switch parasitic information. Finally, the proposed method is experimentally validated using a 5 kW cascode GaN-FET-based SST platform.

Keywords: cascode GAN-FET; SSTS; switch loss model; degradation aware controller; linear quadratic regulator (LQR); lifetime estimation

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1. Introduction

In recent years, a number of studies have been conducted to find reliable power electronics alternatives to traditional transformers. Two of the most promising alternatives are solid-state transformers (SSTs) and high-temperature superconducting (HTS) transformers [1–3]. While both technologies offer significant advantages over traditional transformers, they differ in their design, capabilities, and potential applications. One of the key advantages of SSTs is their ability to control power flow, which makes them ideal for power electronics applications. SSTs will replace traditional transformers in modern industry, including use in electric vehicle charging and smart-grid applications, due to their low cost, high efficiency (>95%), and compact features [1]. Power semiconductor switches are among the most vulnerable components in a power electronic system (PES) [4]. These switches commonly experience high-frequency (HF) electro-thermal stresses in their SSTs during dynamic operation. Thus, monitoring switch aging and degradation and implementing a proactive degradation-sensitive control strategy are vital for real-world applications [5].

Switches mainly experience HF stresses during the HF dual active bridge (DAB) stage, as shown in Figure 1 [1]. A DAB control strategy minimizes the inductor current to achieve

zero-voltage switching (ZVS) [6]. These methods are promising, but they achieve adaptive control without evaluating switch degradation.

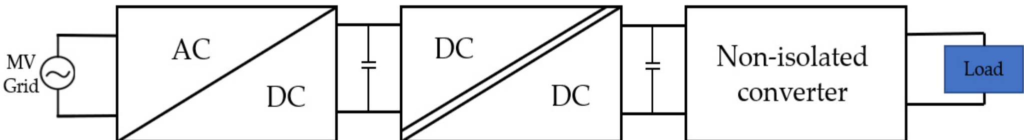

Figure 1. Block diagram of the solid-state transformer (SST) for an EV charging application.

The integration of renewable energy sources and new technologies into power systems has led to the development of a new reliability framework for modern power electronic systems [7]. Another study introduced a comprehensive approach that uses a photovoltaic inverter as an example to predict power electronic converter reliability, address wear-out failures, and optimize power system design, operation, and maintenance [8]. With the increasing demand for more electrical systems, reliability assessment and standardization have become increasingly important [7,8]. The development of guidelines is vital to achieving this objective, and current efforts are focused on creating them. Furthermore, this approach is applicable not only to the entire power electronic system but also to individual components. State-of-the-art DAB-control-based protection systems focus on post-fault scenarios [9–13], mainly by carrying out fault tolerance operations after a switch failure. Therefore, they require costly hardware redundancies and high system complexity, which commonly increase the system's size and weight [9,10]. Redundancy-based network-level power routing is not feasible in standalone SST-based EV charging applications [12]. In these applications, topology transformation methods can bypass fatal switch failure effects for a limited time. However, these methods double the current through the switch, resulting in higher switch stress and accelerated aging, which causes premature SST failure. They also require computationally exhaustive fault detection and isolation procedures. A power-sharing control strategy is proposed to improve the reliability of power converters in DC microgrids by adjusting their loadings based on prior thermal damages, aiming to extend their lifespan and enhance the overall system reliability [14]. Previous studies [12–15] have relied solely on thermal loading information to determine the stage of degradation. In contrast, accelerated life testing (ALT) can provide additional insights into the degradation pattern, which have not been utilized in this study. In [11] and [13], an adaptive but complicated and costly cooling method for junction temperature control was proposed to extend switch life.

So far, SST control and protection strategies based on monitoring switch degradation have rarely been studied. If successful, these could offer a new, effective solution without costly redundancies. An SST could integrate switch health status into a controller to intelligently identify its health-optimal operating point. Techniques based on thermal cycle counting have a limited capacity to identify switch degradation; instead, they derate the PES based on the number of thermal cycles elapsed [9–11,15]. Thus, these methods fail to derate the PES if the switch is degraded early. Switch degradation mapping is critical to utilize the benefits of PES derating.

In this paper, a new degradation-sensitive controller is proposed for a cascode GaN-FET-based SST. The proposed controller uses intelligent thermal-cycle-counting methods and ALT-based switch degradation mapping to ensure safe and robust operation over the SST's life as well as to enable operation at optimal operating conditions for switch health. A degraded switch deteriorates quickly if the SST continues operating at rated conditions and causes early failure. To address this issue, the proposed controller estimates the optimal switch health condition at which to derate. This intelligent derating allows the SST to reach its target life and avoid unexpected shutdown. A linear quadratic regulator (LQR) determines these rating and derating conditions, estimating the optimal phase shift to ensure the SST's stability and robustness to system disturbance. A fast-behavioral switch loss model is used to identify switch degradation instantaneously with low complexity,

enabling adaptive, real-time operation. This model does not require parasitic parameter estimation and exhaustive computational effort calculation, in contrast to existing analytical loss models. Although our approach is specifically developed for SST, it should be applicable to other power electronics systems as well.

The rest of the paper is organized as follows. In Section 2, the proposed controller's fundamentals are explained. Online switch lifetime mapping is discussed in Section 3, followed by accelerated-aging-based degradation mapping in Section 4. The design of the proposed controller is presented in Section 5, the design and performance of the LQR in Section 6, and experimental testing and validation in Section 7. The contributions of this paper and future research directions are explored in the conclusion in Section 8.

2. Principles of the Proposed Controller

The Coffin–Manson method estimates an application's remaining useful life based on its operating conditions [16]. This model solely addresses the effect of instantaneous operating conditions on the life of the switch [9–11,15], monitoring the number of cycles elapsed to identify the level of degradation. As degradation is random, the switch might degrade at an accelerated rate, so this model includes high variance. Thus, it is important to complement this model with fault-precursor-based identification of degradation severity. Accelerated life testing (ALT)-based degradation mapping provides a switch degradation trajectory, which allows accurate switch-degradation severity assessment and offline planning of degradation-sensitive control [17]. Another essential feature of a degradation-sensitive controller is the ability to identify abrupt changes. The proposed controller intelligently integrates online lifetime-mapping features, degradation mapping based on accelerated life testing, and identification of unexpected degradation to derate the SST for life extension. The principles of the proposed degradation-sensitive controller are shown in Figure 2.

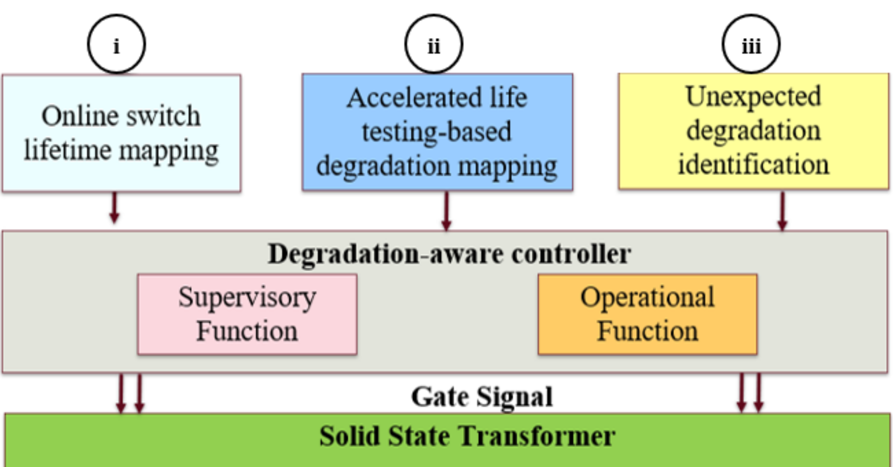

Figure 2. Structure of the proposed degradation-sensitive SST controller.

The proposed controller uses information from the following three blocks:

i. Online switch lifetime mapping;
ii. Accelerated life testing (ALT)-based degradation mapping;
iii. Identification of unexpected degradation.

In block i, the number of cycles to failure (N_f) is estimated online based on the proposed behavioral switch loss model. In block ii, switch degradation is mapped based on the switch's fault precursor trajectory under ALT. On-state resistance ($R_{DS,ON}$) shows the highest sensitivity to switch degradation in cascode GaN-FETs [17,18]. This $R_{DS,ON}$ trajectory is statistically analyzed, and a degradation probability is mapped based on ALT. In block iii, $R_{DS,ON}$ is measured online and regularly evaluated to identify any sudden changes in switch health.

The proposed controller has two functions—(i) a supervisory function and (ii) an operational function, as shown in Figure 2. In the supervisory function, dynamic programming is used to identify the switch's health status and estimate the optimal degradation-sensitive operating conditions based on the three blocks of inputs. In the operational function, an LQR regulates the optimal phase-shift angle based on the set degradation-sensitive operating point.

The following sections briefly describe the functions of the three blocks of the proposed controller.

3. Online Switch Lifetime Mapping

Block i estimates N_f based on the junction temperature, which is estimated using a switch loss model. The procedure is shown in Figure 3. This block's three main components are the switch loss model, R-C Foster-network-based junction temperature estimation, and lifetime estimation. The switch loss causes are the mean junction temperature ($T_{J,m}$) and junction temperature variation (ΔT_J). Wire-bond lift-off and solder fatigue are the two dominant open-circuit failure mechanisms triggered by HF thermo-mechanical stress. A mismatched coefficient of thermal expansion (CTE) between different layers increases the severity of this stress [17,19]. These dominant mechanisms result in wire-bond cracks and solder degradation or eventual lift-off. In the following subsections, these three components are discussed.

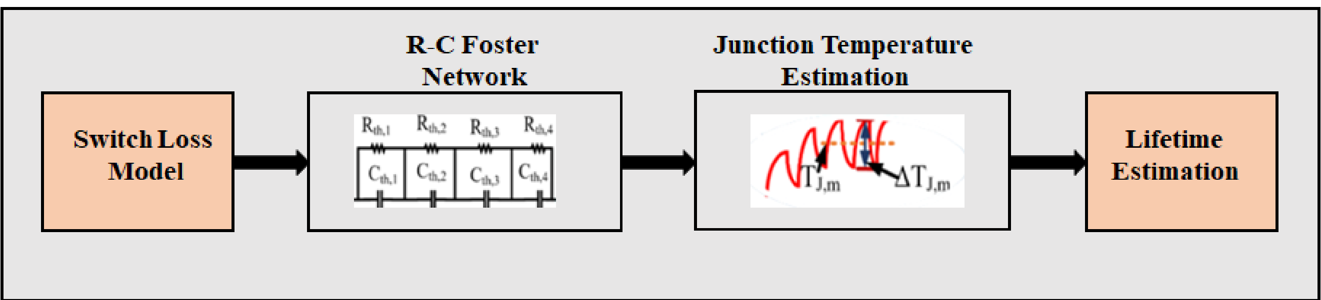

Figure 3. Block structure of the online switch lifetime mapping.

3.1. Switch Loss Model for Cascode GaN-FETs

A fast and accurate behavioral loss model is proposed. In the cascode structure, a low-voltage (LV) Si-MOSFET is cascoded with a normally-on GaN-HEMT. The turn-off loss is different, especially from IGBT, due to the absence of a tailing current. An analytical loss model for cascode GaN-FETs was developed in [20–24] based on complex cascode-structure-induced parasitic capacitances and inductances. This analytical model thus requires a computationally exhaustive process and proprietary information. Additionally, this model requires expensive testing for parameter extraction. Piecewise linear models are faster but less accurate, and the effect of the PCB parasitic is not considered [25]. The proposed model was developed by analyzing and modeling the switching transition behavior of drain-source voltage (V_{DS}) and drain current (I_d) in the half-bridge configuration to overcome these challenges.

Moreover, this behavioral model uses parameters easily extractable from the datasheet and double pulse test (DPT). This behavioral model reflects the effects of parasitic capacitances and commutation inductors. Thus, the proposed model is adaptable to high-frequency applications.

The switch loss has two components: switching loss (P_{sw}) and conduction loss (P_{cond}), calculated as follows:

$$P_{Loss} = P_{cond} + P_{sw} \tag{1}$$

Conduction loss can be estimated as follows:

$$P_{cond} = I_L^2 R_{DS,ON} \tag{2}$$

where I_L is the RMS load current and $R_{DS,ON}$ is the function of temperature and switch health status. P_{sw} is the summation of turn-on and turn-off power losses.

3.1.1. Turn-on Loss Calculation

Commonly, a cascode GaN-FET's turn-on is modeled by LV Si-MOSFET, normally on GaN-HEMT's complex physics-based interactions. The proposed behavior-based model inherently addresses the effects of parasitic capacitors and commutation inductors and is thus accurate. The proposed model does not require the solving of complex high-degree polynomials and differential equations. The switching transition of V_{DS} and I_d during turn-on is shown in Figure 4a, and is divided into four regions, as follows:

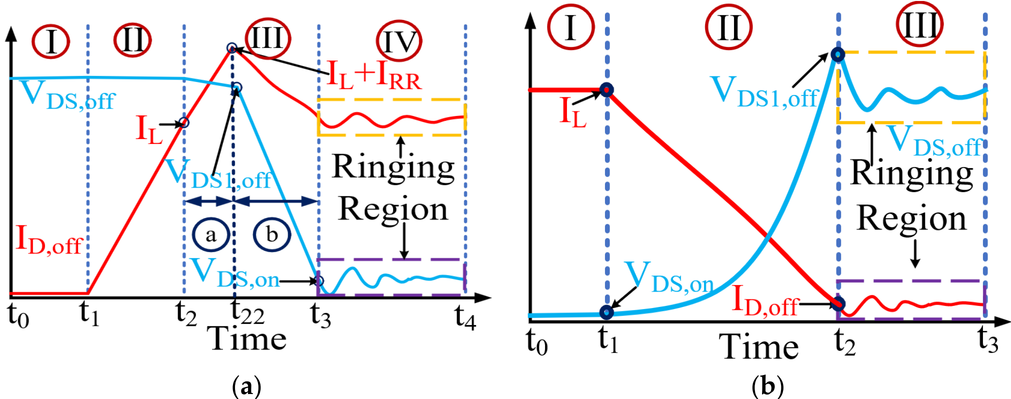

Figure 4. V_{DS} and I_d of a cascode GaN-FET: (**a**) during turn-on transition; (**b**) during turn-off transition.

- **Region I:** LV Si Gate Charging

The LV Si-MOSFET controls the switching transitions of the cascode GaN-FET. The turn-on process starts when the LV Si-MOSFET's gate voltage reaches the threshold and a conducting channel is established in LV Si-MOSFET. The gate-drive loss (P_{dri}) can be expressed as follows:

$$P_{dri}(t) = Q_G V_G f_s \quad (3)$$

where Q_G is the gate charge, V_G is the gate voltage, and f_s is the switching frequency. I_d starts rising when the gate-source voltage (V_{GS}) of GaN-HEMT reaches its threshold and causes turn-on loss in cascode GaN-FET due to V-I overlapping. This V-I overlapping starts at t_1, as shown in Figure 4a.

- **Region II:** Increasing Drain Current

In this region, the GaN-HEMT is fully turned on. I_d increases linearly and reaches load current (I_L). Thus, I_d can be modeled in the proposed model as follows:

$$I_d(t) = t\frac{d}{dt}I_{rise} \quad (4)$$

where $0 \leq I_d < I_L$ and $t_1 \leq t < t_2$, and dI_{rise}/d_t is the rising rate of I_d, which is a constant. The value of dIrise/dt depends on the commutation inductances. The value is estimated from the DPT. During this period, V_{DS} is assumed to be constant at $V_{DS,OFF}$. The energy loss during this period is expressed as follows:

$$E_{turn-on-II} = \int_{t_0}^{t_1} V_{DS}(t)I_d(t)dt = \frac{1}{2}(t_1 - t_o)^2 V_{DS,OFF}\left(\frac{d}{dt}I_{rise}\right) \quad (5)$$

- **Region III:** Decreasing drain-source voltage

In the half-bridge, two switches in one leg switch complementarily. In region III, I_L supplies I_d to the top switch and reverse-conducting current (I_{RR}) to the bottom switch. I_d rises at dI_{rise}/d_t until it reaches I_L + I_{RR}. There are two sub-regions in region III. In sub-region a, I_d increases due to commutation inductances and internal parasitics. The behavior of I_d is modeled as follows:

$$I_d(t) = t\frac{d}{dt}I_{rise} + I_L \tag{6}$$

where $I_L \leq I_d < I_L + I_{RR}$ and $t_2 \leq t < t_{22}$. In this sub-region, dIrise/dt remains the same as in region II. V_{DS} linearly drops to an off-state V_{DS} ($V_{DS,OFF}$) during this time. This drop is due to the increase in I_d over I_L. The behavioral model of V_{DS} can be expressed as follows:

$$V_{ds}(t) = V_{ds,off} + t\frac{d}{dt}V_{DS,1} \tag{7}$$

where $dV_{DS,1}/d_t$ is the falling rate of V_{DS}. The energy loss in this sub-region is as follows:

$$\begin{aligned} E_{turn-on-III} &= \int_{t_2}^{t_{22}} V_{DS}(t)I_d(t)dt \\ &= \tfrac{1}{3}(t_{22}-t_2)_3\left(\tfrac{d}{dt}V_{DS,1}\right)\left(\tfrac{d}{dt}I_{rise}\right) + \tfrac{1}{2}(t_{22}-t_2)^2V_{DS,off} \\ &\left(\tfrac{d}{dt}I_{rise}\right) + \tfrac{1}{2}(t_{22}-t_2)^2I_L\left(\tfrac{d}{dt}V_{DS,1}\right) + (t_{22}-t_2)V_{DS,off}I_L \end{aligned} \tag{8}$$

In subregion b, the reverse recovery charge needs to be removed from the bottom switch. The rate of change in I_d is defined by the reverse recovery current of the bottom switch. In this sub-region, I_d falls from I_L + I_{RR} to I_L when V_{DS} falls from $V_{DS,OFF}$,1 to $V_{DS,ON}$. The internal parasitics of the cascode structure cause these transitions. The analytical model requires internal parasitic information, which is not available. In the proposed model, the behaviors of I_d and V_{DS} can be modeled as follows:

$$I_d(t) = (I_L + I_{RR}) - t\frac{d}{dt}I_{fall} \tag{9}$$

$$V_{DS}(t) = V_{DS,Off,1} - t\frac{d}{dt}V_{DS,fall} \tag{10}$$

This model inherently addresses the effects of parasitics, which affect the rates of change in V_{DS} and I_d. Thus, the modeling approach ensures speed and accuracy. The energy loss is calculated as follows:

$$\begin{aligned} E_{turn-on-III,fall} &= \int_{t_{22}}^{t_3} V_{DS}(t)I_d(t)dt \\ &= (I_L+I_{RR})V_{DS,Off,1}(t_3-t_{22}) - \tfrac{1}{2}(t_3-t_{22})^2\left(\tfrac{d}{dt}I_{fall}\right)V_{DS,Off,1} - \tfrac{1}{2}(I_L \\ &+I_{RR})(t_3-t_{22})^2\left(\tfrac{d}{dt}V_{DS,fall}\right) + \tfrac{1}{3}(t_3-t_{22})^3\left(\tfrac{d}{dt}I_{fall}\right)\left(\tfrac{d}{dt}V_{DS,fall}\right) \end{aligned} \tag{11}$$

- **Region IV:** Ringing Region

In this region, I_d and V_{DS} behave like a damping system and reach their steady states at I_L and $V_{DS,ON}$, respectively. These tendencies can be modeled as follows:

$$I_d(t) = A_1 \exp(-\alpha_1 t)\sin(\omega_{01}t + \theta) + I_L \tag{12}$$

$$V_{DS}(t) = A_2 \exp(-\alpha_1 t)\sin(\omega_{01}t + \psi) + V_{DS,ON} \tag{13}$$

where A_1 and A_2 are the amplitudes of I_d and V_{DS}, respectively; α_1 is the decay rate of I_d and V_{DS}; and ω_{01} is the frequency of I_d and V_{DS}, respectively. At the start of this region, I_d is I_L, V_{DS} is $V_{DS,ON}$, and θ and ψ are zero. The loss in this region is as follows:

$$E_{turn-on-IV} = \int_{t_3}^{t_4} V_{DS}(t) I_d(t) dt \quad (14)$$

where $E_{turn\text{-}on\text{-}IV}$ is a function of ω_{01}, α_{01}, A_1, and A_2. These parameters are estimated from the double-pulse test. The total turn-on loss is the summation of the losses in regions I, II, and III:

$$E_{on} = E_{turn-on,II} + E_{turn-on,III} + E_{Turn-on,IV} \quad (15)$$

3.1.2. Turn-off Loss Calculation

Like turn-on loss, turn-off loss is modeled by analyzing the switching transition behavior. This model is fast and easily implementable without any proprietary information and costly testing. The turn-off transition of V_{DS} and I_d during the turn-off process is shown in Figure 4b, where the turn-off region is divided into three regions.

- **Region-I:** Gate Capacitor Discharge

The turn-off process starts when V_g is zero and initiates the discharge process of the gate-source capacitor of the LV Si-MOSFET. In this region, there are insignificant changes in V_{DS} and I_d. Thus, there is only an insignificant gate-drive loss, similar to that in Equation (3).

- **Region II:** Decreasing Drain Current

In region II, GaN-HEMT is shut down due to the interaction between the gate capacitance of the LV MOSFET and GaN-HEMT. I_d decreases from I_L to zero. V_{DS} increases from $V_{DS,ON}$ to $V_{ds2,off}$, which is greater than the input voltage (V_{in}). These behaviors of I_d and V_{DS} can be modeled as follows:

$$I_d(t) = I_L + t \frac{d}{dt} I_{fall} \quad (16)$$

where $I_d(t_1) = I_L$ at $t = t_1$ and $I_d(t_2) = 0$ at $t = t_2$.

$$V_{DS}(t) = V_{DS,on} + t \frac{d}{dt} V_{DS,rise} \quad (17)$$

where $V_{DS}(t_1) = V_{DS,ON}$ at $t = t_1$ and $VDS(t_2) = V_{DS,off}$ at $t = t_2$. These behavioral models address the effects of the parasitic components on the switching transition while avoiding complex modeling and exhaustive calculations. The energy loss in this region is as follows:

$$E_{turn-off-II} = \int_{t_1}^{t_o} V_{DS}(t) I_d(t) dt = I_L V_{DS,on}(t_1 - t_o) - \frac{1}{2}(t_1 - t_o)^2 \left(\frac{d}{dt} I_{fall}\right) - \frac{1}{2} I_L (t_1 - t_o)^2 \left(\frac{dV_{DS,rise}}{dt}\right) + \frac{1}{3}(t_1 - t_o)^3 \left(\frac{dV_{DS,rise}}{dt}\right)\left(\frac{d}{dt} I_{fall}\right) \quad (18)$$

- **Region III:** Ringing Region

In region III, I_d and V_{DS} reach steady-state conditions at zero and $V_{DS,OFF}$, respectively. During this period, I_d and V_{DS} behave like an underdamped system. This behavior is modeled as follows:

$$I_d(t) = A_3 \exp(-\alpha_2 t) \sin(\omega_{02} t) \quad (19)$$

$$V_{DS}(t) = \Delta V_{DS} \exp(-\alpha_2 t) \cos(\omega_{o2} t) \quad (20)$$

where, at $t = t_3$, $I_d = 0$ and $V_{DS} = V_{DS,OFF}$, A_3 is the amplitude of the overdamped system, α_2 is the decaying rate, and ω_{o2} is the decaying frequency. The turn-off loss is as follows:

$$E_{turn-off-III} = \int_{t_2}^{t_3} V_{DS}(t) I_d(t) dt \quad (21)$$

where $E_{turn\text{-}on\text{-}III}$ is a function of ω_{02}, α_{02}, A_3, and ΔV_{DS}. These parameters are estimated from the DPT. The total turn-off loss is the summation of the losses as follows:

$$E_{off} = E_{turn-off,II} + E_{turn-off,III} \quad (22)$$

This behavioral model is a fast and efficient alternative to complex analytical loss models. Addressing parasitic capacitances and commutation inductances using the time series behavioral model results in fast and accurate switch loss estimation.

3.2. R-C Foster-Model-Based Junction Temperature Estimation

The R-C Foster model is the second component in block I, as shown in Figure 3. Switch loss is translated into T_J using the R-C Foster model as follows:

$$T_J = P_{loss} Z_{th} + T_c \quad (23)$$

where T_J is the switch's junction temperature, Z_{th} is the thermal impedance, and T_C is the case temperature. Z_{th} is estimated as follows:

$$Z_{th} = \sum_{i=1}^{n} r_i \left(1 - e^{\frac{-t}{\tau_i}}\right) \quad (24)$$

where r_i is the thermal resistance of the switch and τi is the thermal time constant. Thermal time constraints are expressed as $\tau_i = r_i\, C_{th,i}$, where $C_{th,i}$ is the thermal capacitance. These thermal parameters are estimated from the switch's transient thermal impedance curve provided in the datasheet.

3.3. Lifetime Estimation

The Coffin–Manson life estimation model relates Nf to $T_{J,m}$ and ΔT_J. This model estimates the instantaneous variation in N_f due to a change in operating conditions. The model can be expressed as follows:

$$N_f = A\left(\Delta T_J^{-b_1}\right) \exp\left(\frac{b_2}{T_{j,\,m} + 273}\right) \quad (25)$$

where $T_{J,m}$ is the minimum junction temperature and A, b_1, b_2, and b_3 are the empirical coefficients. These empirical coefficients and the estimated value, T_J, include estimation error uncertainties. Switch lifetime consumption accelerates due to changes in ΔT_J and $T_{J,m}$, as follows:

$$D.A.F = \left(\frac{\Delta T_{j,1}}{\Delta T_{j,2}}\right)^{-b1} \exp\left(\frac{b_2}{T_{j_1,\,m} + 273} - \frac{b_2}{T_{j_2,\,m} + 273}\right) \quad (26)$$

where D.A.F is the degradation acceleration factor when the operation point changes from (ΔT_{J1}, $T_{J1,m}$) to (ΔT_{J2}, $T_{J2,m}$) due to switch degradation. The damage to the switch is estimated based on Miner's linear damage rule as follows:

$$C = \sum \frac{n_i}{N_f} \quad (27)$$

where C is the switch's consumed lifetime and n_i is the number of cycles consumed by the switch. The information on consumed lifetime is used with ALT-based switch degradation mapping to address deviations in the operating conditions and switch lifetime acceleration.

4. Degradation Mapping Based on Accelerated Life Testing

The typical lifetime of a power semiconductor switch is 10–12 years [5]. ALT maps this trajectory to a logical timeframe. ALT of a cascode GaN-FET provides critical insight

into the relationship between $R_{DS,ON}$ trajectory dynamics and consumed life. The $R_{DS,ON}$ trajectory shows sensitivity to packaging-related failures in the cascode GaN-FET, such as wire-bond lift-off (WBLO) and solder crack [18,26]. Switch degradation is mapped by analyzing the $R_{DS,ON}$ trajectories.

In this paper, a power-cycling ALT is used for mapping the $R_{DS,ON}$ trajectory. The ALT conditions and switch degradation mappings are provided in Section 7.2. The $R_{DS,ON}$ trajectories show that there are three distinct regions in the life of the cascode GaN-FET—(i) the healthy region, (ii) the slow degradation (SD) or constant degradation (CD) region, and (iii) the exponential degradation (ED) region. These tendencies in the $R_{DS,ON}$ trajectory are shown in Figure 5a. There are also $R_{DS,ON}$ trajectories that are outliers to the typical trajectories, as shown in Figure 5b. These outlier trajectories bias the mean $R_{DS,ON}$ trajectory. It is logical to model the degradation trajectory using the median $R_{DS,ON}$ trajectory, which is not significantly affected by outliers. This median trajectory is modeled as follows:

$$P_t(R_{DS,ON} \leq R_{DS,ON,med}) = \frac{1}{2} \tag{28}$$

where $R_{DS,ON,\,med}$ is the median of the $R_{DS,ON}$ trajectories. This mapping of degradation using Equation (28) is shown in Figure 5b.

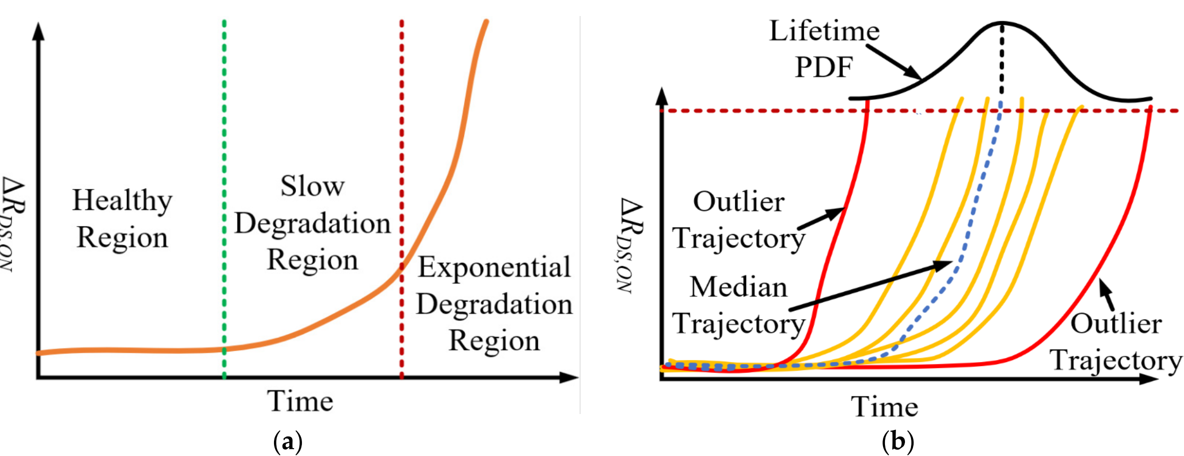

Figure 5. (**a**) $R_{DS,ON}$ trajectory for a cascode GaN-FET; (**b**) median $R_{DS,ON}$ trajectory for a cascode GaN-FET.

5. A Degradation-Sensitive Controller for SSTS

The proposed controller operates using two functions: a supervisory function and an operational function, as shown in Figure 2. The dynamically programmed supervisory function determines a switch-health-sensitive operating point. Based on this operating point, the LQR process estimates the optimal phase shift for the SST.

5.1. Dynamic Programmed Supervisory Function

Dynamic programming uses switch degradation mapping to estimate the necessary operating conditions to achieve a target lifetime for the SST. To achieve the target lifetime under the proposed method, the SST operates using the optimal derating trajectory based on the cost function, as follows:

$$J = \min\left(C_{rated} - \sum_{i=1}^{3} C_{degraded,i}\right) \tag{29}$$

where C_{rated} is the rated lifetime under constant junction temperature variation and $C_{degraded,i}$ is the consumed lifetime. The cost function is minimal when the rated value is equal to a switch's lifetime. The objective of the dynamically programmed supervisory function is to maximize J by adaptively selecting operating conditions based on switch

health status. This strategy is shown graphically in Figure 6. This strategy ensures constant junction temperature variation and uniform lifetime consumption. The controller is designed as follows:

Minimize: $\text{Arg}_{\max} C_{degraded} = (C_1 + C_2 + C_3)$
Subject to:
Constraint 1: $C_1 > 0, C_2 > 0, C_3 > 0$
Constraint 2: $0.8P_{rated} \leq P \leq P_{rated}$
Constraint 3: $C_{degradate} \leq C_{rated}$
Constraint 4: $P_{II} > P_{III}$

where C_1, C_2, and C_3 are consumed life in regions I, II, and III, respectively. The derating algorithm is shown in Figure 6. As the switch will be more degraded in the exponential degradation (ED) region than in the slow degradation (SD) region, it is logical to impose higher derating in the ED region. Based on the constraints, the allowed operating conditions are shown in Figure 7. When the switch is healthy, the SST operates as rated. However, the SD and ED regions' operating conditions are programmed based on constraints 1–4. If the SST operates at P_{min}, it will have a maximum lifetime, but it will violate constraint 3. If the SST operates at P_{rated}, J will be maximized, but the SST will fail before its target lifetime. Different combinations of operating conditions in these two regions lead to different lifetimes for the SST. To integrate these dynamic operating conditions, Equation (26) is used to estimate lifetime consumption under each condition. E_{on} and E_{off} are integrated into the proposed controller as a look-up table to reduce the computational burden.

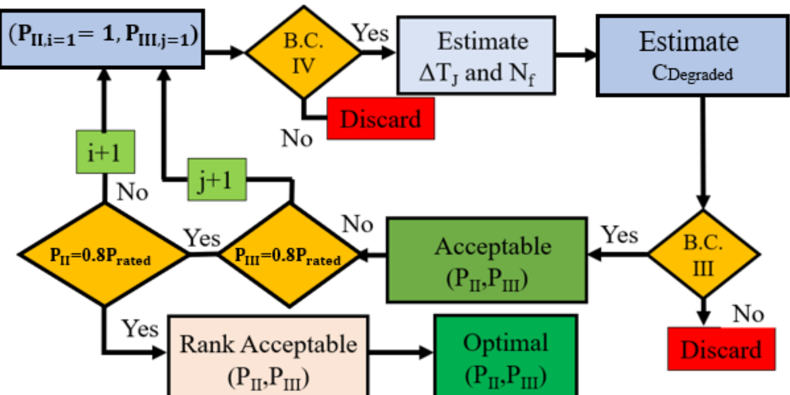

Figure 6. Optimal operating condition estimation algorithm.

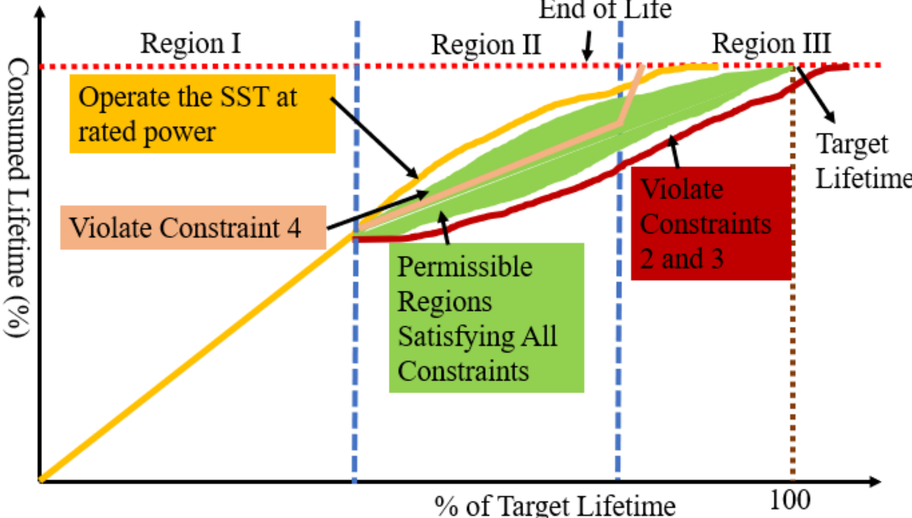

Figure 7. Degradation-sensitive dynamically programmed operating conditions.

5.2. LQR-Based Operational Function

A regulator is required to control the DAB stage in SST to deliver the reference voltage. In the proposed controller, the operational function uses an LQR as this regulator. In this sub-section, this LQR is described; the LQR ensures the optimal phase-shift angle for the rated or derated operating condition set by the supervisory function. The LQR shows robust performance under system disturbance and estimates the optimal phase-shift angle to ensure efficiency. The LQR design requires a state-space model of the DAB stage. The equivalent circuit in the DAB is shown in Figure 8, where L is the HF transformer's leakage inductance, VAB is the inverter output, and VCD is the rectifier input voltage.

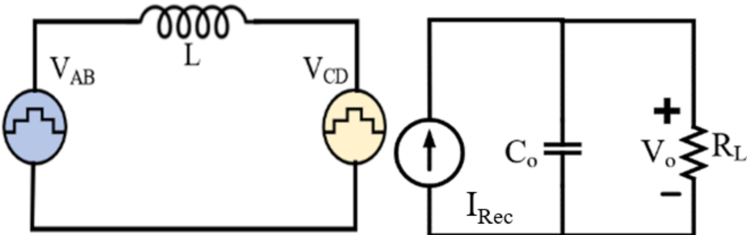

Figure 8. Equivalent circuit of the DAB stage of the SST.

The average model of the output stage of the DAB is shown in Figure 8. Using Kirchhoff's current law,

$$\mathrm{Co}\frac{\mathrm{dVo}}{\mathrm{dt}}+\frac{\mathrm{Vo}}{\mathrm{R_L}}-\frac{\mathrm{ViD}(1-\mathrm{D})}{2\mathrm{Lf_s}}=0 \tag{30}$$

where V_i is the input voltage, V_o is the output voltage, RL is the load, C_o is the output capacitor, and f_s is the switching frequency. The small-signal model of this output average model for small variations in v_o and d is as follows:

$$\frac{dv_o}{dt}=\frac{-vo}{R_L C_o}+\frac{V_i(1+2D)}{2LC_o f_s}d \tag{31}$$

The state-space model of the DAB is as follows:

$$\dot{x}=Ax+Bu \tag{32}$$

where

$$A=\begin{bmatrix}0 & 1\\ 0 & -\frac{1}{R_L C_o}\end{bmatrix},\ B=\begin{bmatrix}0\\ \frac{V_i(1+2D)}{2LC_o f_s}\end{bmatrix} x=\begin{bmatrix}\int v_o dt\\ v_o\end{bmatrix} \text{and } u=d$$

In this state-space model, a new variable, $\int v_o dt$, is introduced, which results in zero steady-state error. The quadratic cost function of the system is as follows:

$$J_{LQR}=\int\left(x^T Q x+u^T R u\right)dt \tag{33}$$

where J_{LQR} is the quadratic cost function, Q is a 2-by-2 positive semi-definite matrix, and R is a scalar that should be positive. The closed-loop poles' locations depend on the choices of Q and R.

In this paper, R = 1 and Q = [q_1 0; 0 q_2]. Thus, q_1 and q_2 determine the speed and damping of the system. For the state feedback, it is assumed that

$$u=-kx \tag{34}$$

where $k=\begin{bmatrix}k_1 & k_2\end{bmatrix}$ represents the feedback gain.

Putting Equation (34) into Equation (35), it is found that

$$J_{LQR} = \frac{1}{2}\int\left[x^T\left(Q + k^T R k\right)x\right]dt \tag{35}$$

The optimal solution for k is found as follows:

$$k = R^{-1}B^T P \tag{36}$$

where P is the solution of the algebraic Recatti equation, as follows:

$$PA + A^T P - PBR^{-1}B^T + Q = 0 \tag{37}$$

6. LQR Design and Its Performance Analysis

The LQR design requires the operating point information as shown in Equation (30). The operating frequency of the SST is 50 kHz; the rated voltage and power are 400 V and 5 kW, respectively; the leakage inductance is 53 µH; and the output capacitance is 120 µF. Based on this operating condition and the system information, the LQR is designed to have sufficient controller speed and zero steady-state error. The root locus and the step response of the modeled LQR controller are shown in Figure 9a,b with R = 1, Q = [50 0;0 10^(−5.5)], and K = [−7.0711 0.0048]. The settling time of the system is 0.043 s, and the overshoot is less than 5%. Thus, the LQR is operating with reasonable speed and accuracy.

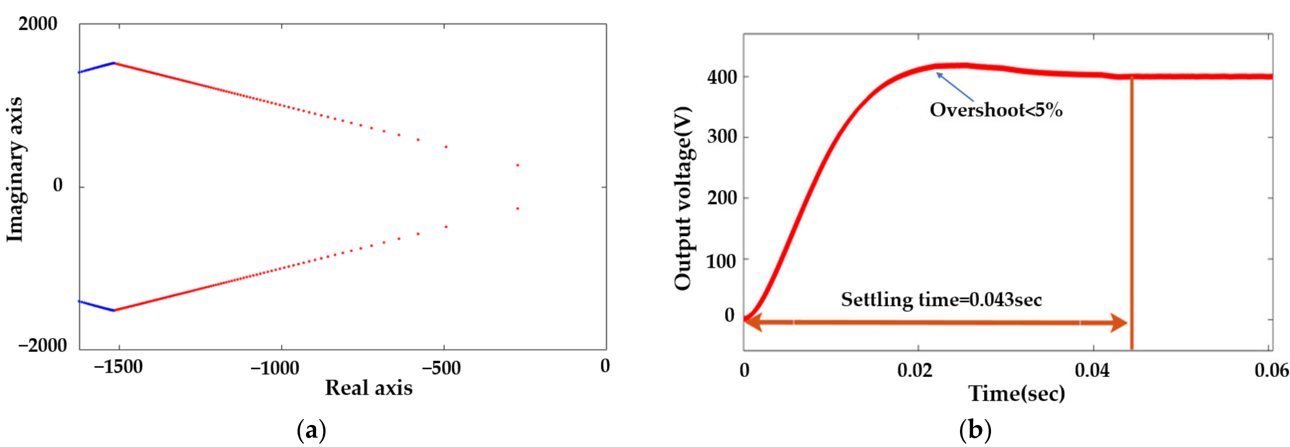

Figure 9. Performance of the designed LQR controller: (**a**) root locus; (**b**) step response.

7. Experimental Testing and Validation

7.1. Validation of the Behavioural Switch Loss Model

Commutation inductance due to the PCB layout plays a vital role in switching loss estimation. These inductances change with the PCB layout, which is application dependent. Thus, it is essential to conduct a DPT on the same PCB layout as the SST to address these inductances' effect on switching loss. V_{DS} and Id measurements require high-bandwidth probes. A differential voltage probe (TMDP0200) and coaxial shunt 0.1 Ω SSDN-10 current sensor are used for fast, high-precision measurements. V_{DS} and I_d are shown in Figure 10 during the turn-on and turn-off transitions. Turn-on and turn-off losses are estimated by calculating energy losses due to the crossover of V_{DS} and I_d. Moreover, these signals are properly aligned to improve the integrity of the testing.

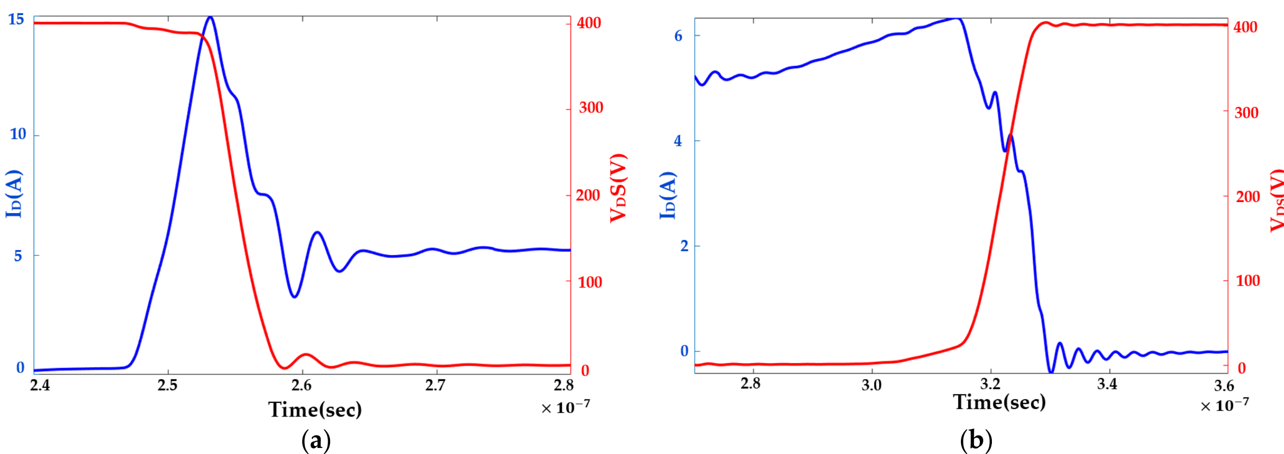

Figure 10. Drain-source voltage and drain current: (**a**) during turn-on; (**b**) during turn-off.

The rates of change in V_{DS} and I_d during turn-on and turn-off are estimated from the DPT test and the datasheet, along with ringing region parameters. These parameters are used in Equations (3)–(25) for switching loss estimation and are integrated into the controller. The estimated switching loss is compared with the measured loss from the DPT at different operating conditions to validate the proposed switching loss model, as shown in Figure 11. This behavioral switching-loss model closely follows the experimental switching loss tendency and has a 2.3% average mean squared error. The model is fast, parameter extraction is easy, and the model follows the experimental model's loss tendency closely.

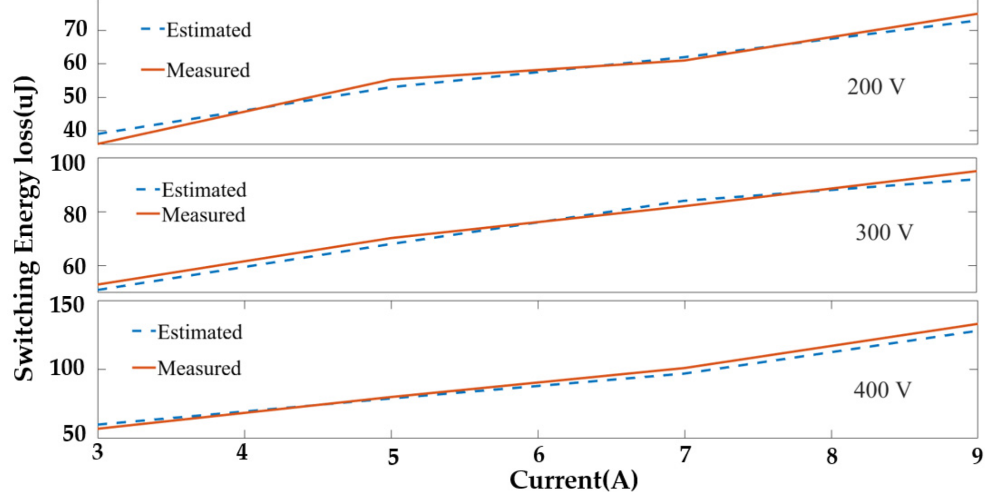

Figure 11. Estimated and measured switching energy loss under different operating conditions.

7.2. Validation of the Degradation-Sensitive Controller

An experimental setup for the degradation-sensitive controller is shown in Figure 12. The operating frequency is 50 kHz, the rated input and output voltage is 400 V, the rated power is 5 kW, and the leakage inductance is 53 µH.

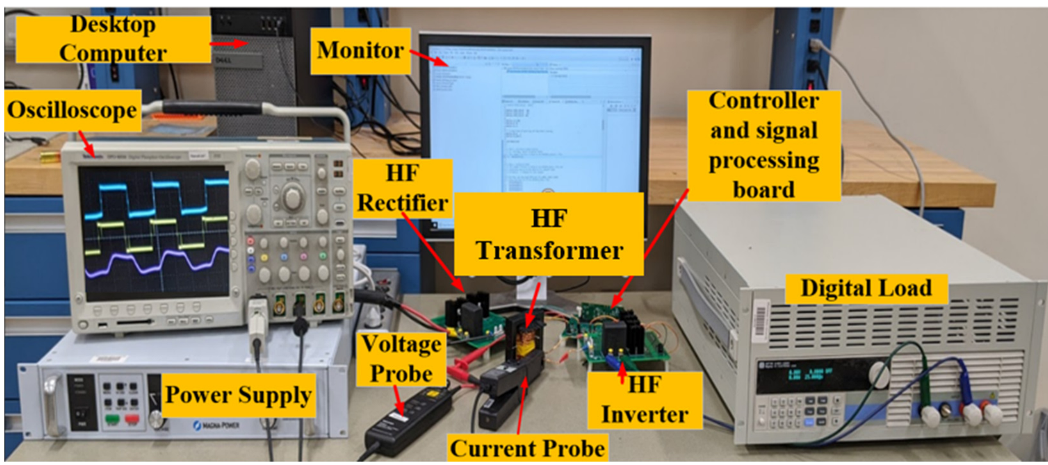

Figure 12. Experimental setup for a cascode GaN-FET-based SST.

The $R_{DS,ON}$ trajectories of the cascode GaN-FET under ALT are shown in Figure 13. In the power cycling ALT test, the switch's case temperature was varied between 25 °C and 100 °C using active-switch heating. To measure $V_{DS,ON}$ and monitor $R_{DS,ON}$ in real time, a signal-conditioning circuit was utilized. For a detailed description of this circuit, please refer to our previous publication [19], and the shunt resistor in the phase leg was used to measure I_d. The $R_{DS,ON}$ measurement was sampled at a steady state to avoid the effect of switching transients. To reduce the effect of noise, 50 $R_{DS,ON}$ samples were averaged. These $R_{DS,ON}$ samples were also temperature scaled.

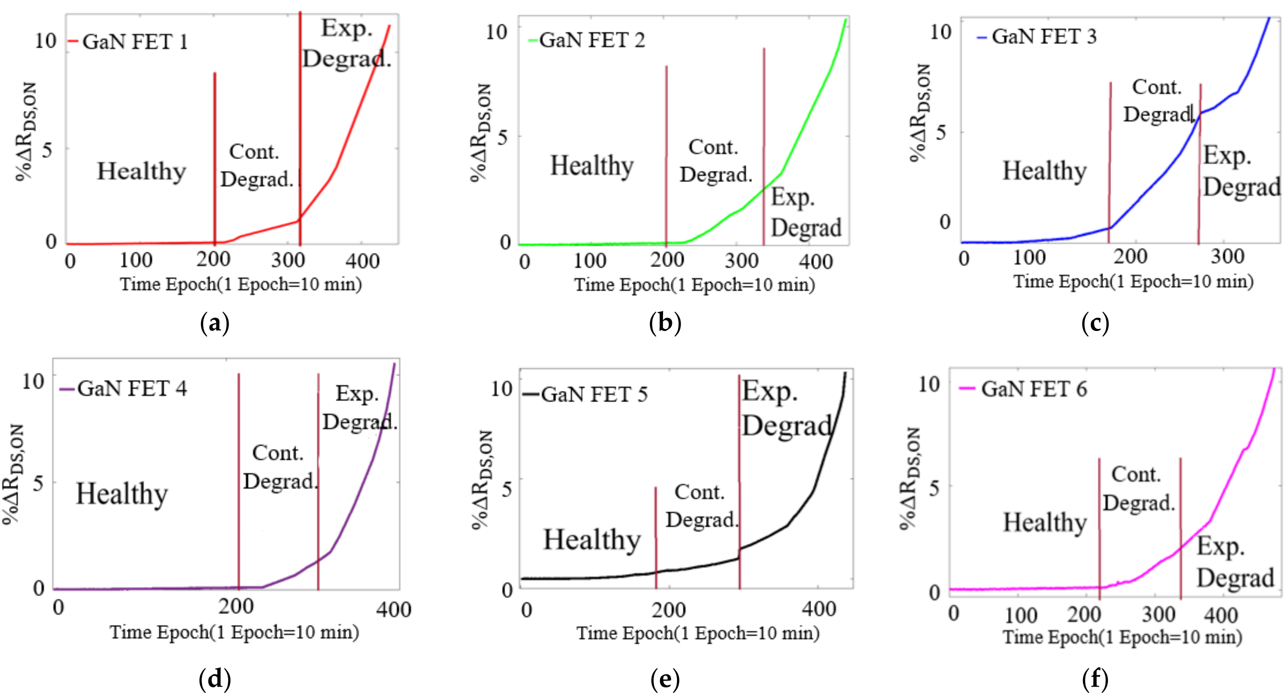

Figure 13. Actual trajectory of $R_{DS,ON}$: (**a**) GaN-FET1, (**b**) GaN-FET2, (**c**) GaN-FET3, (**d**) GaN-FET4, (**e**) GaN-FET5, and (**f**) GaN-FET6.

It was observed that, until 60% of the way through their life, the switches were in the healthy region. In this region, $\Delta R_{DS,ON}$ is between 0% and 2%. From 60% to 80% of the switches' lifetime, the switches were in the SD region, where $\Delta R_{DS,ON}$ is between 2% and 7%. When $\Delta R_{DS,ON}$ is greater than 7%, the switch is in the ED region. The statistically modeled median $R_{DS,ON}$ and the dynamically programmed estimated optimal operating trajectory are shown in Figure 14.

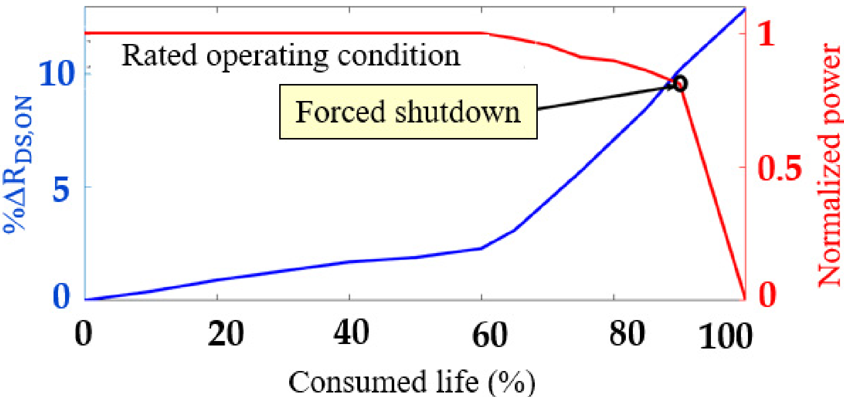

Figure 14. $R_{DS,ON}$ trajectory mapping and dynamically programmed operating point mapping.

The SST was operated with a new switch, a 40% degraded switch, and an 80% degraded switch to validate the proposed control system's applicability. The $\Delta R_{DS,ON}$ values were 1.6% and 7% for the 40% and 80% degraded switches, respectively. The switches were degraded using ALT. The SST operates at a rated inductor current of V_o = 400 V when the switch is healthy, as shown in Figure 15. As a 40% degraded switch is also in the healthy region, the SST keeps operating in the rated condition. The inductor current is decreased when the degradation-sensitive degradation controller identifies the switch as being in the ED region, as shown in Figure 15. The optimal operating condition was identified as V_o = 360 V.

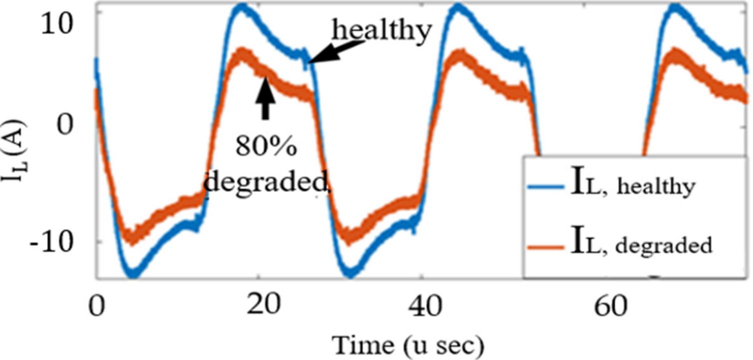

Figure 15. Inductor current in the rated condition and in a degraded condition.

The derated operating condition reduces the junction temperature experienced by the switch. The lifetime profiles for different values of $T_{J,m}$ and ΔT_J are shown in Figure 16. The PDFs and cumulative density functions (CDFs) of N_f at (ΔT_J = 10 °C, $T_{J,m}$ = 50 °C) and (ΔT_J = 11 °C, $T_{J,m}$ = 51 °C) are shown in Figure 17. When $T_{J,m}$ and ΔT_J are reduced by 1 °C, the CDF becomes less steep. If the switch keeps operating in the rated condition, it will fail at 96% of the rated lifetime. The proposed derating condition considers switch degradation and achieves the rated lifetime, extending the switch's life by 4%. This extended life is crucial for scheduling maintenance before the switch fails.

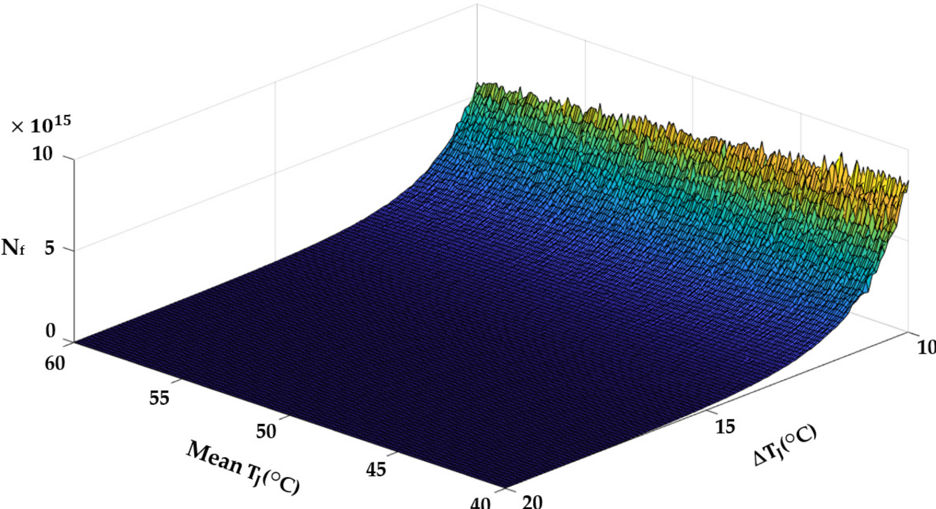

Figure 16. Lifetime profiles for different values of ΔT_J and $T_{J,m}$.

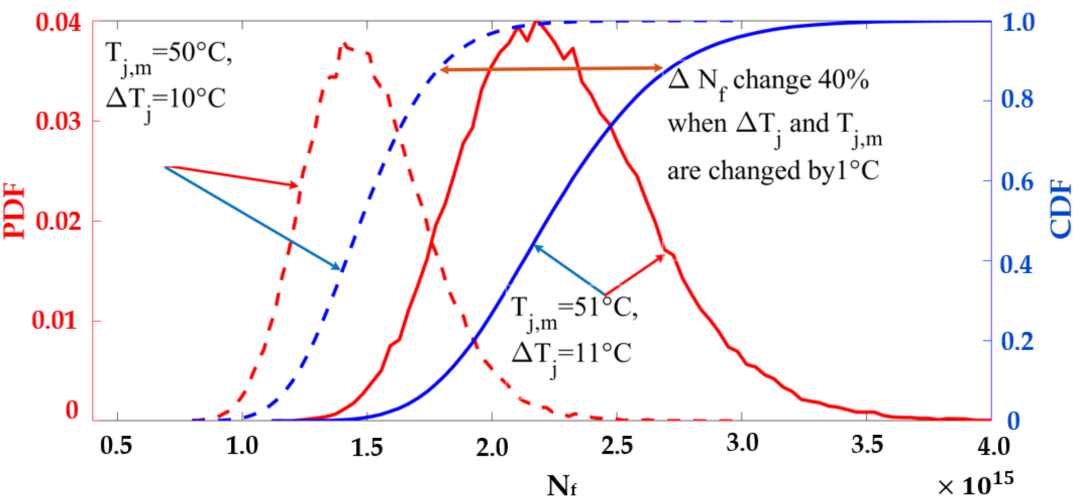

Figure 17. The effects of ΔT_J and $T_{J,m}$ on switch lifetime and switch degradation.

8. Conclusions

This paper proposes a degradation-sensitive controller for an SST that intelligently derates the system's power based on the switch's health in order to prevent system failure before the end of the switch's expected lifetime. The proposed controller increases the SST's lifetime by 4% over a traditional controller by derating the SST to 80% of its rated power. The proposed approach involves mapping switch degradation to derating levels, with the system operating at its rated conditions until 60% of its consumed life, followed by a gradual reduction of power levels based on switch degradation, and a forced shutdown if degradation exceeds 90%, effectively extending the lifetime of the system. This lifetime extension is achieved by reducing $T_{J,m}$ and ΔT_J limits by 1 °C. The objective of this strategy is to maintain a consistent temperature variation while ensuring that $T_{J,m}$ does not increase. This is particularly important because an increase in its value can significantly reduce the device's lifetime. Although the proposed controller derates the SST with switch degradation, this extended lifetime is significant for maintenance scheduling and avoidance of unexpected failure.

The proposed fast behavioral cascode GaN-FET switch loss model shows an average mean squared error of 2.3% and does not require proprietary switch information. The model parameters are easily extractable from the datasheet and DPT, and the loss model does not require exhaustive computation. Though it is developed for SST, it should be applicable to

other power electronics systems as well. The integration of health-monitoring systems and degradation-sensitive controllers into digital twin and cloud computing platforms could be useful for industrial and electric transport maintenance and asset management.

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References

1. Shadfar, H.; Ghorbani Pashakolaei, M.; Akbari Foroud, A. Solid-state transformers: An overview of the concept, topology, and its applications in the smart grid. *Int. Trans. Electr. Energy Syst.* **2021**, *31*, 9. [CrossRef]
2. Irannezhad, F.; Heydari, H. Conducting a Survey of Research on High Temperature Superconducting Transformers. *IEEE Trans. Appl. Supercond.* **2020**, *30*, 1–13. [CrossRef]
3. Moradnouri, A.; Ardeshiri, A.; Vakilian, M. Survey on High-Temperature Superconducting Transformer Windings Design. *J. Supercond. Nov. Magn.* **2020**, *33*, 2581–2599. [CrossRef]
4. Held, M.; Jacob, P.; Nicoletti, G.; Scacco, P.; Poech, M.-H. Fast Power Cycling Test of IGBT Modules in Traction Application. In Proceedings of the International Conference on Power Electronics and Drive Systems (PEDS), Singapore, 26–29 May 1997; pp. 1–6.
5. Bayerer, R.; Herrmann, T.; Licht, T.; Lutz, J.; Feller, M. Model for Power Cycling lifetime of IGBT Modules—Various factor influencing lifetime. In Proceedings of the International Conference on Integrated Power Systems (CIPS), Virtual, 11–13 March 2008; pp. 1–6.
6. Wu, F.; Feng, F.; Gooi, H.B. Cooperative Triple-Phase-Shift Control for Isolated DAB DC–DC Converter to Improve Current Characteristics. *IEEE Trans. Ind. Electron.* **2019**, *66*, 7022–7031. [CrossRef]
7. Peyghami, S.; Palensky, P.; Blaabjerg, F. An Overview on the Reliability of Modern Power Electronic Based Power Systems. *IEEE Open J. Power Electron.* **2020**, *1*, 34–50. [CrossRef]
8. Peyghami, S.; Wang, Z.; Blaabjerg, F. A Guideline for Reliability Prediction in Power Electronic Converters. *IEEE Trans. Power Electron.* **2020**, *35*, 10958–10968. [CrossRef]
9. Wang, X.; Castellazzi, A.; Zanchetta, P. Temperature control for reduced thermal cycling of power devices. In Proceedings of the European Conference on Power Electronics and Applications (EPE), Lille, France, 2–6 September 2013; pp. 1–10.
10. Lemmens, J.; Vanassche, P.; Driesen, J. Optimal Control of Traction Motor Drives Under Electrothermal Constraints. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 249–263. [CrossRef]
11. Andresen, M.; Ma, K.; Buticchi, G.; Falck, J.; Blaabjerg, F.; Liserre, M. Junction Temperature Control for More Reliable Power Electronics. *IEEE Trans. Power Electron.* **2018**, *33*, 765–776. [CrossRef]
12. Marquez, A.; Leon, J.I.; Vazquez, S.; Franquelo, L.G.; Buticchi, G.; Liserre, M. Power Device Lifetime Extension of Dc-Dc Interleaved Converters via Power Routing. In Proceedings of the IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018; pp. 5332–5337.
13. Murdock, D.; Torres, J.; Connors, J.; Lorenz, R. Active thermal control of power electronic modules. *IEEE Trans. Ind. Appl.* **2006**, *42*, 552–558. [CrossRef]
14. Peyghami, S.; Davari, P.; Blaabjerg, F. System-Level Reliability-Oriented Power Sharing Strategy for DC Power Systems. *IEEE Trans. Ind. Appl.* **2019**, *55*, 4865–4875. [CrossRef]
15. Weckert, M.; Roth-Stielow, J. Lifetime as a control variable in power electronic systems. Emobility–Electrical Power Train, Leipzig, Germany, 8–9 November 2010; IEEE: Piscataway, NJ, USA, 2010; pp. 1–6. [CrossRef]
16. Jacques, S.; Caldeira, A.; Batut, N.; Schellmanns, A.; Leroy, R.; Gonthier, L. A Coffin-Manson model to predict the TRIAC solder joints fatigue during power cycling. In Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 30 August–1 September 2011; pp. 1–8.
17. Haque, M.S.; Choi, S. Support Vector Regression Assisted Auxiliary Particle Filter based Remaining Useful Life Estimation of GaN FET. In Proceedings of the IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018; pp. 1525–1530.

18. Xu, C.; Ugur, E.; Yang, F.; Pu, S.; Akin, B. Investigation of Performance Degradation in Enhancement-Mode GaN HEMTs under Accelerated Aging. In Proceedings of the 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 98–102.
19. Haque, M.S.; Choi, S. Sparse Kernel Ridge Regression Assisted Particle Filter Based Remaining Useful Life Estimation of Cascode GaN FET. *IEEE Trans. Ind. Electron.* **2020**, *68*, 7516–7525. [CrossRef]
20. Gareau, J.; Hou, R.; Emadi, A. Review of Loss Distribution, Analysis, and Measurement Techniques for GaN HEMTs. *IEEE Trans. Power Electron.* **2020**, *35*, 7405–7418. [CrossRef]
21. Christen, D.; Biela, J. Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge. *IEEE Trans. Power Electron.* **2019**, *34*, 3700–3710. [CrossRef]
22. Huang, X.; Li, Q.; Liu, Z.; Lee, F.C. Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 2208–2219. [CrossRef]
23. Li, Q.; Liu, B.; Duan, S.; Wang, L.; Xu, B.; Luo, C. Analytical Switching Loss Model of Cascode GaN HEMTs Based Totem-Pole PFC Converters Considering Stray Inductances. In Proceedings of the 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia, Xi'an, China, 16–18 May 2018; pp. 118–124.
24. Xin, Y.; Chen, W.; Sun, R.; Shi, Y.; Liu, C.; Xia, Y.; Wang, F.; Maolin, L.; Li, J.; Zhou, Q.; et al. Analytical Switching Loss Model for GaN-Based Control Switch and Synchronous Rectifier in Low-Voltage Buck Converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 1485–1495. [CrossRef]
25. Murillo Carrasco, L.C.; Forsyth, A.J. Energy Analysis and Performance Evaluation of GaN Cascode Switches in An Inverter Leg Configuration. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015; pp. 2424–2431.
26. Huang, X.; Liu, Z.; Lee, F.C.; Li, Q. Characterization and Enhancement of High-Voltage Cascode GaN Devices. *IEEE Trans. Electron. Devices* **2014**, *62*, 270–277. [CrossRef]

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