

Article

Degradation-Sensitive Control Algorithm Based on Phase Optimization for Interleaved DC–DC Converters

Jaeyoon Jeong¹, Sangshin Kwak^{1,*}  and Seungdeog Choi^{2,*}¹ School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, Republic of Korea² Department of Electrical and Computer Engineering, Mississippi State University, Starkville, MS 39762, USA

* Correspondence: sskwak@cau.ac.kr (S.K.); seungdeog@ece.msstate.edu (S.C.)

Abstract: As the use of interleaved DC–DC converters in electric vehicles (EVs) increases, research on reliability improvement is required. In the case of interleaved DC–DC converters, degradation occurs between transistors and capacitors. In particular, transistor degradation imbalances cause an increase in output capacitor RMS current, which increases power loss and accelerates capacitor degradation. This degradation affects system reliability by increasing thermal stress. In this paper, based on a degraded 2-leg interleaved DC–DC boost converter, research to reduce the converter's output capacitor RMS current was conducted. The output capacitor RMS current according to the transistor degradation imbalance was analyzed. As a result, it was confirmed that the transistor degradation imbalance causes an increase in the capacitor RMS current. To address this issue, a phase optimization algorithm for reducing increased capacitor RMS current is presented in this paper. Next, the phase optimization algorithm is mathematically analyzed. Finally, its efficacy is proved through simulations and experiments.

Keywords: silicon carbide MOSFET; degradation; 2-leg interleaved DC–DC boost converter; capacitor RMS current; phase optimization



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1. Introduction

Numerous studies are being conducted to enhance the efficiency and performance of DC–DC converters. For increasing their efficiency, interleaved DC–DC converters are being actively developed. Interleaved DC–DC converters are being actively used to increase converter efficiency, and various topologies have been developed, including interleaved buck, boost, buck–boost, SEPIC, and the Cuk converter [1–3]. The interleaved buck converter is used to step down the voltage, the interleaved boost converter is used to step up the voltage, and the interleaved buck–boost is a hybrid of the two. The interleaved SEPIC and Cuk converters have a structure in which an additional capacitor is connected between the input inductor and the output terminal. A number of inductors can be connected to the input terminal of interleaved DC–DC converters. In addition, currents with different phases flow through the legs to which the inductors are connected. Interleaved converters are generally used in two forms: 2-leg and 3-leg. Furthermore, they have the advantages of reduced inductor size and increased switching frequency. However, interleaved DC–DC converters require more transistors compared to conventional DC–DC converters, meaning degradation in terms of imbalance can occur between the transistors. This degradation imbalance increases the thermal stress of certain transistors, which can result in system failure. When transistors fail, a gate-source short or drain-source short can occur, which affect other circuit components and the entire power conversion system. Moreover, degradation not only occurs in transistors but also in capacitors. When capacitors are degraded, the equivalent series resistance (ESR) value increases. As a result, the increased ESR causes a decrease in efficiency and reliability of the system. Thus, the degradation of transistors and capacitors increases their power losses, accelerating the

degradation. Accordingly, since interleaved DC–DC converters are mainly used in mobility systems, research has been actively conducted on improving their reliability [4–7].

Transistors and capacitors are generally considered the main causes of failure in converters [4,8]. To estimate the degradation state of transistors and capacitors, loss models and thermal models have been proposed. In addition, various studies have been conducted to estimate their reliability in online and offline systems [4–15]. Furthermore, the development of control algorithms to delay degradation is ongoing [15–18]. Among these various algorithms, current magnitude control algorithms have mainly been developed that reduce power losses of the more degraded leg [17,18] in which less current flows in the degraded leg and more current flows in the other leg. However, when the current magnitude difference of each leg increases, the root mean square (RMS) current of the output capacitor increases. Moreover, when the converter has been operating for an extended period, degradation of the capacitors progresses similarly to transistors. Therefore, an increase in the capacitor RMS current results in an increased risk of capacitor failure.

In this paper, a phase optimization algorithm is proposed for reducing increased capacitor RMS current. The first stage is to derive a capacitor RMS current formula (including phase variables) through a mathematical analysis. After this, the phase is optimized through the MATLAB function. Then, the optimized phase is applied to the degraded interleaved converter. To apply the phase optimization algorithm, a 2-leg interleaved DC–DC boost converter based on a silicon-carbide metal-oxide-semiconductor-field-effect-transistor (SiC-MOSFET) is used. In the past, devices such as insulated gate bipolar transistors (IGBTs) have been widely used. However, the use of SiC-MOSFETs (which are wide-bandgap (WBG) transistors) is increasing. In SiC-MOSFETs, degradation occurs in its gate oxide layer and bond wire due to the high kinetic energy of the electrons and their deterioration during operation. Accordingly, to degrade the SiC-MOSFET, a high electric field (HEF) degradation experiment is performed [19,20]. Subsequently, the current magnitude of a specific leg is reduced by using a more degraded SiC-MOSFET. Next, the changes in capacitor RMS current according to current magnitude variations are analyzed. At this time, the capacitor RMS current varies depending on the phase. Finally, the proposed phase optimization algorithm is verified by applying the optimized phase conditions to experiments and simulations.

In Section 2, the characteristics of conventional 2-leg interleaved converters are analyzed, and a mathematical analysis of the phase optimization algorithm is conducted in Section 3. In Section 4, the results of applying the proposed phase optimization algorithm to a simulation are analyzed. Finally, the experimental results and conclusions are presented in Sections 5 and 6, respectively.

2. Conventional Interleaved DC–DC Boost Converter

There are various interleaved converter topologies, such as interleaved buck, boost, buck–boost, SEPIC, and Cuk converters. In this paper, research is conducted on a 2-leg interleaved DC–DC boost converter. In conventional 2-leg interleaved DC–DC boost converters, two inductors are connected to the input side in parallel, and the input currents flowing through each inductor are controlled by transistors. Moreover, these currents have a phase difference of 180° . A circuit diagram of the converter used in this paper is displayed in Figure 1a. The line connected to L1 is termed L1-leg, while the line connected to L2 is termed L2-leg. The 2-leg interleaved converter uses two transistors, and the output voltage is controlled by adjusting their duty cycle (D). In Figure 1a, V_i is input voltage, and V_o is output voltage. The transistor and diode connected to the L1-leg are M1 and D1, and the transistor and diode connected to the L2-leg are M2 and D2. $i_{L,1}$ and $i_{L,2}$ are inductor currents of L1-leg and L2-leg, respectively. $i_{D,1}$ is the current flowing through D1, and $i_{D,2}$ is the current flowing through D2. i_c and i_o are output capacitor current and output load current, respectively. In interleaved DC–DC converters, the output voltage and inductor current are controlled by a digital signal processor, usually a proportional-integral (PI) controller. Next, the output value of the PI controller is compared with the carrier, and the

generated switching signal is transmitted to the transistors (M1, M2) through the gate driver. In this paper, the converter operates in continuous conduction mode (CCM). The inductor current waveform of each leg is displayed in Figure 1b. One period of inductor current (T_s) is the reciprocal of the switching frequency. For the L1-leg current, the transistor (M1) turns on, and the inductor current increases during the applied time (DT_s). Subsequently, from (DT_s) to (T_s), the transistor is turned off, and the inductor current decreases. In addition, a current that has a phase difference of 180° from the current of the L1-leg flows in the L2-leg. For the L2-leg current, transistor (M2) turns on at ($0.5T_s$), and the inductor current increases during the applied time (DT_s). Subsequently, from ($D + 0.5$) T_s to ($1.5T_s$), the transistor is turned off, and the inductor current decreases. Here, I_r is the reference current value flowing through the inductor of each leg.

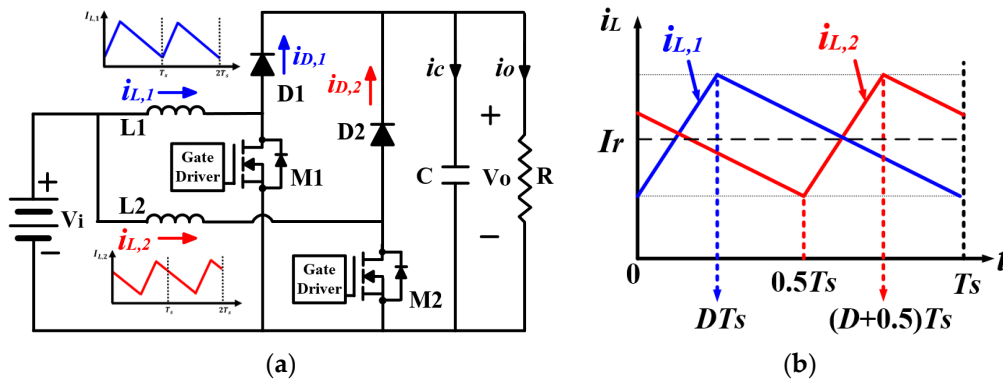


Figure 1. Conventional 2-leg interleaved DC–DC boost converter: (a) circuit diagram; (b) inductor current waveform of each leg.

When degradation occurs in a specific leg of a transistor, thermal stress increases due to the increased drain-source on-resistance (ΔR_{DS}). Since this can cause accelerated degradation of the transistor, methods for reducing the current magnitude of the degraded leg have been proposed. Figure 2a shows the inductor current waveform assuming that the L1-leg of the transistor is degraded. In addition, the inductance of each leg has the same value as L (i.e., $L_1 = L_2 = L$). To reduce power losses of the transistor in the L1-leg, the current magnitude is reduced, and the current magnitude of the L2-leg is increased by a corresponding value.

As demonstrated in Figure 2a, when the current magnitude of each leg changes by ΔI , the average current in each leg inductor ($I_{r,1}$, $I_{r,2}$) can be calculated using Equations (1) and (2).

$$I_{r,1} = I_r - \Delta I, \tag{1}$$

$$I_{r,2} = I_r + \Delta I. \tag{2}$$

When the duty cycle is less than 0.5, the expression for the inductor current of each leg displayed in Figure 2a is calculated as follows:

$$i_{L,1}(t) = \begin{cases} I_{r,1} - \frac{V_i D_1 T_s}{2L} + \frac{V_i t}{L}, & (0 \leq t < D_1 T_s) \\ I_{r,1} + \frac{V_i D_1 T_s}{2L} + \frac{(V_i - V_o)(t - D_1 T_s)}{L}, & (D_1 T_s \leq t < T_s) \end{cases}, \tag{3}$$

$$i_{L,2}(t) = \begin{cases} I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(0.5 - D_2) T_s}{L} + \frac{(V_i - V_o)t}{L}, & (0 \leq t < 0.5 T_s) \\ I_{r,2} - \frac{V_i D_2 T_s}{2L} + \frac{V_i(t - 0.5 T_s)}{L} & (0.5 T_s \leq t < (0.5 + D_2) T_s) \\ I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)t}{L} - \frac{(V_i - V_o)(0.5 + D_2) T_s}{L} & ((0.5 + D_2) \leq t < T_s) \end{cases}, \tag{4}$$

where V_i is the input voltage, V_o is the output voltage, D_1 is the duty cycle applied to the L1-leg of the transistor, and D_2 is the duty cycle applied to the L2-leg of the transistor.

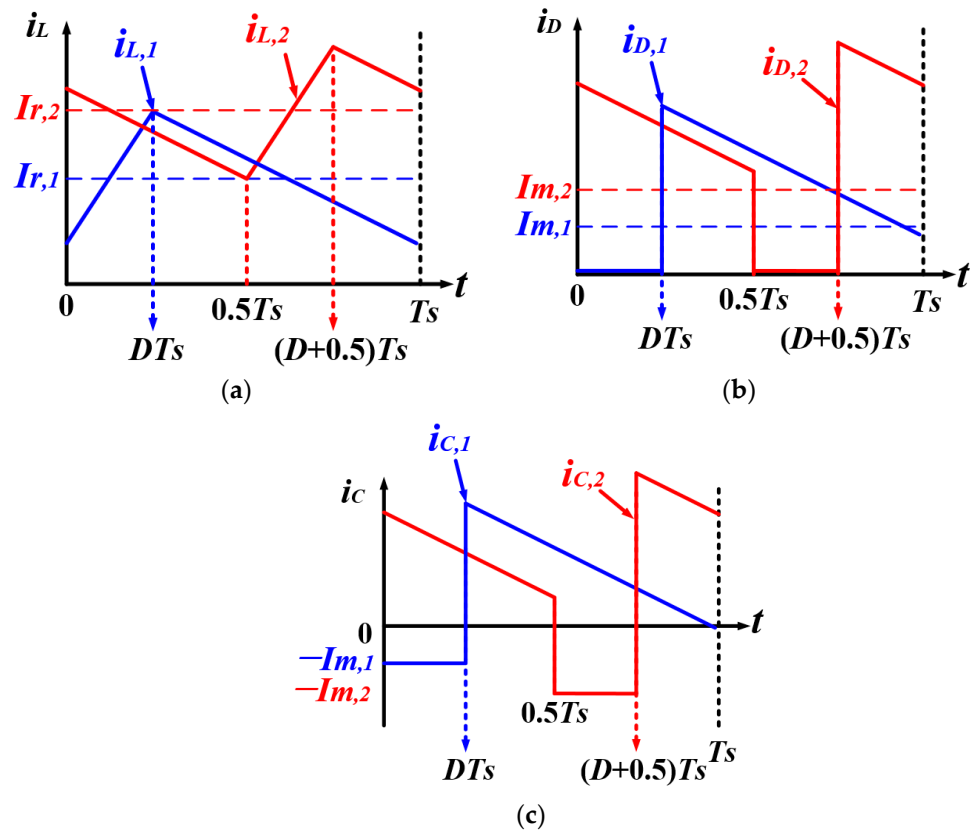


Figure 2. (a) Inductor current waveform of each leg. (b) Diode current waveform of each leg. (c) Capacitor current waveform by each leg.

Figure 2b shows the diode current waveform of each leg. Since the diode current only flows when the transistor is off, it is calculated as follows:

$$i_{D,1}(t) = \begin{cases} 0, & (0 \leq t < D_1 T_s) \\ I_{r,1} + \frac{V_i D_1 T_s}{2L} + \frac{(V_i - V_o)(t - D_1 T_s)}{L}, & (D_1 T_s \leq t < T_s) \end{cases} \quad (5)$$

$$i_{D,2}(t) = \begin{cases} I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(0.5 - D_2) T_s}{L} + \frac{(V_i - V_o)t}{L}, & (0 \leq t < 0.5 T_s) \\ 0, & (0.5 T_s \leq t < (0.5 + D_2) T_s) \\ I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)t}{L} - \frac{(V_i - V_o)(0.5 + D_2) T_s}{L}, & ((0.5 + D_2) \leq t < T_s) \end{cases} \quad (6)$$

In addition, the average value of the diode current of each leg ($I_{m,x}$ ($x = 1$ or 2)) is calculated as follows:

$$I_{m,x} = \frac{1}{T_s} \int_0^{T_s} i_{D,x}(t) dt. \quad (7)$$

Next, subtracting the average value of the diode in each leg (Equation (7)) from Equations (5) and (6), the capacitor current formula of each leg is calculated as follows:

$$i_{C,1}(t) = \begin{cases} -I_{m,1}, & (0 \leq t < D_1 T_s) \\ I_{r,1} + \frac{V_i D_1 T_s}{2L} + \frac{(V_i - V_o)(t - D_1 T_s)}{L} - I_{m,1}, & (D_1 T_s \leq t < T_s) \end{cases} \quad (8)$$

$$i_{C,2}(t) = \begin{cases} I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(0.5 - D_2) T_s}{L} + \frac{(V_i - V_o)t}{L} - I_{m,2}, & (0 \leq t < 0.5 T_s) \\ -I_{m,2}, & (0.5 T_s \leq t < (0.5 + D_2) T_s) \\ I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)t}{L} - \frac{(V_i - V_o)(0.5 + D_2) T_s}{L} - I_{m,2}, & ((0.5 + D_2) \leq t < T_s) \end{cases} \quad (9)$$

Equations (8) and (9) are the capacitor currents of each leg and are displayed in Figure 2c. The output capacitor RMS current ($I_{C,RMS}$) is calculated with Equation (10) using Equations (8) and (9). Next, $I_{C,RMS}$ is calculated by increasing the current variation (ΔI) of each leg, as displayed in Figure 3.

$$I_{C,RMS} = \sqrt{\frac{1}{T_s} \int_0^{T_s} \{i_{C,1}(t) + i_{C,2}(t)\}^2 dt} \quad (10)$$

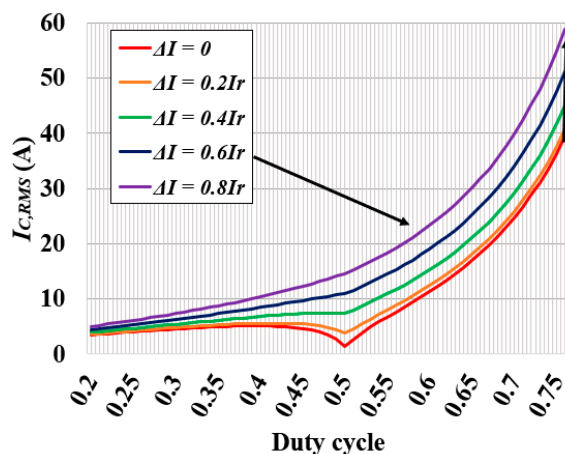


Figure 3. $I_{C,RMS}$ variation according to the amount of inductor current change (ΔI).

As demonstrated in Figure 3, as ΔI increases, $I_{C,RMS}$ also increases. Furthermore, the capacitor power loss (P_{cap}) is calculated as follows:

$$P_{cap} = ESR_f \times (I_{C,RMS})^2, \quad (11)$$

where ESR_f is the equivalent resistance of the capacitor and depends on the frequency (f) [5,6,14]. Therefore, the increase in $I_{C,RMS}$ results in an increase in the capacitor power loss and thermal stress. In other words, increasing ΔI delays further degradation of the degraded transistors while accelerating the degradation of the output capacitor. As capacitor degradation progresses in accordance with the transistor, the accelerated degradation of the capacitor reduces the reliability of the system. To solve this problem, the next sections explain a phase optimization algorithm that minimizes increases in $I_{C,RMS}$ according to increases in ΔI .

3. Mathematical Analysis of Proposed Phase Optimization Algorithm

In this section, to reduce $I_{C,RMS}$, a mathematical analysis of the optimization phase is explained when ΔI is increased. For this optimization, the phase of the L2-leg current is shifted by " a " T_s from the conventional phase ($0.5 T_s$). $I_{C,RMS}(a)$ is a formula that includes the phase variable " a " and is calculated using Equations (12)–(18). However, as demonstrated in Equations (12) and (13), " $i_{C,1}(t) + i_{C,2}(a, t)$ " varies according to the amount of phase shift $a \times T_s$. In other words, $I_{C,RMS}(a)$ is calculated as the square of Equation (13), and Equation (12) depends on the range of " a ". When D_1 and D_2 are less than 0.5, the range of " a " is classified into the three intervals (i), (ii), and (iii), as shown in Figure 4.

For example, since “ $i_C(a, t) = i_{C,1}(t) + i_{C,2}(a, t)$ ” has different values when $t < D_1T_s$, the integral interval must be different. Therefore, $i_{C,2}(a, t)$ and $I_{C,RMS}(a)$ in the three intervals are calculated using Equations (14)–(18).

$$I_{C,RMS}(a) = \sqrt{\frac{1}{T_s} \int_0^{T_s} \{i_C(a, t)\}^2 dt}, \tag{12}$$

$$i_C(a, t) = i_{C,1}(t) + i_{C,2}(a, t), \tag{13}$$

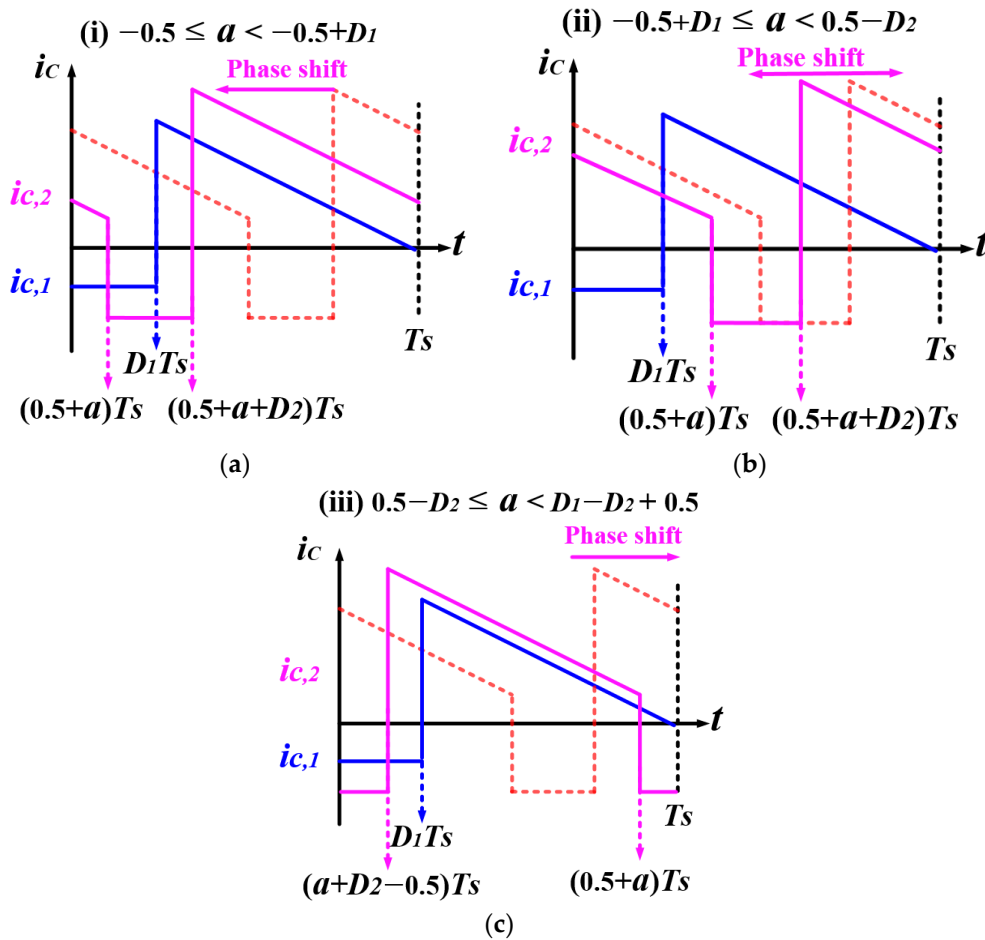


Figure 4. Capacitor current waveforms with phase shift. (a) at interval (i) $-0.5 \leq a < -0.5 + D_1$, (b) at interval (ii) $-0.5 + D_1 \leq a < 0.5 - D_2$, (c) at interval (iii) $0.5 - D_2 \leq a < D_1 - D_2 + 0.5$.

(i) $-0.5 \leq a < -0.5 + D_1$

$$i_{C,2}(a, t) = \begin{cases} I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(0.5 - D_2 - a)T_s}{L} + \frac{(V_i - V_o)t}{L} - I_{m,2}, & (0 \leq t < (a + 0.5)T_s) \\ -I_{m,2}, & ((a + 0.5)T_s \leq t < (a + 0.5 + D_2)T_s) \\ I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(t - (a + 0.5 + D_2)T_s)}{L} - I_{m,2}, & ((a + 0.5 + D_2) \leq t < T_s). \end{cases} \tag{14}$$

At $-0.5 \leq a < -0.5 + D_1$, the capacitor RMS current is calculated using Equations (8) and (12)–(14), which gives Equation (15).

$$I_{C,RMS}(a) = \left[\frac{1}{T_s} \left(\int_0^{(0.5+a)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5)T_s}^{D_1 T_s} \{i_C(a,t)\}^2 dt + \int_{D_1 T_s}^{(a+0.5+D_2)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5+D_2)T_s}^{T_s} \{i_C(a,t)\}^2 dt \right) \right]^{1/2}. \tag{15}$$

(ii) $-0.5 + D_1 \leq a < 0.5 - D_2$

At $-0.5 + D_1 \leq a < 0.5 - D_2$, using Equations (8) and (14), the capacitor RMS current is calculated through Equations (12) and (13), which gives Equation (16).

$$I_{C,RMS}(a) = \left[\frac{1}{T_s} \left(\int_0^{D_1 T_s} \{i_C(a,t)\}^2 dt + \int_{D_1 T_s}^{(a+0.5)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5)T_s}^{(a+0.5+D_2)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5+D_2)T_s}^{T_s} \{i_C(a,t)\}^2 dt \right) \right]^{1/2}. \tag{16}$$

(iii) $0.5 - D_2 \leq a < 0.5$

At $0.5 - D_2 \leq a < 0.5$, using Equations (8) and (17), the capacitor RMS current is calculated through Equations (12) and (13), which gives Equation (18).

$$i_{C,2}(a,t) = \begin{cases} -I_{m,2}, & (0 \leq t < (a + D_2 - 0.5)T_s) \\ I_{r,2} + \frac{V_i D_2 T_s}{2L} + \frac{(V_i - V_o)(t - (a + D_2 - 0.5)T_s)}{L} - I_{m,2}, & ((a + D_2 - 0.5)T_s \leq t < (a + 0.5)T_s) \\ -I_{m,2}, & ((a + 0.5) \leq t < T_s) \end{cases}, \tag{17}$$

$$I_{C,RMS}(a) = \left[\frac{1}{T_s} \left(\int_0^{(a+D_2-0.5)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+D_2-0.5)T_s}^{D_1 T_s} \{i_C(a,t)\}^2 dt + \int_{D_1 T_s}^{(a+0.5)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5)T_s}^{T_s} \{i_C(a,t)\}^2 dt \right) \right]^{1/2}. \tag{18}$$

When the duty cycle is ≥ 0.5 , the $I_{C,RMS}(a)$ formula can be derived in the same way as when the duty cycle is < 0.5 . When D_1, D_2 are ≥ 0.5 , the range of "a" is classified into three sections in the same way as when the duty cycle is < 0.5 . Therefore, the capacitor current $i_{C,2}(a,t)$ and the capacitor RMS current $I_{C,RMS}(a)$ in each section are calculated by Equations (15), (18), and (19). When the duty cycle is ≥ 0.5 , like (i), $I_{C,RMS}(a)$ is calculated through Equations (8) and (12)–(15), at $D_1 - D_2 - 0.5 \leq a < 0.5 - D_2$. Next, at $0.5 - D_2 \leq a < D_1 - 0.5$, using Equations (8) and (18), which is the capacitor current, the capacitor RMS current is calculated using Equations (12) and (13), which is Equation (19).

$$I_{C,RMS}(a) = \left[\frac{1}{T_s} \left(\int_0^{(a+D_2-0.5)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+D_2-0.5)T_s}^{(a+0.5)T_s} \{i_C(a,t)\}^2 dt + \int_{(a+0.5)T_s}^{D_1 T_s} \{i_C(a,t)\}^2 dt + \int_{D_1 T_s}^{T_s} \{i_C(a,t)\}^2 dt \right) \right]^{1/2}. \tag{19}$$

At $D_1 - 0.5 \leq a < D_1 - D_2 + 0.5$, like (iii), using Equations (8) and (17), which is the capacitor current, the capacitor RMS current is calculated using Equations (12) and (13), which is Equation (18).

Based on the previous analysis, the optimized phase value, a , that minimizes the capacitor RMS current is obtained through a MATLAB function. Subsequently, the optimized phase value, a , is converted into degrees ($\Delta\theta$). The relationship between $\Delta\theta$ and, a is then calculated using Equation (20). Here, $\Delta\theta$ is the phase degree difference between the L1-leg and the L2-leg.

$$\Delta\theta = (a + 0.5)360^\circ. \tag{20}$$

Figure 5 shows the corresponding optimized angle ($\Delta\theta$) when current variation ΔI is between $0.2I_r$ and $0.8I_r$. As seen in Figure 5, when the duty cycle is < 0.5 , $I_{C,RMS}(a)$ is minimized when $a'' = -0.5 + D_1$. In addition, when ΔI increases, it is evident that $\Delta\theta$, which minimizes $I_{C,RMS}(a)$, converges to 180° as the duty cycle increases from 0 to 0.5. Here, $I_{C,RMS,op}$ is the capacitor RMS current when the phase is optimized, and $I_{C,RMS,180}$ is the capacitor RMS current when the phase difference between the two legs is 180° . Figure 6 shows the change of $I_{C,RMS}(a)$ between when the phase difference between the two legs is 180° and when the 2-leg interleaved converter's phase is optimized. The capacitor RMS current decreases when the phase is optimized, as displayed in Figure 6. Simulations

and experiments were then conducted to confirm that the proposed phase optimization algorithm decreased the capacitor RMS current.

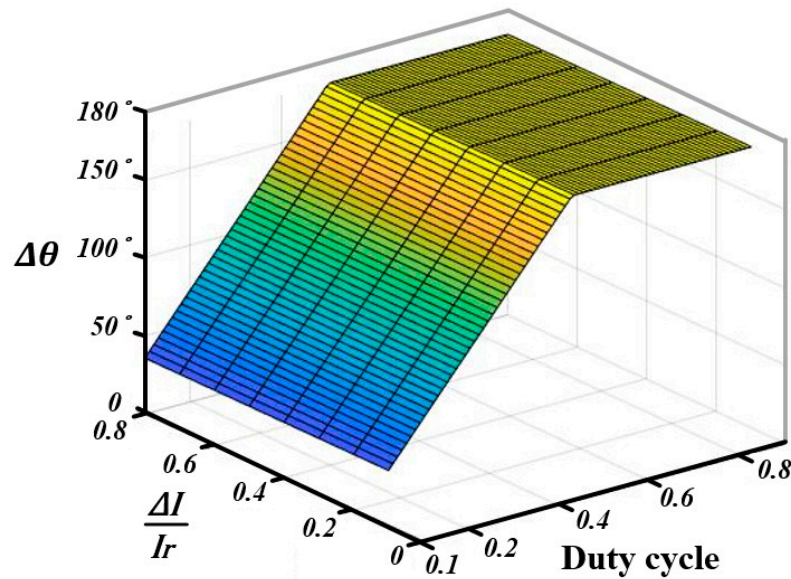


Figure 5. Minimization $I_{C,RMS}$ optimization phase graph.

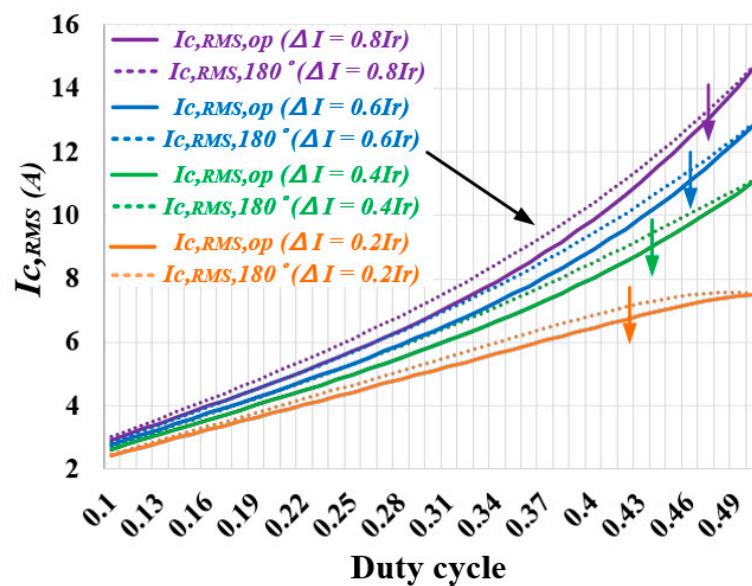


Figure 6. Variation of $I_{C,RMS}$ before and after phase optimization.

4. Simulation Results of Proposed Phase Optimization Algorithm

Simulations were conducted based on the phase optimization described in Section 3. Here, a PSIM (PowerSIM) simulator was used to operate the 2-leg conventional interleaved DC–DC converter shown in Figure 1a. Table 1 presents the circuit parameter values of the converter.

Assuming degradation of the L1-leg of the transistor, the current flowing through the L1-leg was reduced in the simulation. Then, the output capacitor RMS current was compared between when the phase difference of the two legs was 180° and when the phase was optimized. Figure 7 shows the capacitor RMS current when the phase difference between the two legs was 180° . First, when the duty cycle = 0.1, $I_{C,RMS}$ was increased by 0.09 A ($\Delta I = 0.2I_r$) to 1.69 A ($\Delta I = 0.8I_r$), and when the duty cycle = 0.2, $I_{C,RMS}$ was increased by 2.11 A ($\Delta I = 0.2I_r$) to 4.19 A ($\Delta I = 0.8I_r$). Next, when the duty cycle = 0.3, $I_{C,RMS}$ was increased by 3.73 A ($\Delta I = 0.2I_r$) to 7.54 A ($\Delta I = 0.8I_r$), and when the duty cycle

= 0.4, $I_{C,RMS}$ was increased by 4.4 A ($\Delta I = 0.2I_r$) to 12.22 A ($\Delta I = 0.8I_r$). Additionally, when the duty cycle = 0.5, $I_{C,RMS}$ was increased by 2.53 A ($\Delta I = 0.2I_r$) to 18.93 A ($\Delta I = 0.8I_r$). The figure shows the same result as presented in Section 3, and it is evident that $I_{C,RMS}$ increased as ΔI increased.

Table 1. Circuit parameters of the simulation.

Circuit Parameters	
L1	1 mH
L2	1 mH
Switching Frequency	20 kHz
R	22 Ω
C	680 μ F
Vi	200 V

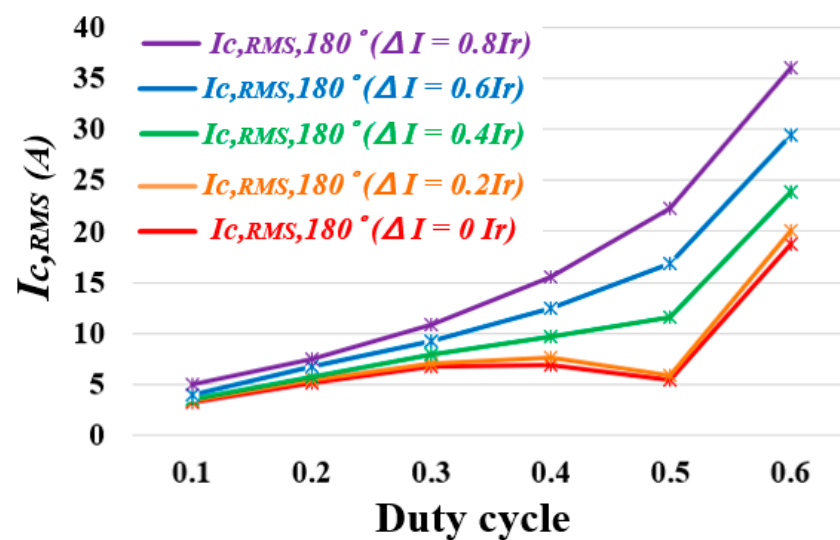


Figure 7. Simulation result: amount of change in $I_{C,RMS,180}$ according to increases in ΔI .

Figure 8 shows the reduction rate of the capacitor RMS current $\Delta I_{C,RMS}(\%)$ when the proposed phase optimization algorithm was performed compared to $I_{C,RMS,180}$. This was calculated using Equation (21). As seen in Figure 8, the capacitor RMS current decreased after optimization, which agreed with the result in Section 3. The capacitor RMS current was reduced by up to 10% after applying the phase optimization algorithm, and the reduction rate was 3% to 5% on average.

$$\Delta I_{C,RMS}(\%) = \frac{(I_{C,RMS,op} - I_{C,RMS,180}) \times 100}{I_{C,RMS,180}}(\%) \quad (21)$$

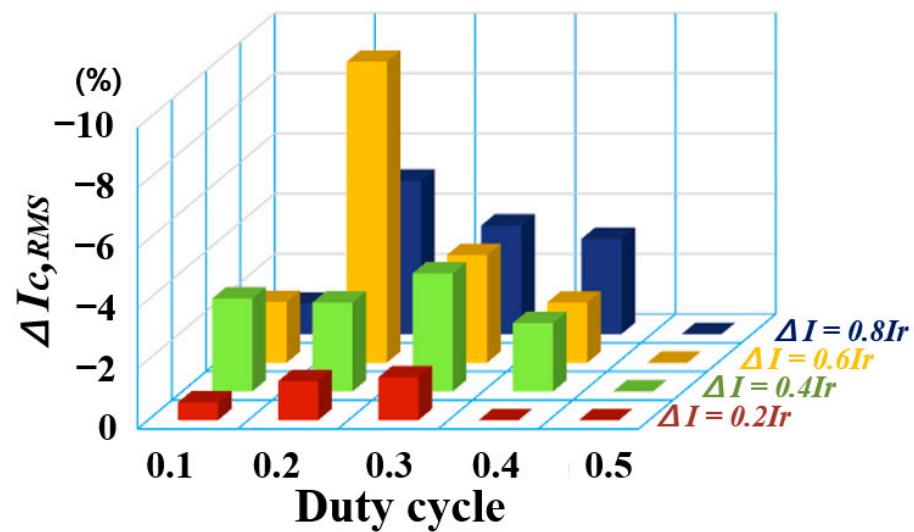


Figure 8. Capacitor RMS current reduction rate when applying the proposed phase optimization algorithm in a simulation.

5. Experiment Results

To prove that the proposed 2-leg interleaving DC–DC converter phase optimization algorithm was effective, experiments were conducted following the simulation presented in Section 4 using the converter presented in Figure 1a (as in the simulation). The experimental setup is displayed in Figure 9. The same circuit parameters as those in Table 1 were also used. However, the converter was controlled by applying 48 V as the input voltage. An RSP-1000-48 power supply was used to apply the input voltage. A TMS320F28335 digital signal processor (DSP) was used to control the switching signal. The diodes used in the test were type UJ2D1230K, and the transistors were type SCT3080AL (SiC–MOSFET, $V_{DSS} = 650$ V, $R_{DS} = 80$ m Ω , $I_{DS} = 30$ A) manufactured by ROHM. The capacitor used in the experiment had a rated voltage of 400 V, a capacitance of 680 μ F, and an ESR of 366 m Ω (20 °C, 120 Hz). The 2-leg interleaved converter was basically controlled in CCM mode. Next, the output capacitor RMS current was compared between when the phase difference of the two legs was 180° and when the phase was optimized. To confirm this, degraded transistors were used in the L1-leg (M1) to decrease its current magnitude. The four types of degraded transistors were labelled A, B, C, and D and were degraded through the HEF experiment. The resistance variations ΔR_{DS} and current variation conditions when using the transistors are displayed in Table 2. ΔR_{DS} of degraded transistor A was 0.107 Ω . When using A, ΔI was $0.1I_r$. ΔR_{DS} of degraded transistor B was 0.154 Ω . When using B, ΔI was $0.2I_r$. ΔR_{DS} of degraded transistor C was 0.523 Ω . When using C, ΔI was $0.3I_r$. ΔR_{DS} of degraded transistor D was 1.23 Ω . When using D, ΔI was $0.4I_r$. Subsequently, the changes in capacitor RMS current according to current variations were analyzed. Figure 10 shows the experimental results, which indicated a change in $I_{C,RMS,180}$ according to the increase in ΔI . The experiment was conducted while changing ΔI from $0.1I_r$ to $0.4I_r$. As a result, the $I_{C,RMS}$ values increased as ΔI increased, similar to the results from Sections 3 and 4. In addition, it was evident that the larger the duty cycle, the larger the increase in $I_{C,RMS}$. Then, to reduce the increased capacitor RMS current, the phase optimization algorithm was applied. Figure 11 shows the experimental results before and after phase optimization. When the duty cycle was 0.3, the output voltage, capacitor current, and each inductor current were measured. Figure 11a demonstrates that the inductor current magnitudes of each leg were the same when the converter’s transistors were not degraded. Figure 11b presents the waveform when the transistor of the L1-leg was degraded. As seen in Figure 11b, the current magnitude of the L1-leg was decreased, while Figure 11c presents the waveform when phase optimization was performed. As seen in Figure 11a–c, it is evident that the output voltage and inductor current were equally controlled. Moreover, there were differences in the capacitor current

waveforms. Referring to these differences, the capacitor RMS current was calculated, and the differences were analyzed.

Table 2. Experimental conditions depending on SiC-MOSFET degradation.

	A	B	C	D
ΔR_{DS}	0.107 Ω	0.154 Ω	0.523 Ω	1.23 Ω
Current Variation (ΔI)	$0.1I_r$	$0.2I_r$	$0.3I_r$	$0.4I_r$

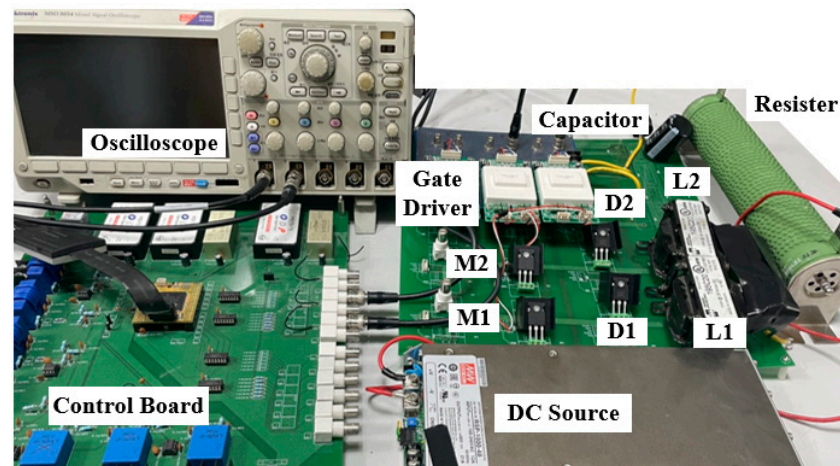


Figure 9. Experiment setup.

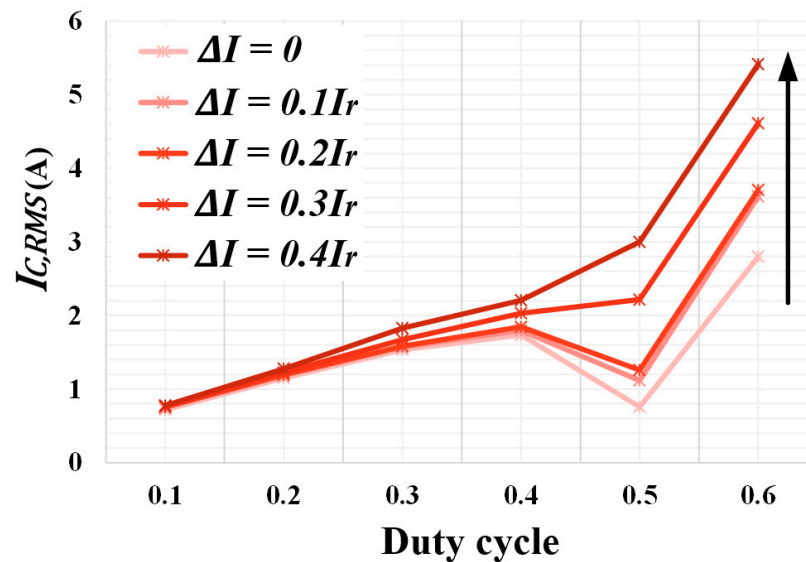


Figure 10. $I_{C,RMS,180}$ variation according to increases in ΔI .

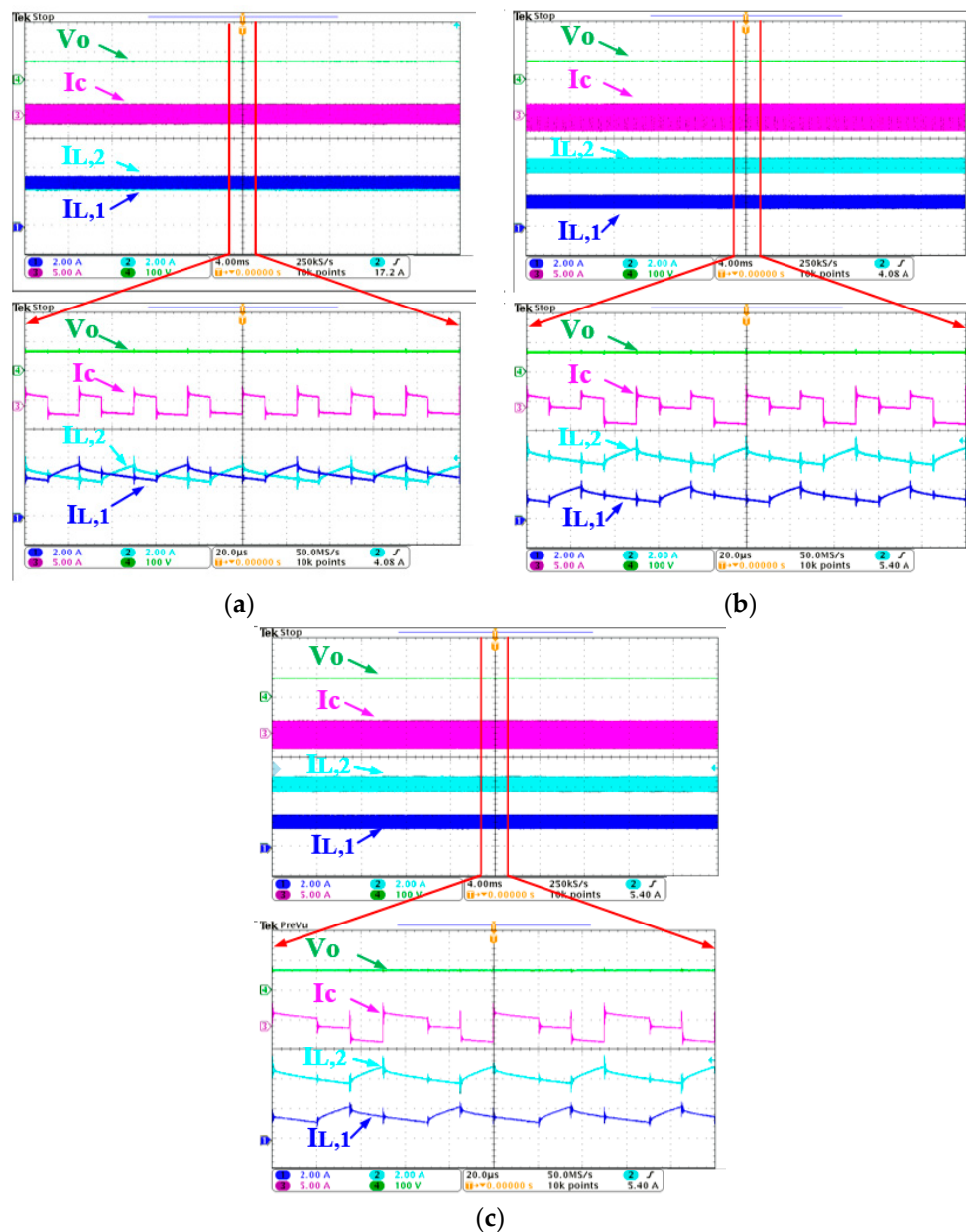


Figure 11. Interleaving converter experimental waveform with duty cycle of 0.3 (a) when there is no change in current magnitude and phase of each leg, (b) when current in L1-leg decreases, and (c) when phase optimization is performed in (b).

Figure 12 presents the experimental results that display the change in capacitor RMS current before and after phase optimization. The experiment was conducted while changing the current variation ΔI from $0.1I_r$ to $0.4I_r$. Moreover, $\Delta I_{C,RMS}(\%)$ was calculated using Equation (21), and the experimental results according to the variation of ΔI and duty cycle were analyzed. As seen in Figure 12, it is evident that $I_{C,RMS}$ decreased when using the proposed phase optimization algorithm when the phase of each leg was optimized. When the duty cycle was less than 0.4, experiments were conducted to measure $I_{C,RMS}$. First, when ΔI was $0.1I_r$, $\Delta I_{C,RMS}(\%)$ was -0.77% to -2.73% , and when ΔI was $0.2I_r$, $\Delta I_{C,RMS}(\%)$ was -1.4% to -2.9% . Next, when ΔI was $0.3I_r$, $\Delta I_{C,RMS}(\%)$ was -1.45% to -4.78% , and when ΔI was $0.4I_r$, $\Delta I_{C,RMS}(\%)$ was -2.18% to -7.49% . In particular, $I_{C,RMS}$ decreased up to 7.49% after applying the proposed phase optimization algorithm when the duty cycle was 0.3 and ΔI was $0.4I_r$. Moreover, since capacitor power loss is proportional to the square of $I_{C,RMS}$, this was reduced by 14%. In addition, it is evident that the larger

the value of ΔI , the larger the reduction rate of $\Delta I_{C,RMS}$ (%). If the degree of degradation imbalance of the transistors increased and ΔI was large, the proposed phase optimization algorithm contributed more to improving capacitor efficiency.

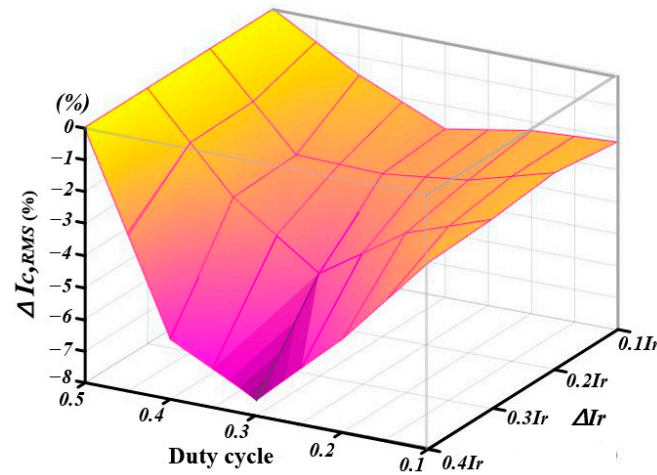


Figure 12. Capacitor RMS current reduction rate when applying the proposed phase optimization algorithm in the experiment.

6. Conclusions

In 2-leg interleaved DC–DC boost converters, the current magnitude difference of each leg can be increased due to the degradation of the imbalance between transistors. However, this increases the output capacitor RMS current and accelerates the degradation of the capacitor. Through mathematical analysis, simulations, and experiments, the increase of capacitor RMS current was confirmed. In this paper, a phase optimization algorithm was proposed to reduce the increased capacitor RMS current. Next, the phase value at which the capacitor RMS current was minimal was derived through mathematical analysis. Subsequently, simulations and experiments were conducted to apply the phase optimization algorithm. As a result, it was confirmed that the capacitor RMS current decreased when phase optimization was applied. In addition, it was revealed that the reduction rate of the capacitor RMS current was higher when the degradation imbalance of the transistors in each leg was larger.

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