

Electronics Letters

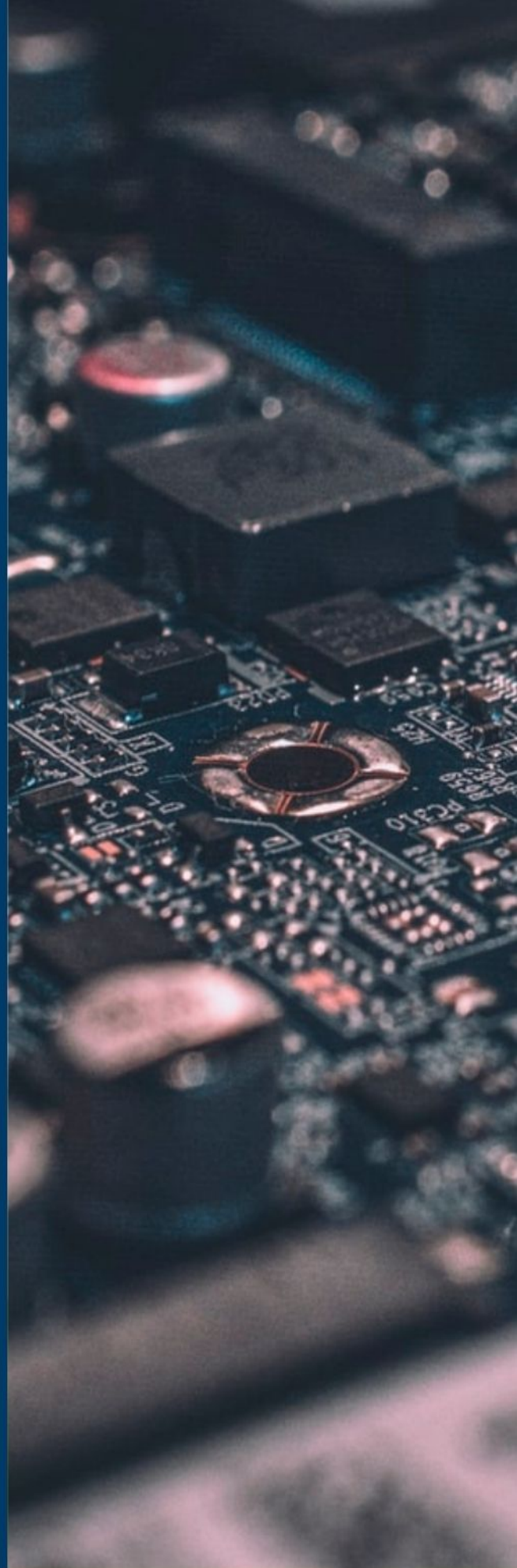
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K-band 0/180° balanced phase shifter with dc-offset cancellation

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K-band 0°/180° phase shifter MMIC based on balanced structure which can be applied to BPSK or QPSK modulator with dc-offset cancellation is presented. The proposed balanced phase shifter consists of four Lange couplers, two quarter-wave transmission lines and four switches for open and short terminations. The proposed structure implemented in GaAs 0.15-μm low noise pHEMT process ensures stable 0/180° phase shift while common-mode signals due to the mismatch in reflections by open and short are fed to the isolation port. The proposed phase shifter is verified by the phase shift of 179 ± 1.5° with the insertion loss of 4.5 ± 0.8 dB from 17.5 to 22.5 GHz. The fabricated phase shifter size is 2.2 × 2.85 mm including test pads.

Introduction: Phase shifters are one of the most widely used components in microwave applications, such as phased-arrays and communication systems. For reliable system performances, phase shifters must generate a desired relative phase shift with low insertion loss variation and good return characteristics. Thus, there have been many techniques such as a reflection type phase shifter with series and parallel LC terminating circuits [1], vector-sum based phase shifter [2] and modified rat-race structure with the Lange coupler [3]. In addition, 0/180° phase shifters configured with the combinations of directional couplers, Wilkinson dividers, or 3-dB couplers are used as BPSK modulators [4, 5]. However, these structures undergo the dc-offset problem [1, 2] or degradation in return characteristics [3] by common mode signals returning to the input owing to the mismatch in reflective circuitry. Thus, a new balanced phase shifter structure that generates stable 0/180° phase shift and cancels unwanted common-mode signal which results in dc-offset is proposed.

Design and analysis: Fig. 1 shows the schematic of the proposed balanced phase shifter configured with four Lange couplers, two quarter-wave transmission lines and four switches with two pairs in an inverted relation. When P3 and P5 are in open state, P2 and P6 are in short state and vice versa. Fig. 2 describes the operation of the proposed phase shifter with respect to control voltages such that the differential-mode signal flows to the output, while common-mode returns 0 or leakage to the isolation port. If an arbitrary voltage wave of V_1^+ is incident and control voltage is high, the voltage signals at nodes A, B, C and D can be expressed as

$$V_A^+ = \frac{1}{2\sqrt{2}} \cdot (\Gamma_S + \Gamma_O) \cdot V_1^+, \quad V_B^+ = \frac{j}{2\sqrt{2}} \cdot (-\Gamma_S + \Gamma_O) \cdot V_1^+ \quad (1)$$

$$V_C^+ = \frac{-1}{2\sqrt{2}} \cdot (\Gamma_S - \Gamma_O) \cdot V_1^+, \quad V_D^+ = \frac{-j}{2\sqrt{2}} \cdot (\Gamma_S + \Gamma_O) \cdot V_1^+$$

where Γ_S and Γ_O denote reflection coefficients of the HEMT switch corresponding to high and low control voltages, respectively. Then, the differential-mode signal to the output according to control voltages can be expressed as

$$V_{out}|_{V_{ctrl}=high} = \frac{V_4^-}{V_1^+} = \frac{-j}{\sqrt{2}} \cdot \frac{V_B}{V_1^+} + \frac{1}{\sqrt{2}} \cdot \frac{V_C}{V_1^+} = -\frac{1}{2} \cdot (\Gamma_S - \Gamma_O) = S_1 \quad (2)$$

$$V_{out}|_{V_{ctrl}=low} = \frac{V_4^-}{V_1^+} = \frac{-j}{\sqrt{2}} \cdot \frac{V_B}{V_1^+} + \frac{1}{\sqrt{2}} \cdot \frac{V_C}{V_1^+} = -\frac{1}{2} \cdot (\Gamma_O - \Gamma_S) = S_2 = -S_1 \quad (3)$$

As seen from (2) and (3), the states, S_1 and S_2 always maintain amplitude and 180° phase balances. If there is a mismatch between Γ_O and Γ_S , that is, $\Gamma_O \neq -\Gamma_S$, the balanced 0/180° phase shift is always generated at the output according to (2) and (3) with a corresponding degradation in the insertion loss.

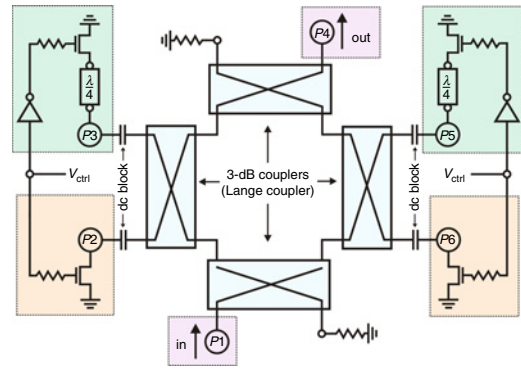


Fig. 1 Schematic of proposed 0/180° balanced phase shifter

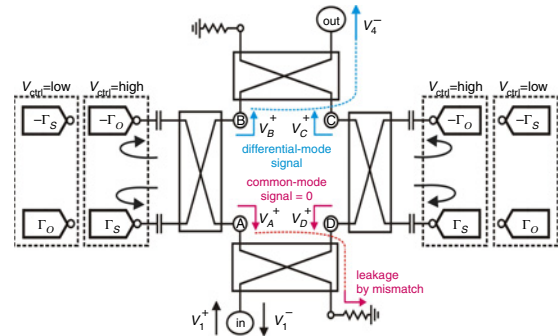


Fig. 2 Simplified schematic of proposed 0/180° balanced phase shifter with high or low control voltages

Similarly, the common-mode signal returning to the input according to control voltages can be expressed as

$$\frac{V_1^-}{V_1^+}|_{V_{ctrl}=high} = \frac{1}{\sqrt{2}} \cdot \frac{V_A}{V_1^+} + \frac{-j}{\sqrt{2}} \cdot \frac{V_D}{V_1^+} \quad (4)$$

$$= \frac{1}{4} \cdot [(\Gamma_S + \Gamma_O) - (\Gamma_S + \Gamma_O)] = 0$$

$$\frac{V_1^-}{V_1^+}|_{V_{ctrl}=low} = \frac{1}{\sqrt{2}} \cdot \frac{V_A}{V_1^+} + \frac{-j}{\sqrt{2}} \cdot \frac{V_D}{V_1^+} \quad (5)$$

$$= \frac{1}{4} \cdot [(\Gamma_O + \Gamma_S) - (\Gamma_O + \Gamma_S)] = 0$$

According to (4) and (5), the signals returning to the input is always 0. Similarly, if there is a mismatch between Γ_O and Γ_S , the common-mode signals return to the isolation port. That is, the dc-offset caused by the reflected common-mode signal can be resolved.

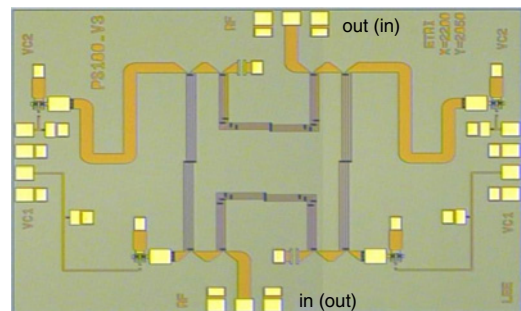


Fig. 3 Photograph of fabricated phase shifter

Measurement result: Fig. 3 shows the fabricated phase shifter using GaAs 0.15-μm low noise pHEMT process and Fig. 4 presents the measured results for the proposed phase shifter. As shown in Fig. 4a, the insertion loss is 4.5 ± 0.8 dB, while input and output return losses are always better than 15 and 12 dB, respectively, from 17.5 to 22.5 GHz. Fig. 4b shows the stable relative phase shift of 179 ± 1.5° and the insertion loss variation of 0.8 ± 0.1 dB from 17.5 to 22.5 GHz.

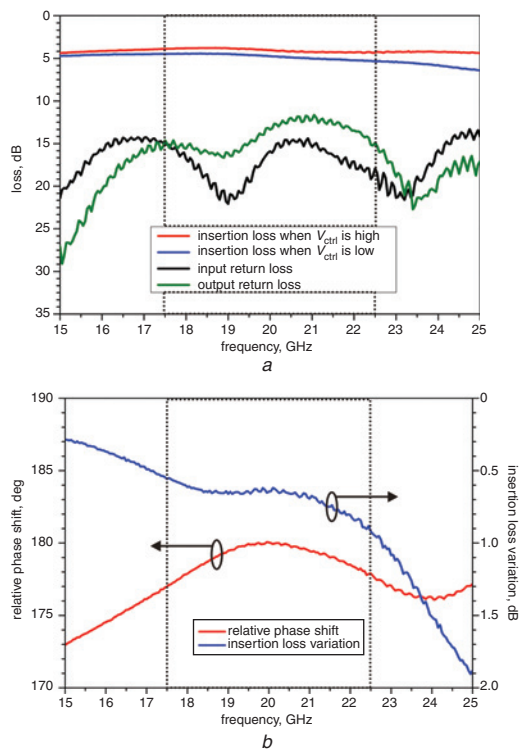


Fig. 4 Measured results for proposed phase shifter
 a Insertion losses, input and output return losses
 b Relative phase shift and insertion loss variation

Conclusion: A balanced phase shifter with a stable $0/180^\circ$ phase shift and dc-offset cancellation regardless of the mismatch in reflective circuits has been presented and verified from 17.5 to 22.5 GHz. The implemented MMIC has a chip size of 2.2×2.85 mm including test pads. The proposed phase shifter shows the relative phase shift of $179 \pm 1.5^\circ$ and the insertion loss variation of 0.8 ± 0.1 dB with input and output return losses better than 15 and 12 dB, respectively.

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One or more of the Figures in this Letter are available in colour online.

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References

- 1 Miyaguchi, K., Hieda, M., Nakahara, K., Kurusu, H., Nii, M., Kasahara, M., Takagi, T., and Urasaki, S.: 'An ultra-broad-band reflection-type phase-shifter MMIC with series and parallel LC circuit', *IEEE Trans. Microw. Theory Tech.*, 2001, **49**, (12), pp. 2446–2452
- 2 Wang, C.-W., Wu, H.-S., and Tzuan, C.-K.C.: 'CMOS passive phase shifter with group-delay deviation of 6.3 ps at K-band', *IEEE Trans. Microw. Theory Tech.*, 2011, **59**, (7), pp. 1778–1786
- 3 Mahon, S.J., Harvey, J.T., and Young, A.C.: 'Wide-band MMIC Kowari mixer/phase shifters', *IEEE Trans. Microw. Theory Tech.*, 2001, **49**, (7), pp. 1229–1234
- 4 Chang, H.-Y., Wu, P.-S., Huang, T.-W., Wang, H., Tsai, Y.-C., and Chen, C.-H.: 'An ultra compact and broadband 15–75 GHz BPSK modulator using 0.13- μ m CMOS process'. *IEEE Microwave Symp. Digest*, California, June 2005
- 5 Chang, H.-Y., Lin, C.-K., and Wang, Y.-C.: 'A 30–130 GHz ultra broadband direct-conversion BPSK modulator using a.5- μ m E/D-pHEMT process', *IEEE Microw. Compon. Lett.*, 2007, **17**, (11), pp. 805–807