sensors

MDPI

Communication

A Wideband True Time Delay Circuit Using 0.25 µm GaN HEMT Technology

Jeong-Geun Kim [1] and Donghyun Baek [2,*]

[1] Department of Electronic Engineering, Kwangwoon University, Seoul 01897, Republic of Korea; junggun@kw.ac.kr
[2] School of Electrical Engineering, Chung-Ang University, Seoul 06974, Republic of Korea
* Correspondence: dhbaek@cau.ac.kr; Tel.: +82-02-820-5828

Abstract: This paper presents a wideband 4-bit true time delay IC using a 0.25 µm GaN HEMT (High-Electron-Mobility Transistor) process for the beam-squint-free phased array antennas. The true time delay IC is implemented with a switched path circuit topology using DPDT (Double Pole Double Throw) with no shunt transistor in the inter-stages to improve the bandwidth and SPDT (Single Pole Single Throw) switches at the input and the output ports. The delay lines are implemented with CLC π-networks with the lumped element to ensure a compact chip size. A negative voltage generator and an SPI controller are implemented in the PCB (Printed Circuit Board) due to the lack of digital control logic in GaN technology. A maximum time delay of ~182 ps with a time delay resolution of 10.5 ps is achieved at DC–6 GHz. The RMS (Root Mean Square) time delay and amplitude error are <5 ps and <0.6 dB, respectively. The measured insertion loss is <6.8 dB and the input and output return losses are >10 dB at DC–6 GHz. The current consumption is nearly zero with a 3.3 V supply. The chip size including pads is 2.45 × 1.75 mm^2. To the authors' knowledge, this is the first demonstration of a true time delay IC using GaN HEMT technology.

Keywords: true time delay; GaN; phased array antenna

Citation: Kim, J.-G.; Baek, D. A Wideband True Time Delay Circuit Using 0.25 µm GaN HEMT Technology. *Sensors* **2023**, *23*, 6827. https://doi.org/10.3390/s23156827

Academic Editors: Stefan Moench and Tobias Erlbacher

Received: 21 May 2023
Revised: 19 July 2023
Accepted: 24 July 2023
Published: 31 July 2023

1. Introduction

Recently, wide bandgap transistors such GaN or SiC technologies are attracting attention for wideband and high-power applications due to their high breakdown voltage. GaN-on-SiC HEMT technology is popular due to its good thermal properties. There are some papers published on GaN-based amplitude and phase control circuits, such as one detailing a phase shifter and an attenuator for high-power and wideband applications [1]. Phased array antennas using the CMOS process are attracting great interest because CMOS technology can enable low size, weight, power, and cost (SWaP-C) phased array antennas for wireless communication applications [2–5]. However, the power handling capability is limited in CMOS technology due to the lower inherent breakdown voltage. Phased array antennas with a narrow bandwidth are usually used due to mostly narrowband applications. To construct a narrowband phased array antenna, a phase shifter or a switching phase from the multi-phased local oscillator is widely used. The constant phase characteristic over the frequency in the phase shifter results in a different steered antenna beam position versus the frequency, which is known as the beam squint phenomenon [6,7]. This results in a limited operation frequency bandwidth. However, a true time delay circuit providing a constant time delay over the frequency has become one of the most essential elements in wideband phased array antennas, since a true time delay can prevent beam squinting. Implementing a true time delay circuit as an integrated circuit is difficult because it requires a large chip area to realize the required time delay. Therefore, reducing the chip size is a very important design issue in true time delay design. Figure 1 shows the various true time delay circuit topologies. A true time delay can be implemented with artificial

transmission delay lines with variable capacitors, as shown in Figure 1a [8]. However, the characteristic impedance is changed when the capacitance is varied, resulting in a high variation in the return losses depending on the capacitances of the varactors. Most true time delays have been realized using an SPDT switch and an artificial time delay with GaAs or MEMS (Micro Electromechanical System) switches, as shown in Figure 1b [9–13]. Since a conventional true time delay requires many SPDT switches and inductors, which results in a high insertion loss and large chip size, the number of switches and the size of inductors should be reduced. Trombone or active distributed true time delay circuits in Figure 1c have been proposed to improve the insertion loss of the true time delay; however, they cannot provide a compact size or flat time delay performance [14–16]. To reduce the delay circuit size, an RC-only tunable delay line circuit has been implemented using CMOS technology [17]. However, it cannot be applied to microwave beamforming applications due to the high insertion loss at high frequencies.

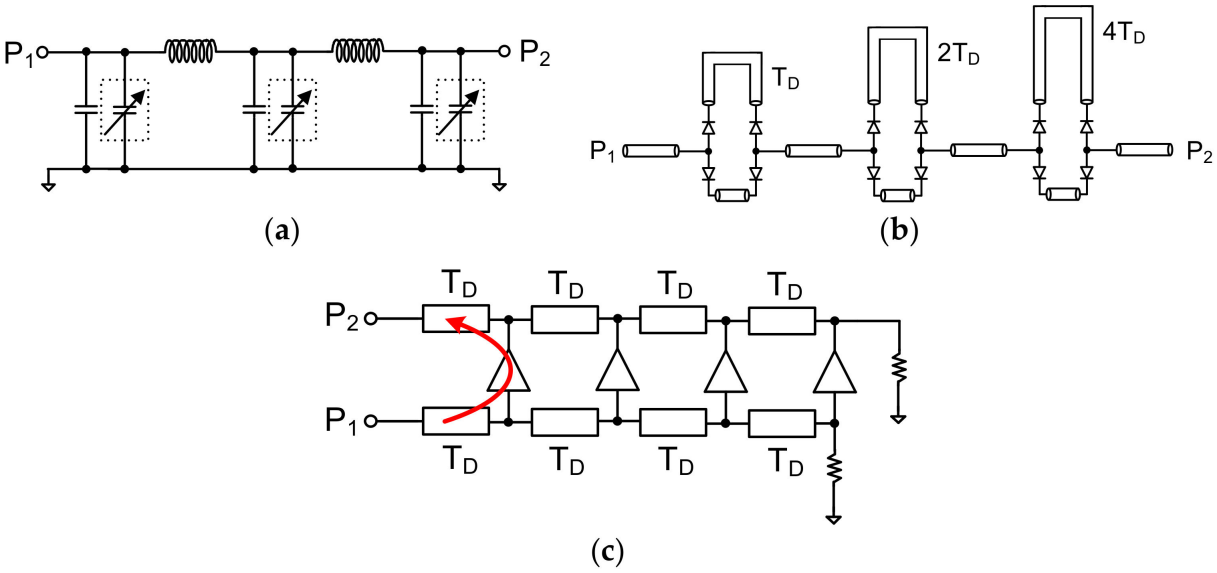


Figure 1. Various true time delay circuit topologies: (**a**) transmission delay line with variable capacitance, (**b**) switched delay line, (**c**) trombone true time delay.

In this paper, a proposed 4-bit true time delay for wideband phased array antennas is presented using 0.25 μm GaN HEMT technology.

2. Design of the GaN 4-bit True Time Delay

Figure 2 shows the proposed GaN-based 4-bit true time delay IC topology. The proposed 4-bit GaN true time delay circuit is composed of two SPDT switches at the input and output ports, three DPDT switches for the through or cross-path connections, and true time delay elements of 12.5, 25, 50, and 100 ps with LC lumped elements. Switch transistors are generally large in GaN technology; thus, the operating frequency bandwidth is limited due to the large parasitic capacitances. However, even though large switch transistors are used, the parasitic elements of the switch transistors can be nearly identical in each time delay state due to the switched path topology. This results in minimal time delay variations regardless of the time delay states. Therefore, a wide operating bandwidth can be achieved in this topology. The maximum time delay of the designed true time delay IC is 187.5 ps, with a time delay resolution of 12.5 ps. This is equivalent to 56.2 mm in electrical length in air. There are various ways to implement delay element circuits. In this design, a CLC π-network is used as shown in Figure 3. The time delay of the π-network is approximately written as:

$$T_D = n\sqrt{LC} \quad (1)$$

where n is the number of sections.

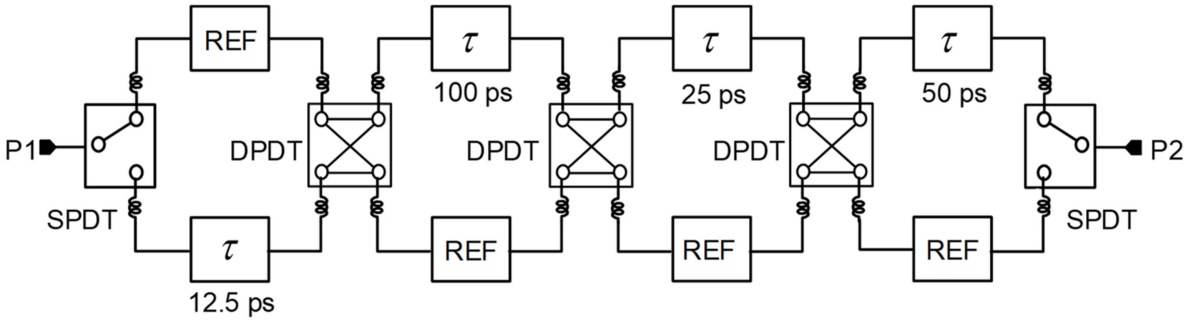


Figure 2. Schematic of the proposed wideband 4-bit GaN true time delay circuit.

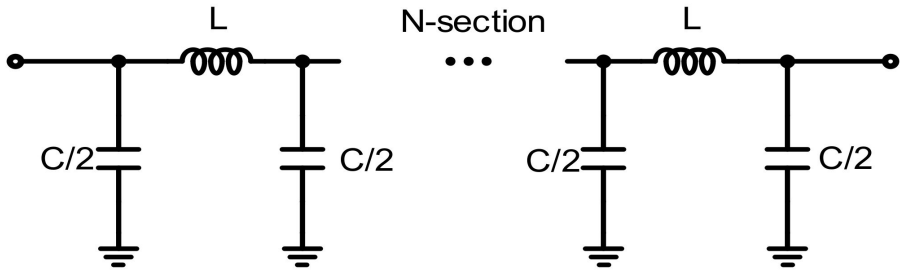


Figure 3. Schematic of the N-section time delay line with a lumped CLC π-network unit cell.

The calculated inductance of L and the capacitance of C are 338 pH and 112 fF, respectively, which obtains the required time delay of 12.5 ps with two sections of the CLC π-network, while maintaining the characteristic impedance of 50 Ω. Four, eight, and sixteen sections of the CLC π-network are used in 25 ps, 50 ps, and 100 ps, respectively. The proposed true time delay employs DPDT switches, which can reduce the number of series switching transistors in the RF signal path. Since the insertion loss of the true time delay is mainly determined by the insertion loss of the series transistors of the SPDT and DPDT switches, the number of series transistors in the RF signal path should be reduced to improve the insertion loss of the true time delay circuit. In the proposed 4-bit true time delay configuration, the RF signal passes through only five series transistors. The insertion loss can be saved by the three series transistors when it is compared to true time delay circuits implemented only with conventional SPDT switches. The proposed true time delay circuit also provides bi-directional operation since it is implemented with only passive devices. As shown in Figure 4a, the series transistors T1 and T2 are used in the SPDT switch for switching the time delay states, and the shunt transistors T3 and T4 are included to improve the RF signal isolation characteristic. For the DPDT switch, only four series transistors, T1, T2, T3, and T4, are used in the DPDT switch in Figure 4b. A reflective switch with shunt transistors is usually implemented in a DPDT switch to improve the isolation characteristic. However, they are not included in this design to reduce the parasitic shunt capacitances because small-size switch transistors are not available in commercial GaN HEMT technology. Even though isolation transistors are not included, a moderate isolation characteristic can be achieved with only series switches at less than 20 GHz. The series inductors L_1 and L_2 are implemented to enhance the input and output return loss performances in the SPDT and DPDT switches. A simulated insertion loss of less than 1.3 dB and an isolation greater than 15 dB at 12 GHz are achieved. Only two interconnecting metal layers are available in the GaN HEMT process; thus, a top–bottom stacked metal line is used to implement the inductors and the microstrip transmission lines to improve the metallic loss in the true time delay line. The shunt capacitances in the true time delay line are implemented with MIM capacitors. Electromagnetic simulation was performed carefully to design all the passive devices such as the inductors and MIM (Metal–Insulator–Metal) capacitors making up the true time delay lines and the RF interconnection lines.

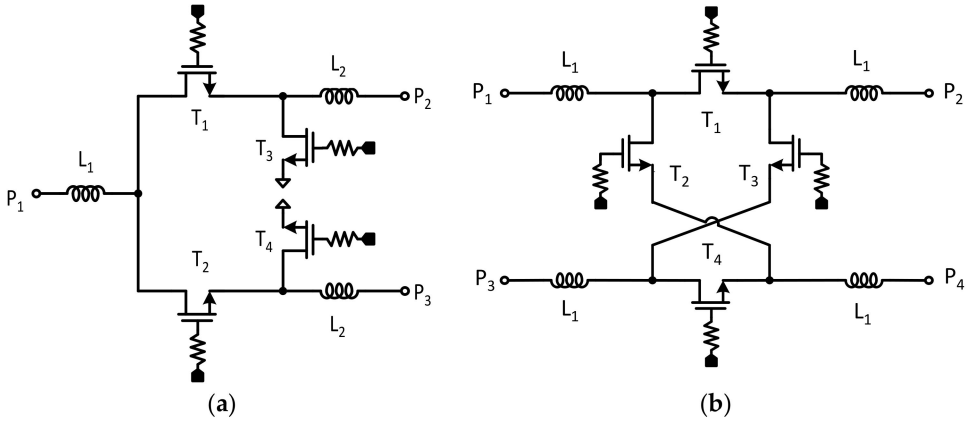


Figure 4. Schematic of (**a**) the GaN SPDT and (**b**) the GaN DPDT switch.

3. Measurement Results

The 4-bit wideband true time delay IC was fabricated using 0.25 µm GaN HEMT technology on a GaN-on-SiC substrate. A microphotograph of the 4-bit GaN true time delay IC is shown in Figure 5. The chip size is 2.45 × 1.75 mm^2, including DC and RF probing pads. The DC and the digital control pads of the GaN true time delay IC are bonded to the test PCB, which includes an external serial-to-parallel interface with a negative gate control voltage generator from the positive 3.3 V voltage to induce a digital control voltage of −3.3 V (off state) and 0 V (on state). Therefore, the complex RF switch control states in the true time delay circuit can be easily configured through the PC-programmable SPI interface. An on-state measurement was performed to characterize the GaN-based true time delay IC using a vector network analyzer and short–open–load–through (SOLT) calibration. Figure 6a shows the test pattern of the GaN SPDT switch. The measured insertion loss (S_{21}) of the GaN SPDT switch is less than 1.4 dB and the measured isolation (S_{31}) is greater than 20 dB at DC–20 GHz, as shown in Figure 6b, when the series transistor T_1 and the shunt transistor T_4 are on and the series transistor T_2 and the shunt transistor T_3 are off in Figure 4. Figure 7 shows the measured insertion loss of the GaN true time delay circuit in all sixteen time delay states. An insertion loss of 6.8 dB is achieved in the reference state at DC–6 GHz. The unwrapped phase characteristics and the relative time delay performance of the GaN true time delay IC in all sixteen time delay states are shown in Figure 8. The time delay is calculated from the measured phase of S_{21} as follows:

$$T_D = \frac{phase\ of\ S_{21}}{2\pi f} \tag{2}$$

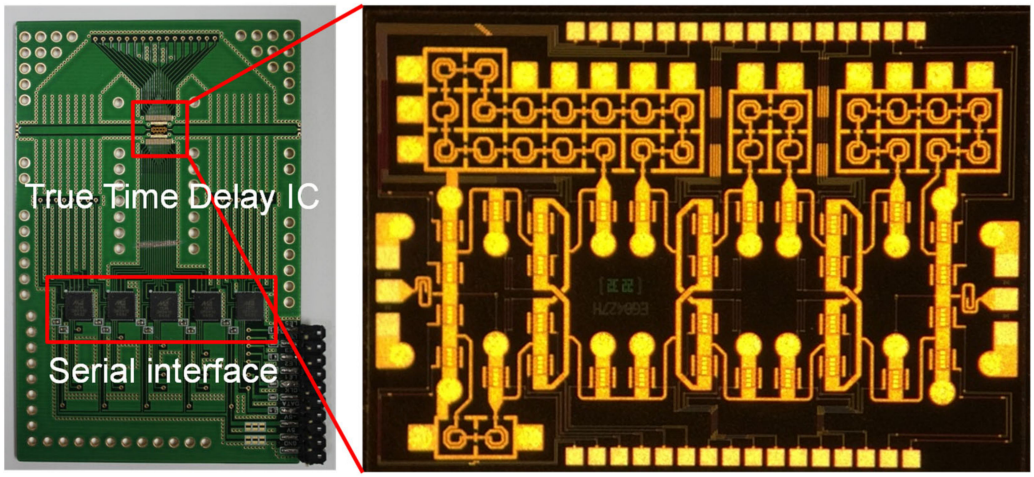
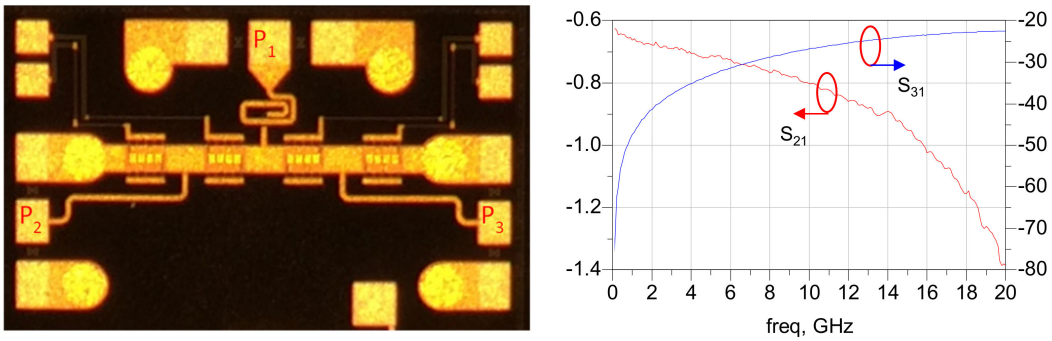


Figure 5. Microphotograph of the GaN-based true time delay circuit and test module.



(**a**) (**b**)

Figure 6. (**a**) Microphotograph of the GaN SPDT switch and (**b**) the measured insertion loss and isolation characteristics.

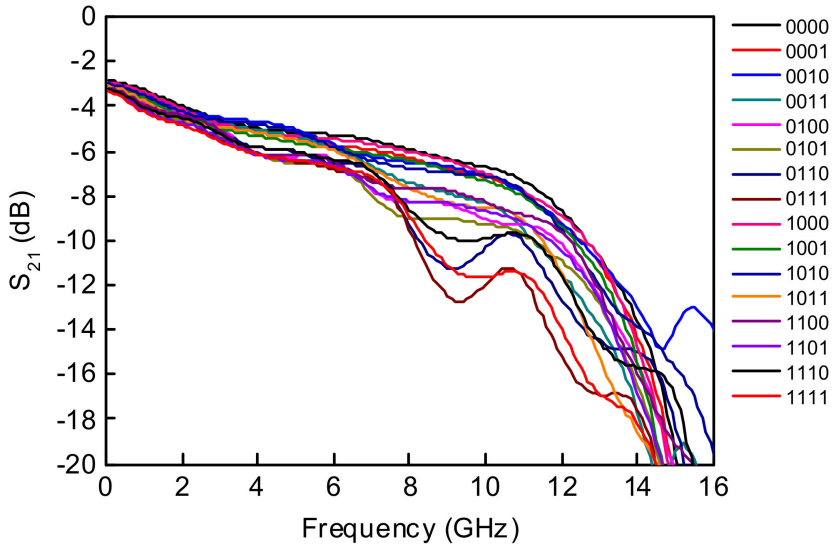
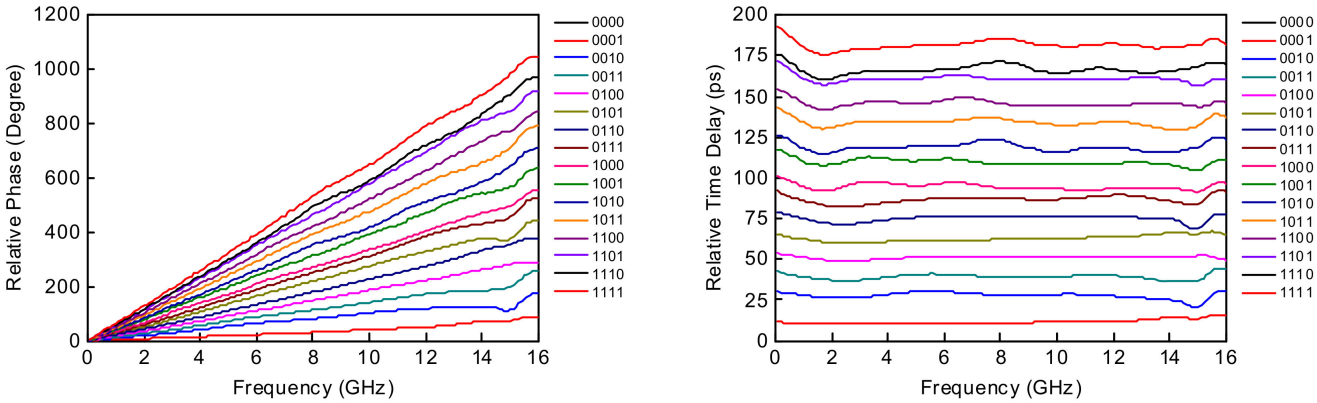


Figure 7. Measured S_{21} of the wideband 4-bit GaN-based true time delay circuit in all sixteen time delay states.



(**a**) (**b**)

Figure 8. Measured (**a**) relative unwrapped phase and (**b**) time delay characteristic of the GaN-based true time delay circuit in all sixteen time delay states.

A maximum time delay of 182 ps is achieved with a time delay resolution of 10.5 ps at 6 GHz, which is equivalent to 54.6 mm in electrical length in air. There are no overlapping time delay states and there is a flat time delay response at DC–6 GHz. Figure 9 shows the measured input and output return losses in all sixteen time delay states and >10 dB at DC–6 GHz. A measured RMS time delay error of <5 ps and an RMS amplitude error of <0.6 dB are achieved at DC–6 GHz in Figure 10. The total DC power consumption is nearly 0 mW with a 3.3 V supply voltage. The performance comparison with previously published true time delay ICs is summarized in Table 1.

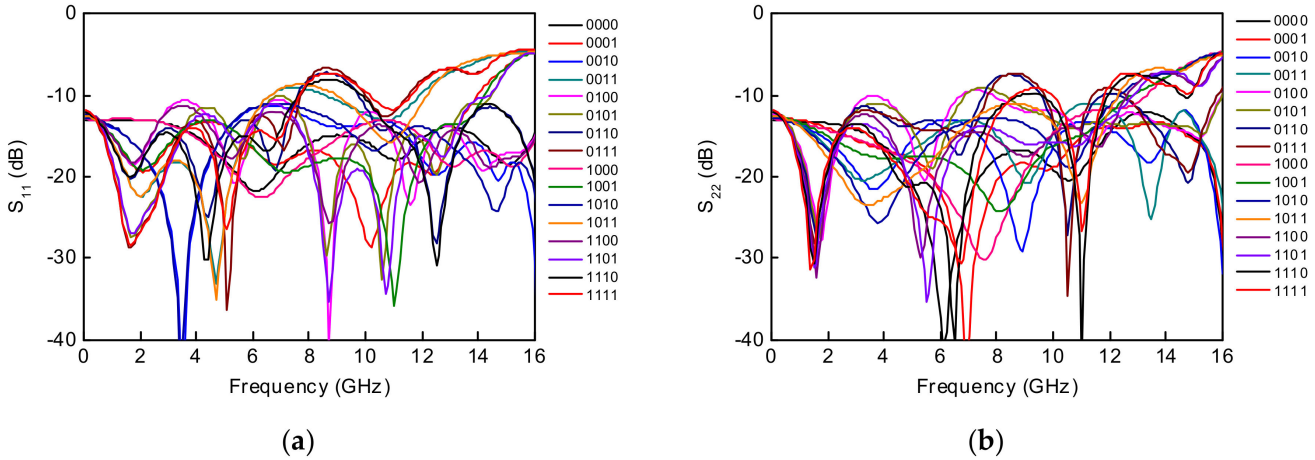


Figure 9. Measured (**a**) S_{11} and (**b**) S_{22} of the wideband 4-bit GaN-based true time delay circuit in all sixteen time delay states.

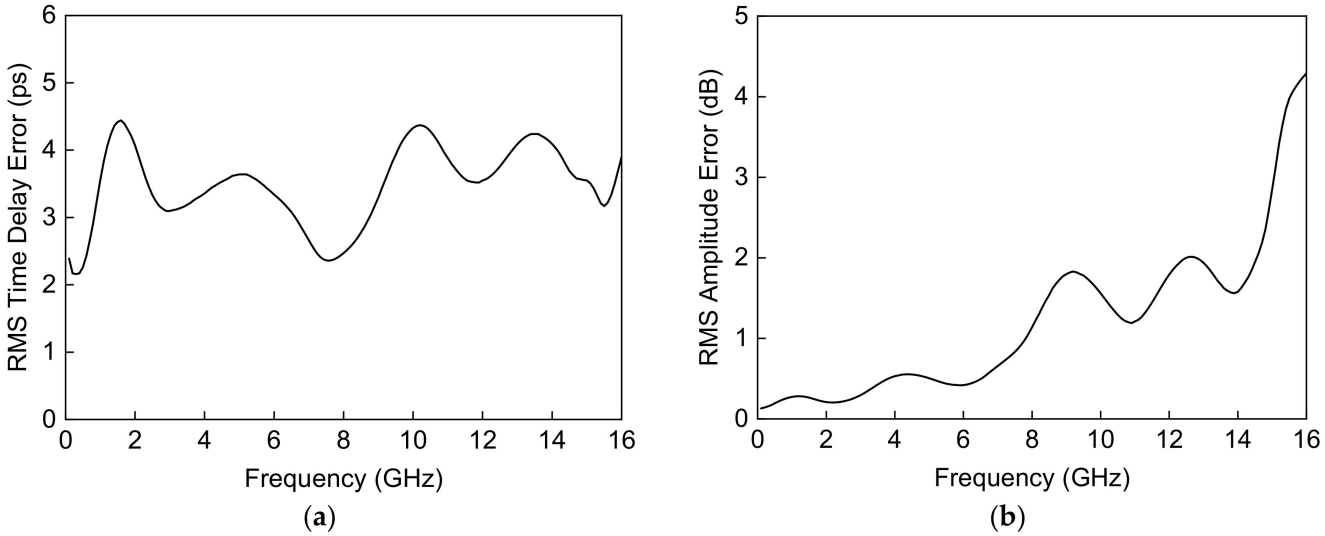


Figure 10. Measured (**a**) RMS time delay error and (**b**) RMS amplitude error of the wideband 4-bit GaN-based true time delay circuit.

Table 1. Performance comparison of the relevant true time delay ICs.

Reference	[5]	[6]	[13]	[16]	This Work
Frequency (GHz)	DC–20	2–20	1–7	6–16	DC–7
Technology	CMOS 0.18 µm	GaAs 0.2 µm	PCB	GaAs 0.25 µm	GaN 0.25 µm
Number of Bits	5	6	7	3	4
Time Delay Range (ps)	106	145	1016	98	182
Time Delay Resolution (ps)	3.3	2.1	8	14	10.5

Table 1. *Cont.*

Reference	[5]	[6]	[13]	[16]	This Work
Insertion Loss of Ref. (dB)	18	11	15.6	3.8–10.5	2.8–8.3
Return Loss of Ref. (dB)	≥12	-	≥12	≥14	≥10
RMS Amplitude Error (dB)	2	-	-	-	≤0.6
RMS Time Delay Error (ps)	1	2.2	-	-	≤5
Chip size (mm^2)	0.88	5.6	710	1.08 *	4.3

* Core only.

4. Conclusions

A wideband 4-bit true time delay IC is presented using 0.25 μm GaN HEMT technology. The proposed true time delay IC is implemented using a DPDT switched path topology with a CLC π-type delay line and exhibits low insertion loss, RMS time delay, and amplitude errors. The maximum time delay range was 182 ps with a time delay resolution of 10.5 ps. The measured insertion loss of the reference state was less than 6.8 dB at DC–6 GHz. The RMS time delay and amplitude errors were less than 5 ps and 0.6 dB, respectively. The DC power consumption was nearly zero. The compact chip size was 2.45 × 1.75 mm^2, including pads. The proposed GaN-based true time delay IC can be applied to high-power and wideband beam-squint-free phased array radar systems.

Author Contributions: Conceptualization, D.B. and J.-G.K.; methodology, D.B. and J.-G.K.; investigation, D.B. and J.-G.K.; writing—original draft preparation, D.B. and J.-G.K.; writing—review and editing, D.B. and J.-G.K.; supervision, D.B.; project administration, D.B. and J.-G.K.; funding acquisition, J.-G.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Nano UAV Intelligence Systems Research Laboratory program of Defense Acquisition Program Administration and Agency for Defense Development. (UD200027ED).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data can be obtained from the authors on request.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Robinson, M.; Danielson, P.; Popovic, Z. Continuous Broadband GaAs and GaN MMIC Phase Shifters. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 56–58. [CrossRef]
2. Kang, D.; Hong, S. A 2–10 GHz Digital CMOS Phase Shifter for Ultra-Wideband Phased Array System. In Proceedings of the 2007 IEEE Radio Frequency Integrated Circuits Symposium, Honolulu, HI, USA, 3–5 June 2007; pp. 395–398.
3. Kim, J.; Park, J.; Kim, J. CMOS true-time delay IC for wideband phased-array antenna. *ETRI J.* **2018**, *40*, 693–698. [CrossRef]
4. Cho, M.; Han, J.; Kim, J.; Kim, J. An X/Ku-band Bi-directional true time delay T/R chipset in 0.13 μm CMOS technology. In Proceedings of the IEEE MTT-S International Microwave Symposium, Tampa, FL, USA, 1–6 June 2014; pp. 1–4.
5. Choi, J.; Cho, M.; Baek, D.; Kim, J. A 5–20 GHz 5-Bit True Time Delay Circuit in 0.18 μm CMOS Technology. *J. Semicond. Technol. Sci.* **2013**, *13*, 193–197. [CrossRef]
6. Willms, J.; Ouacha, A.; Boer, L.; Vliet, F. A wideband GaAs 6-bit true-time delay MMIC employing on-chip digital drivers. In Proceedings of the 2000 European Microwave Conference, Paris, France, 2–5 October 2000; pp. 309–312.
7. Ouacha, A.; Alfredson, M.; Wilden, H. 638 mm Relative Delay 9-Bits MMIC TTD for Active Phased Array SAR/MTI. In Proceedings of the 2004 European Microwave Conference, Amsterdam, The Netherlands, 11–15 October 2004; pp. 309–312.
8. Lee, W.; Valdes-Garcia, A. Continuous True-Time Delay Phase Shifter Using Distributed Inductive and Capacitive Miller Effect. *IEEE Trans. Microw. Theory Tech.* **2019**, *67*, 3053–3063. [CrossRef]
9. Barker, N.; Rebeiz, G. Distributed MEMS True-Time Delay Phase Shifters and Wide-Band Switches. *IEEE Trans. Microw. Theory Tech.* **1998**, *46*, 1881–1890. [CrossRef]
10. Kim, M.; Hacker, J.; Mihailovich, R.; DeNatale, J. A DC-to-40 GHz Four-Bit RF MEMS True-Time Delay Network. *IEEE Microw. Wirel. Compon. Lett.* **2001**, *11*, 56–58. [CrossRef]

11. Sánchez-Escuderos, D.; Herranz-Herruzo, J.; Ferrando-Rocher, M.; Valero-Nogueira, A. True-Time-Delay Mechanical Phase Shifter in Gap Waveguide Technology for Slotted Waveguide Arrays in K a-Band. *IEEE Trans. Antennas Propag.* **2021**, *69*, 2727–2740. [CrossRef]
12. Shin, D.; Yom, I.; Kim, D. 4–20 GHz GaAs True-Time Delay Amplifier MMIC. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 1119–1121. [CrossRef]
13. Yoon, M.; Nam, S. 7-Bit Multilayer True-Time Delay up to 1016 ps for Wideband Phased Array Antenna. *IEICE Trans. Electron.* **2019**, *E102-C*, 622–626. [CrossRef]
14. Chu, T.; Roderick, J.; Hashemi, H. An Integrated Ultra-Wideband Timed Array Receiver in 0.13 µm CMOS Using a Path-Sharing True Time Delay Architecture. *IEEE J. Solid State Circuits* **2007**, *42*, 2834–2850. [CrossRef]
15. Ghazizadeh, M.; Medi, A. Novel Trombone Topology for Wideband True-Time-Delay Implementation. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 1542–1552. [CrossRef]
16. Hao, D.; Zhang, W.; Liu, Y. A Low Insertion Loss Variation Trombone True Time Delay in GaAs pHEMT Monolithic Microwave Integrated Circuit. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 889–891. [CrossRef]
17. Elamien, M.; Sheldon, A.; Maundy, B.; Belostotski, L.; Elwakil, A. Delay-Tunable Compact RC-Only All-Pass Filter. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 461–464. [CrossRef]