Comparisons of Loss Reduction Techniques Based on Pulsewidth Modulation and Model Predictive Control for Three-Phase Voltage Source Inverters

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Abstract: Due to the lack of comparative studies between discontinuous pulse-width modulation and model predictive control methods for reducing switching losses in two-level three-phase voltage source inverter, a comparative analysis of a generalized discontinuous pulse-width modulation and two model predictive control approaches for reducing switching losses is studied in this paper. Both generalized discontinuous pulse-width modulation and two model predictive control approaches are described and conducted in the simulation and experiment. The output performance is obtained by these methods after conducting in various conditions, including switching frequency, output power, and load conditions. It is validated that the generalized discontinuous pulse-width modulation control scheme achieves a better control performance at steady-state, while two model predictive control schemes have better transient-state performance with a superior dynamic. Additionally, the generalized discontinuous pulse-width modulation approach achieves better reducing switching losses performance and has slightly higher efficiency than that of two model predictive control approaches.

Keywords: two-level three-phase; voltage source inverter; discontinuous PWM; model predictive control; reduce switching losses

1. Introduction

Due to the requirements of high-power demand in numerous industrial applications, voltage source converters are used as an alternative in high-power high voltage [1–3]. Although many different converter structures are proposed with advantages such as high efficiency, low total harmonic distortion (THD), fault tolerance, and so on [4,5], nevertheless, the major aspect of all components used in industrial applications is cost. Therefore, a two-level voltage source inverter (VSI) is a popular converter structure which always competes against the cost of state-of-the-art converter structures due to its simplicity and low-cost requirements [6,7]. However, these conventional two-level VSIs have some limitations in operating at high frequency due to corresponding mainly with high switching losses, which decreases the system's efficiency. Although using low-power loss switching devices is a simple answer, this increases the cost of the converter system. As indicated in literature, the losses of the converter can be classified as conduction and switching losses. Among them, the switching losses are of particular importance since they are the only losses that can be controlled in the modulation stage. By modifying the modulation stage in the control of converter, the switching loss of the converter can be lowered without using additional hardware and increasing the cost of the converter system.

Numerous methods have been extensively developed in the literature to minimize the switching loss and increase the efficiency of converter [8,9]. The most known reducing switching loss strategy is based on carrier-based pulse-width modulation (CBPWM) method.

By considering a proper zero-sequence voltage injection, discontinuous PWM (DPWM) can be obtained, which can yield low switching losses [10,11]. In the most common DPWM methods, the zero-sequence voltage is injected so that reference voltage of one phase is always clamped to the positive or negative dc-rail. The clamped phase is alternated throughout the fundamental cycle. Among several developed DPWM approaches, generalized DPWM (GDPWM) with generalized phase-shift dependent discontinuous modulation waveforms, which capture all of the known discontinuous modulation signals, has been discovered and considered as the most popular strategy [12,13]. In GDPWM, the clamping duration per fundamental period does not exceed $120°$, and the clamping interval consistently aligns with the peak of the phase current. This strategic positioning effectively decreases the switching losses since they are directly proportional to the current magnitude.

In addition to PWM strategies, there has been extensive research on the use of model predictive control (MPC) for VSI due to its exclusive advantages, including intuitive concepts, a fast dynamic response, and flexible tackling of multiple control objectives and constraints [14,15]. Generally, MPC employs a discrete model to predict future system states and applies one optimal switching state obtained by minimizing an objective cost function. Employing a longer sampling time is often the straightforward approach to decrease the switching frequency of MPC [16]. However, a more precise discrete model is crucial to account for the dynamics of variables accurately. An alternative approach is to limit the available switching states based on the previous switching state of the converter [17]. Implementing this approach necessitates an additional stage of calculating the possible switching states, which can significantly increase the processing time. A comparable option involves predicting the switching losses and choosing the optimal switching state using either a loss evaluation criterion as described in [18] or by adding an additional term related to the converter loss in the cost function [19]. However, determining the appropriate weighting factor for the additional terms is also a challenging task. To overcome these limitations, the authors in [20] developed a predictive control method with future zero-sequence voltage to reduce switching losses in three-phase VSI. This first MPC scheme (MPC1) modifies the predicted reference voltages using an injected future zero-sequence voltage to generate a clamping interval corresponding to the phase leg with the largest output current. The second MPC scheme (MPC2), developed in [21], reduces the switching loss of VSI by determining the clamping interval of phase leg using future reference voltages and output currents. Once the optimal clamping interval of phase leg is determined, the possible switching states are selected in a manner that maintains the switching state of a corresponding phase leg.

This proposed work investigates a comparative study of the performance of reducing switching loss control schemes, including GDPWN, MPC1, and MPC2 approaches, using in two-level three-phase VSI. The steady-state and transient-state performance have been observed and analyzed during various conditions. In Section 2, a two-level three-phase VSI system used in simulation and experiment, reducing switching loss control schemes, is presented. Section 3 presents the simulation and experiment results, as well as output performance comparison under various conditions. Section 4 concludes this paper.

2. System and Reducing Switching Losses Control Schemes of VSI

2.1. Two-Level Three-Phase VSI

The typical topology of a two-level three-phase VSI is shown in Figure 1a. In Figure 1a, V_{dc} refers to dc-link voltage, while C_{dc} represents the dc-link capacitor. S_{x1} and S_{x2} denote the upper and lower switch of phase $-x$ $(x = a, b, c)$ in VSI. The VSI is connected to a *RL* load. The phase $-x$ output current is denoted by $i_{ox}(x = a, b, c)$. Figure 1b depicts the experiment setup, which consists of a two-level three-phase VSI connected to an *RL* load. The control algorithms are implemented on a control board using a digital signal processor (DSP) board (TMS320F28335). The DSP receives the output current signals through the current sensors. Using the sensed signals, the DSP operates the control algorithm to generate appropriate switching signals to the power switches of VSI. The control algorithm

in DSP is implemented using the Code composer studio (CCS) tool after connecting DSP and the computer through JTAG debug probe.

(a)

(b)
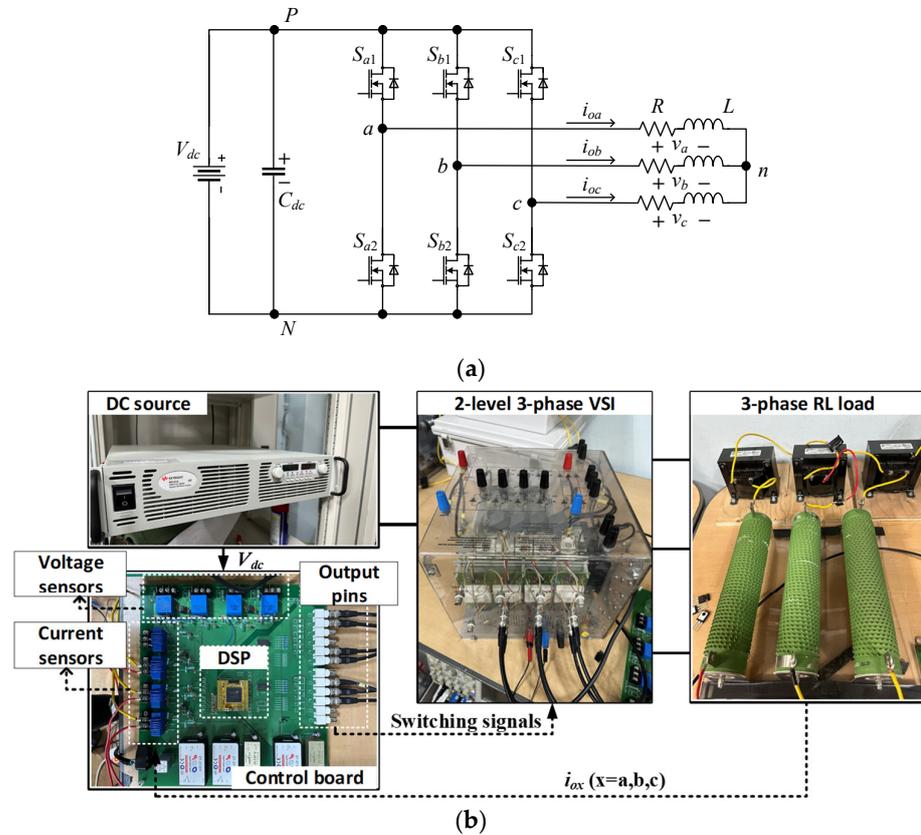
Figure 1. (**a**) Typical two-level three-phase VSI configuration, (**b**) corresponding experiment setup of two-level three-phase VSI.

2.2. Reducing Switching Losses Control Schemes

The operating principle of GDPWM is explained first. Next, MPC1 and MPC2 approaches are described.

As indicated earlier, CBPWM has the capability to achieve various control objectives by adding distinct zero-sequence voltages v_{ZSV} to reference voltage $v_{ref,x}$ for each phase [22]. Equation (1) represents $v_{mod,x}$ $(x = a, b, c)$, the modified reference voltage of phase $-x$ after adding v_{ZSV} to $v_{ref,x}$. The CBPWM technique for the VSI varies depending on which voltage is employed as the zero-sequence voltage in (1)

$$v_{mod,x} = v_{ref,x} + v_{ZSV} \quad (x = a, b, c) \tag{1}$$

DPWM is distinguished by the ability to decrease switching losses by keeping the switching state during a designated period. Regarding control of VSI using DPWM, the non-switching interval is 120° in each phase. Among different available DPWM methods, the GDPWM is the most effective in reducing switching losses. This can be achieved by keeping the switching state unchanged when the corresponding absolute output current is the largest. The implementation of GDPWM involves using a zero-sequence voltage, calculated as follows.

$$v_{ZSV} = \begin{cases} 0.5V_{dc} - v_{max}, \; if \; |i_{max}| > |i_{min}| \\ -0.5V_{dc} - v_{min}, \; if \; |i_{min}| > |i_{max}| \end{cases} \tag{2}$$

In (1), v_{ZSV} indicates the zero-sequence voltage or offset voltage to implement GDPWM. v_{max} and v_{min} denote the maximum and minimum among $v_{ref,a}$, $v_{ref,b}$, and $v_{ref,c}$, respectively.

Additionally, i_{max} represents the output current in the phase with the largest reference voltage. Conversely, i_{min} is the output current in the phase with the smallest reference voltage. The implementation of GDPWM-based proportional-integral (PI) control is achieved by employing the current control scheme and PWM technique, as shown in Figure 2.
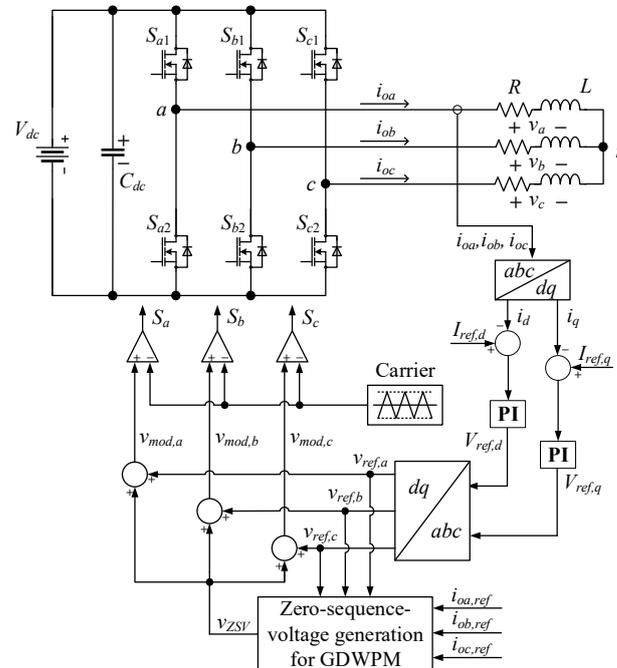

Figure 2. Control block diagram of GDPWM-based PI control.

Different from conventional MPC for two-level three-phase VSI, the two MPC approaches use predictive voltage for the prediction process. The future reference voltage vectors $v_{ref,x}(k)$ can be determined from the measured output current $i_{ox}(k)$ and corresponding reference current $i_{ox,ref}(k)$ as follows.

$$v_{ref,x}(k) = \frac{1}{T_{sp}}\left\{Li_{ox,ref}(k+1) + (RT_{sp} - L)i_{ox}(k)\right\} \quad (x = a, b, c) \tag{3}$$

In (3), T_{sp} denotes the sampling time. This equation (3) indicates that when the converter voltage $v_x(k)$ at time instant k is set to $v_{ref,x}(k)$, the current $i_{ox}(k)$ will be identical to its corresponding reference current $i_{ox,ref}(k+1)$. Hence, to regulate the output current using predictive voltage for prediction process, the task is to select one voltage vector from the eight possibilities that meet the requirements set by the given cost function below.

$$g_v = \left| v_{ref,x}(k) - v_x(k) \right| \tag{4}$$

The complete control block of MPC using predictive voltage is depicted in Figure 3.

In the MPC1 approach, future voltage vectors $v_{ref,x}(k)$ are modified by injecting a future zero-sequence voltage to generate a clamping interval corresponding to the phase leg with the largest output current. The MPC1 generates the future zero-sequence voltage $v_{ZSV}(k)$ in a way that the modified future reference voltage $v_{mod,x}(k)$ after adding $v_{ZSV}(k)$, allowing for clamping one leg that conducts the corresponding largest output current to either the positive or negative dc-rail. The future zero-sequence voltage can be calculated as follows.

$$v_{ZSV}(k) = \begin{cases} 1 - v_{nref,max}(k), & if \ |i_{max}(k)| > |i_{min}(k)| \\ -1 - v_{nref,min}(k), & if \ |i_{min}(k)| > |i_{max}(k)| \end{cases} \tag{5}$$

where $v_{nref,max}(k)$ and $v_{nref,min}(k)$ represent the normalized maximum and normalized minimum reference voltages. Depending on the absolute magnitude of maximum and minimum reference currents, $i_{max}(k)$ and $i_{min}(k)$, respectively, the phase leg corresponding to $v_{nref,max}(k)$ or $v_{nref,min}(k)$ will be clamped to either the positive or negative dc-rail. The entire block diagram of MPC1 is depicted in Figure 4.
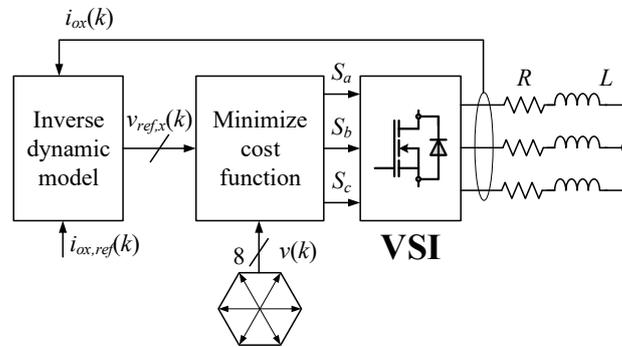

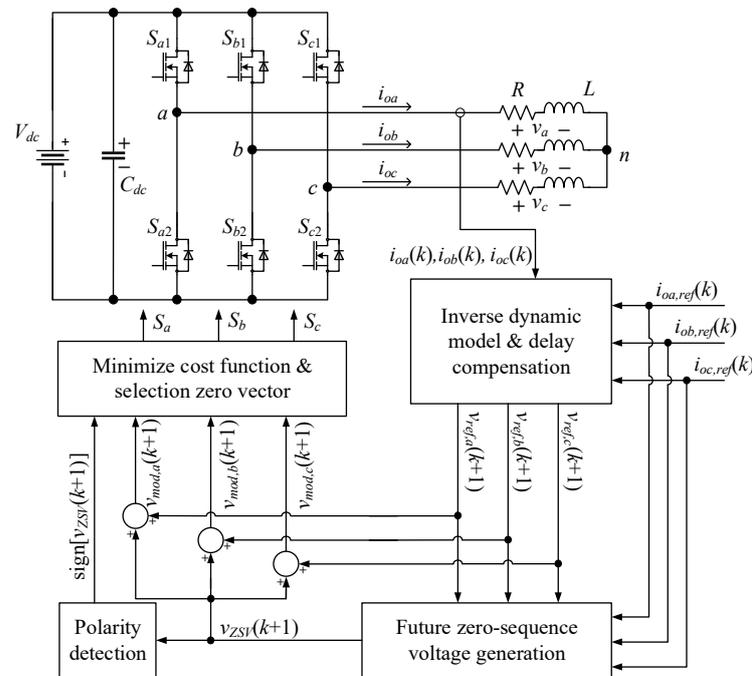**Figure 3.** Block diagram of predictive voltage MPC.

Figure 4. Block diagram of MPC1.

Instead of modifying the future reference voltage, the MPC2 approach identifies the most optimal phase among three-phase legs to be clamped in every sampling period. Similar to the MPC1 approach, the future reference voltages $v_{ref,x}(k)$ are sorted depending on their magnitude to find out the maximum and minimum future reference voltages, $v_{ref,max}(k)$ and $v_{ref,min}(k)$, respectively. Between the two-phase legs corresponding to $v_{ref,max}(k)$ and $v_{ref,min}(k)$, the phase with a higher reference current is clamped to the positive or the negative dc-rail. After one of the three-phase legs in VSI is determined to be clamped, a switching strategy will preselect possible voltage vectors that allow for clamping the corresponding phase leg. It has been shown that each phase leg of VSI has four available voltage vectors that maintain the switching state of the corresponding switch. The entire block diagram of MPC2 is depicted in Figure 5.
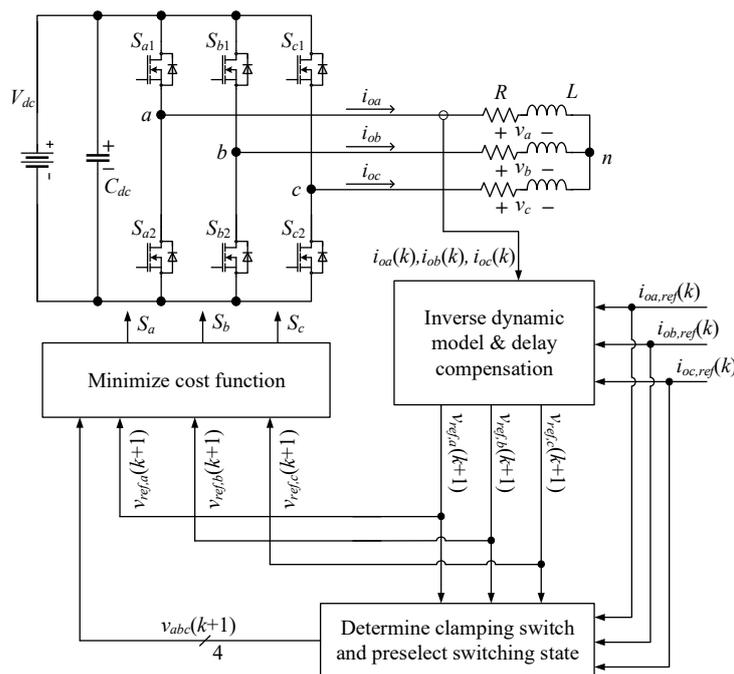
Figure 5. Block diagram of MPC2.

3. Performance Comparison and Analysis

This section presents the output performance of three-phase VSI acquired by implementing GDPWM, MPC1, and MPC2. The condition for simulation and experiment to analyze the performance of three control schemes are shown the same as in Table 1. The load angle in this study describes the phase angle difference between voltage and current caused by *RL* load. The simulation is conducted using PSIM simulation program, whereas the experiment is conducted by using the prototype in Figure 1b.

Table 1. Parameters in simulation and experiment.

Parameter	Value	
	GDPWM	**MPC**
dc-link voltage V_{dc} (V)	220	
dc-link capacitance (µF)	680	
Load resistor R (Ω)	10	
Load inductor L_f (mH)	10	
Load angle (degree)	20	
Sampling time T_{sp} (µs)	50	
Fundamental frequency f (Hz)	60	
Carrier frequency f_c (kHz)	7	x
Reference current (A)	5	5
Proportional gain K_p	5	x
Integral gain K_i	100	x

Concerning the PSIM simulation program, it is specialized software designed for electronic circuit simulation that is primarily used to create power electronics and motor drive simulations, as well as other electronic circuits [23]. PSIM stands out with its user-friendly graphical interface, simplifying the setup and simulation of intricate power circuits for power electronics engineers. Although MATLAB and PSpice also offer graphical

interfaces, they are more commonly used through scripting and coding, which may require greater expertise [24]. Moreover, PSIM boasts interactive simulation capabilities, enabling users to modify parameter values and observe voltages/currents during simulations. An added advantage of PSIM is its built-in C compiler, allowing users to input C code directly into the program without the need for separate compilation, facilitating the implementation of functions or control methods with ease and flexibility. Additionally, PSIM supports the Thermal Module, enabling the calculation of semiconductor device losses (conduction and switching losses) based on device information from manufacturers' datasheets.

The principle of MPC method is to select the optimal switching option that minimizes a cost function, and as a result, no commutation is compelled during every sampling period. In fact, a single switching state can serve as the optimal selection for two or more sample periods. This characteristic results in a variable switching frequency. The average switching frequency per power device f_{sw_avg} will be defined as the average value of the switching frequencies of the six controlled power semiconductor devices in the VSI circuit. Thus

$$f_{sw\_avg} = \sum_{i=1}^{2} \frac{f_{S_{xi}}}{6} \ (x = a, b, c) \tag{6}$$

where $f_{S_{xi}}$ is the switching frequency during a time interval of the power semiconductor device number i ($i = 1, 2$) of phase $-x$ ($x = a, b, c$). For a fair comparison, the carrier frequency f_c and sampling frequency f_{sp} are set to achieve similar average switching frequency in both GDPWM and MPC methods.

Figure 6 illustrates the output current waveforms and corresponding switching patterns at steady state obtained by the GDPWM, MPC1, and MPC2 methods in both simulation and experiment. The output currents acquired through three control schemes exhibit sinusoidal waveforms and demonstrate accurate magnitude and phase. Both GDPWM and MPC methods are capable of tracking the reference current. The phase $-a$ output current i_{oa} obtained by three control schemes shows a negligible deviation from the corresponding reference current i_{refa}, as shown in Figure 6a–c. As can be seen from the switching patterns of three-phase legs, all three approaches have similar non-switching intervals in each phase, where each phase is clamped to either the positive or negative dc-rail for $120°$ in one fundamental period.
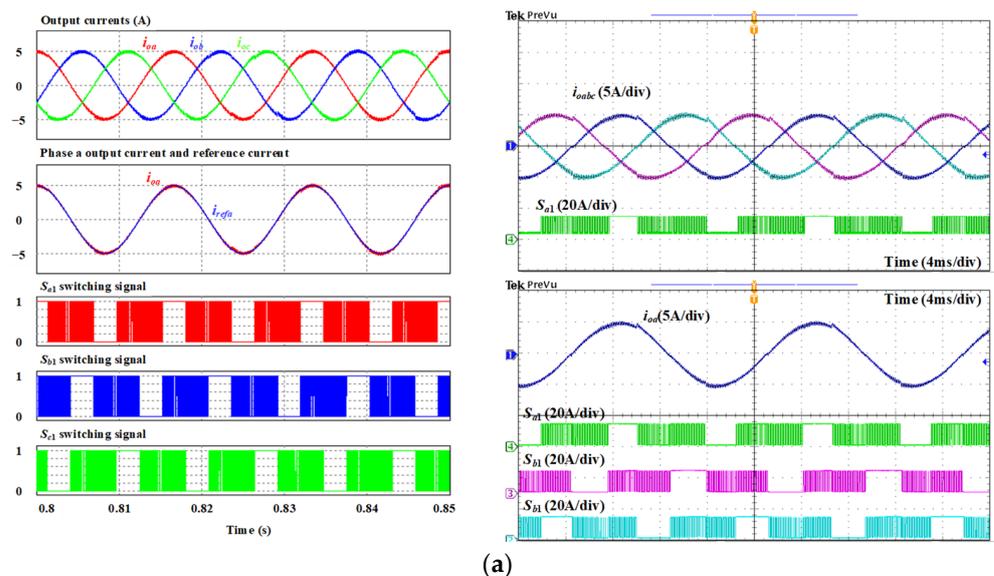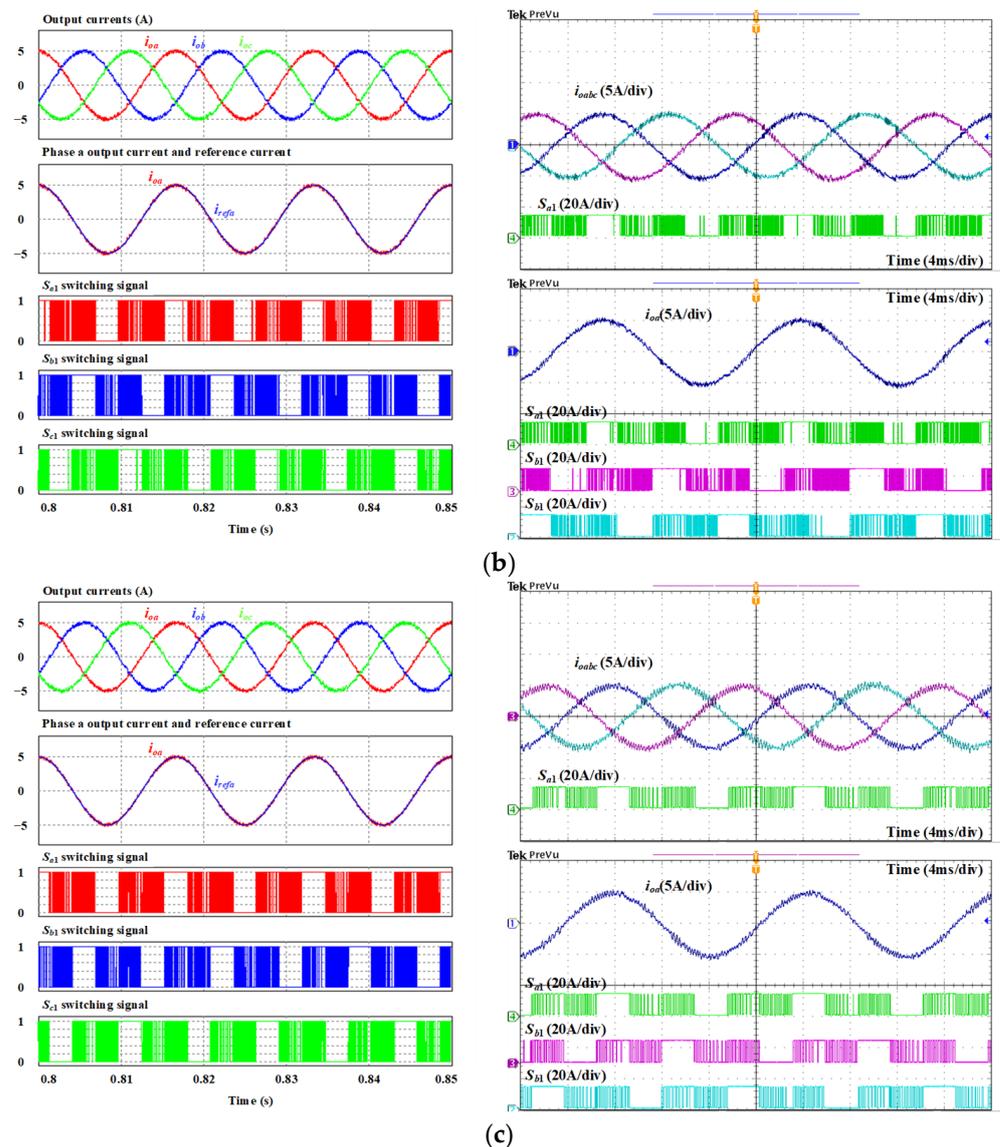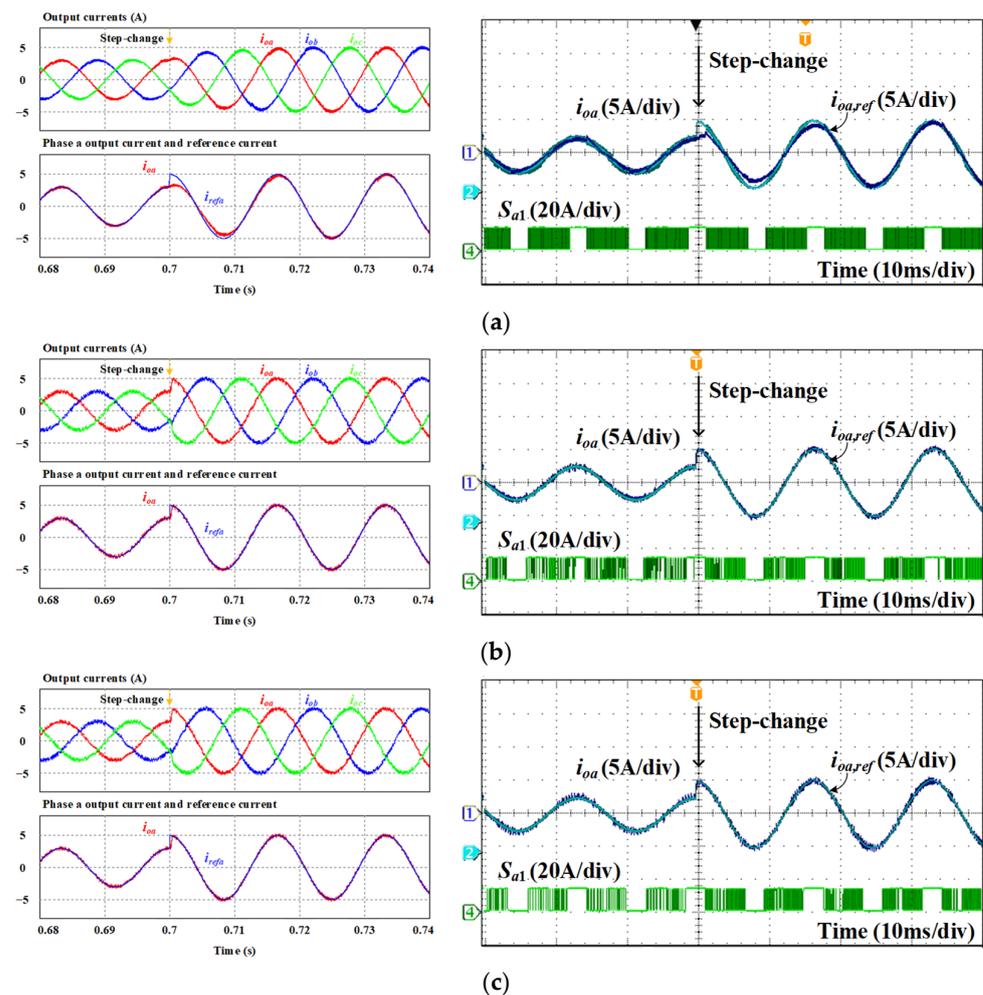

(**a**)

Figure 6. *Cont.*

Figure 6. Output current and switching pattern at steady state in simulation (left-hand side) and experiment (right-hand side). (**a**) GDPWM, (**b**) MPC1, (**c**) MPC2.

Regarding the dynamic performance, Figure 7 illustrates the output current waveforms at transient-state obtained by the GDPWM, MPC1, and MPC2 methods in simulation and experiment. The transient state is generated by applying an abrupt change in the magnitude of reference current from 2.5 A to 5 A. It should be noted that as the PI controller in the GDPWM method requires enough time to achieve the first steady state corresponding to 2.5 A of magnitude of reference current, this means that the output current correctly follows the output current reference. Therefore, the left-hand side figure in Figure 7 has the origin of time not equal to zero. In this manner, the dynamic performance of the output current can be evaluated. It can be seen that in Figure 7b,c, the MPC methods exhibit superior dynamic performance where the output current immediately changes its magnitude following the change of corresponding reference current with a negligible overshoot in both simulation and experiment results. Meanwhile, the GDPWM method requires more time to achieve the change of reference current. Thus, transient-state performance of MPC methods is better than the GDPWM approach with less settling and rise time, which are required to achieve the desired set point.

Figure 7. Output current and switching pattern at transient state in simulation (left-hand side) and experiment (right-hand side). (**a**) GDPWM, (**b**) MPC1, (**c**) MPC2.

The calculated values from simulation results are presented to thoroughly assess output performance, switching frequency, and switching loss reduction capability obtained by the GDPWM, MPC1, and MPC2 methods. The power losses are calculated by the thermal module in the PSIM simulation program by using parameters from the IGBT module's datasheet (Semikron SK60GM123). Figure 8a–e illustrate the performance comparison between GDPWM, MPC1, and MPC2 methods regarding switching frequency, output current THD, and power losses. As indicated earlier, the switching frequency and sampling frequency are set to achieve a comparable average switching frequency obtained by three control schemes. As shown in Figure 8a, the phase and average switching frequencies acquired by GDPWM, MPC1, and MPC2 approaches are similar. The comparable average switching frequency is achieved at approximately 4.7 kHz. In Figure 8b, the phase and average switching frequencies obtained by three control schemes are presented. It can be realized that the GDPWM method generates output currents with the lowest THD value. Meanwhile, the MPC1 and MPC2 approaches have higher average THD than that of GDPWM by about 37% and 35%, respectively. The difference of output current THD between MPC and MPC2 methods is negligible. Regarding the power loss performance, Figure 8c–e show that the three control schemes have similar conduction loss. The two MPC approaches also have similar switching loss and total loss, but the GDPWM shows lower switching loss compared to the two MPC approaches. The two MPC approaches have higher total switching loss and total loss than that of GDPWM by about 16% and 11%, respectively.
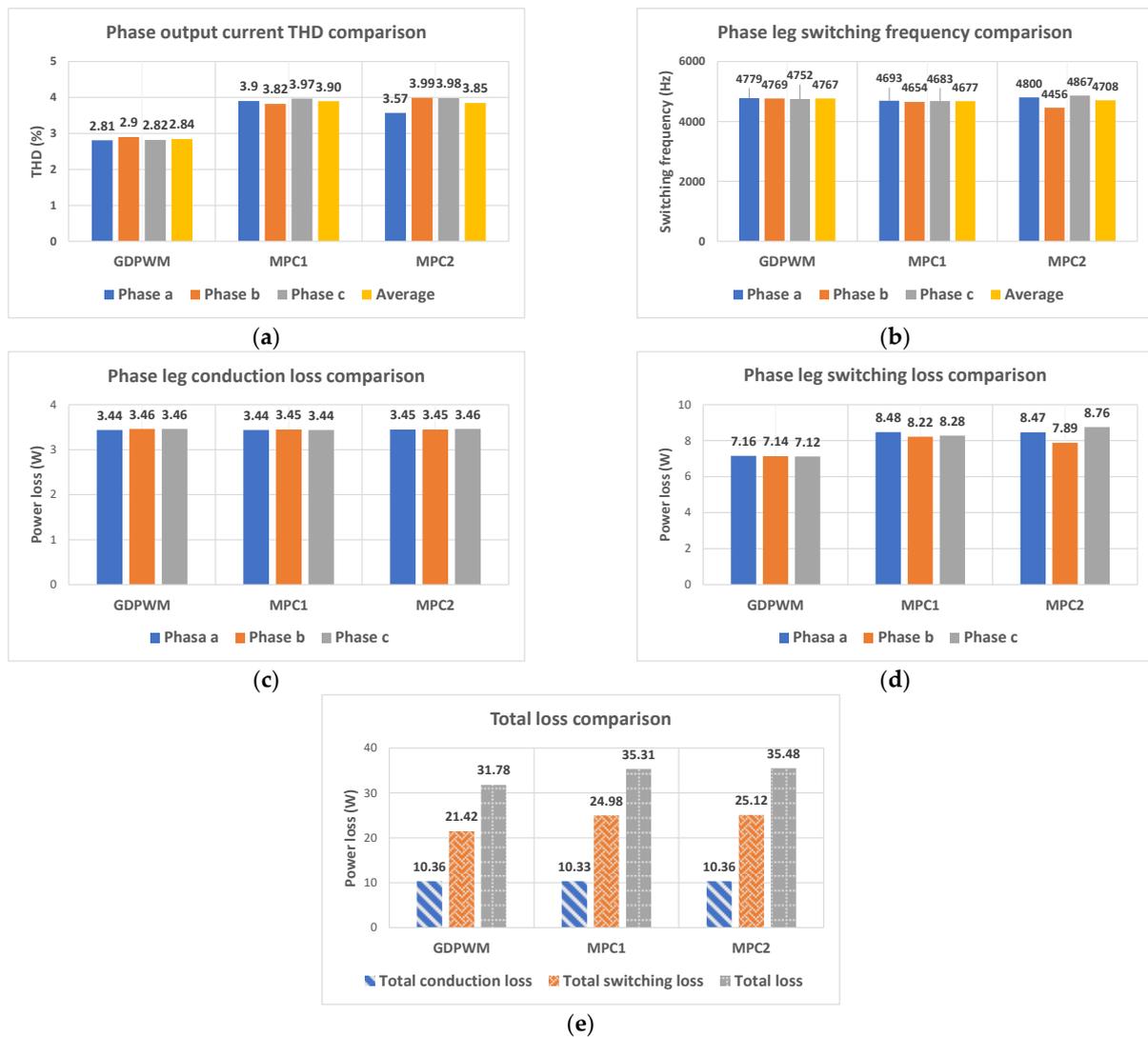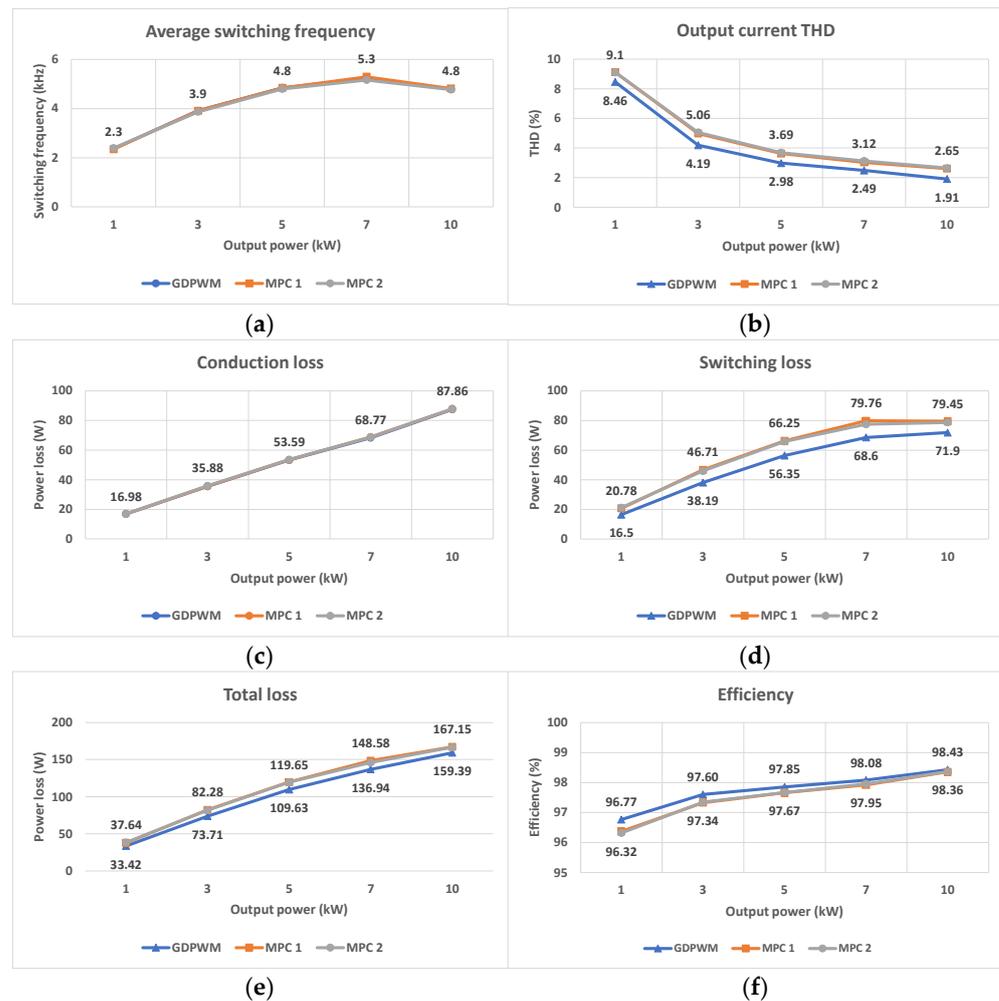
Figure 8. Simulated performance comparison. (**a**) Switching frequency, (**b**) Output current THD, (**c**) Conduction loss, (**d**) Switching loss, (**e**) Total loss.

To further assess the performance between GDPWM, MPC1, and MPC2 methods, the comparison among three methods is conducted under various conditions, including different switching frequencies, different output powers, and different load conditions. First, the output performance comparison is conducted under different switching frequency conditions. As shown in Figure 9a, the carrier frequency in GDPWM method and sampling frequency in MPC methods are increased to change the switching frequency. It should be noted that the carrier and sampling frequencies are adjusted to achieve similar average switching, as shown in Figure 9a. Thanks to the increase in switching frequency, the average current THD decreases. It can be seen in Figure 9b that the average output current THD obtained by three methods decreases following the rise of switching frequency. It can be noticed that the output current obtained by two MPC methods is higher than that of GDPWM. The difference in output current THD between GDPWM method and two MPC methods ranges from 20% to 35%. Because the conduction loss is not affected by the switching frequency, the conduction obtained by GDPWM and two MPC methods is similar. Meanwhile, the switching loss and total loss increases following the rise of switching frequency. The two MPC approaches have higher switching loss and total loss compared to that of GDPWM by about 16% and 11%, respectively. Thus, GDPWM has slightly higher efficiency than the two MPC methods, as shown in Figure 9f.
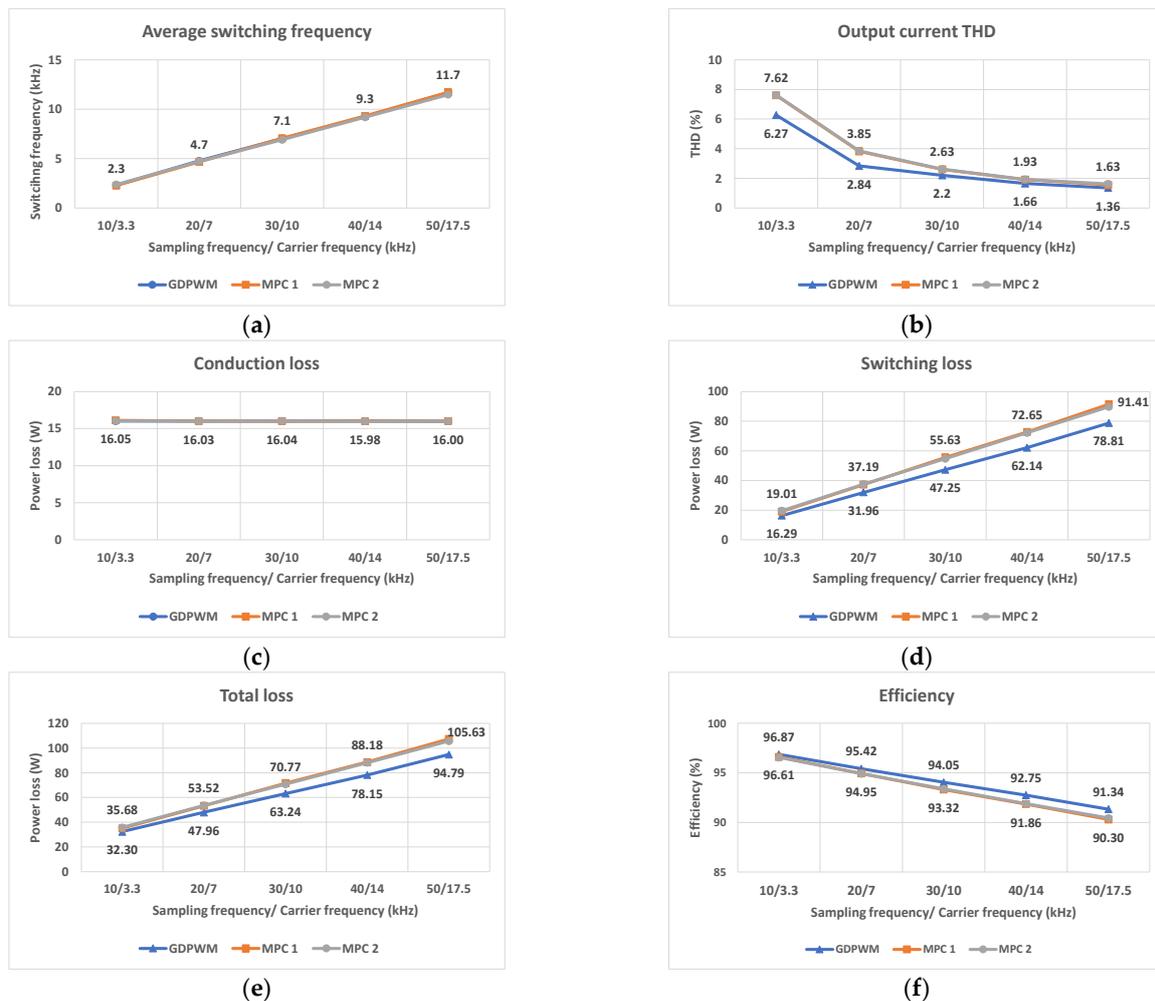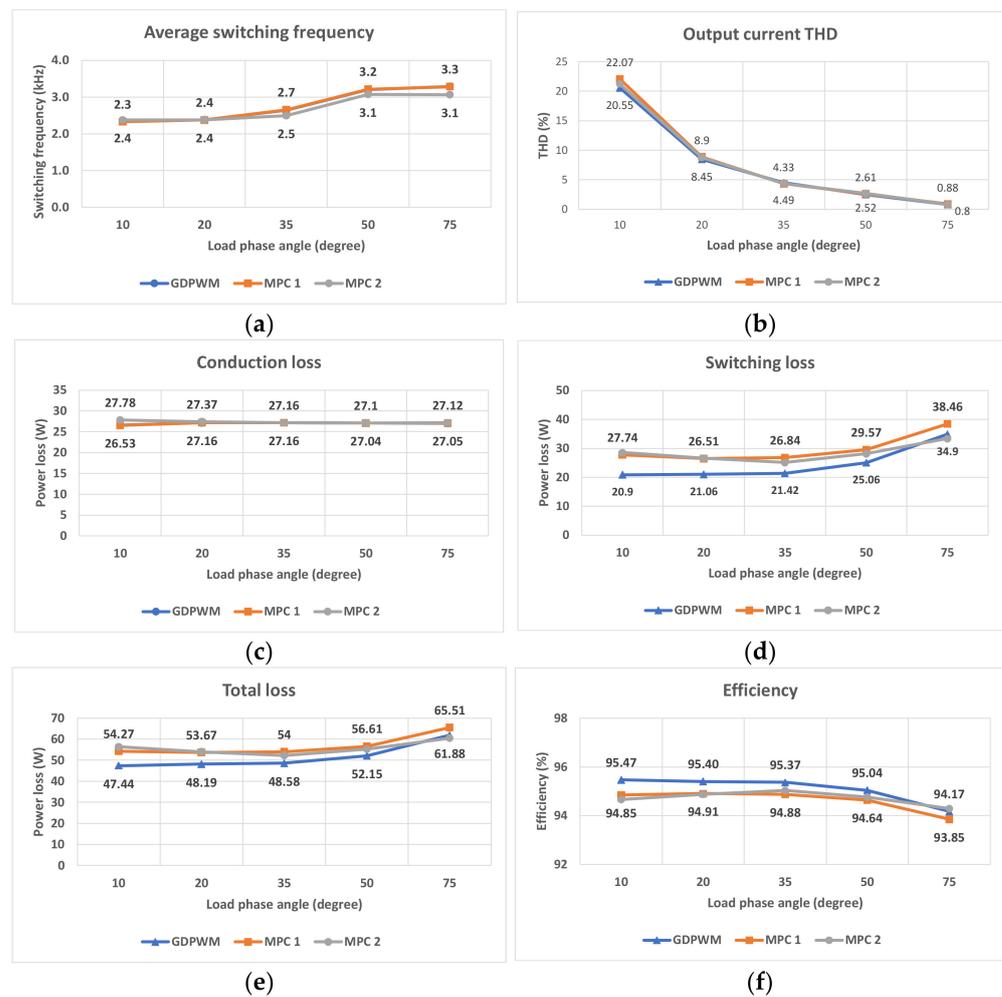
Figure 9. Simulated performance comparison versus various switching frequency conditions. (**a**) Switching frequency, (**b**) Output current THD, (**c**) Conduction loss, (**d**) Switching loss, (**e**) Total loss, (**f**) Efficiency.

The output performance comparison, conducted under different output power conditions, is shown in Figure 10a–f. As shown in Figure 10a, the carrier frequency in GDPWM method and sampling frequency in MPC methods are adjusted to achieve similar average switching following the variation of output power condition. Following the increase of output power, the average current THD obtained by three control schemes decreases. It can be seen in Figure 10b that the average output current THD obtained by three methods decreases following the rise of output power. It can be noticed that the output current obtained by two MPC methods is higher than that of GDPWM. The difference of output current THD between GDPWM method and two MPC methods ranges from 10% to 35%. Because the conduction loss is not affected by the switching frequency, the conduction obtained by GDPWM and two MPC methods are similar, as shown in Figure 10c. However, due to the increase in output power, the corresponding conduction loss increases as well. Meanwhile, the switching loss and total loss increase following the rise of output power. The difference in switching loss between the two MPC methods and GDPWM method decreases when the output power increases. This difference is highest at 1 kW output power of 26%, while it is lowest at 10 kW output power of about 10%, as shown in Figure 10d. Consequently, the difference of total loss between the two MPC methods and GDPWM method decreases when the output power increases. This difference ranges from 5% to 13% depending on the output power conditions, as shown in Figure 10e. In terms of efficiency, the GDPWM method has slightly higher efficiency than the two MPC approaches.
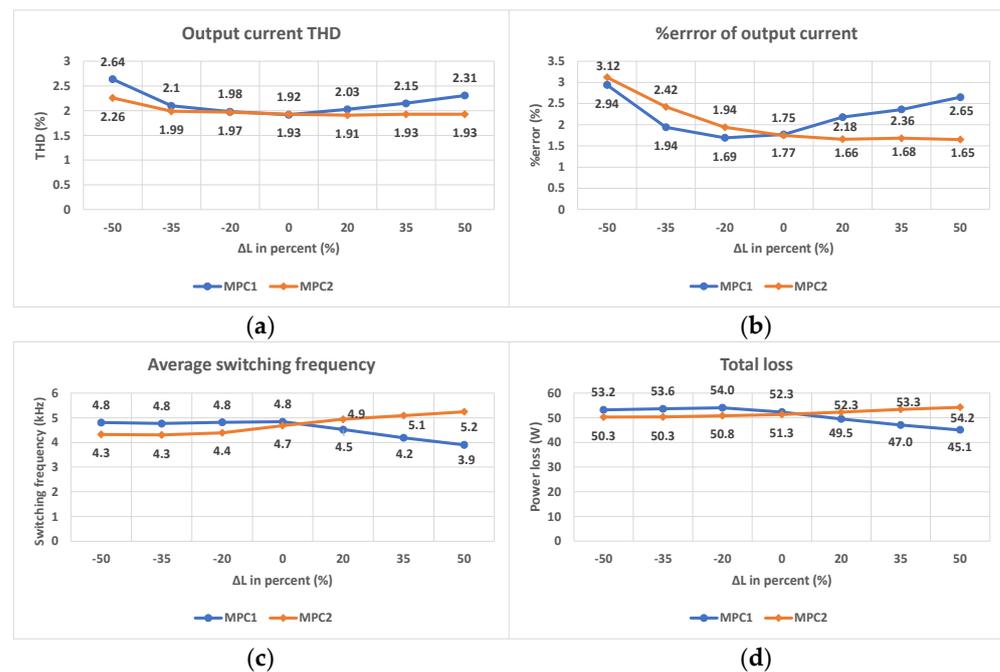
Figure 10. Simulated performance comparison versus various output power conditions (**a**) Switching frequency, (**b**) Output current THD, (**c**) Conduction loss, (**d**) Switching loss, (**e**) Total loss, (**f**) Efficiency.

Figure 11a–f illustrate the comparison of output performance under various load conditions. To modify the phase angle, the output inductance of the VSI is increased. As shown in Figure 11a, the carrier frequency in GDPWM method and sampling frequency in MPC methods are appropriately adjusted to achieve similar average switching following the variation of load condition. Following the increase of load phase angle, the average current THD obtained by three control schemes decreases significantly. It can be seen in Figure 11b that the average output current THD obtained by three methods decreases following the rise of load phase angle. It is noticed that the output current obtained by two MPC methods is higher than that of GDPWM. The difference of output current THD between GDPWM method and two MPC methods decreases following the increase of phase angle. Additionally, this difference is slight. Because the conduction loss is not affected by the switching frequency, the conduction obtained by GDPWM and two MPC methods are similar, as shown in Figure 11c. Simultaneously, the switching loss and total loss experience a relative increase as the load phase angle rises. As the load phase angle increases, the difference in switching loss between the two MPC methods and the GDPWM method diminishes. This difference is highest at 10° load phase angle of about 33%, while it is lowest at 75° load phase angle of about 10%, as shown in Figure 11d. As a result, the contrast in total loss between the two MPC methods and the GDPWM method diminishes with an increase in the load phase angle. The variation in this distinction ranges from 6% to 11%, varying following the conditions of the load phase angle, as depicted in Figure 11e. In terms of efficiency, the GDPWM method has slightly higher efficiency than the two MPC approaches.

Figure 11. Simulated performance comparison versus various load conditions. (**a**) Switching frequency, (**b**) Output current THD, (**c**) Conduction loss, (**d**) Switching loss, (**e**) Total loss, (**f**) Efficiency.

The PWM method does not require the information of load, so it is not affected when a parameter mismatch of load or even an unbalanced load exists. Meanwhile, the load information is crucially required for the prediction model. The behavior of MPC1 and MPC2 methods under parameter mismatch of load inductance, including various performances such as average THD, %error of output current, average switching frequency, and total loss, are shown in Figure 12a–d. The horizontal axis of line charts in Figure 12 presents the difference between the model parameter inductance and the actual inductance. As shown in Figure 12a, the output current THD acquired by the MPC2 method is maintained well under load inductance error. The output current THD obtained by the MPC1 method increases considerably when the load inductance error exceeds 35%. In Figure 12b, the %error of output current obtained by the MPC1 significantly increases by about 60% when the load inductance error is 50%. The %error of output current obtained by the MPC2 significantly increases when the model parameter inductance is lower than the actual inductance. Meanwhile, when the model parameter inductance is higher than the actual one, the %error of output current obtained by the MPC2 method slightly decreases. When the model parameter inductance is lower than the actual one, the MPC1 method has a similar average switching frequency. However, when the model parameter inductance is higher than the actual one, the average switching frequency decreases. This leads to the reduction of total loss obtained by the MPC1 method, as shown in Figure 12d. Contrastingly, the average switching frequency of MPC2 method decreases when the model parameter inductance is lower than the actual one and vice versa.
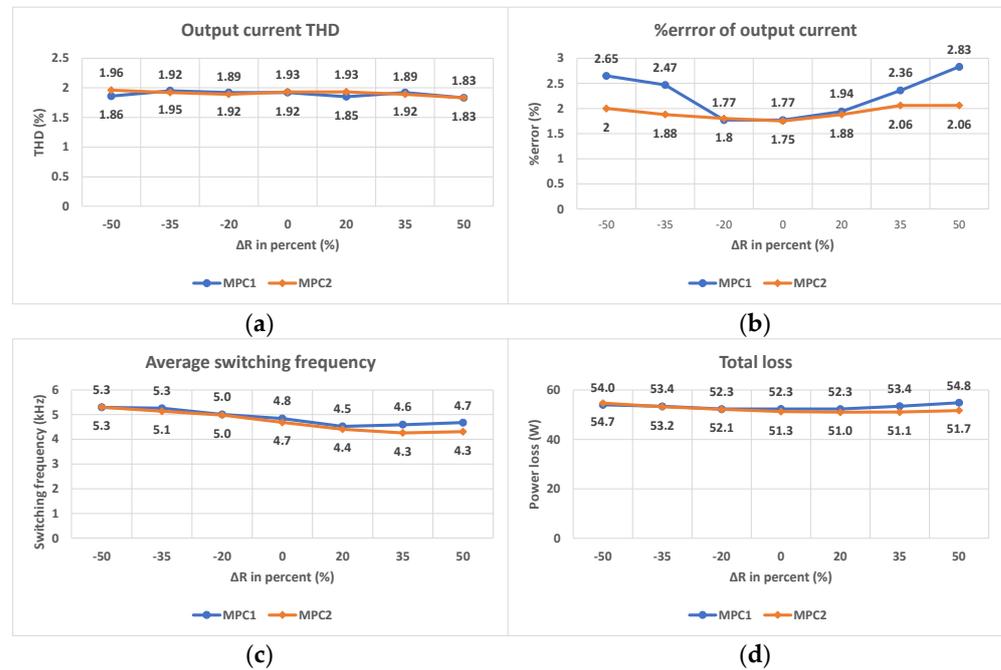
Figure 12. Simulated performance comparison versus parameter mismatch of load inductance. (**a**) Output current THD, (**b**) %error of output current, (**c**) Switching frequency, (**d**) Total loss.

The behavior of MPC1 and MPC2 methods under parameter mismatch of load resistance, including various performances such as average THD, %error of output current, average switching frequency, and total loss, are shown in Figure 13a–d. The horizontal axis of the line charts in Figure 13 presents the difference between the model parameter resistance and the actual resistance. As shown in Figure 13a, the output current THD obtained by two MPC methods is maintained well under load resistance error. The output current THD slightly changes, even when the load resistance error is 50%. In Figure 13b, the %error of output current obtained by the MPC1 significantly increases by about 60% when the load resistance error is 50%. The %error of output current obtained by the MPC2 slightly increases when the model parameter resistance is lower or higher than the actual resistance. In case the model parameter resistance is lower than the actual one, the average switching frequency obtained by two MPC methods increases, while the average switching frequency slightly decreases when the model parameter resistance is higher than the actual one. As for total power loss, the total loss of MPC1 method increases in the case that the load resistance error is higher than 35%. Meanwhile, the MPC2 method maintains a similar total loss when the model parameter resistance is higher than the actual one. It can be realized that the effect of load resistance mismatch is lower than the load inductance mismatch.

The behavior of MPC1 and MPC2 methods under parameter mismatch of load resistance, including various performances such as average THD, %error of output current, average switching frequency, and total loss, are shown in Figure 13a–d. The horizontal axis of the line charts in Figure 13 presents the difference between the model parameter resistance and the actual resistance. As shown in Figure 13a, the output current THD obtained by two MPC methods is maintained well under load resistance error. The output current THD slightly changes, even when the load resistance error is 50%. In Figure 13b, the %error of output current obtained by the MPC1 significantly increases by about 60% when the load resistance error is 50%. The %error of output current obtained by the MPC2 slightly increases when the model parameter resistance is lower or higher than the actual resistance. In case the model parameter resistance is lower than the actual one, the average switching frequency obtained by two MPC methods increases, while the average switching frequency slightly decreases when the model parameter resistance is higher than the actual one. As for total power loss, the total loss of MPC1 method increases in case the load

resistance error is higher than 35%. Meanwhile, the MPC2 method maintains a similar total loss when the model parameter resistance is higher than the actual one. It can be realized that the effect of load resistance mismatch is lower than the load inductance mismatch.

Figure 13. Simulated performance comparison versus parameter mismatch of load resistance. (**a**) Output current THD, (**b**) %error of output current, (**c**) Switching frequency, (**d**) Total loss.

4. Conclusions

Control algorithms for GDPWM and two MPC approaches for reducing switching losses in two-level three-phase VSIs have been presented. The performance of these approaches has been thoroughly evaluated and compared using both simulation and experiment results under various conditions. It should be highlighted that all control schemes have been thoroughly designed and tuned to achieve optimal performance. This involves careful consideration of the average switching frequency, and appropriate tuning of the PI gain to ensure a fair comparison among them. As for steady-state performance, the GDPWM approach gives the best performance with relatively low output current THD compared to two MPC approaches. On the other hand, MPC1 and MPC2 approaches have faster current transient than the GDPWM scheme. Different from the non-required tuning process in MPC1 and MPC2 approaches, GDPWM requires more effort and complexity. However, the MPC approaches require precise load information for predictive model generation. Regarding reducing losses performance, at the same average switching frequency, the GDPWM has a lower switching loss compared to the two MPC approaches by approximately 10%. Thus, the efficiency of VSI implemented by GDPWM is slightly higher than that of the two MPC approaches. Table 2 shows a summary of comparative results between GDPWM, MPC1, and MPC2 methods based on the operating principle, and simulation results.

Table 2. Summary of performance comparison.

Performance	Control Method		
	GDPWM	**MPC1**	**MPC2**
Average output current THD	Lowest	High	High
Switching frequency/loss reduction capability	Highest	High	High

Table 2. *Cont.*

Performance	Control Method		
	GDPWM	MPC1	MPC2
Efficiency	Highest	High	High
Dynamic response	Slow	Fast	Fast
Effect of load inductance mismatch	Non-affected	High	Low
Effect of load resistance mismatch	Non-affected	High	Low

Author Contributions: Conceptualization, S.K. and S.C.; methodology, S.K. and S.C.; software, M.H.N.; validation, M.H.N.; formal analysis, M.H.N.; investigation, M.H.N.; resources, S.K.; data curation, M.H.N.; writing—original draft preparation, M.H.N.; writing—review and editing, S.K. and S.C.; visualization, M.H.N.; supervision, S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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