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Developing a TEI-Aware PMIC for Ultra-Low-Power System-on-Chips

Kyu-Bae Lee , Jina Park, Eunjin Choi, Mingi Jeon and Woojoo Lee *

School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, Korea; leegb2014@cau.ac.kr (K.-B.L.); graffitti88@cau.ac.kr (J.P.); eunjin8269@cau.ac.kr (E.C.); alsrlfkdl@cau.ac.kr (M.J.)
* Correspondence: space@cau.ac.kr

Abstract: As the demand for ultra-low-power (ULP) devices has increased tremendously, system-on-chip (SoC) designs based on ultra-low-voltage (ULV) operation have been receiving great attention. Moreover, research has shown the remarkable potential that even more power savings can be achieved in ULV SoCs by exploiting the temperature effect inversion (TEI) phenomenon, i.e., the delay of the ULV SoCs decreases with increasing temperature. However, TEI-aware low-power (TEI-LP) techniques have a critical limitation in practical terms, in that dedicated power management-integrated circuits (PMICs) have not yet been developed. In other words, it is essential to develop PMICs that automatically bring out the full potential of the TEI-LP techniques as the chip temperature changes. With the aim of designing such PMICs, this paper first conducted a study to find the most suitable DC-DC converter for PMICs and then developed a control algorithm to maximize the effectiveness of the TEI-LP techniques. Furthermore, we have developed a compact hardware controller for the algorithm to operate most energy efficiently on ULP-SoCs.

Keywords: PMIC; system-on-chip; temperature effect inversion; ultra-low-power

Citation: Lee, K.-B.; Park, J.; Choi, E.; Jeon, M.; Lee, W. Developing a TEI-Aware PMIC for Ultra-Low-Power System-on-Chips. *Energies* **2022**, *15*, 6780. https://doi.org/10.3390/en15186780

Academic Editor: Abu-Siada Ahmed

Received: 10 August 2022
Accepted: 7 September 2022
Published: 16 September 2022

1. Introduction

With the explosive growth of wearable and Internet of Things (IoT) devices and the advent of the artificial intelligence (AI) era, demand for ultra-low-power (ULP) system-on-chips (SoCs) is ever-increasing [1,2]. Ultra-low-power (ULP) SoCs consume much less power than conventional low-power design techniques based on ultra-low-voltage (ULV) operating circuitry technology [3]. ULP SoC can consume tens of times less power than conventional normal voltage operating SoC. However, the disadvantage is that the ULP SoC operation speed is very slow and cannot be more than tens of MHz, but even this is not a problem for wearable and IoT devices that can perform applications sufficiently well at this speed.

Recent studies on ULP SoCs have shown that the speed-to-temperature characteristics of ULP SoCs are very different from nominal voltage-operating SoCs, i.e., the operating speed of ULP SoCs increases significantly with temperature rise [2,4]. This phenomenon is the opposite of the properties of the well-known temperature and circuit speed, which is called temperature effect inversion (TEI) [5,6]. Many researchers have actively used this phenomenon to apply it to dynamic power and thermal management methods, and as a result, various TEI-aware low-power (TEI-LP) techniques have been developed [1,4,7–11].

Although the TEI-LP techniques clearly demonstrate the potential to drive ULP SoCs with lower power, these technologies are delaying their advancement to commercial technologies due to obvious limitations: First, the designs of DC-DC Converters have been gradually studied in the research area, but only a few ([12–14]) can work with the ULV operating platforms. Even though these results work in the ULV region, they have the disadvantage of power conversion efficiency (η) under certain load conditions or requiring additional complex circuitry. There have been studies on DC-DC converters for ULV

operation to improve η in wide low-power conditions [15], but there are still problems. It does not take into account the characteristics of the TEI, only the work in the ULV domain. This is because there has been no power management-integrated circuits (PMICs) that can implement the TEI-LP techniques in actual SoCs. For example, in the case of the TEI-aware voltage scaling technique (TEI-VS) that drives the SoC with the lowest supply voltage while maintaining the target clock frequency of the SoC [2,8–10], which is the most well-known technique among the TEI-LP techniques, a PMIC could derive the most optimal supply voltage level for the change in the chip temperature by considering the characteristics of the DC-DC converter. In other words, without finding a suitable DC-DC converter and developing of PMICs that automatically maximize the potential of the TEI-VS according to changes in chip temperature, this technique has no choice but to remain in the research stage.

To tackle this limitation, we conducted research and development with the aim of developing dedicated PMICs for TEI-LP techniques. To this end, we first conducted a study to find the most suitable one for TEI-VS among various types of commercial DC-DC converters. As a result, we were able to determine the most suitable switched capacitor DC-DC converter for the target ULP-SoC. Next, we developed a control algorithm to obtain the most optimal supply voltage for each given temperature in consideration of the conversion efficiency of the DC-DC converter. In this process, we recognized the situation that the optimal supply voltage level data through TEI-VS for each temperature of SoC is fundamentally insufficient. In other words, due to the PVT (process, voltage and temperature) variation, it is necessary to conduct an experiment for each chip in order to obtain the corresponding data. Furthermore, in order to obtain high-resolution data, it is necessary to test the results of the TEI-VS application by changing the chip temperature minutely, which is nearly impossible in reality. Therefore, we devised a method that can extract high-resolution data only from TEI-VS results by temperature with low resolution and applied it to the control algorithm of PMIC that developed it.

In accordance with the characteristics of ULP-SoC, we considered the most energy-efficient way to operate the developed algorithm in the target SoC, and as a result, we finally designed a compact hardware controller IP dedicated to the proposed algorithm. To verify the functional correctness of the developed IP, we designed a RISC-V-based ULP-SoC. After embedding the corresponding IP in this SoC, platform-level functional verification was completed through FPGA prototyping.

The remainder of this paper is organized as follows. Section 2 elucidates the TEI phenomenon in ULP-SoCs and the TEI-VS. Section 3 describes the analysis of the impact of DC-DC converters on TEI-VS and the research on which converter should be selected. Section 4 covers the details of PMIC controller development. Section 5 is the work of verifying the developed PMIC, which develops a prototype ULP-SoC containing PMIC and reports the results of the performing testbench using it. Finally, Section 6 concludes the paper.

2. TEI-LP Techniques

2.1. TEI Phenomenon

The biggest influence on the delay of logic gates τ in the ULP-SoC is the on-current of the transistor I_{on}, in that $\tau \propto 1/I_{on}$. As a temperature T-dependent function, I_{on} can be expressed with the gate-source voltage V_{gs}, the threshold voltage V_{th}, the subthreshold swing coefficient S, and the carrier mobility μ, as shown in the following equation [6]:

$$I_{on} \propto \mu(T) \cdot e^{\frac{V_{gs}-V_{th}(T)}{S(T)}} : V_{gs} \leq V_{th} \quad (1)$$

V_{th}, S, and μ are temperature-dependent device parameters, whereby V_{th} and μ decrease while S increases with rising T. More specifically, in (1), V_{th} affects I_{on} the most, and μ has a slight deceleration effect in the opposite direction. As a consequence, I_{on} increases as T rises, and, in turn, τ decreases. Due to this phenomenon, the worst-case corner of the

ULP-SoCs occur at the lowest operating T. This unique characteristic of the ULP-SoCs is called *Temperature Effect Inversion* (TEI).

We have fabricated an ULP-SoC, which is called TEI-inspired SoC platform (TIP), using 28 nm FDSOI technology through previous work in [2], and this chip has been able to demonstrate that the TEI phenomenon occurs on the actual chip. Figure 1 is the result of measuring the maximum operating speed while maintaining the supply voltage of the chip as the temperature changes. From the figure, it can be clearly seen that the operating speed of the SoC increases as T increases. In addition, it can be confirmed that the worst-case timing corner is determined at the lowest temperature (−10 °C).

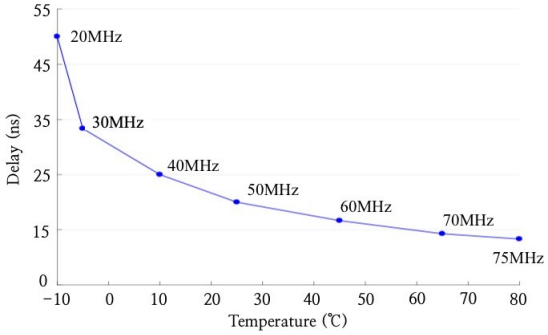

Figure 1. TEI phenomenon in a ULP-SoC fabricated in 28 nm FDSOI technology.

2.2. TEI-Aware Voltage Scaling

SoC must be designed in consideration of normal operation in all operating temperatures in the manufacturing process. That is, in the case of ULP-SoCs, since the worst-case timing corner occurs in the minimum operating temperature, the target clock frequency of the chip, f_{target}, is determined based on this. Therefore, if the chip operates at a temperature higher than the minimum operating temperature T_{min}, a positive delay margin is generated, which is called a TEI-benefit.

As seen in Figure 2, the worst-case corner delay occurred at −25 °C, and the delay decreased while the temperature increased. This TEI phenomenon can be exploited to down scale the voltage level while maintaining the f_{target} [6]. More specifically, the worst-case corner delay of the circuit operating at 0.75 V is the same as the delay at 18 °C when the same circuit is operated at 0.7 V. That is, at 18 °C, the operating speed of the circuit is the same even if the supply voltage of the circuit is lowered from 0.75 V to 0.7 V. When the threshold temperature T_{th} is defined as the temperature at which the voltage can be lowered according to the voltage control resolution of the DC-DC converter (e.g., 0.05 V in the figure) while maintaining the circuit speed, there are several T_{th}'s in the operating temperature range of the circuit, as shown in the figure. Furthermore, the higher the T_{th}, the more aggressive the voltage scaling is possible.

The TEI benefit makes it possible to develop new low-power techniques different from traditional low-power techniques, such as dynamic voltage and frequency scaling (DVFS) or dynamic power management (DPM). For example, if the target clock frequency can be maintained even if the voltage is lowered to some extent due to the increase in the temperature of the chip, we can scale down the supply voltage to the lowest voltage allowed at a given temperature, thereby achieving considerable power savings. This can be theoretically reviewed in more detail through the equation of power consumption in terms of supply voltage V_{DD}, which is as follows:

$$P_{dynamic} = \alpha \cdot C \cdot V_{DD}^2 \cdot f, \quad P_{static} = V_{DD} \cdot I_{off} \tag{2}$$

where $P_{dynamic}$ and P_{static} are the dynamic power and static power consumption of the total power P_{total}, respectively, α is the activity factor, C is the capacitance, and f is the operating clock frequency. Exploiting the TEI-benefit, V_{DD} can be lowered at a certain $T > T_{min}$, while maintaining f_{target}. From (2), lowering V_{DD} drives significant power savings. This

technique is called TEI-VS, the most well-known among TEI-LP technologies [2,8–10]. For example, as shown in Figure 3, when the TIP is operated at 50 and 100 MHz clock frequencies, the required supply voltage at each worst-case corner was 0.54 and 0.61 V, respectively. However, as T increased, it is possible to maintain 50 and 100 MHz clock frequencies at 0.48 and 0.54 V supply, respectively, at 20 °C, and power consumption is reduced by 22.1% and 22.7%, respectively, compared to the case where TEI-VS is not applied. In addition, we can confirm that the supply voltage can be further lowered as T increases, and the power-saving effect becomes larger.

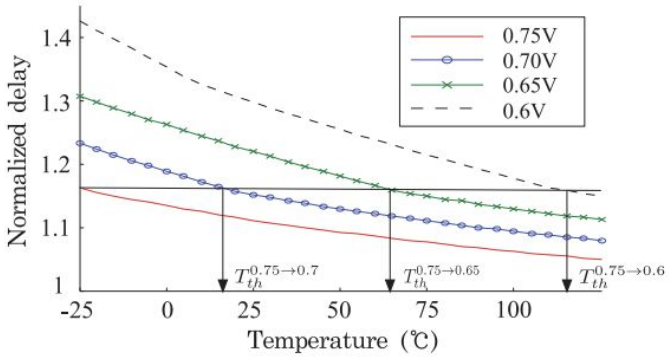

Figure 2. Concept of voltage scaling technique using the TEI phenomenon.

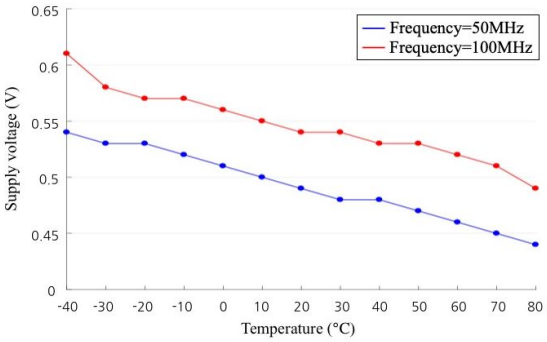

Figure 3. Minimum supply voltage by temperature, measured from the TIP.

3. TEI-VS with DC-DC Converters

Components in the ULP-SoC operate through DC supply. Each component has its own operating voltage range and has a different voltage accuracy requirement [16]. If an unstable voltage is supplied, a malfunction may occur, so it is essential to supply a proper supply voltage for the stable operation of a chip and efficient power management. Therefore, it is very important to select and use a DC-DC converter capable of appropriate power management that stably supplies the required voltage through a chip.

In general, DC-DC converters can be classified into three types, low-dropout regulators (LDOs), switched-capacitor regulators (SCs), and inductive switching regulators, according to circuit implementation and operation principles. From the point of view of on-chip DC-DC converters, LDO and SC are the most widely used since they have the advantages of easy integration and low area overhead compared to inductive switching regulators. In this paper, we also explore LDOs and SCs capable of on-chip integration as DC-DC converters suitable for our goals in PMIC design for the TEI-VS.

Previous studies on TEI-VS have only considered the reduction in power consumption for the SoC itself but have not considered the power dissipation according to voltage conversion, which is the power consumption of the DC-DC converter P_{CONV}. When defining the power savings of SoC owing to TEI-VS as $PS_{TEI\text{-}VS}$, if P_{CONV} is greater than $PS_{TEI\text{-}VS}$, it can cause a serious problem that TEI-VS is not valuable at all. Otherwise, it

still raises the question of whether the effect of TEI-VS is exaggerated. Therefore, this paper first conducts a study to find an answer to this question. The results of the study on TEI-VS considering a DC-DC converter are introduced by distinguishing when LDO is used and when SC is used through the following subsections.

3.1. TEI-VS Using an LDO

In general, LDOs are step-down regulators that only generate an output voltage lower than the input voltage, and the input and output operate linearly [17]. LDO operates through a voltage-controlled current source and provides adjustable output voltage. It is the easiest type of DC-DC converter to implement with a simple configuration and few external components while supporting low noise and high voltage stability. However, as the voltage difference between inputs and outputs is large, heat generation increases and efficiency decreases, so it is limitedly used for small-level voltage conversions. However, our target is for the ULP SoC platform, only for the near-/sub-threshold region. Therefore it does not have the problem of using LDO because of a conversion efficiency issue; it makes sense to use LDO in near/sub-threshold circuits, and it has already been used [18,19].

To find the most suitable LDO for the target ULP-SoC TIP, we explored commercial LDOs closely. The selection criterion was based on the TEI-VS experiment result of TIP, such that the voltage scaling range of LDO must support ultra-low voltage (e.g., 0.44 to 0.61 V), and the conversion efficiency should be sufficiently high. As a result, the TPS7A13 model [20] of Texas instruments was selected.

Subsequently, we conducted an experiment to measure the power consumption according to voltage scaling using TPS7A13. During the experiment, we operated the TIP at 50 MHz clock frequency and T range from −40 to 80 °C. At −40 °C, the worst-case corner, the supply voltage to meet the target f was 0.54 V. Based on this, we set the input voltage of LDO to 0.54 V. The output voltage of LDO followed the TEI-VS result according to T change. The results of the experiment are reported in Table 1. As can be seen in the table, LDO reduces the effectiveness of TEI-VS by about 40% at 80 °C. In other words, from the table, we can observe that LDO fully exhibits the power-saving effect of TEI-VS at low temperatures (i.e., less than 0 °C) but limits the effect seriously in that $PS_{incl,LDO}/PS_{TEI\text{-}VS}$ decreases with increasing temperature. In this regard, from a practical perspective, whereby the operating temperature range of most ULP-SoCs is commonly 0 °C, using LDO may not be the optimal solution to fully exploit TEI-VS.

Table 1. Results of power savings when TEI-VS is applied to TIP, $PS_{TEI\text{-}VS}$, and final power savings when the power consumption of LDO P_{LDO} is included, $PS_{incl,LDO}$.

T (°C)	V_{DD} (V)	$PS_{TEI\text{-}VS}$ (%)	$PS_{incl,LDO}$(%)
−40	0.54	0	0
−30	0.53	3.28	2.46
−20	0.53	4.4	3.61
−10	0.52	8.14	5.61
0	0.51	12.03	6.85
10	0.5	15.53	8.78
20	0.49	19.22	10.98
30	0.48	21.68	12.02
40	0.48	22.25	12.53
50	0.47	26.35	15.39
60	0.46	29.31	17.01
70	0.45	32.88	19.46
80	0.44	35.65	21.03

3.2. TEI-VS Using an SC

SCs are distinguished into three types: a buck type that produces a low output, a boost type that produces higher output, and a buck-boost type that can be used in both cases. SCs have the advantage of providing higher power conversion efficiency, which can be up to 98% depending on the operating conditions and having design flexibility, good thermal performance, and a wide input voltage range [21]. However, in general, SCs have disadvantages in that the switching process creates a higher output noise, requires a lot of external components, is more difficult to control the output voltage than LDO, and takes up more space [22].

The advantages of SCs, i.e., easy on-chip integration and compliance efficiency, make SC widely used for PMICs for ULP-SoCs. Moreover, recent studies on SCs are further accelerating their use [23,24]. Accordingly, there are various types of SCs in the market, and we had to first select the most suitable SC for TIP among them. We selected LTC1261 from Analog Devices [25] as the target SC according to the requirements that the output voltage should be adjusted to a high resolution, and the minimum input voltage should be sufficiently low pursuant to the TIP. Although the LTC1261 is a converter that is typically used to regulate the positive supply to a negative voltage, it has the advantage of controlling the output voltage V_{out} with an ultra-low voltage, according to the circuit diagram in Figure 4. For example, when $C1$, $C2$, $C3$, $C4$, and $R2$ are set to 1 µF, 0.1 µF, 100 µF, 3.3 µF, and 124 kΩ, respectively, V_{out} can be obtained as follows.

$$V_{out} = V1 - 10\mu A(Rs + 124k) \tag{3}$$

Similar to the LDO experiment in Section 3.1, we then performed an experiment to measure the power consumption according to voltage scaling using LTC1261, whereby the schematic used at this time is illustrated in Figure 4. The results of the experiment are reported in Table 2. Through this table and Table 2, it can be seen that the difference between the case of using SC and the case of LDO is clear. First, the power consumed by SC, P_{SC}, is greater than P_{LDO} at a low temperature (e.g., $T \leq 0$ °C), so that the final chip power saving, including P_{SC}, $P_{incl.SC}$ is lower than $P_{incl.LDO}$. However, as shown in Figure 5, as T increases, $P_{SC}/PS_{TEI\text{-}VS}$ decreases rapidly, and as a result, P_{SC} over $PS_{TEI\text{-}VS}$ becomes negligible when $T \geq 30$ °C. This result concludes that although the effect of SC on TEI-VS may differ depending on the T (i.e., the higher the temperature, the better), by taking the most practical temperature condition of the ULP-SoCs into consideration, SC is certainly more suitable for TEI-VS than LDO.

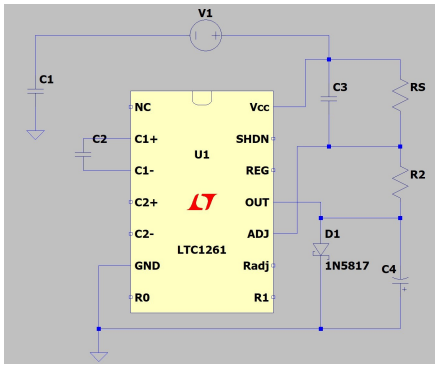

Figure 4. Schematic used for the SC simulations.

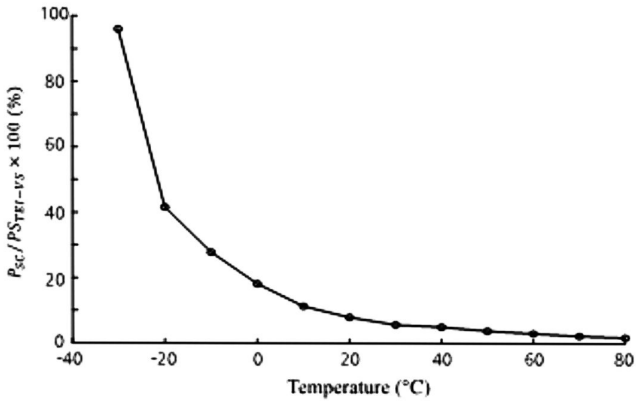

Figure 5. Graph of the result of SC simulations.

Table 2. Results of final power savings when the power consumption of SC P_{SC} is included, $PS_{incl,SC}$.

T (°C)	V_{DD} (V)	$PS_{incl,SC}$ (%)
−40	0.54	0
−30	0.53	0.16
−20	0.53	1.36
−10	0.52	4.29
0	0.51	8.59
10	0.5	11.78
20	0.49	14.74
30	0.48	18.64
40	0.48	21.59
50	0.47	24.35
60	0.46	27.83
70	0.45	31.14
80	0.44	34.87

4. PMIC Controller for TEI-VS

PMIC is essential to realize the power saving of ULP-SoC by applying TEI-VS. Such a PMIC must be able to control the optimal supply voltage suitable for the chip temperature obtained from the temperature sensor mounted within the chip, considering not only the existing TEI-VS results but also the power consumption of the DC-DC converter. In this paper, we develop PMIC for TEI-VS for the first time.

The discriminatory function that PMICs dedicated to TEI-VS must have compared to existing PMICs is that minimum supply voltage must be supplied according to temperature changes. The easiest way to consider achieving this may be to secure data for all sets of (T,V_{DD}) once in advance, store it in the Look-Up-Table (LUT), and load and use the corresponding V_{DD} at each given T. However, considering that it is obvious that the higher the resolution of T's at which the TEI-VS can be applied, the greater the effect of the TEI-VS, this software-based approach may be practically impossible. The reason is that (i) it is difficult to implement more than a certain interval due to the constraints of memory space, and (ii) experiments to acquire (T,V_{DD}) are very time-consuming and labor-intensive. Moreover, considering the PVT variation of the chip, (T,V_{DD}) data must be obtained for each chip, which greatly reduces the practicality, (iii) P_{SC} must also be considered to obtain the optimal V_{DD}, which is significantly influenced by the output current of the SC I_{SC}. For

this reason, I_{SC} should be included as an additional factor in the dataset, which increases the difficulty of implementing this LUT utilization approach exponentially. Further, if safety is not taken into consideration, the ULV platform will break. For example, when the temperature rises, it does not matter because the supply voltage is lower than it was before. However, as the temperature decreases, the voltage value should be high. In such a situation, if only efficiency is considered when designing a PMIC, the optimal voltage may be lower than the minimum supply voltage, which may cause a critical error in operation. Therefore, to prevent such issues, the algorithm should guarantee safety protection.

Therefore, we propose a PMIC hardware controller as the most practical way to develop the PMIC for the TEI-VS. To do that, we first develop an algorithm for the controller to find the optimal V_{DD}, V_{opt}, that maximizes $PS_{incl.SC}$ V_{opt} according to the given T monitored in real-time. As a way to obtain $PS_{incl.SC}$ for any T, we derived the $PS_{TEI\text{-}VS}$ (T,V_{opt}) function through cubic spline approximation [26] using several datasets (in our experiment, 13 datasets measured at 10 °C from −40 °C to 80 °C) obtained during the chip testing stage. Based on this, the derived V_{opt} at T can be expressed by the following equation:

$$V_{opt}(T) = p_3 \cdot T^3 + p_2 \cdot T^2 + p_1 \cdot T + p_0 \quad (4)$$

where p_3, p_2, p_1, and p_0 are the parameters acquired from the aforementioned approximation. At the same time, $PS_{TEI\text{-}VS}$, when using the current V_{DD}, is also calculated so that we perform the first comparison between $PS_{TEI\text{-}VS}(V_{opt})$ and $PS_{TEI\text{-}VS}(V_{DD})$. If the former is larger than the latter, V_{opt} should become a candidate to be examined whether it is still a gain to scale the voltage to V_{opt} even considering P_{SC}. Further, P_{SC} is derived from I_{SC} and V_{opt}, and used. Then, if there is a gain, the current V_{DD} should be switched to V_{opt}. Figure 6 shows a diagram of the proposed PMIC control algorithm. Meanwhile, we may need to consider the safety issue that can arise when the temperature drops or changes rapidly. As a conservative approach, a method of maintaining the voltage slightly higher than V_{opt} and then gradually lowering the voltage to the V_{opt} value may be considered. Alternatively, a method of repeatedly maintaining a value higher than V_{opt} and a value of V_{opt} [9] may be adopted. In addition, we may need to consider the switching time of SC, in that if the time taken for voltage scaling is longer than the time taken for temperature change, a fatal error may occur in the SoC. Fortunately, in general, the temperature change in the chip to require a chip voltage scaling to be made in minutes [11], whereas the switching time of the SC is a few ms or less [27], so unless there is a special case, it may be unnecessary to seriously consider this.

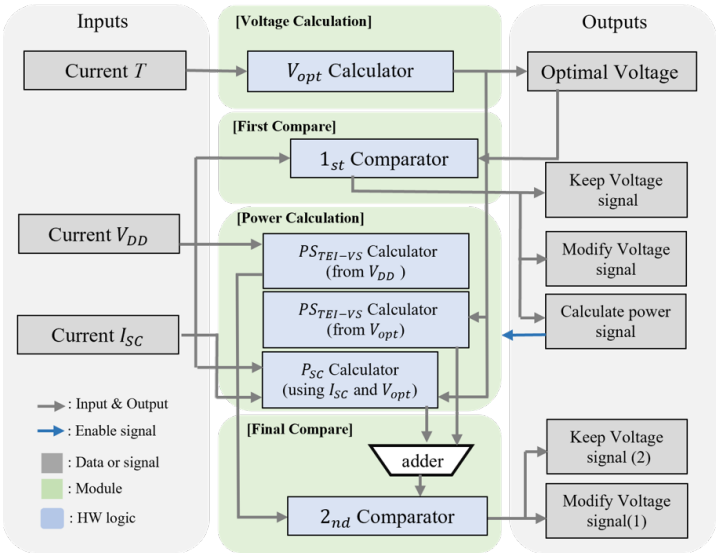

Figure 6. Diagram of the proposed PMIC control algorithm.

Next, we designed a hardware IP that performs the proposed algorithm. For the communication protocol of the IP, we chose an advanced peripheral bus (APB), which is a bus architecture suitable for IP operating at low power without requiring high performance [28,29], was used. As shown in Figure 6, the main logic of the PMIC controller is composed of V_{opt} Calculator, 1st and 2nd Comparators, $PS_{TEI\text{-}VS}$ Calculator, and P_{SC} Calculator.

Among the hardware logic implemented, the V_{opt} Calculator that performs a spline approximation to obtain V_{opt} according to current T has the greatest influence on the overall IP delay. A process for determining p_3, p_2, p_1, and p_0 for each section and a process for deriving V_{opt} must be performed in this logic. In particular, $min(p_3, p_2, p_1, p_0)$ is about 0.0002122, which is very small, and V_{opt} is also small, so floating point operations are required. However, given the size of the ULP platform, adding a full floating-point module is unreasonable. To this end, we designed the V_{opt} Calculator with appropriately sized FPU modules (e.g., floating point addition and multiplication). This results in a significant performance improvement by several to several tens of times compared to when the algorithm is implemented as software. That is because executing the proposed algorithm with a core without an FPU significantly slows the speed used in the cores, and ULP-SoCs tend not to have an FPU, while the PMIC controller we developed contains the required FPU function, enabling the algorithm to be executed much faster. In addition, to improve the operation speed, we used the method of performing two multiplication module instances instead of sequentially performing the operation, as shown in Figure 7. Through this, only four cycles were required for the operation, which is a three-times faster performance improvement than the sequential operation.

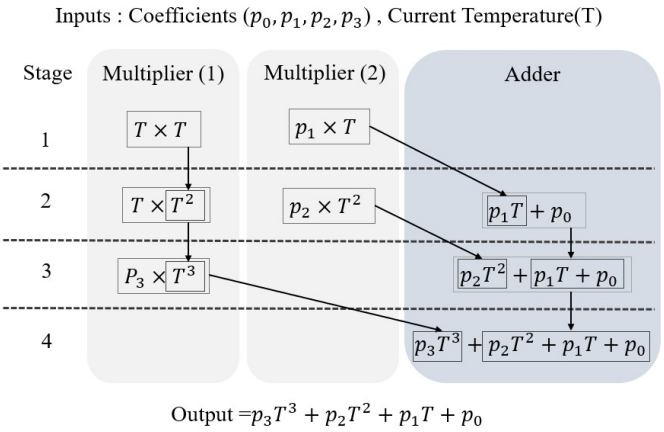

Figure 7. Operation flow of the V_{opt} Calculator.

5. Verification

To verify the function and effectiveness of the PMIC controller, we have implemented a complete verification system, including an ULP-SoC platform, by using RISC-V eXpress [2]. Specifically, the prototype platform was designed to have a dual-core, and for this, two ORCA cores [30] based on the RISC-V were implemented on the platform; the core of each was created as a single core without FPU. Additionally, this platform has a 512 KB SRAM memory and peripherals, including UART, I2C, etc. Finally, all the IPs are interconnected with our pre-developed network-on-chip (NoC). Since the PMIC controller uses the data measured from the actual TIP chip, this architecture is also configured exactly the same as the existing TIP except for the PMIC controller. The detailed prototype architecture of the developed ULP-SoC, including the PMIC controller, is described in Figure 8.

We then prototyped the ULP-SoC in Figure 8 using a Digilent Arty-A7 100T board [31], as shown in Figure 9. To this end, the synthesis was carried out through Xlinx Vivado [32], and the synthesis results are reported in Table 3. As reported in the table, the PMIC controller consumes 1430 look-up tables (LUTs) and 1367 flip-flops (FFs), which take only 5.83% and 5.74% of the entire SoC.

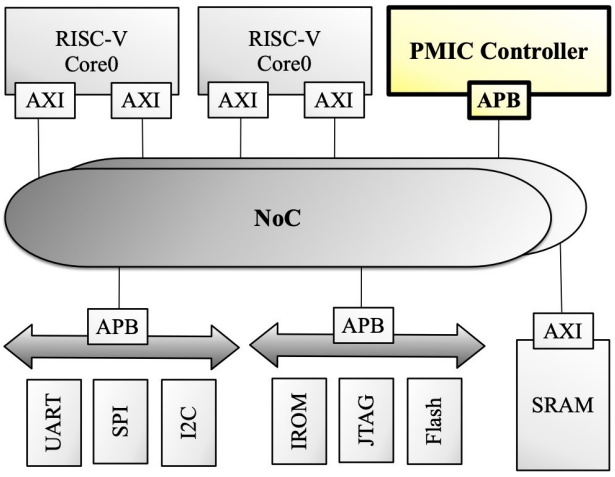

Figure 8. Architecture of the developed ULP-SoC.

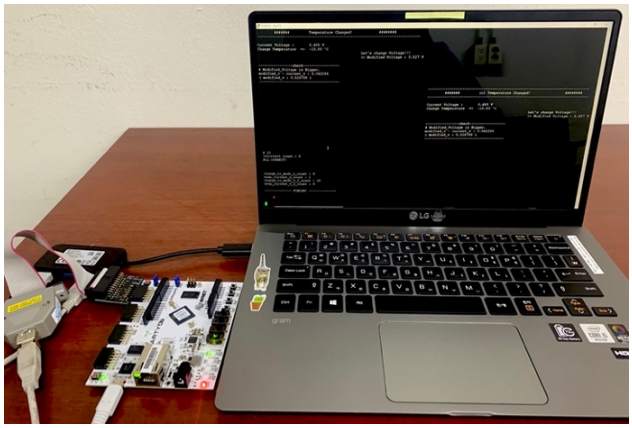

Figure 9. Simulation with FPGA prototyping.

Table 3. Resource consumption proportion on the FPGA.

	LUTs (%)	**FFs (%)**
Cores (×2)	49.63	27.07
PMIC Controller	5.83	5.74
Peripherals	5.59	7.08
NoC	31.53	45.54
EtC	7.42	14.57
Total	100	100

We developed a testbench application that randomly generates a temperature between −40 and 80 °C, adds the input value, and outputs the optimal V_{DD} calculation result using a PMIC controller in the developed ULP-SoC. Next, in order to verify the acceleration performance of the PMIC controller, we developed control algorithm software and simultaneously developed a baseline ULP-SoC prototype without a PMIC controller.

Finally, we set the testbench application to perform the results for a total of 20 random T values and then performed it in both the baseline and proposed ULP-SoC prototypes. As a result, it was confirmed that the total execution time of the application on the ULP-SoC with the PMIC controller took 266 cycles, while the time it took to execute the software only with an ORCA core without FPU reached 41,583 clk. Through this, we can conclude

that the developed PMIC controller is not only the result of the most practical approach but also is far superior in terms of the TEI-VS processing speed.

6. Conclusions

ULP-SoCs are designed based on a circuit operating as ULV, resulting in a TEI phenomenon. It is well known that TEI-LP is a technology that actively utilizes this to drive ULP-SoC with lower power, and TEI-VS, among many TEI-LP technologies, shows excellent power consumption reduction performance. However, studies on PMIC, the only way to implement TEI-VS, have not been conducted so far, and due to this, it can be said that the practical ability of TEI-VS technology is still unverified. In this paper, first, TEI-VS was researched in consideration of the power conversion efficiency of a DC-DC converter, and a practical experiment using commercial LDO and SC was conducted to answer the question of how to find the DC-DC converter most suitable for TEI-VS. Next, the control algorithm of the PMIC dedicated to the TEI-VS in consideration of the DC-DC converter was proposed, and the hardware IP design, which is the most practical method, was conducted to implement the proposed algorithm. Finally, a RISC-V-based ULP-SoC with a PMIC controller was developed, and through experiments performed using the prototype, it was verified that the developed PMIC controller functions normally and exhibits excellent performance.

Author Contributions: K.-B.L., J.P., E.C., M.J. and W.L. were the main researchers who initiated and organized the research reported in the paper, and all authors were responsible for analyzing the simulation results and writing the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2020R1F1A106647413), and in part by the Chung-Ang University Research Scholarship Grants in 2021.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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