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# Systematic Engineering of Metal Ion Injection in Memristors for Complex Neuromorphic Computing with High Energy Efficiency

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**Neuromorphic electronics attract significant attention as a new computing architecture. Despite much effort for achieving practical neuromorphic systems, it is still challenging to construct a synapse array ideal for complex neural networks. Herein, a novel strategy for developing a highly integrated crossbar array of a one-selector–one-memory (1S–1R) synapse by systematically engineering ion injection is demonstrated. In the proposed synapse, an electrochemical metallization (ECM) memristor consisting of unstable filaments and a typical ECM device with stable filaments act as a selector with a low leakage current and a stable memory device, respectively. To overcome the voltage-matching issues in constructing the 1S–1R synapse with high integration density, ion injection related with the electrical properties is optimized in the ECM devices via the distribution of active metal nanoparticles at the interface. The developed synapse possesses a high on/off ratio, superior selectivity, low operating current, and stable multilevel conductance, compared to the previously reported devices. High feasibility for complex neuromorphic systems is demonstrated, and the neural network based on the developed synapse array exhibits reliable parallel computation with high energy efficiency. This promising concept of realizing complex neuromorphic electronics is a fundamental building block for the practical artificial intelligence.**

## 1. Introduction

Neuromorphic electronics mimicking biological nervous systems have attracted significant attention as a new computing architecture with high energy efficiency, for overcoming the von Neumann bottleneck issue.[1–3] In realizing artificial intelligence based on hardware neuromorphic systems, a bio-realistic synaptic memory is a requisite component. Specifically, for neuromorphic computing such as analog vector–matrix multiplication, memory devices should meet various requirements, including multilevel states with nonvolatility and high integration density.[4,5]

A resistive switching device, known as a memristor, is a promising candidate as a memory component for hardware-based neural networks owing to its simple two-terminal configuration, which allows for crossbar–circuit integration.[6–8] In neuromorphic systems based on the crossbar arrays of memristors, the one-selector–one-memory (1S–1R)-structured cell is generally utilized as an artificial synapse to prevent crosstalk between neighboring cells, which causes write disturbance during learning operations.[9–11] Therefore,

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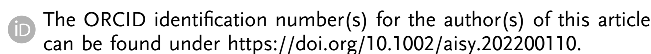
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aisy.202200110.

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**DOI: 10.1002/aisy.202200110**

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considerable effort has been made to develop a selector with low leakage characteristics. However, it is still challenging to achieve a practical 1S–1R cell for highly integrated systems, because the on/off ratio of the cell is inherently restricted due to the strict voltage-matching criteria between the selector and the memory device.[12,13]

To date, various types of mechanisms for the resistive switching phenomena in memristors have been reported, including ionic charge transfer,[14,15] oxygen vacancy ordering,[16,17] and electrochemical metallization (ECM).[18–21] Among them, the ECM-based devices are favorable for realizing the complex neural networks in the view points of scalability and synaptic functionality.[18,20,21] In ECM-based memristors, the resistive switching characteristics are induced by the growth (or dissolution) of a metallic nanofilament according to specific external electric stimuli.[19] In addition, continuous conductance tuning is enabled via the control of the filament size.[21] In recent studies, it was reported that an ECM-based memristor can serve as a selective device with a low leakage current and excellent compatibility with conventional complementary metal–oxide–semiconductor systems.[22,23] In this case, volatile threshold switching is achieved via the formation of unstable metallic filaments. However, a promising way for precisely controlling the structure of the metallic filaments and the memory volatility of the ECM device has not been demonstrated, and the realization of an ECM-based 1S–1R synapse for highly integrated neural networks was barely possible due to the constraints on the voltage-matching requirements.[12,13] Thus, it is essential to devise a strategy for developing an ECM-based 1S–1R synapse with a high on/off ratio.

Here, we demonstrate a practical 1S–1R synapse with high on/off ratio for highly integrated neural networks (see **Figure 1**a). The filament stability and the resultant memory characteristics of the ECM memristors were controlled precisely by ion-injection engineering. Specifically, silver nanoparticles were inserted into the interface between the electrode and the insulator, and the injection of metal ions in the ECM devices was adjusted via the distribution of Ag particles, as shown in Figure 1b. A selector with low leakage current was developed by employing an ECM memristor with a systematically engineered filament structure. Additionally, the operating voltages of the selector were effectively optimized to meet the voltage-matching conditions for constructing the practical 1S–1R synapse operating with low energy by controlling the ion injection. The developed synapse cell exhibited a high on/off ratio of about $10^4$, and the conductance of the cell was stably tuned under the pulse operation. Moreover, in the crossbar arrays of our synapse cell, the sneak current path was prevented completely, and the reliable parallel logic computation was implemented with high energy efficiency. In an analysis based on numerical simulations, the developed 1S–1R synapse demonstrated potential capabilities for realizing complex learning systems.

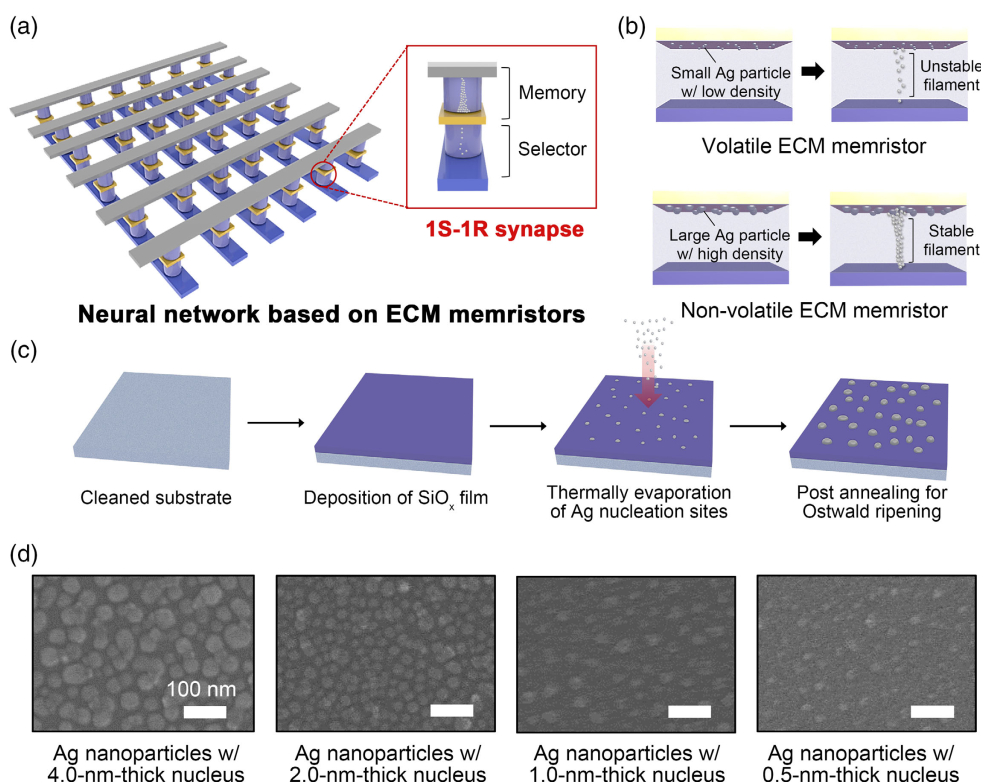


**Figure 1.** Fabrication of the one-selector–one-memory (1S–1R) synapse for highly integrated neural networks. a) Schematics presenting the neural network based on the electrochemical metallization (ECM) memristors. b) The ECM memristor configuration for controlling the ion injection. c) The fabrication process for producing the interfacial Ag particles of the ECM memristor via Ostwald ripening. d) Distribution of the interfacial Ag nanoparticles with different-sized nuclei, as investigated via field-emission scanning electron microscopy.

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## 2. Results and Discussion

To control the injection of metal ions in the ECM memristor, inert metals of gold and indium tin oxide (ITO) were utilized as the top and bottom electrodes, respectively (rather than an active metal for ion injection, such as Ag and Cu), with interfacial Ag nanoparticles introduced between the top electrode and an insulator of silicon oxide ($SiO_x$), as shown in Figure 1b. An Ostwald-ripening-based self-assembly method was used to produce the interfacial nanoparticles (see Figure 1c).[24] The Ag nucleation sites were first prepared via thermal deposition at a low rate of 0.1 Å $s^{-1}$. During the thermal evaporation process, the as-deposited metal atoms balled up on the oxide layer since the surface energy of Ag is far higher than $SiO_x$.[25,26] The Ag nanoclusters were then formed using a post-annealing step at 300 °C. According to the kinetics of Ostwald ripening, Ag nuclei can coalesce as a nanocluster under high-temperature conditions.[27,28] Moreover, the number density and size of the formed Ag particles were controlled via the thickness of the nucleus, as shown in Figure 1d. As the nucleus thickness decreased from 4.0 to 0.5 nm, the average diameter of the particle was reduced from about 32 to about 13 nm, and the number density of the particle also decreased. Note that the Ag particles were maintained after the top electrode deposition (see Figure S1, Supporting Information).

Let us discuss the control of memory volatility in the ECM memristor by adjusting the injection of metal ions. Here, four types of memristor with different density of interfacial Ag particles were fabricated (Devices 1, 2, 3, and 4) using particles with average diameters of approximately 13, 19, 22, and 32 nm, respectively (see **Figure 2**a). The current–voltage ($I$–$V$) characteristics of the devices were first analyzed as shown in Figure 2b. We set three different compliance currents (CCs) of $10^{-6}$, $10^{-5}$, and $10^{-4}$ A in measuring the $I$–$V$ curves of the devices. In all the devices, the electroforming process was performed to trigger the formation of filaments,[29,30] as shown in Figure S2, Supporting Information. For Devices 1 and 2, the volatile threshold switching characteristics were observed irrespective of the CC values, and the hold voltage ($V_{hold}$), whereby a device switches back to a high-resistance state (HRS), was reduced as the CC values were increased. This means that the unstable filaments were formed in the devices, and the growth of the filaments was controlled by

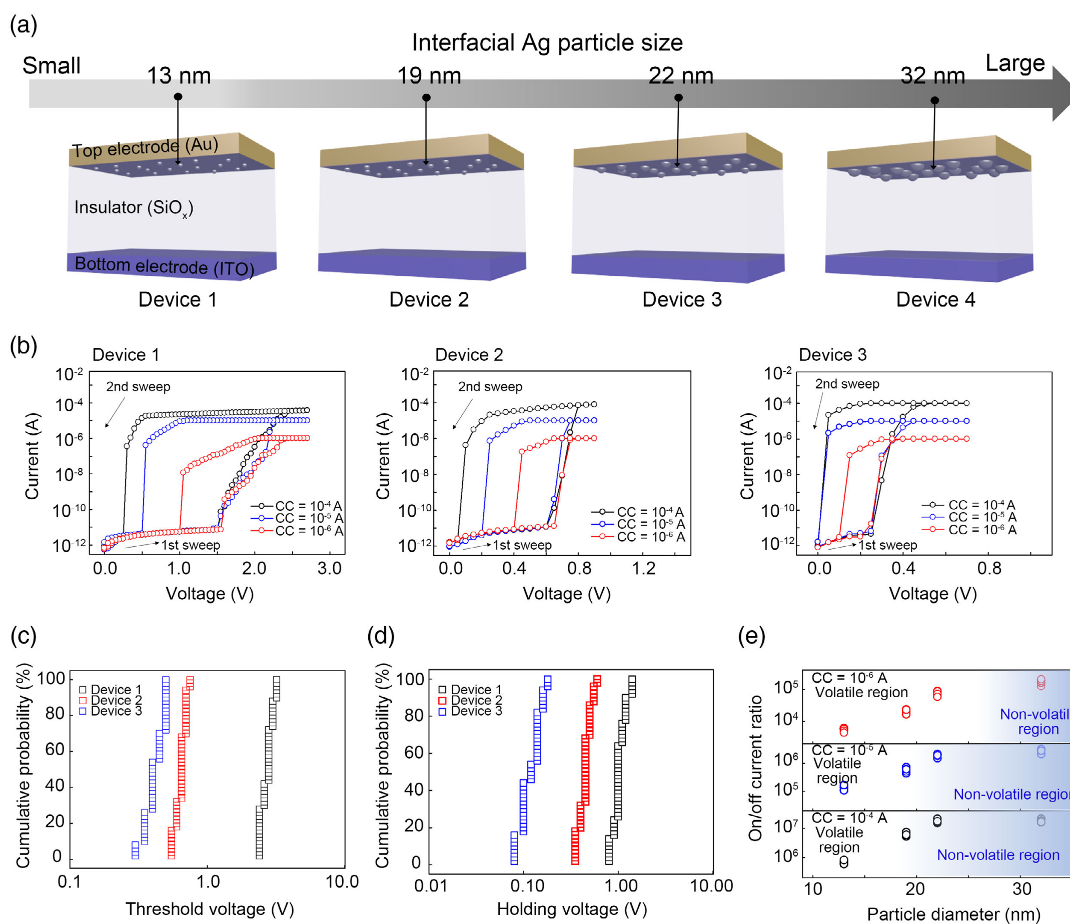


**Figure 2.** Control of memory volatility in the ECM memristor. a) Structures of the four types of ECM memristor with different-sized interfacial Ag particles (Devices 1, 2, 3, and 4 consisting of the particles with an average diameter of approximately 13, 19, 22, and 32 nm, respectively). b) Current–voltage curves of the devices. c) Distribution of the threshold switching voltages of the devices during the repeated cycle tests at the compliance current of $10^{-6}$ A. d) Dispersion of the holding voltages of the devices during the repeated cycles at the compliance current of $10^{-6}$ A. e) On/off current ratio of the devices according to the interfacial Ag particle size.

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the CC. Note that $V_{hold}$ is largely dependent on the filament thickness of the ECM device.[21] Moreover, at a CC of $10^{-4}$ A, the maximum current values of Devices 1 and 2 (about $3 \times 10^{-5}$ and $8 \times 10^{-5}$ A, respectively) were lower than the CC, in the low-resistance state (LRS), being an indicative of the self-CC behavior. These self-CC characteristics of the devices were reliably observed under the repeated cycles of the voltage sweeps (see Figure S3, Supporting Information). Importantly, the self-CC characteristics of the selective device are useful tools for reducing the complexity of the external circuit system.[31] In contrast, Device 3 exhibited volatile memory characteristics only under a CC of $10^{-6}$ A, while Device 4 was operated as a nonvolatile memory regardless of the CC (see Figure S4, Supporting Information). This means that the growth of the metallic nanofilaments is governed by both the CC and the injection of ions. As the size and density of the Ag particles increased (see Figure S5, Supporting Information), the ion injection is achieved in more global terms, resulting in the enhancement of the filament stability and the nonvolatile memory characteristics in the ECM memristor (see Table S1, Supporting Information). In addition to the memory volatility, important factors for the selective device are the operating voltages including a threshold switching voltage ($V_{th}$) and $V_{hold}$. Figure 2c,d shows the distributions of $V_{th}$ and $V_{hold}$ in the devices (Devices 1, 2, and 3) investigated for 50 cycles at CC of $10^{-6}$ A, respectively. Here, the operating voltages of the device were effectively changed according to the variations in ion injection. Typically, in ECM devices, the growth of the filaments is dominated by the electrochemical redox reaction and the ion migration,[32,33] which means that the switching voltage and the filament stability can be tuned via the injection of metal ions. Given that selector–memory voltage matching is a challenging issue for high-density 1S–1R artificial synapses,[11,12] we can consider that our proposed ECM device with controllable operating voltages is feasible for realizing complex neural networks. Figure 2e presents the on/off current ratio of the ECM memristor according to the Ag particle conditions. Here, while the on/off ratio was improved with the increase in particle size and number, at the same time, the device gradually transitioned from volatile switching characteristics to a nonvolatile memory. This implies that a practical ECM selector with a high on/off ratio can be obtained by optimizing the interfacial particle distribution.

To explore the effect of ion injection on the growth of the metallic nanofilament in the ECM memristor, four types of lateral-type devices with different electrode thicknesses were prepared (i.e., L-devices 1, 2, 3, and 4 with electrode thicknesses of 30, 80, 130, and 180 nm, respectively (see **Figure 3**a)). In all the devices, the gap between the electrodes was 30 µm. In typical ECM memristors, since the active electrode is thicker, more metal ions are generated under an electric field.[34] Figure S6, Supporting Information, exhibits the *I*–*V* curves of the devices. In all cases except L-device 1 (which had insufficient metal ions), volatile resistive switching phenomena were confirmed, and L-device 2 showed the self-compliance characteristics due to restricted ion injection. In addition, the $V_{th}$ and $V_{hold}$ values were reduced as the electrode thickness and the resultant number of generated ions were increased, which is consistent with the results shown in Figure 2b–d. To analyze the filament structure, the *I*–*V* curves of specific devices (L-devices 2, 3, and 4) at the LRS were replotted into $\ln(I/V^2)$–$1/V$ scale,[35,36] as shown in Figure 3b. In all the graphs, a linear relationship with a negative slope was observed, while the absolute slope value used for estimating the barrier width was significantly smaller in L-device 4

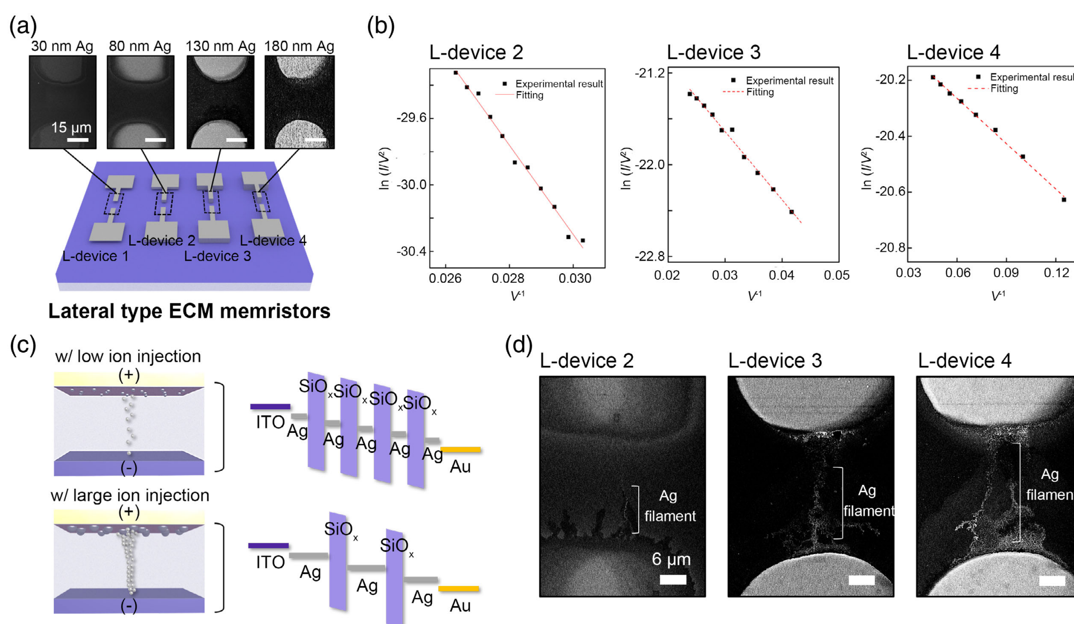


**Figure 3.** Dynamics of the unstable filament growth in the ECM memristor with restricted ion injection. a) Four types of the lateral-type ECM memristor with electrodes with different thicknesses (L-devices 1, 2, 3, and 4 with electrode thicknesses of 30, 80, 130, and 180 nm, respectively). b) The $\ln(I/V^2)$ versus $1/V$ curves of the lateral-type devices. This figure was replotted from in Figure S4, Supporting Information, which was measured at the compliance current of $10^{-6}$ A. c) Schematics illustrating the energy band diagrams for the volatile ECM memristors with the different ion injections. d) Geometric structures of the unstable filaments in the lateral-type devices, as observed via field-emission scanning electron microscopy.

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(about 5) than in L-device 2 (about 268). Such tendency was also observed in our vertical-type devices (Device 1, Device 2, and Device 3), as shown in Figure S7, Supporting Information. In the LRS, the devices followed the tunneling conduction mechanism, and the barrier width was effectively reduced by the increase in the number and size of the Ag particles. This means that the filament structure was controlled effectively by the density of the ion injection.[35,36] As shown in Figure 3c, in the ECM memristors with limited ion injection, the unstable filament was formed under the set process, which led to a tunneling current at the LRS. Moreover, a thicker filament was obtained in the device with greater ion injection, resulting in the reduction of the insulating barrier width. We observed the active surface of the specific devices (L-devices 2, 3, and 4) to directly confirm the unstable filament growth (see Figure 3d). Following a voltage sweep for threshold resistive switching, each device was investigated using field-emission scanning electron microscopy. In all the devices, an unstable filament consisting of Ag nanoparticles was confirmed, and the thinner filament was observed in the case with the lower ion injection, which is accordance with the results in Figure 3b. It should be noted that the lateral diffusion of the metal atoms is more facilitated when the metallic filament in the ECM memristors is thinner.[29,37]

We then realized the 1S–1R-structured artificial synapse by stacking the two different ECM memristors (see **Figure 4**a). The memristor with the interfacial Ag nanoparticles was utilized as the selector and was connected serially to the typical $SiO_x$-based ECM device acting as a multilevel memory. In constructing the synapse with a high on/off current ratio, the electrical characteristics of the ECM memory were first obtained, as shown in Figure S8, Supporting Information. To satisfy the strict voltage conditions, the interfacial particle distribution of the ECM selector was optimized using the same process as for Device 2 in Figure 2. We inserted the Ag particles into the interfaces of the top electrode/insulator and the bottom electrode/insulator, for bipolar threshold switching in the selector (see Figure S9, Supporting Information). As shown in Figure 4b, the developed synapse cell was operated stably as a reversible nonvolatile memory with selective characteristics. At the positive voltage sweeps, the device was transited from the HRS to the LRS, and the resistance state of the device was switched back to the HRS under the negative voltage conditions. The on/off current ratio between the HRS and the LRS at the reading voltage of 0.7 V and selectivity of the device were approximately $10^4$ and $10^5$, respectively, which are considerably higher than the results obtained in previous studies (see Table S2, Supporting Information).[23,38–43] Note that the selectivity of the device was calculated by a ratio between the LRS currents, at the reading voltage (0.7 V) and a half of the reading voltage (0.35 V). Moreover, a current level of our synapse at the LRS (about $10^{-5}$ A) was reduced to less than one-hundredth of the typical memory (about $10^{-3}$ A as shown in Figure S8, Supporting Information), due to the selector acting as an external resistor for suppressing the overshoot phenomenon of the ECM memory.[44] This implies that our developed cell is ideal for realizing highly integrated memory systems and neural networks with high energy efficiency. In the theoretical simulation, the crossbar array of our synapse cell exhibited a high integration density larger than 5.7 Gbit, which is vastly superior to the memristors reported previously[23,38–43] (see Figure S10 and Table S2, Supporting Information). Figure 4c presents the reproducibility

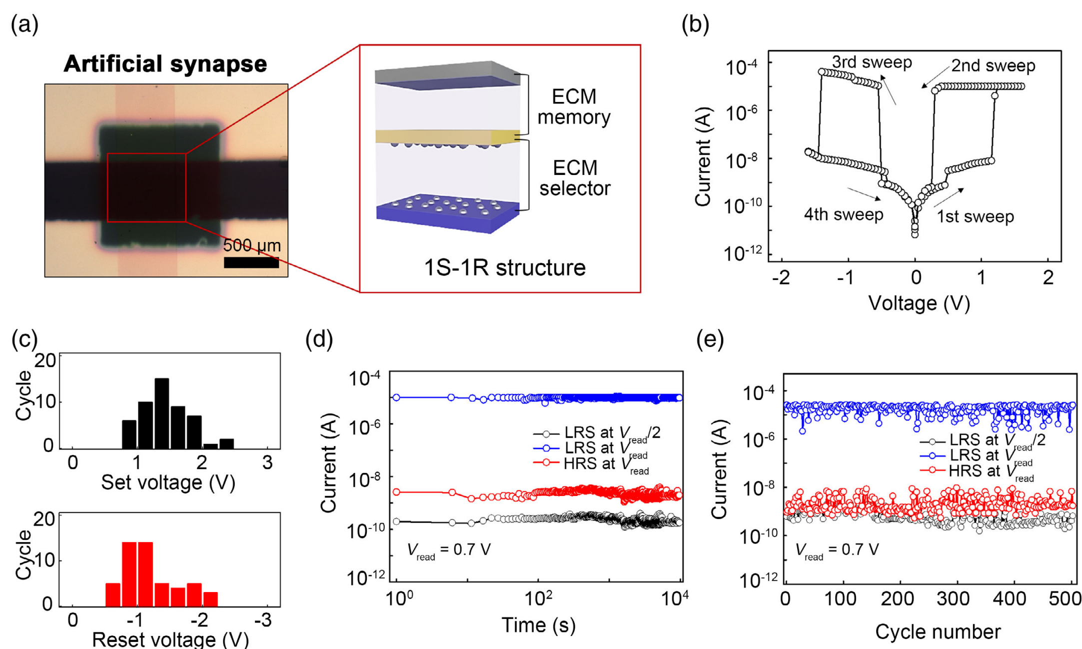


**Figure 4.** Development of the 1S–1R-structured artificial synapse. a) A microscopic image of the artificial synapse consisting of the two different ECM memristors for a memory and a selector. Inset image presents the schematics of the developed synapse structure. b) Current–voltage curves of the device. c) Distributions of the switching voltages of the device in the repeated cycle tests. d) Retention characteristics of the device. A reading voltage ($V_{read}$) of 0.7 V was used. e) Electrical endurance performances of the device. A $V_{read}$ of 0.7 V was utilized, and the cycle tests consisting of the voltage sweeps were performed.


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of the resistive switching in the synapse cell. The variations in the set and reset voltages were measured during 50 cycles, and the attendant temporal changes were evaluated according to the ratio of the standard deviation to the average, which was found to be approximately 0.26 and 0.35, respectively. These results are comparable to those of typical ECM memristors.[44] Additionally, we investigated the distribution of the switching voltages for eight different cells, as shown in Figure S11, Supporting Information. The dispersions of the switching voltages exhibited slight fluctuations due to the stochastic formation of the metallic filaments in the ECM memristor. However, the reliable growth of the filament has been reported in the ECM memristor with the localized ion injection, suggesting that the reliability and the device-to-device uniformity of our synapse can be facilely enhanced.[24,45] Figure 4d,e shows the memory retention and endurance performances of the device, respectively. We used the ramped voltage stresses (instead of pulse voltage stresses) in the endurance measurement, because the voltage sweeping mode is effective to estimate the device conductance accurately.[46] Note that, in realizing the artificial neural network for offline learning systems, the endurance performance of the synapse cell is less strict than that in spiking neural network.[5] The memory states with selectivity were stably maintained for a duration of $10^4$ s, and the device exhibited the reproducible switching characteristics in the repeated 500 cycle tests involving the set and reset voltage sweeps. Furthermore, the reversible resistive switching behaviors were also confirmed in several different cells in a single substrate (see Figure S12, Supporting Information). This means that the developed device can function as a stable artificial synapse for realizing the artificial neural networks. To further confirm the capability of our synapse for practical applications, the transient response of the device was measured at voltage pulses of 2.0 V (for the set process) and −2.0 V (for the reset process), as shown in Figure S13, Supporting Information. The switching times of the device were approximately 27 and 72 μs for the set and reset processes, respectively. In typical ECM memristors, the growth (or rupture) of the metallic filaments is mainly governed by the voltage amplitude, and thus, the switching speed of our synapse can be greatly improved by increasing the amplitude of the pulse.[32,33] Another essential property of the artificial synapse for realizing parallel computation of neuromorphic electronics is the multilevel memory state of the device.[3,5,47] The multilevel conductance of the developed device was thus investigated under the pulse conditions (see Figure S14, Supporting Information). In typical ECM memristors, the metallic filament formation and the resultant resistive switching are achieved abruptly, and thus, the conductance is changed nonlinearly under the repeated electric stimuli with the constant amplitude.[47] To tune the device conductance linearly, varying voltage pulses were used for the measurement. In the potentiation process, the pulse amplitude was increased from 2.1 to 2.5 V, while the pulse width was fixed at 20 μs. In contrast, in terms of depression, the amplitude of the 20 μs voltage pulse was reduced from −2.2 to −2.6 V. The device exhibited reliable multilevel memory states throughout the repeated pulse operation. Moreover, each conductance state was maintained stably (see Figure S15, Supporting Information).

For realizing various applications of neuromorphic computing systems, such as artificial intelligence and pattern–recognition systems, it is important to achieve analog vector–matrix multiplication in the synapse arrays.[4–6] To verify the applicability of the proposed 1S–1R synapse to the practical learning systems directly, we developed a synapse array with a size of 4 × 4, as shown in **Figure 5**a. Then, our neural network based on the 1S–1R synapse was trained in terms of Boolean logic operators, including AND, OR, NAND, and NOR (see Figure S16, Supporting Information). Following the training processes, the target weights were effectively updated to the synapse cells, as shown in Figure 5b. The results indicated that the undesired sneak current leading to write disturbance problems was suppressed effectively in our developed array. Figure 5c shows the configuration of the constructed neural network for Boolean logic. A single layer was composed of four input neurons and four output neurons connected by 16 synapses. In our system, $V_a$ and $V_b$ are two different logic inputs, while $I_{AND}$, $I_{OR}$, $I_{NAND}$, and $I_{NOR}$ denote the output currents for the AND, OR, NAND, and NOR logic computations, respectively. We applied 0.7 V for a logic input of "1" and 0.07 V for the input of "0," to the word lines, and measured the currents at the bit lines for $I_{AND}$, $I_{OR}$, $I_{NAND}$, and $I_{NOR}$. The pulse width of the input voltages was 100 ns. The obtained current for each bit line was compared with a threshold value of 20 μA to determine the logic output. In the case where the bit line current was lower (or higher) than 20 μA, the output was determined as "0" (or "1"). Figure 5d presents the logic operation of our simple neural network according to the two binary inputs. In our system, the logic computation of AND, OR, NAND, and NOR was reliably demonstrated, which implies that our developed synapse array can be utilized for practical applications pertaining to artificial intelligence. Although the average computation energy for each logic in the developed system consisting of the 26 kΩ sensing resistors (see Figure S17, Supporting Information) was approximately 1.28 pJ, similar to that in CMOS counterparts,[48] our system consumes zero standby energy with high computing speed.

To specifically explore the potential of our synapse array for complex neuromorphic computing, a theoretical analysis was conducted in terms of pattern recognition using the SPICE simulation. A dataset for the Fashion Modified National Institute of Standards and Technology (MNIST)[49] was used in the recognition simulation, and a single-layer neural network which is composed of the 784 input neurons for the images with 28 × 28 pixels, and the 10 output neurons for the classes of fashion images was constructed (see Figure 5e). Note that the Fashion MNIST dataset consist of 70 000 gray scale images (60 000 learning images and 10 000 test images) for each class of fashion images. The detailed neural network training processes were as follows. The training process based on the non-negative weights was performed in the 784 × 10 synapses, and the properties of the synapse cell including the conductance memory states were obtained in Figure S14, Supporting Information. The software weights constrained as positive values are feasible to be effectively transferred to the conductance of the hardware synapse cell.[3] It should be noted that in the neural networks for the Fashion MNIST pattern recognition, the operating performances of the software system based on the non-negative weights are close to those of the system involving negative weights (see Figure S18, Supporting Information). As the common conditions in the software training based on TensorFlow (Google's


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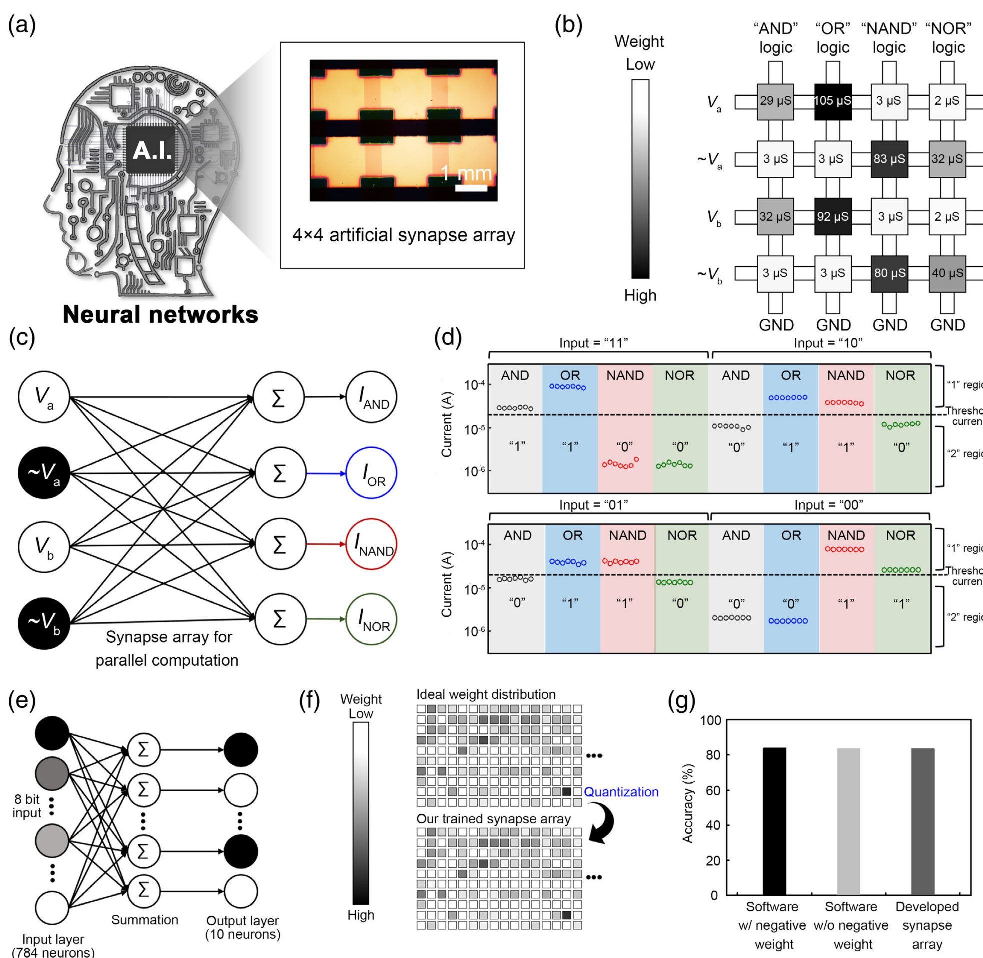


**Figure 5.** Realization of the neural networks based on the developed synapse cell. a) A microscopic image of the developed synapse array and schematics illustrating its application. b) Distributions of the synaptic weights in the synapse array after training for Boolean logic (AND, OR, NAND, and NOR) operations. c) Diagram of the trained neural network for the logic operations. d) Parallel computation for AND, OR, NAND, and NOR utilizing the realized synapse array. e) Schematic diagram of the neural network for recognizing a dataset of the Fashion Modified National Institute of Standards and Technology. f) Distributions of the synaptic weights in the ideal software system and the trained synapse arrays. g) Accuracy for recognizing the fashion images, after training 50 epochs for the ideal software systems and the developed synapse-based neural network.

machine-learning framework), we adopted softmax activation function for the output weights,[50] and utilized the adaptive momentum estimation optimizer[51] and the sparse categorical crossentropy loss function.[52] As shown in Figure 5f, after training, each cell weight was converted into the conductance of our artificial synapse, and quantized to a specific level in certain cases. In the hardware simulations, the quantized weight values were directly implemented as resistor elements on the synapse array. For inference of the arrays, the input voltage between 0 and 1 V was set, and the output current of each bit line was confirmed. In classifying the fashion images, our trained neural network exhibited an accuracy of approximately 84%, which is extremely close to that of the ideally simulated software systems (see Figure 5g). Under the training processes, the recognition accuracy of each system was improved with increasing the epochs at the initial step; however it shows a tendency to saturate after about 10 epochs owing to the convergent properties in the neural networks[53] (see Figure S18, Supporting Information). Moreover, when the 100 ns voltage pulse was utilized as the input signals, our developed system with the sensing resistors of 1 mΩ consumed approximately 2.56 nJ in recognizing each fashion image, being indicative of the high energy efficiency, which is vastly superior to that of the von Neumann computing system.[54]

## 3. Conclusion

In conclusion, we implemented the crossbar arrays of an ECM-based synapse for practical neuromorphic computing systems. We developed the 1S–1R synapse with a high on/off ratio and low operating current by utilizing the ECM memristors with the systematically engineered ion injection. It was found that the memory volatility was effectively controlled by the ion injection in addition to the various electrical properties of the memristor, including its operating voltages, on/off ratio, and self-compliance characteristics. In constructing the 1S–1R


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structured artificial synapse, the ion injection in the ECM device acting as a selector was optimized to achieve the voltage matching with the memory device. Our developed synapse exhibited a superior on/off ratio (about $10^4$) and selectivity (about $10^5$) with controllable multilevel conductance, both of which are ideal for highly integrated neuromorphic electronics. Moreover, the crossbar arrays of our synapse theoretically exhibited a high integration density of over 5.7 Gbit as well as the reliable parallel computation of Boolean logic. In addition, the neural networks incorporating our synapse array demonstrated good applicability for realizing practical learning systems with high energy efficiency. Our hardware-based neural networks effectively recognized the complex fashion images with an accuracy of approximately 84%, which is close to that of the ideal software-based neural networks. The recognition process for each complex image was achieved with the ultralow energy consumption (about 2.56 nJ). This promising strategy for achieving highly integrated neuromorphic electronics would provide a fundamental building block for developing the next-generation computing systems linked to artificial intelligence.

## 4. Experimental Section

The geometrical profiles of the films were measured using an atomic force microscope (XE-100, PSIA), while the electrical characteristics of all devices were measured utilizing a semiconductor parameter analyzer (4200-SCS, Keithley) integrated with an ultrafast *I–V* module (4225-PMU, Keithley). In the electrical measurements of the vertical memristors and the artificial synapse, the scanning voltage was applied to the top electrode, and the bottom electrode was grounded. All the electrical measurements were performed in an ambient air condition. The distribution of the interfacial Ag nanoparticles in the devices and the Ag nanofilament structure in the lateral-type memristors were observed utilizing a field-emission scanning electron microscopy instrument (S-4800, Hitachi).

In preparing the ECM memristors with the interfacial metallic particles (Devices 1, 2, 3, and 4), an ITO-patterned glass substrate was cleaned sequentially by ultrasonication in acetone, isopropyl alcohol, and deionized water for 30 min. As an insulating layer, silicon oxide ($SiO_x$) of 200 nm thick was produced over the substrate via plasma-enhanced chemical vapor deposition (PECVD) (PlasmaPro System100, Oxford). To form the interfacial Ag particles for Device 1, Device 2, Device 3, and Device 4, Ag films with thicknesses of 0.5, 1.0, 2.0, and 4.0 nm were deposited, respectively, by the thermal evaporation at 0.1 Å $s^{-1}$ under $10^{-6}$ Torr. Each Ag film was baked at 300 °C for 1 h, to obtain the Ag nanoparticles. For the top electrode, a gold film of 50 nm thick was thermally evaporated at 2.0 Å $s^{-1}$ under $10^{-6}$ Torr. The active area for each vertical-type device was $0.5 \times 0.5$ mm.

To fabricate the lateral-type ECM memristors (L-devices 1, 2, 3, and 4), first, a glass substrate was cleaned sequentially via ultrasonication in acetone, isopropyl alcohol, and deionized water for 30 min. For the insulator, $SiO_x$ of 200 nm thickness was produced over the substrate via the PECVD (PlasmaPro System100, Oxford). As the electrodes for L-devices 1, 2, 3, and 4, Ag films with thicknesses of 30, 80, 130, and 180 nm were thermally deposited on the oxide film, respectively, at 0.8 Å $s^{-1}$ under $10^{-6}$ Torr. The active area for each lateral-type device was $0.03 \times 0.03$ mm.

In fabricating the artificial synapse, the ECM memristor with the interfacial Ag particles was first prepared as a selector, and the typical ECM memory device was vertically stacked onto the prepared selector. An ITO-patterned glass substrate was cleaned sequentially via ultrasonication in acetone, isopropyl alcohol, and deionized water for 30 min. Note that the ITO pattern acted as a bottom electrode in the synapse. The bottom interfacial particles were formed on the substrate by thermally evaporating an Ag film with thickness of 1 nm at 0.1 Å $s^{-1}$ under $10^{-6}$ Torr. The Ag film was annealed at 300 °C for 1 h. As the insulator of the selector, $SiO_x$ of 200 nm thick was formed over the substrate using the PECVD (PlasmaPro System100, Oxford). Then, the top interfacial particles were produced on the oxide film by the same process as the bottom particles. For the top electrode of the selector, and the bottom electrode of the memory, a 50 nm thick gold layer was thermally evaporated on the top interfacial particles, at the rate of 2.0 Å $s^{-1}$ under $10^{-6}$ Torr. We formed the memory insulator of a 200 nm $SiO_x$ film on the gold electrode by PECVD (PlasmaPro System100, Oxford). As the top electrode of the synapse, a silver layer with 50 nm thickness was thermally deposited at the rate of 0.8 Å $s^{-1}$ under $10^{-6}$ Torr. The active area of the 1S–1R synapse was $0.5 \times 0.5$ mm.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.


## Acknowledgements

S.E.K. and M.-H.K. contributed equally to this work as the first author. This work was supported by the National Research Foundation of Korea (NRF) under grant funded by the Korea Government (MSIT) (Grant no. 2020R1F1A1075436). This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (2021M3F3A2A03017764). This research was supported by Samsung Electronics Co. and the BK21 FOUR project funded by the Ministry of Education, Korea (Grant no. 4199990113966).


## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.


## Keywords

artificial synapses, memristors, neural networks, one selector-one memory, parallel computation

Received: May 2, 2022
Revised: May 23, 2022
Published online: June 21, 2022



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