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Performance Evaluation of Per-Phase Model Predictive Control Schemes for Extending Lifespan of Voltage Source Converters

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Abstract: Unequal thermal stress among the phase legs of a multiphase converter leads to a reduction in the useful lifespan and reliability of that converter in general. Increasing the converter's lifespan by relieving the stressed phase leg, which suffers excessive thermal stress due to aging, is crucial. This paper evaluates two control concepts, including two per-phase model predictive control methods for extending the lifespan of a voltage source inverter. These two per-phase techniques alter the switching pattern to reduce the losses of the most aged phase leg. Hence, the loss and the corresponding thermal stress of the leg that has aged the most are reduced. In such a way, the lifespan and reliability of the converter are prolonged. Two per-phase model predictive control techniques are executed in both simulation and experiment environments, where the corresponding results are provided to evaluate the behavior of these control strategies, considering several operational aspects both in steady state and transient operation. In addition to static load conditions, two per-phase techniques are verified for the correct operation under dynamic load (induction motor) conditions.

Keywords: per-phase; model predictive control; lifespan; voltage source converter

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1. Introduction

The increasing number of power electronics applications in industry, consumer electronics, and transportation leads to an increasing importance of power converters for power systems. Due to the simplicity of their structure and their ability to handle the voltage by keeping the system stable, two-level three-phase dc/ac voltage source inverters (VSIs) are now extensively used in motor drives, active filters, unified power flow controllers in power systems, and uninterrupted power supplies to generate controllable frequency and ac voltage magnitudes [1–4]. The lifespan of a power converter is mainly based on the lifespan of power switches. Hence, it requires improving the lifespan of power switches to prolong the lifespan of a converter. The main reason for aging states or failure in power switches and capacitors is thermal stress [5,6]. It is widely recognized that thermal stress is a crucial factor in determining the lifespan of power devices. Thus, increasing a converter's lifespan by relieving stressed power switches, which suffer excessive thermal stress, is necessary.

The most commonly used method to lower the junction temperature of power devices is switching frequency control [7]. The switching frequency is a loss-dependent variable that mainly affects the switching losses of power semiconductor devices. Thus, the switching frequency is usually used to adjust a converter's junction temperature [7]. In [8,9], for a two-level inverter used in an adjustable speed drive application, switching frequency reduction techniques based on junction temperature change have been presented. However, this will introduce a lot of calculations and depend on the parameter accuracy. The discontinuous pulse-width modulation (DPWM) [10–12] is a widely used technique that works by clamping the converter's output reference voltage to the upper rail or lower rail of a dc link during a defined period of time to prevent the corresponding power device from

switching. Thus, the switching loss is reduced. The consequent mean value of junction temperature and its variance are also decreased as a result of the decreased power device loss during the clamping period. However, because of the switching loss reduction in both three-phase legs, the output current performance of the VSI is decreased with a higher total harmonic distortion (THD). The model predictive control (MPC) method, referred to as a class of digital control algorithms, uses the model of the system to predict the future behavior of a converter and thus select the optimal switching state to precisely operate the converter [13–16]. In [17], a cost function is added through a linear low-pass filter to lower the power loss under the MPC strategy implementation. By excluding switching states that are predicted to have greater power losses, this filter helps reduce thermal stress. Nonlinear constraints, however, might have an impact on how accurate the linear filter is. Nonlinear restrictions could lead to the filter being mistaken and have a substantial impact on how the MPC problem is formulated. The author in [18] introduces a predictive control technique based on preselecting the switching states to evenly distribute the power loss in three-phase legs as well as decrease the switching loss. The capability of MPC to simultaneously control multiple targets is one of its advantages. Along with other control objectives, like output currents, voltage, etc., an additional cost function is added to the traditional MPC method to decrease the number of switching transitions or the junction temperature of switching devices [19,20]. However, it can be difficult to adjust the weighting factor for every control objective in the cost function. Additionally, the output performance of the converter might be decreased due to the existence of multiple control objectives in a cost function.

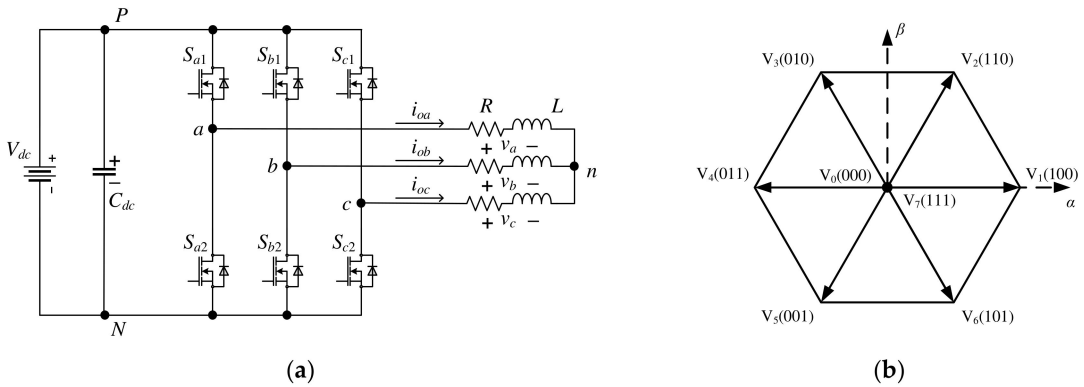
It can be seen that previous studies mainly focused on uniformly reducing the switching loss of an entire converter without considering the different aging states among phase legs. In three-phase VSIs, the different aging states and predicted lifespans for each phase leg might be caused by unequal operating stress, switch failure, or switch replacement in the past. Furthermore, their manufacturing processes are considered a potential cause of the failure of semiconductor devices. Therefore, increasing a converter's lifespan by relieving the most stressed phase leg or the leg that has aged the most, which suffers excessive thermal stress due to aging, is crucial. Hence, several per-phase techniques, which aim at reducing the thermal stress of the leg that has aged the most, are proposed. The strategy in [21] alters the switching strategy to reduce the loss of a particular power switch in a three-level neutral-point-clamped converter by using redundant switching states. In [22], the author proposed a PWM method using a hybrid offset voltage injection to decrease the switching loss in the most aged leg. However, due to using direct output currents as a condition to detect the clamping regions, this method is mainly effective under a unity-power-factor load. Meanwhile, the author in [23] modified the DPWM1 technique to lower the switching loss in a particular phase leg of a voltage source rectifier. Regarding the MPC techniques, which will be evaluated in this study, the first considered technique is per-phase MPC with an offset voltage injection method, termed per-phase MPC1 [24]. Unlike conventional MPC, the per-phase MPC1 technique employs modified predicted reference voltages to control the phase currents and reduce the switching loss in a specific phase leg. It achieves this by generating a predicted zero-sequence voltage (ZSV) and introducing it to the predicted reference voltage of the targeted phase leg, effectively limiting that phase leg's operation by clamping it to the upper or lower rails of a dc link. These clamping periods make the considered aged leg keep its switching state for a period of time. Per-phase MPC1 can generate a maximum clamping period of 120° in both the upper and lower rails of the dc link for the targeted aged leg. Regarding the remaining per-phase MPC method, a per-phase MPC technique with the preselection of a switching state [25], termed per-phase MPC2, will be discussed. The approach of preselecting the switching state defines the clamping period of the leg that has aged the most and the related switching states from the available voltage vectors of the VSI based on the predicted reference voltages. By choosing the optimal switching state among the preselected voltage vectors by evaluating a predefined cost function, the switching frequency and power loss in the leg that has aged the most are lowered. The lifespan of the leg that has aged the

most will rise due to a reduction in thermal stress, which will also increase the lifespan of the VSI. As for the per-phase MPC techniques, they require determining the leg that has aged the most. The diagnosis methods require an aging indicator to identify the current aging status of the power semiconductor devices. Aging indicator identification on power semiconductor devices has been carried out by performing accelerated aging experiments with the monitoring of selected parameters. Accelerated aging tests allow the effects of failure mechanisms to be analyzed and aging indicators to be identified. Various electrical aging indicators for IGBTs have been investigated and proposed in the literature, such as changes in the collector–emitter on-state voltage, $V_{ce,on}$ [26,27], the threshold voltage, V_{th} [28,29], and the temperature [30–32]. However, the diagnosis method is outside of the scope of this study, so a detailed description is not included.

The objective of this paper is to discuss, evaluate, and compare the features and performance of VSIs controlled by two per-phase MPC schemes. Fundamental principles, operation concepts, and performance outcomes are employed to establish a comparison between two per-phase MPC approaches. From this comparison and evaluation, the better technique will be determined in terms of reducing the switching loss of a specific phase leg in a VSI to extend the corresponding lifespan. Additionally, the two per-phase MPC methods are compared by employing them in various settings in terms of the sampling frequency, output power, load condition, and parameter uncertainty. This helps tailor the selection of per-phase MPC methods based on the unique requirements and constraints of a particular situation or problem. These methods are conducted in both a simulation and an experiment to obtain comparable results. This study is structured as follows. The control concepts of the two per-phase MPC methods are reviewed after an overview of two-level three-phase VSIs. Then, the simulation and experiment outcomes are discussed for a comparison between the per-phase MPC1 and per-phase MPC2 approaches.

2. Per-Phase MPC Methods for VSI

Figure 1a shows a model of the system used in this study. It includes a two-level three-phase VSI and a resistive–inductive RL load. The two-level three-phase VSI comprises three-phase legs that have the capability to link the load terminals either to the positive (P) rail or negative (N) rail through the control of two power switches within each leg. The upper and lower power switches in each phase leg are denoted by S_{x1} and S_{x2} $(x = a, b, c)$, respectively. With three phases and two states for each phase, there are a total of eight distinct switching configurations. Thus, the VSI applied to the load corresponds to eight voltage vectors, as presented in Figure 1b.



(**a**) (**b**)

Figure 1. (**a**) Configuration of 2-level 3-phase VSI; (**b**) voltage space vectors of 2-level 3-phase VSI.

As indicated earlier, the different aging states and predicted lifespans in the three-phase legs might have been caused by unequal operating stress, switch failure, or switch replacement in the past. Figure 2a depicts the consideration that phase a is the leg that has aged the most.

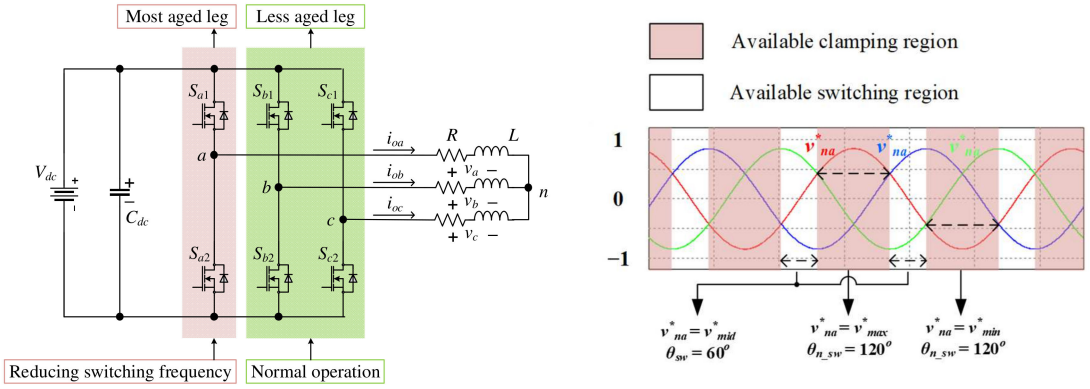


Figure 2. (**a**) Example where phase *a* is the leg that has aged the most and the principle of per-phase control for increasing lifespan. (**b**) Available clamping and switching region of phase *a* ("*" stands for reference).

The general idea of per-phase control for increasing the lifespan of a phase leg is to reduce the corresponding switching frequency and loss by decreasing the number of commutations of the most aged power switches. This can be realized by not changing the switching state of the leg that has aged the most for a period of time. Hence, the thermal stress on the most aged devices can be decreased, and the consequent lifespan of the converter can be prolonged until the next maintenance. Figure 2b illustrates the normalized reference voltages, v^*_{na}, v^*_{nb}, and v^*_{nc}. As mentioned earlier, this study considers phase *a* to be the leg that has aged the most. The possible clamping and switching regions can be chosen by considering the immediate magnitude of the reference voltages. After normalization, the normalized reference voltages are sorted based on their magnitudes and given as follows:

$$\begin{cases} v^*_{max}(k) = \max\left[v^*_{na}(k),\ v^*_{nb}(k), v^*_{nc}(k)\right] \\ v^*_{mid}(k) = \text{mid}\left[v^*_{na}(k),\ v^*_{nb}(k), v^*_{nc}(k)\right] \\ v^*_{min}(k) = \min\left[v^*_{na}(k),\ v^*_{nb}(k), v^*_{nc}(k)\right] \end{cases} \tag{1}$$

It can be seen from Figure 2b and by following (1) that the maximum clamping period in a specific leg can reach 120° in both the upper and lower rails. In this case, the normalized reference voltage of the leg that has aged the most (phase *a* in this case) will be the maximum or minimum voltage. During the clamping periods, the switches of the leg that have aged the most maintain their state during a 120° period of time. This leads to a notable decrease in the switching frequency and loss. This principle is used in both the per-phase MPC techniques.

First, the operational concept of per-phase MPC1 is reviewed, followed by a description of per-phase MPC2. For all the per-phase control techniques, the same maximum clamping angle of 120° is applied in the two control schemes discussed.

2.1. Per-Phase MPC1

The model prediction stage and the cost function minimization stage are the two main stages of an MPC method. MPC performance is influenced by the adequate quality of the prediction model, which depends on the specific application under consideration. In this case, the prediction model of the 2-level three-phase VSI, depicted in Figure 1a, corresponds to the equation of the three-phase *RL* load as follows:

$$v_x = Ri_{ox} + L\frac{di_{ox}}{dt}\ (x = a, b, c) \tag{2}$$

where v_x is the voltage generated by the inverter and i_{ox} is the load current. By applying a sampling period, T_{sp}, and the Euler approximation algorithm, the relation between the discrete-time variables can be described as

$$i_{ox}(k+1) = \left(1 - \frac{RT_{sp}}{L}\right) i_{ox}(k) + \frac{T_{sp}}{L} v_x(k) \ (x = a, b, c) \tag{3}$$

Equation (3) is used to obtain a prediction for the future value of the load current, $i_{ox}(k+1)$, considering all possible voltage vectors, v_x, generated by the inverter and the measured current in the kth sampling interval. The future value of the load current is predicted for the eight switching states generated by the inverter by means of (3). The predicted reference voltage, $v_x^*(k)$, is obtained by substituting $i_{ox}^*(k+1)$ for $i_{ox}(k+1)$ in (4) and rearranging as follows:

$$v_x^*(k) = \frac{1}{T_{sp}} \left\{ L i_{ox}^*(k+1) + \left(RT_{sp} - L\right) i_{ox}(k) \right\} \tag{4}$$

By comparing $v_x^*(k)$ to the eight available voltage vectors, the optimal switching state that achieves the smallest difference between them will be selected. This selection aims to minimize the difference between the predicted output voltage and the reference voltage at the $k+1$ instant. As a result, the cost function, g, for conventional MPC is formulated as follows:

$$g_v = |v_x^*(k) - v_x(k)| \ (x = a, b, c) \tag{5}$$

Figure 3 depicts a block diagram of conventional MPC using the predicted reference voltage.

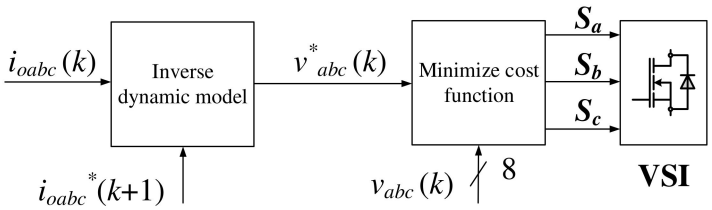


Figure 3. Block diagram of conventional MPC ("*" stands for reference).

Regarding per-phase MPC1 [24], to lower phase a's switching frequency, the predicted ZSV is defined following the available clamping and switching regions of phase a as follows:

$$\begin{cases} v_{ZSV}(k) = 1 - v_{max}^*(k) if \ v_{max}^*(k) = v_{na}^*(k) \\ v_{ZSV}(k) = -1 - v_{min}^*(k) if \ v_{min}^*(k) = v_{na}^*(k) \\ v_{ZSV}(k) = -\frac{v_{max}^*(k) + v_{min}^*(k)}{2} \ other \ cases \end{cases} \tag{6}$$

The predictive zero-sequence voltage is produced in such a way that the particular phase a converter's reference voltage in (4), with a predictive zero-sequence voltage injection, connects the corresponding phase to the upper or lower dc-link rail to create a non-switching region. By using (6), a clamping period of 120° will be generated when adding the predicted ZSV to the predicted reference voltages, which keeps the switching states of phase a unchanged for a corresponding period of time. The modified predicted reference voltages, $v_x^{**}(k+1)(x = a, b, c)$, are produced by adding the predicted ZSV to the predicted reference voltages as $v_x^{**}(k) = v_x^*(k) + v_{ZSV}(k) \ (x = a, b, c)$, as shown in Figure 4. Hence, the cost function in per-phase MPC1 will be described as

$$g_v = |v_x^{**}(k) - v_x(k)| \ (x = a, b, c) \tag{7}$$

In per-phase MPC1, relying solely on the cost function in Equation (7) does not ensure an accurate selection of switching states that correspond to a zero-voltage vector. Incorrectly choosing the zero-voltage vector could lead to undesired switching actions, thereby raising

switching losses. Consequently, when selecting zero-voltage vectors, the polarity of the predicted *ZSV* is carefully considered.

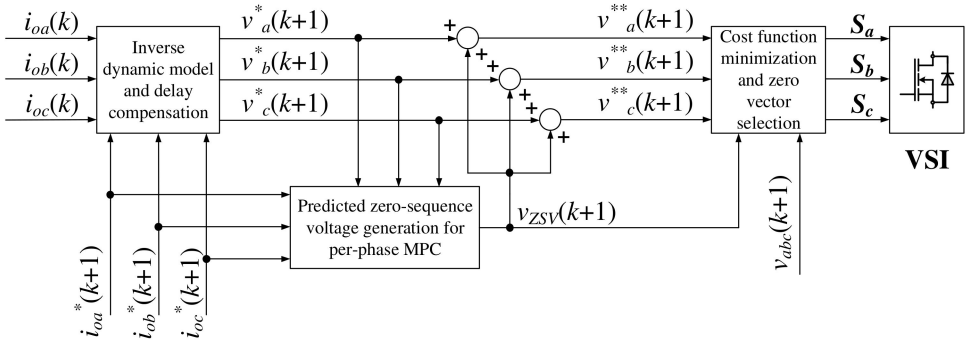


Figure 4. Block diagram of per-phase MPC1 ("*" stands for reference, "**" stands for modified reference).

2.2. Per-Phase MPC2

Different from the per-phase MPC1 method, a switching state preselection algorithm is employed in the following per-phase MPC technique, termed per-phase MPC2 [25]. Figure 5 illustrates the control diagram of per-phase MPC2. If we assume phase *a* is the leg that has aged the most, the best switching state will be chosen among the preselected voltage vectors $V_1(100)$, $V_2(110)$, $V_6(101)$, and $V_7(111)$. These voltage vectors can maintain the ON-state of the upper switch in phase *a*, resulting in a decrease in the number of commutations, as shown in Figure 5b. In the same manner, the preselected voltage vectors $V_3(010)$, $V_4(011)$, $V_5(001)$, and $V_0(000)$ can maintain the ON-state of the lower switch in phase *a*. Hence, one of these four preselected voltage vectors is chosen by evaluating the same cost function in (5) as in conventional MPC. The upper and lower switches in the leg that has aged the most will be kept in their switching states when the corresponding predicted reference voltage is identified as $v^*_{max}(k)$ or $v^*_{min}(k)$. Conventional MPC is implemented in the remaining situations using the eight switching states that are available. This switching state preselection algorithm also generates a maximum clamping period of 120°, as in the previous per-phase MPC1 method.

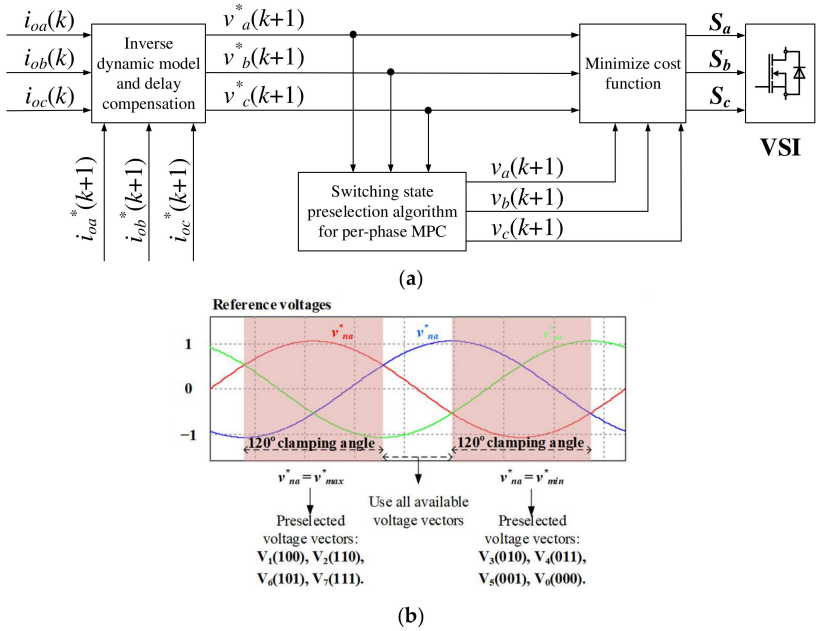


Figure 5. (**a**) Block diagram of per-phase MPC2. (**b**) Switching state preselection when considering phase *a* is the leg that has aged the most ("*" stands for reference).

3. Performance Comparison

In this section, a performance comparison between the two per-phase MPC techniques is carried out in both a simulation and an experiment using the parameters listed in Table 1. Furthermore, in both the control schemes, phase a is considered the leg that has aged the most.

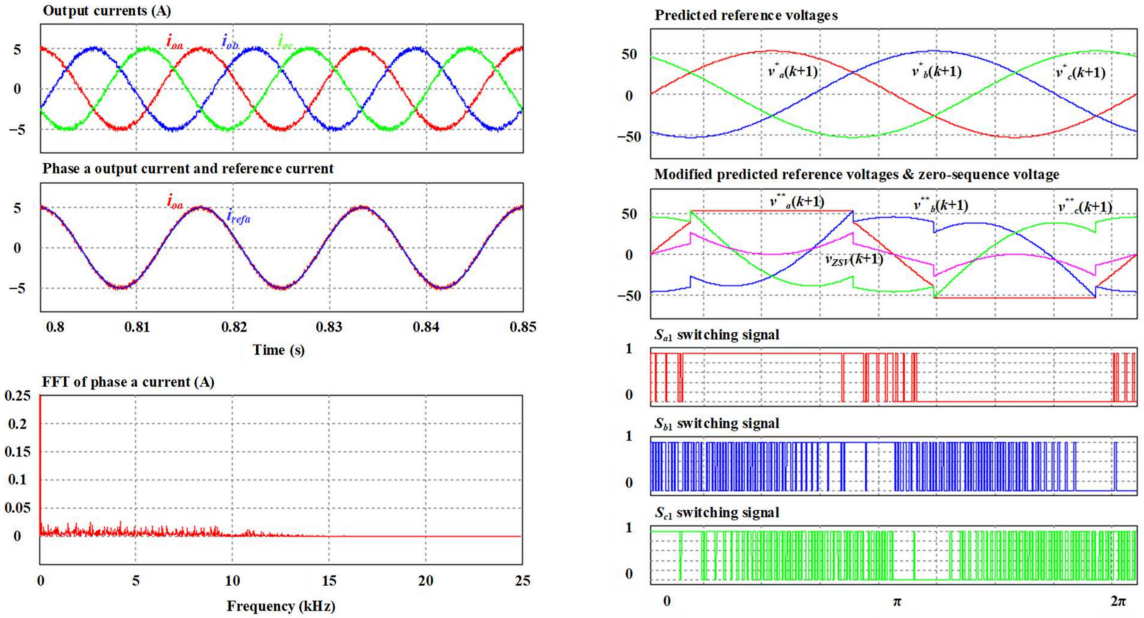
Table 1. Parameters of 2-level 3-phase VSI.

Parameter	Value
dc-link voltage V_{dc} (V)	200
dc-link capacitance (μF)	680
Load resistance R (Ω)	10
Load inductance L_f (mH)	10
Sampling frequency f_{sp} (kHz)	20
Fundamental frequency f (Hz)	60
Carrier frequency f_{cr} (Hz)	4.1

Figure 6 presents the steady-state results of the output current, fast Fourier transform (FFT) of phase a current, and switching signals acquired by the per-phase MPC1, per-phase MPC2, and space vector PWM (SVPWM) approaches. Since the regular MPC method chooses the optimal switching that minimizes a cost function, no commutations are forced every sample period. In fact, one switching state can be the optimal selection for two or more sample periods. This leads to a variable switching frequency. The average switching frequency per power device, f_{sw_avg}, will be defined as the average value of the switching frequencies of the six controlled power semiconductor devices in the VSI circuit. Thus,

$$f_{sw\_avg} = \sum_{i=1}^{2} \frac{f_{S_{ai}} + f_{S_{bi}} + f_{S_{ci}}}{6} \tag{8}$$

where $f_{S_{xi}}$ is the switching frequency during a time interval of the power semiconductor device number i $(i = 1, 2)$ of phase x $(x = a, b, c)$. For a fair comparison, the carrier frequency, f_c, and the sampling frequency, f_{sp}, are set to achieve a similar average switching frequency in both the per-phase MPC and SVPWM methods.



(**a**)

Figure 6. *Cont.*

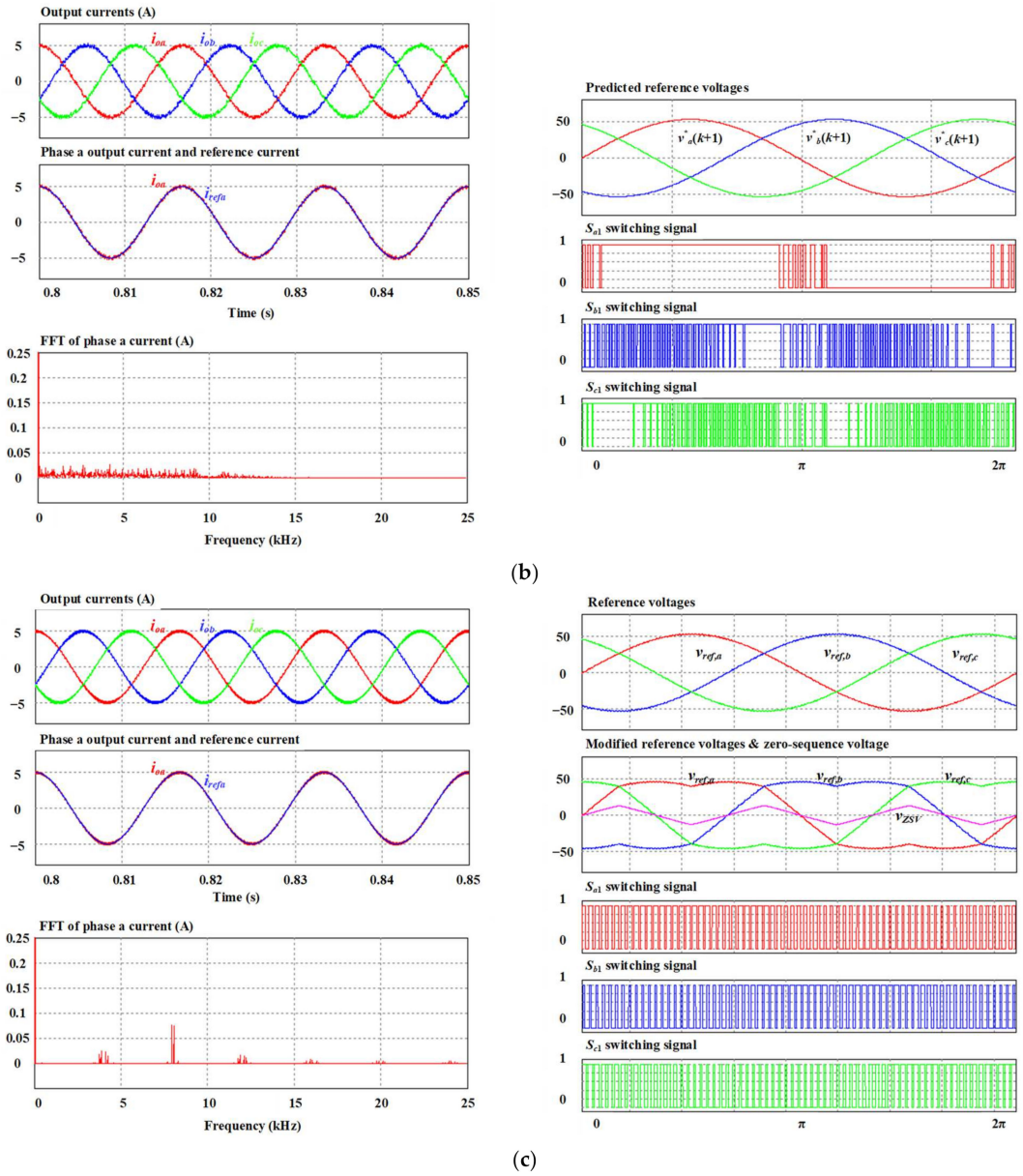


Figure 6. Simulation results of steady-state performance attained by (**a**) per-phase MPC1, (**b**) per-phase MPC2, and (**c**) SVPWM ("*" stands for reference, "**" stands for modified reference).

The output currents obtained using the three control methods have a sinusoidal waveform and an accurate phase and magnitude. The phase *a* output current, i_{oa}, acquired by the three approaches show a small difference from the reference current, i_{refa}. However, it can be noticed that the current quality and ripple content (or THD) are different among the control schemes because the per-phase MPCs are the nonconstant switching frequency control method. The FFT of the phase *a* output current has a wide range of frequencies. The FFT of the phase *a* output current is uniformly distributed across the frequency spectrum, reducing the individual harmonic component amplitudes. The FFT of the phase *a* output current obtained using the SVPWM method presents characteristic sidebands near the carrier frequency, $f_{sp} = 4.1$ kHz, as shown in Figure 6c. Hence, the peak amplitude of the spectral content of the per-phase MPC methods is evidently lower than that of the SVPWM method.

On the right-hand side of Figure 6a, the waveforms of the predicted reference voltage, the modified predicted reference voltages, the predicted *ZSV*, and the switching signal in one fundamental period obtained using the per-phase MPC1 method are presented.

As can be observed, the modified predicted reference voltage of phase a consists of two clamping periods of 120° at the positive and negative dc-link rails. This results in the power semiconductor device, S_{a1}, keeping its switching state for a two-thirds fundamental cycle. Meanwhile, the generated predicted ZSV, which is injected into the sinusoidal reference voltages, does not generate the clamping periods in phases b and c. Regarding these waveforms obtained through the per-phase MPC2 scheme in Figure 6b, the power semiconductor device S_{a1}'s switching state contains a clamping period, which corresponds to the cases where the phase a reference voltage is determined as $v^*_{max}(k)$ or $v^*_{min}(k)$. Meanwhile, the SVPWM has a continuous switching pattern in both three-phase legs, as shown in Figure 6c.

In terms of dynamic performance, Figure 7 illustrates the transient-state output current waveforms acquired by the per-phase MPC1, per-phase MPC2, and SVPWM approaches. The magnitude of the reference current is increased from 3A to 5A to induce a transient state. This allows for an assessment of the dynamic behavior of the output current. In Figure 7, both the per-phase MPC schemes have excellent dynamic performance. The waveforms in Figure 7a,b show that the system is highly stable since the current quickly follows the new reference value without any overshoot. Figure 7c shows the output currents in response to the current step using SVPWM. The plot of the phase a output current and its reference indicate a lower dynamic performance compared to the two per-phase MPC approaches. To increase the dynamic performance of the PWM method, decoupling terms can be added to the PI controllers, or the PI gains can be increased. It should be noted that the increase in PI gains might lead to uncontrolled oscillation about the set point and instability in the system.

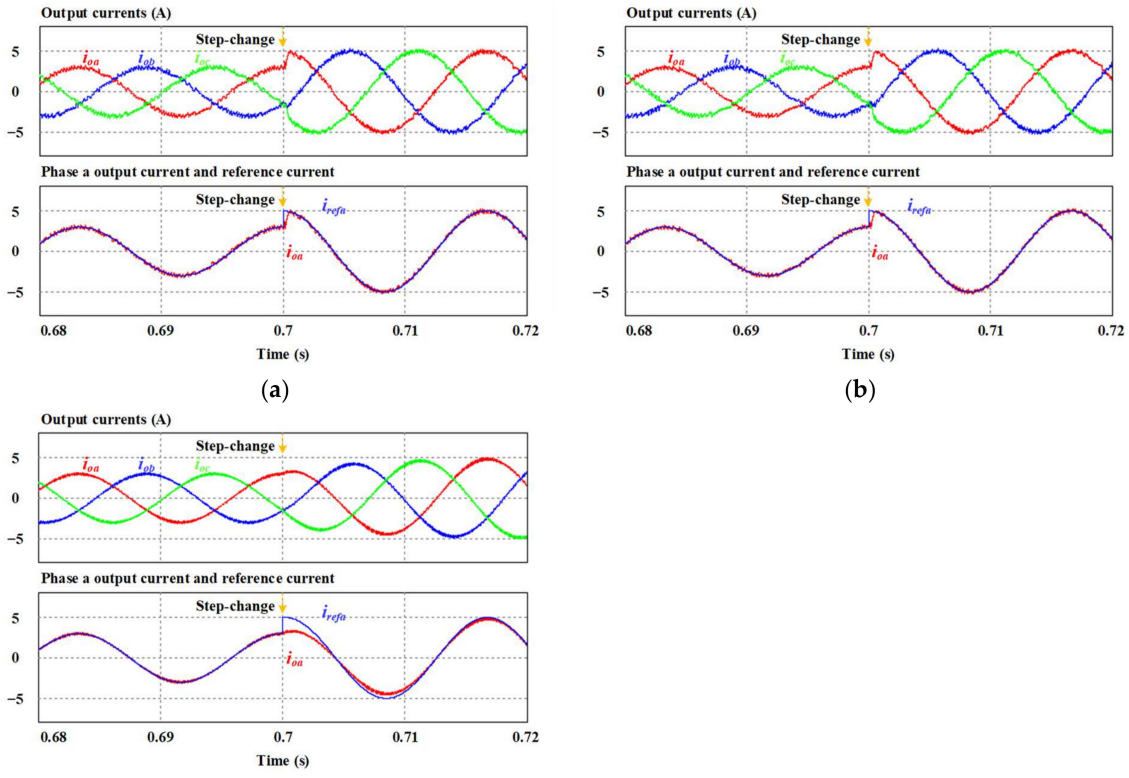


Figure 7. Simulation results of transient-state performance attained by (**a**) per-phase MPC1, (**b**) per-phase MPC2, and (**c**) SVPWM.

Parameter uncertainty can degrade the control system's performance and even affect the system's stability. In the MPC technique, the prediction model critically relies on having accurate load parameters. Figure 8 shows the behavior of the output currents and

switching state under a load inductance mismatch obtained with only the per-phase MPC1 and per-phase MPC2 methods. The same condition is applied to the load inductance as in the parameter mismatch of the dc-link voltage. In the first part of the waveforms, the equivalent inductance is half of the actual inductance; the middle shows that the equivalent inductance is correct; and the last shows that the equivalent inductance is 1.5 times higher than the actual one. The same condition is tested for the load resistance in Figure 9. It can be seen from Figure 9a,b that the output currents obtained from the two approaches are properly controlled with a sinusoidal form and an accurate magnitude. However, the current ripples obtained by per-phase MPC1 are slightly higher than those of per-phase MPC2. Additionally, the switching frequency decrease capability under per-phase MPC1 is decreased when the equivalent load inductance is higher than the actual load inductance. In terms of the parameter mismatch of the load resistance, both per-phase MPC1 and per-phase MPC2 properly control the output currents with negligible ripples. The switching frequency decrease capability is not degraded. Therefore, it can be concluded that per-phase MPC1 is affected by the parameter mismatch of the load more than per-phase MPC2.

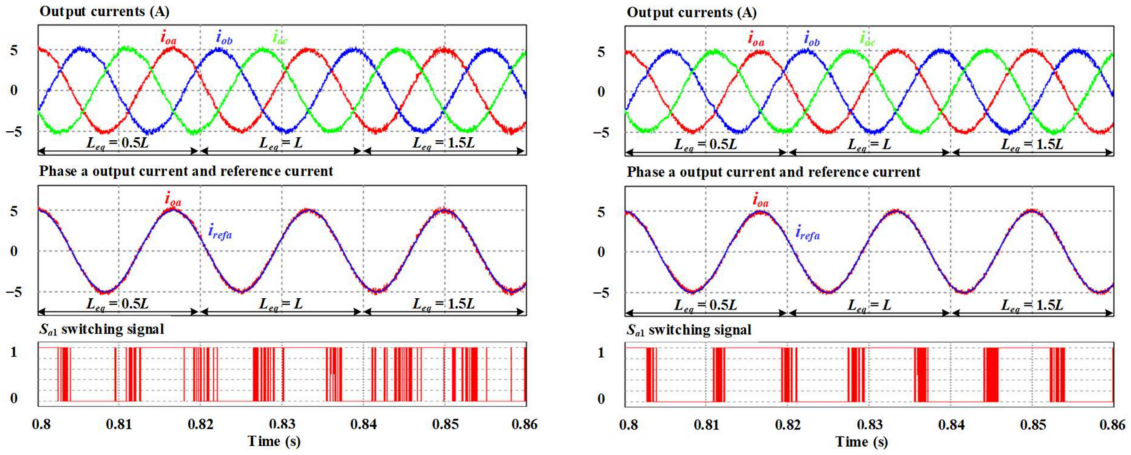


Figure 8. Waveform of output currents under parameter mismatch in the load inductance obtained through (**a**) per-phase MPC1 and (**b**) per-phase MPC2.

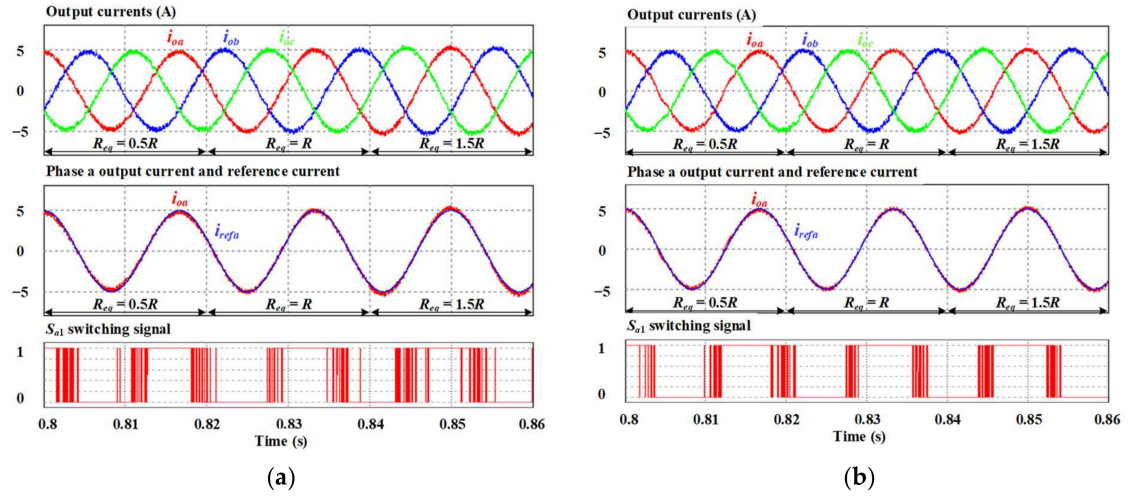


Figure 9. Waveform of output currents under parameter mismatch in the load resistance obtained through (**a**) per-phase MPC1 and (**b**) per-phase MPC2.

The values calculated from the simulation results are shown to comprehensively evaluate the output performance acquired using the per-phase MPC1, per-phase MPC2,

and SVPWM methods. Figure 10a–d present a performance comparison among the per-phase MPC1, per-phase MPC2, and SVPWM methods, including the THD value of the output current, switching frequency, and loss. The power loss of the semiconductor devices is calculated using the Thermal Module in the PSIM program with the actual device's parameter from the IGBT datasheet. Figure 10a presents an output phase current THD comparison between the three approaches. The THD value of the phase *a* current obtained through per-phase MPC2 is smaller than that obtained using the per-phase MPC1 method. However, due to the fact that the output current THD in phase *b* and phase *c* obtained through per-phase MPC2 is significantly high, the average THD obtained through per-phase MPC2 will still be similar to that obtained using the per-phase MPC1 method. Meanwhile, the output current THD in both three-phase legs obtained through SVPWM is the same and smaller than that obtained using the two per-phase MPC approaches. This is explained by the use of a PWM modulator, which is capable of shifting the main switching harmonics into a high-frequency region (around multiples of the switching frequency), and this leads to lower current harmonics. As shown in Figure 10b, the three control schemes have a similar average switching frequency at about 4.1 kHz. Per-phase MPC2 lowers the switching frequency in phase *a* most, with a 22% lower frequency than for per-phase MPC1. However, the switching frequency in the remaining phases is significantly high. Meanwhile, the SVPWM has a constant switching frequency in both the three-phase legs.

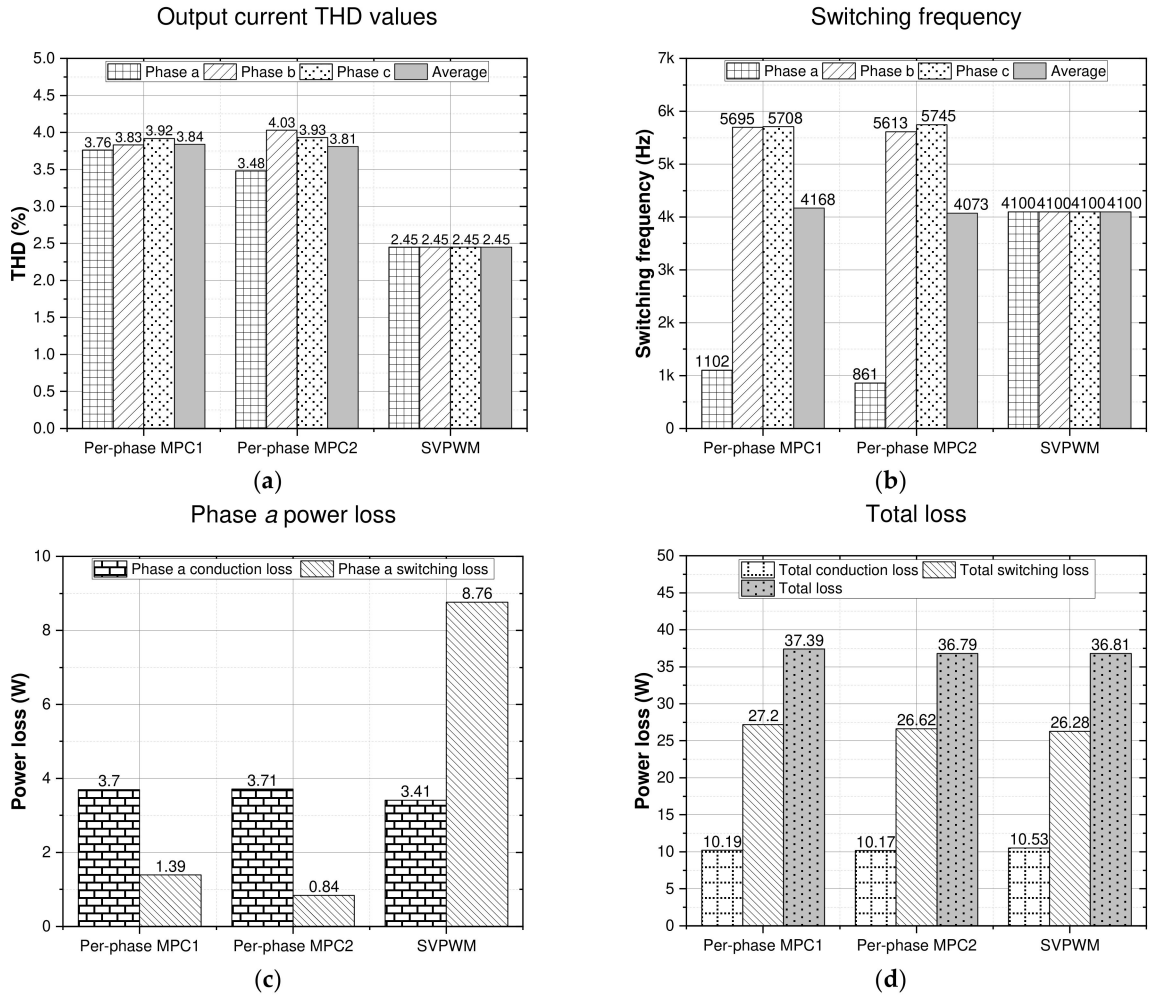


Figure 10. Output performance comparison among per-phase MPC1, per-phase MPC2, and SVPWM. (**a**) Phase current THD; (**b**) switching frequency; (**c**) phase *a* power loss; (**d**) VSI power loss.

Regarding the power loss performance comparison, thanks to the significant reduction in the switching frequency in phase *a*, the corresponding switching losses of phase *a*

are relatively low. As shown in Figure 10c, the phase a switching loss obtained through per-phase MPC2 is the lowest among the three control schemes, as it is about 33% lower than that of per-phase MPC1 and 75% lower than that of SVPWM. Although the phase a switching loss is decreased in the per-phase MPC methods, the switching losses in the two remaining phase legs increase. This leads to the total switching loss and total loss obtained by the two per-phase MPC methods and the SVPWM schemes being similar, as shown in Figure 10d. The total loss attained through per-phase MPC2 is marginally lower than for the per-phase MPC1 and SVPWM approaches.

In order to further clarify the performance of the per-phase MPC approaches, a comparison among the two per-phase MPC methods is implemented under different circumstances, including a variety of sampling frequencies, output powers, and load angles. Figure 11 shows the phase and average output current THD under different sampling frequency conditions obtained by the two per-phase MPC approaches. The THD values of the output currents obtained by the two per-phase MPC techniques decrease as the sampling frequency increases. The average output current THD of per-phase MPC1 is slightly lower than that of per-phase MPC2.

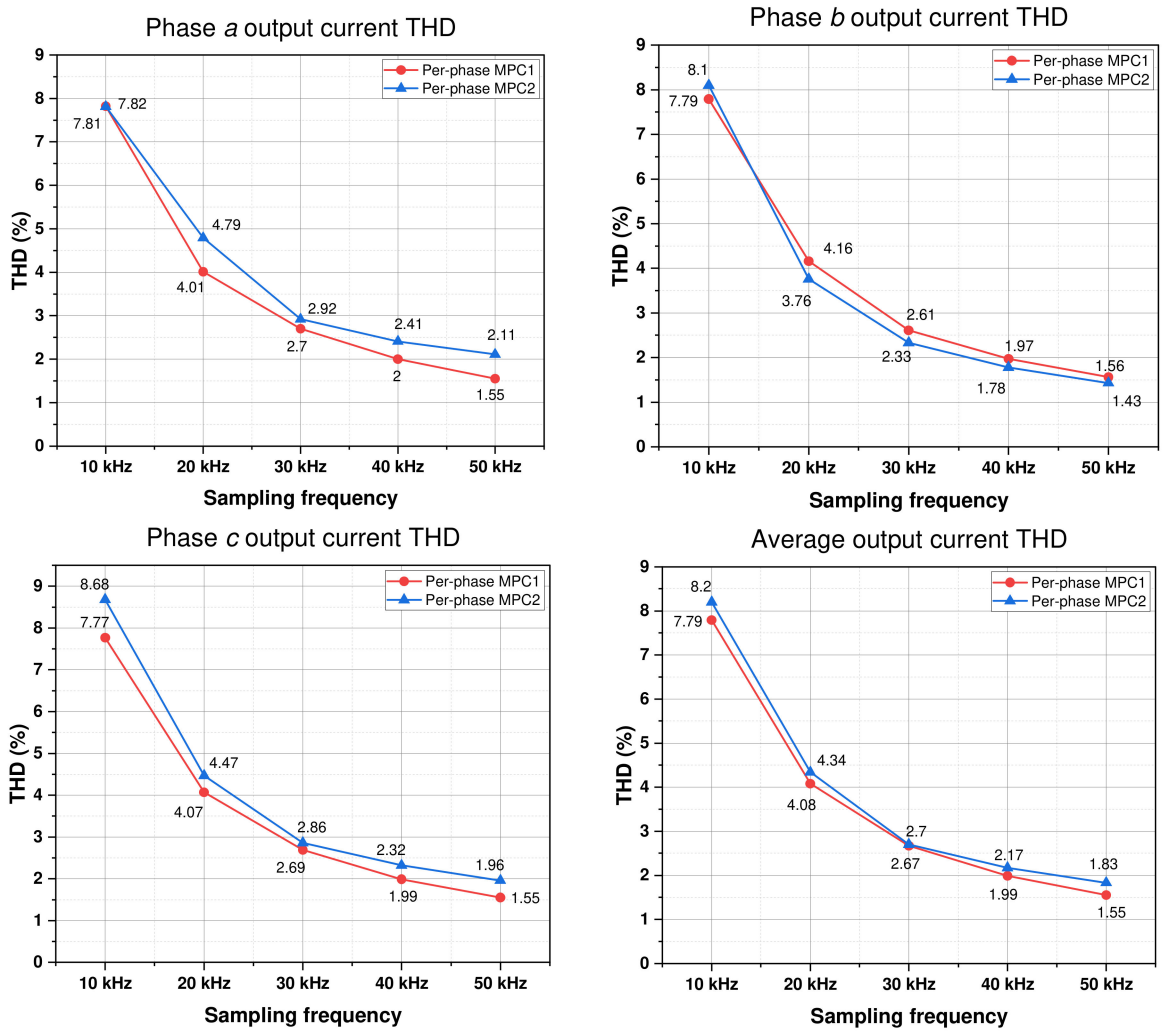


Figure 11. Phase output current THD comparison under variation in sampling frequency (V_{dc} = 200 V, $\theta = 20°$, and $I^* = 5$ A).

In Figure 12, the average frequency of per-phase MPC1 is slightly higher than that of per-phase MPC2 by about 7%. Under different sampling frequencies, per-phase MPC2

decreases the switching frequency of phase *a* the most. The switching frequency of phase *a* obtained through per-phase MPC2 is lower than that of per-phase MPC1 by about 35%.

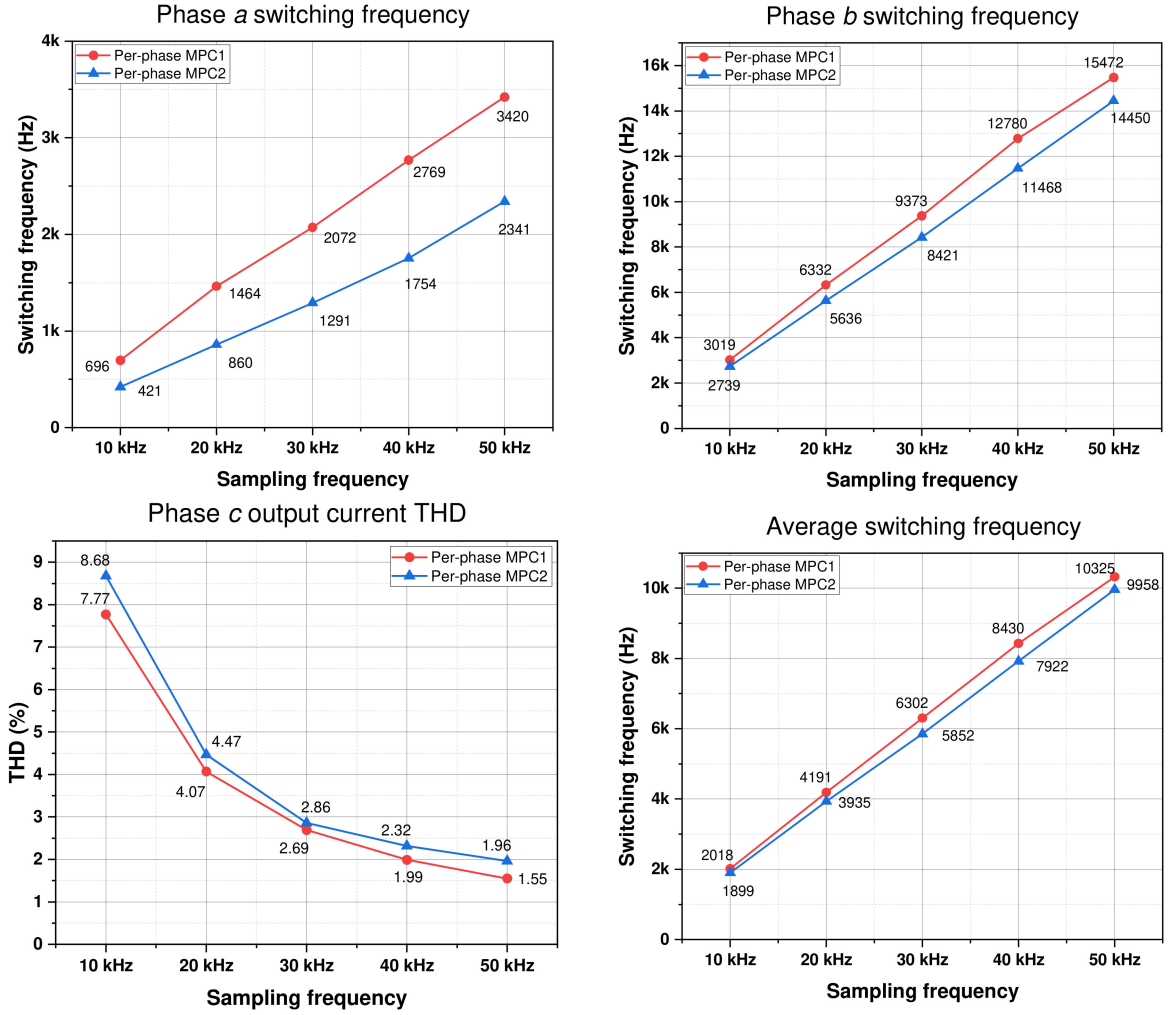
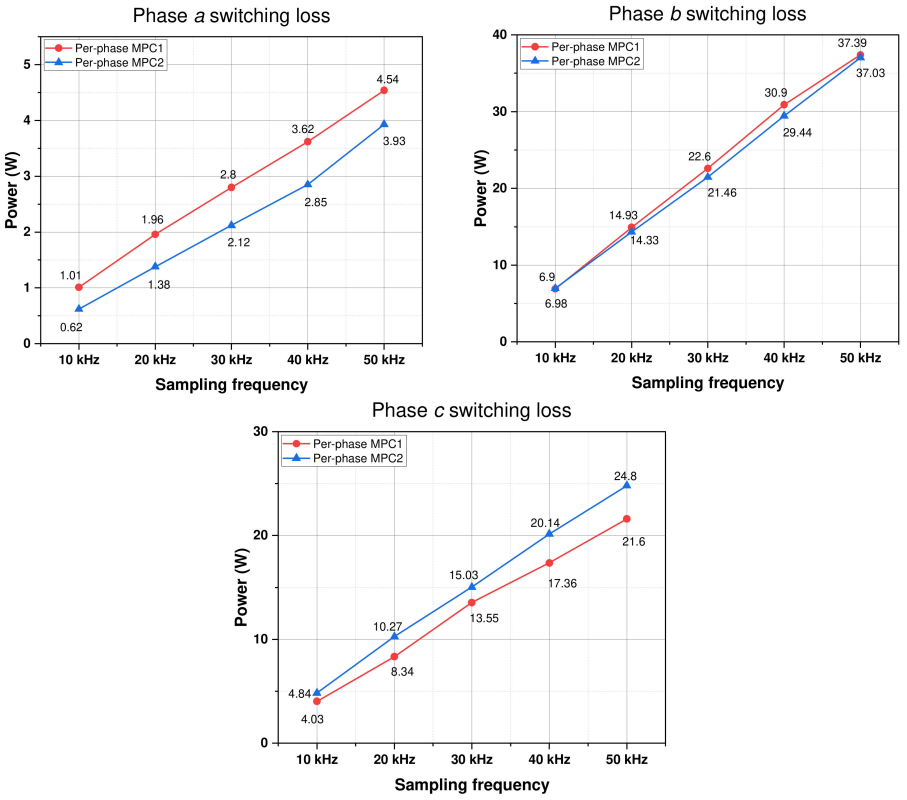
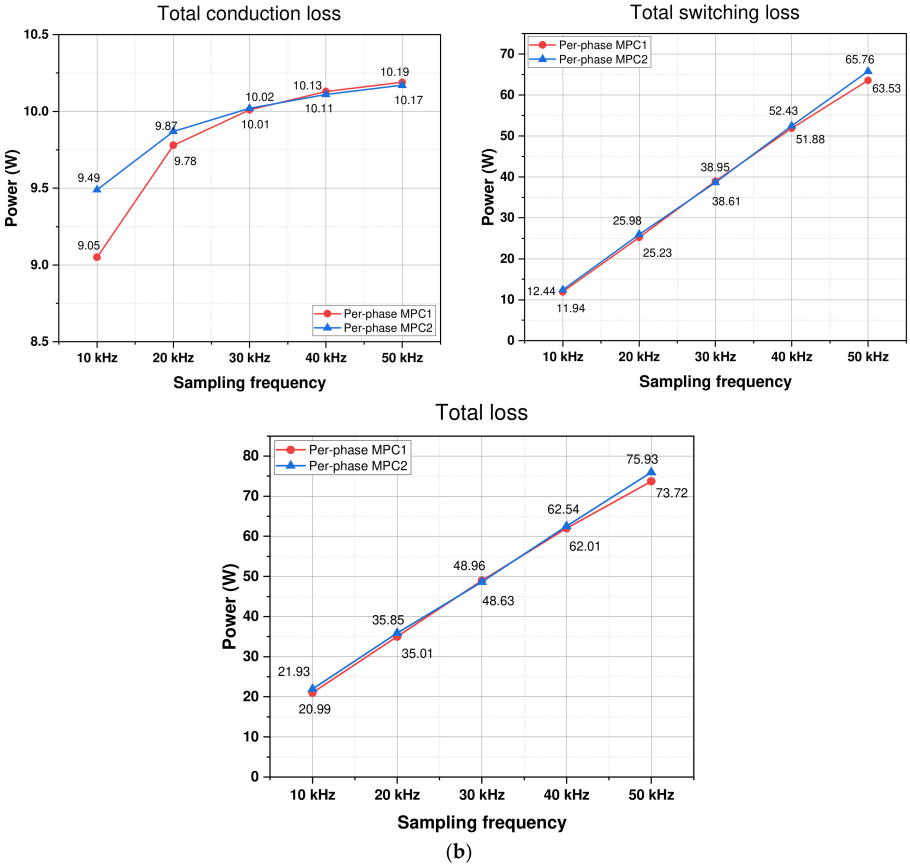


Figure 12. Switching frequency comparison under variation in sampling frequency (V_{dc} = 200 V, $\theta = 20°$, and $I^* = 5$ A).

Regarding the conduction loss acquired through the two MPC approaches, the difference in the conduction loss between the two techniques under different sampling frequency conditions is small. The phase *a* switching loss acquired through per-phase MPC2 is the lowest, as shown in Figure 13a. This switching loss is lower than that of per-phase MPC1 by about 20–30%. However, because the switching losses in the remaining phase legs increase, the two per-phase MPC methods have a similar total loss.



(**a**)



(**b**)

Figure 13. (**a**) Switching loss and (**b**) total loss comparison results under variation in sampling frequency ($V_{dc} = 200$ V, $\theta = 20°$, and $I^* = 5$ A).

Figure 14 shows the phase and average output current THD under different output power conditions obtained through the two per-phase approaches. The THD value of the output current obtained through the two schemes decreases when the output power increases. The per-phase MPC2 method has the highest output current THD when the output power is large. The average output current THD of per-phase MPC1 is slightly lower than that of per-phase MPC2.

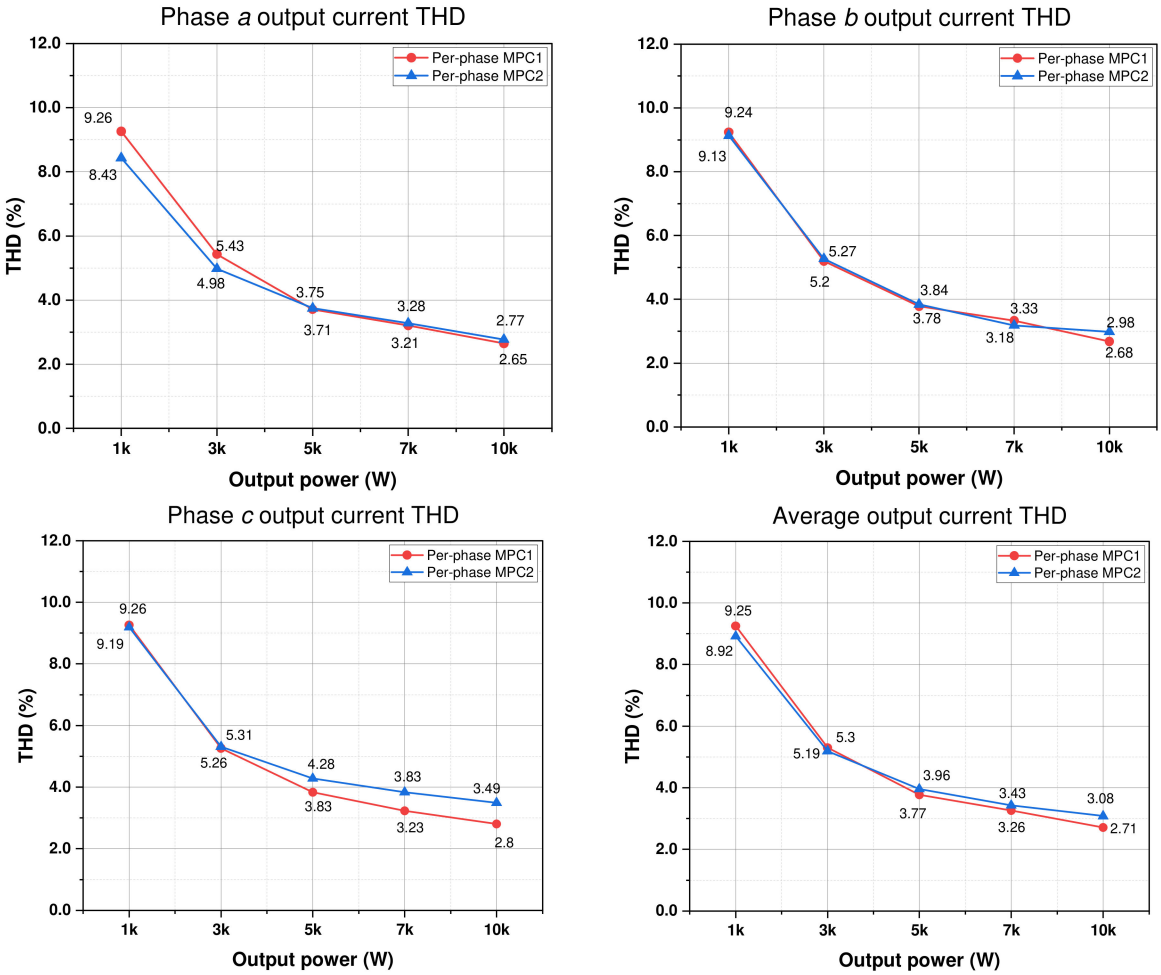


Figure 14. Phase output current THD comparison under variation in output power (V_{dc} = 720 V, $\theta = 20°$, and f_{sp} = 20 kHz).

In Figure 15, the average switching frequencies of the two per-phase control schemes are similar, with a small difference when the output power varies. The switching frequency of phase *a* is reduced the most by per-phase MPC2. The switching frequency obtained through per-phase MPC2 is lower than that of per-phase MPC1 by about 30%.

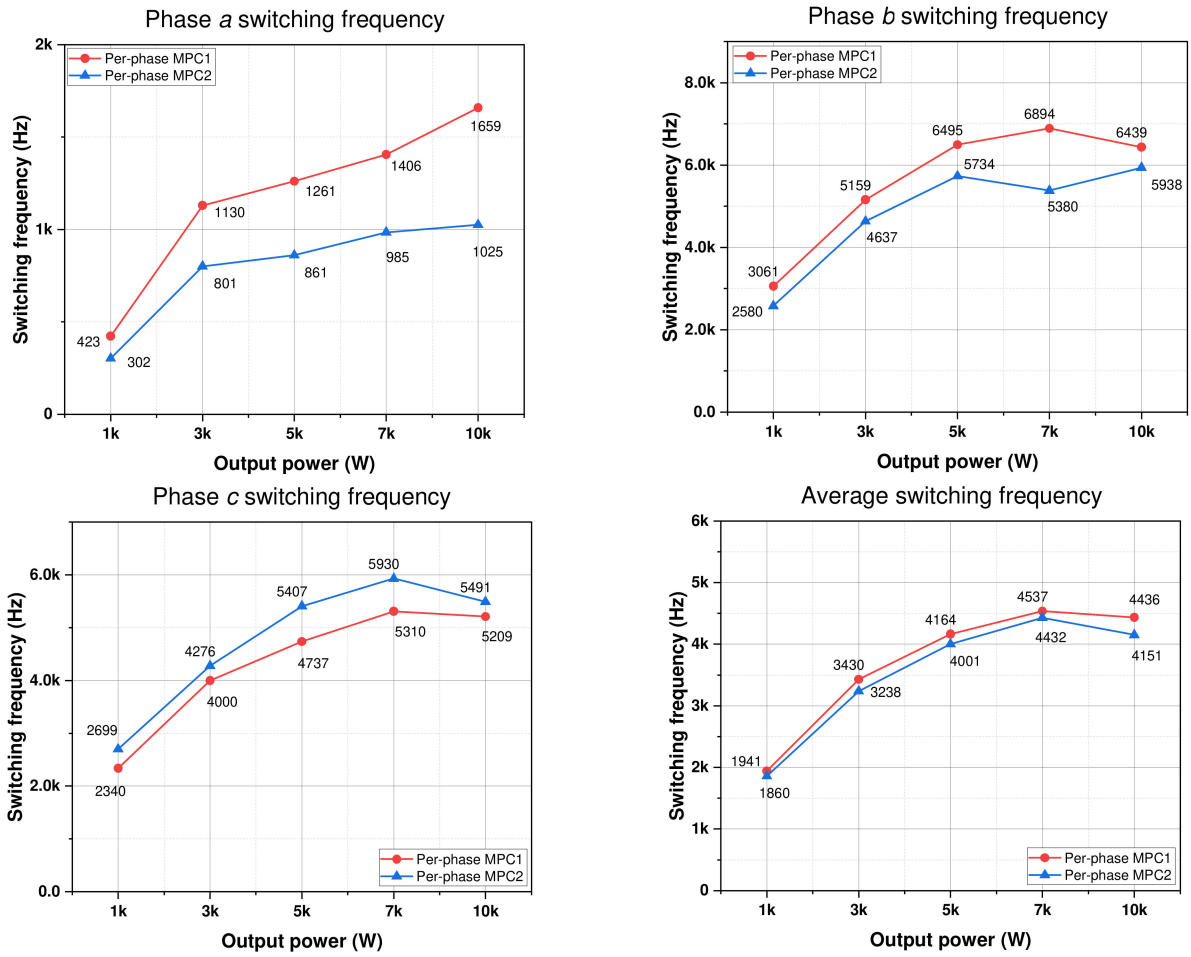
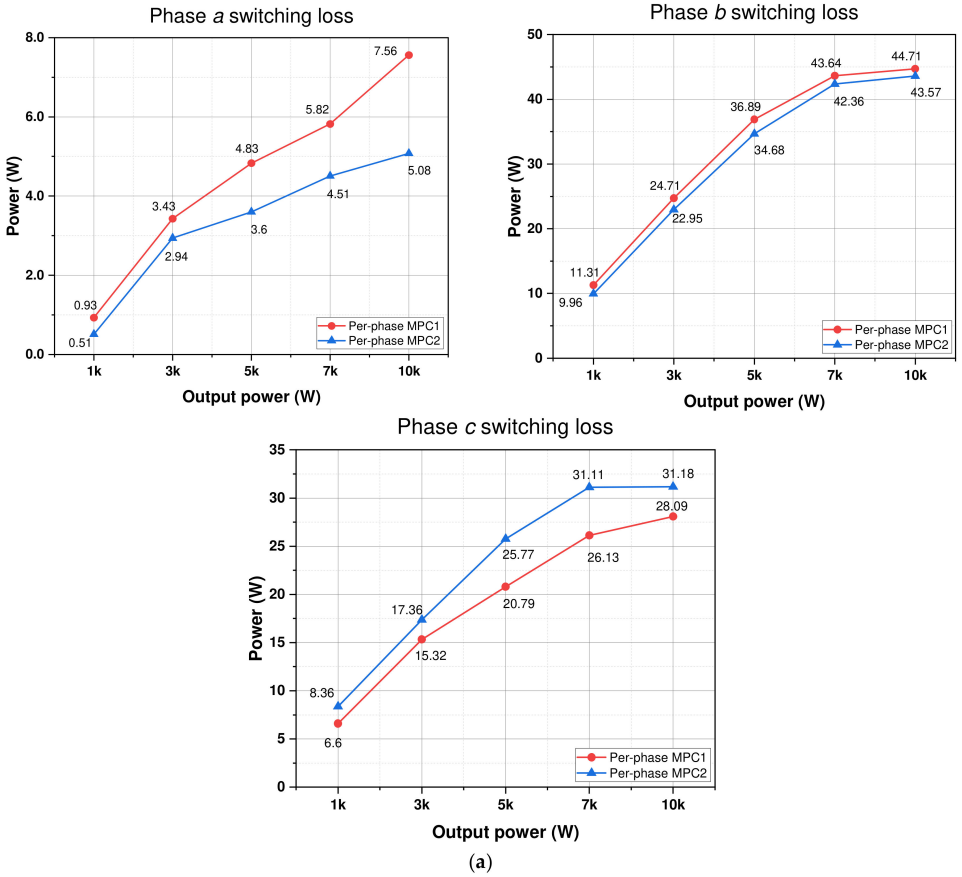
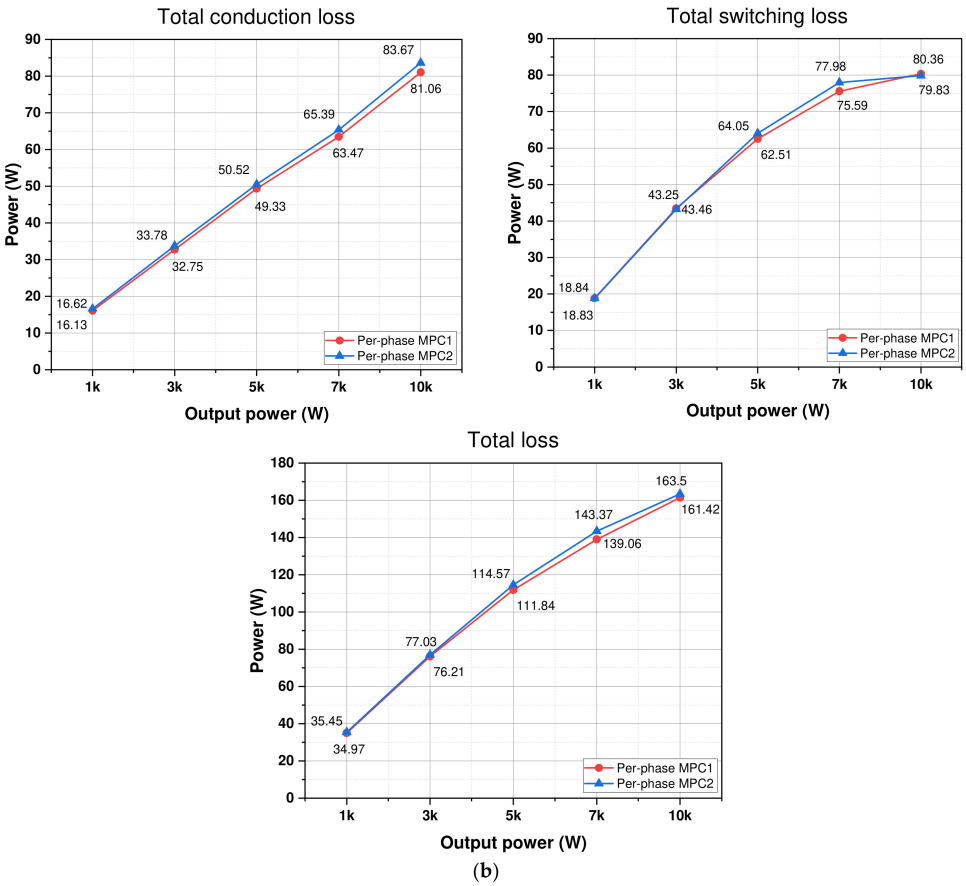


Figure 15. Phase switching frequency comparison under variation in output power (V_{dc} = 720 V, $\theta = 20°$, and f_{sp} = 20 kHz).

Regarding the conduction loss acquired through the two approaches, the difference in the conduction loss between the two techniques under various output powers is small. The switching loss of phase *a* acquired with per-phase MPC2 is the lowest. This switching loss is lower than that of per-phase MPC1 by about 20–35%, as shown in Figure 16a. However, because the switching losses in remaining phase legs increase, the two per-phase MPC methods have similar total losses.



(**a**)



(**b**)

Figure 16. (**a**) Switching loss and (**b**) total loss comparison under variation in output power ($V_{dc} = 720$ V, $\theta = 20°$, and $f_{sp} = 20$ kHz).

Figure 17 shows the phase and average output current THD under different load conditions obtained using the two per-phase approaches. The THD value of the output currents acquired with the two per-phase MPC approaches decreases when the phase load angle rises. Under different load conditions, the average THD of the output current attained with per-phase MPC1 and per-phase MPC2 are similar.

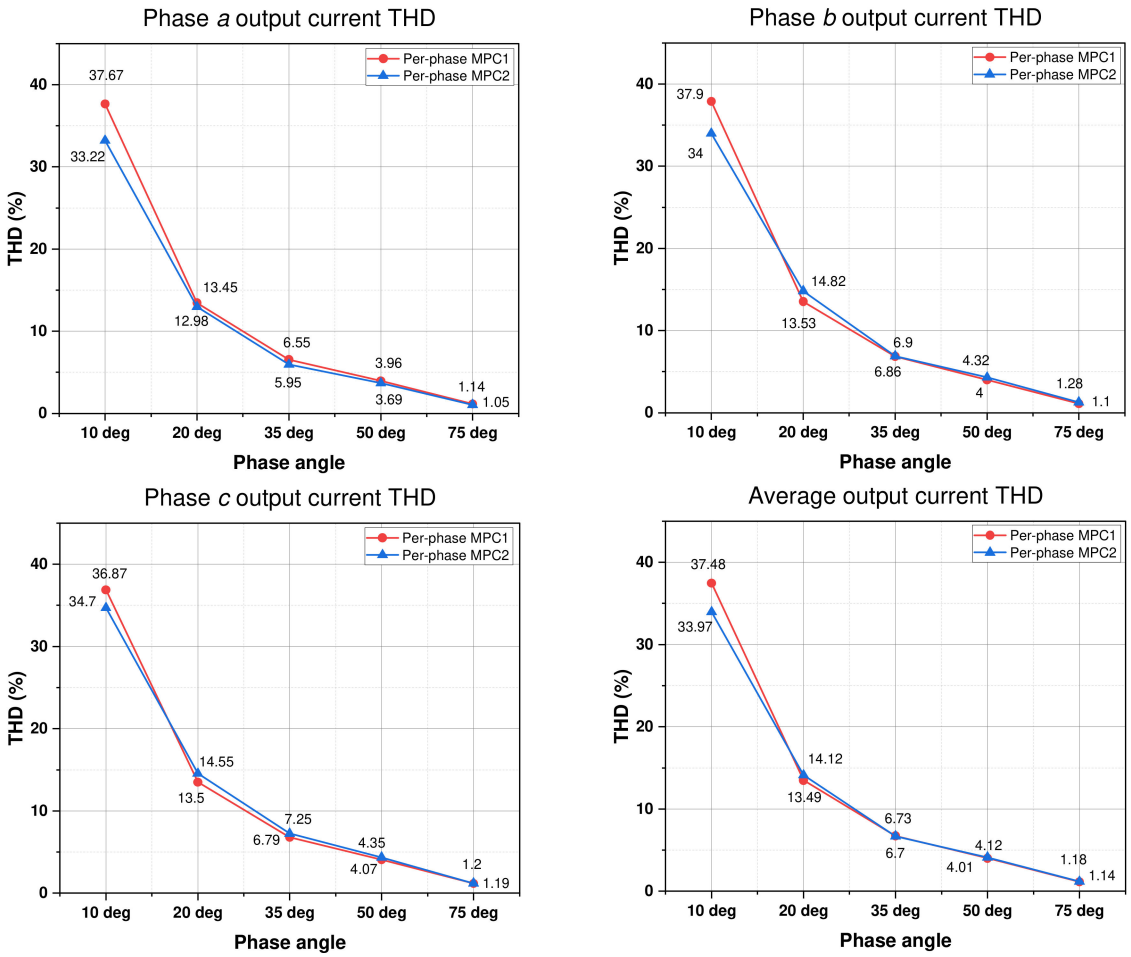


Figure 17. Phase output current THD comparison under variation in load angle (V_{dc} = 720 V, P_{out} = 1 kW, and f_{sp} = 20 kHz).

In Figure 18, the difference in the average switching frequency between the two control schemes is negligible under different load conditions. Under different load conditions, the switching frequency of phase *a* is decreased the most by per-phase MPC2. The switching frequency obtained with the per-phase MPC2 method is lower than that of per-phase MPC1 by about 30%.

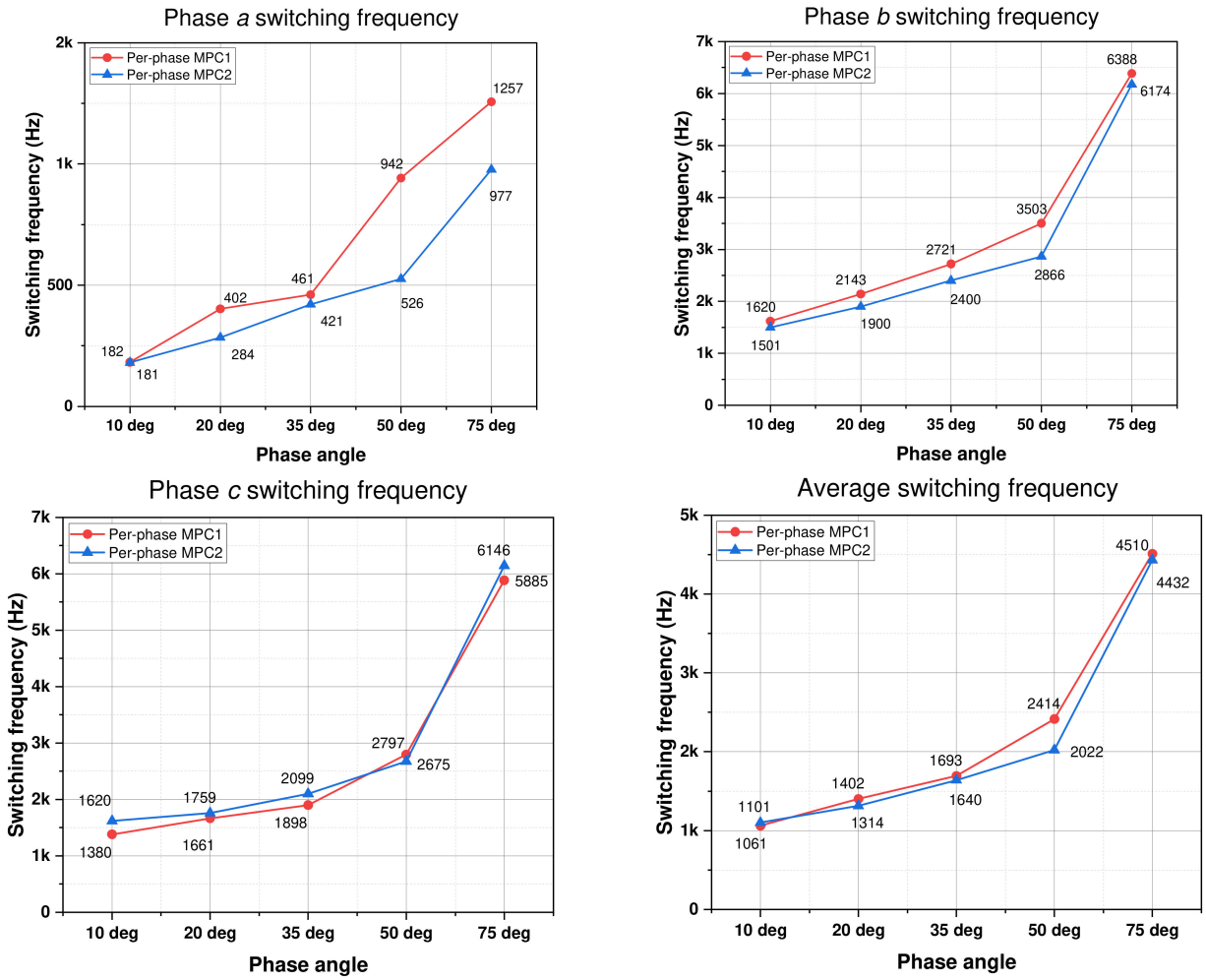


Figure 18. Phase switching frequency comparison under variation in load angle (V_{dc} = 720 V, P_{out} = 1 kW, and f_{sp} = 20 kHz).

A comparison of the power loss between the per-phase techniques under a variety of load conditions is depicted in Figure 19. Regarding the conduction loss acquired through the two per-phase MPC approaches, the difference in the conduction loss between the two techniques under different load conditions is small. The switching loss of phase *a* acquired with per-phase MPC2 is the lowest. This is lower than the switching loss of per-phase MPC1 by about 20–30%. However, due to the switching losses in the remaining phase legs increasing, the two per-phase MPC methods have similar total losses.

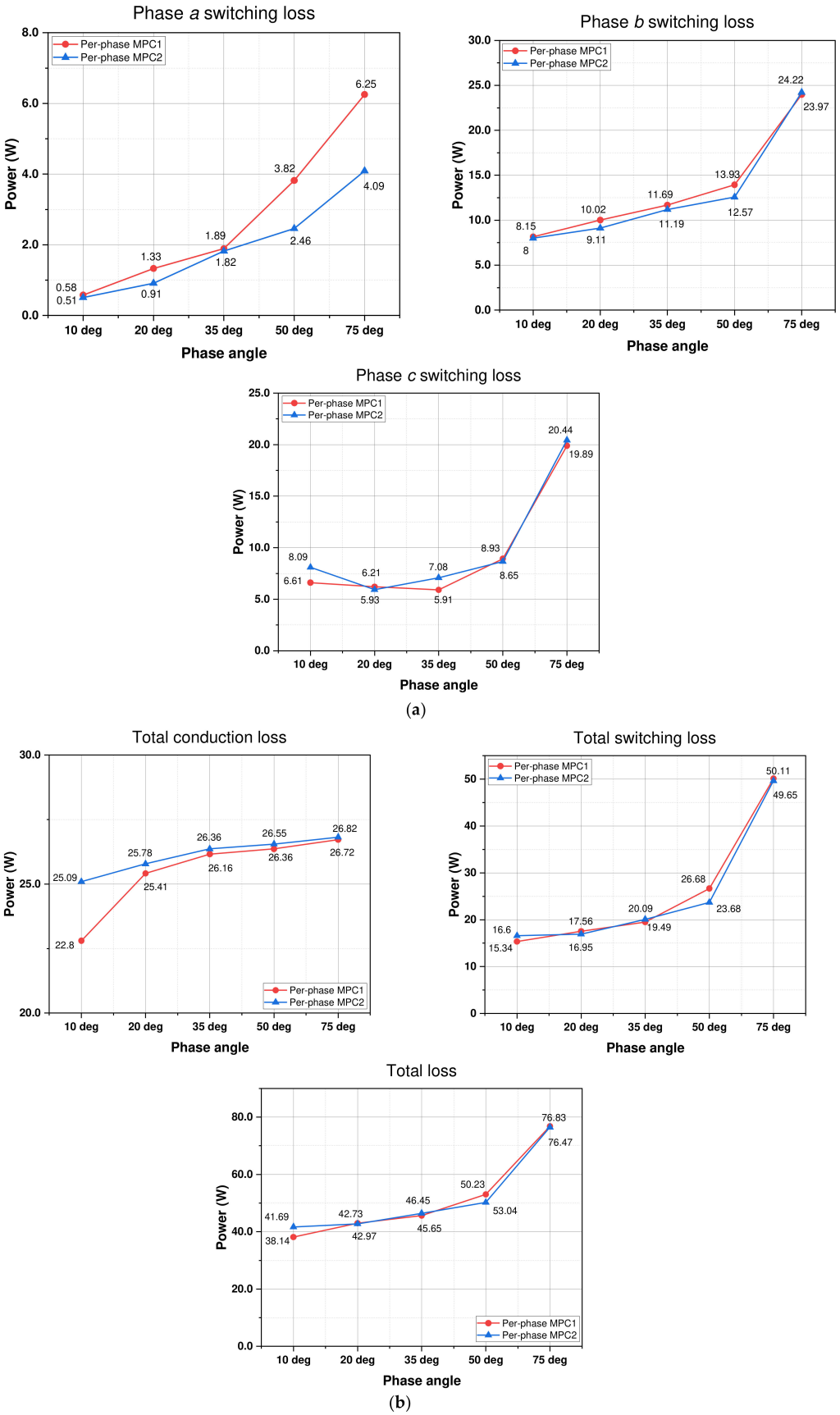


Figure 19. (**a**) Switching loss and (**b**) total loss comparison under variation in load angle (V_{dc} = 720 V, P_{out} = 1 kW, and f_{sp} = 20 kHz).

Figure 20 displays the performance of the per-phase MPC1 and per-phase MPC2 methods when there exists a parameter mismatch in the load inductance. This performance evaluation includes several aspects, such as the average THD value, the switching frequency and switching loss in phase *a*, and the %error of the output current. In Figure 20, the vertical axis in the line charts illustrates the variance between the model parameter and the real value of load inductance. As observed in Figure 20a, the average output current THD obtained using the per-phase MPC1 and MPC2 methods varies slightly with a 25% load inductance variance. When the load inductance variance is 50%, the average THD of the output current increases. In particular, the average THD attained using the per-phase MPC1 and MPC2 methods significantly rises as the real value of the load inductance is 75% larger than the value of the model parameter. Figure 20b,c illustrate that the capability of the per-phase MPC methods to reduce the switching frequency diminishes when the model parameter of the inductance exceeds its actual value. When the model parameter inductance is 75% smaller than the real inductance, there is a notable increase in the %error of the output current. This increase is substantial, reaching about 3.3 times for per-phase MPC1 and about 2.6 times for per-phase MPC2 compared to the normal condition. In comparison between the per-phase MPC1 and per-phase MPC2 methods, the MPC1 method is affected by a load inductance mismatch more than the MPC2 method.

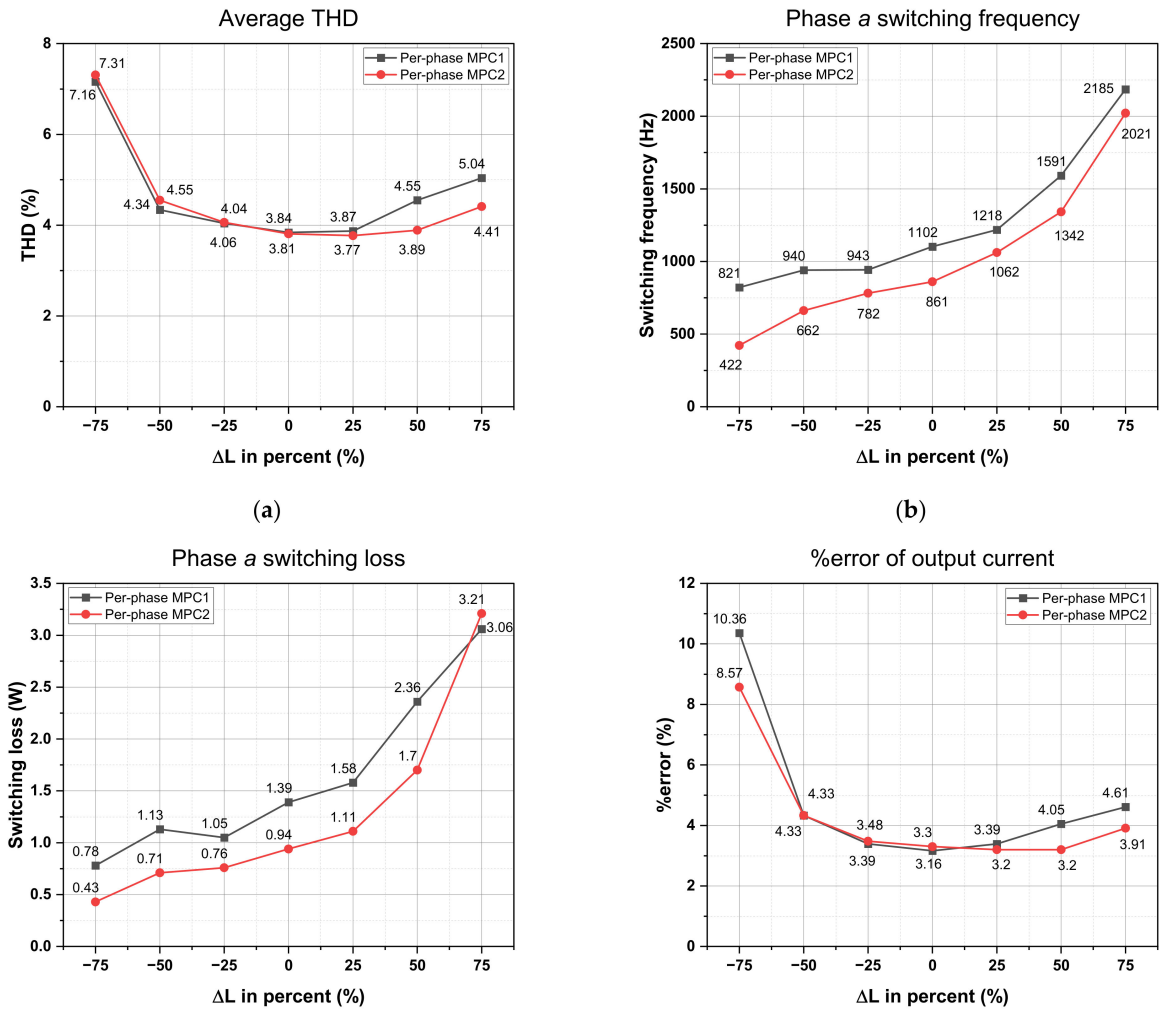


Figure 20. Performance comparison between per-phase MPC1 and per-phase MPC2 methods under load inductance parameter mismatch: (**a**) average THD of output current, (**b**) phase *a* switching frequency, (**c**) phase *a* switching loss, and (**d**) %error of load currents.

Similar to the parameter mismatch of the load inductance, Figure 21 displays the performance of the per-phase MPC1 and per-phase MPC2 methods when there is a parameter mismatch in the load resistance with similar aspects. Figure 21a illustrates that the average output current THD obtained using the two per-phase methods slightly varies with a 50% smaller and 75% larger load resistance variance. When the model parameter resistance is 75% smaller than the real one, the average THD of the output current obtained with per-phase MPC2 increases significantly. Regarding the methods' capability to reduce the switching frequency, per-phase MPC2 performs well even when the variation between the model parameter value of the load resistance and the real value is 75%. Meanwhile, the capability to reduce the switching frequency of per-phase MPC2 is lowered when the variation between the model parameter value of the load resistance and the real value is 55%. Especially when the model parameter resistance is 75% smaller than the real resistance, the phase *a* switching frequency obtained through per-phase MPC1 significantly increases. Figure 21c depicts a phase *a* switching loss comparison between the two per-phase MPC approaches. The phase *a* switching loss obtained with the two per-phase MPC methods significantly increases when the model parameter resistance is 50% and 75% smaller than the actual resistance. As observed in Figure 21d, per-phase MPC1 only can maintain the output current error with a 25% load resistance variance. When the difference between the model parameter resistance and the actual one is higher than 50%, the %error of the output current acquired with per-phase MPC1 rises notably. Meanwhile, per-phase MPC2 can maintain the output current error even with a 50% load resistance variance. In comparison between the per-phase MPC and per-phase MPC2 methods, the MPC1 method is affected by the load resistance mismatch more than the MPC2 method.

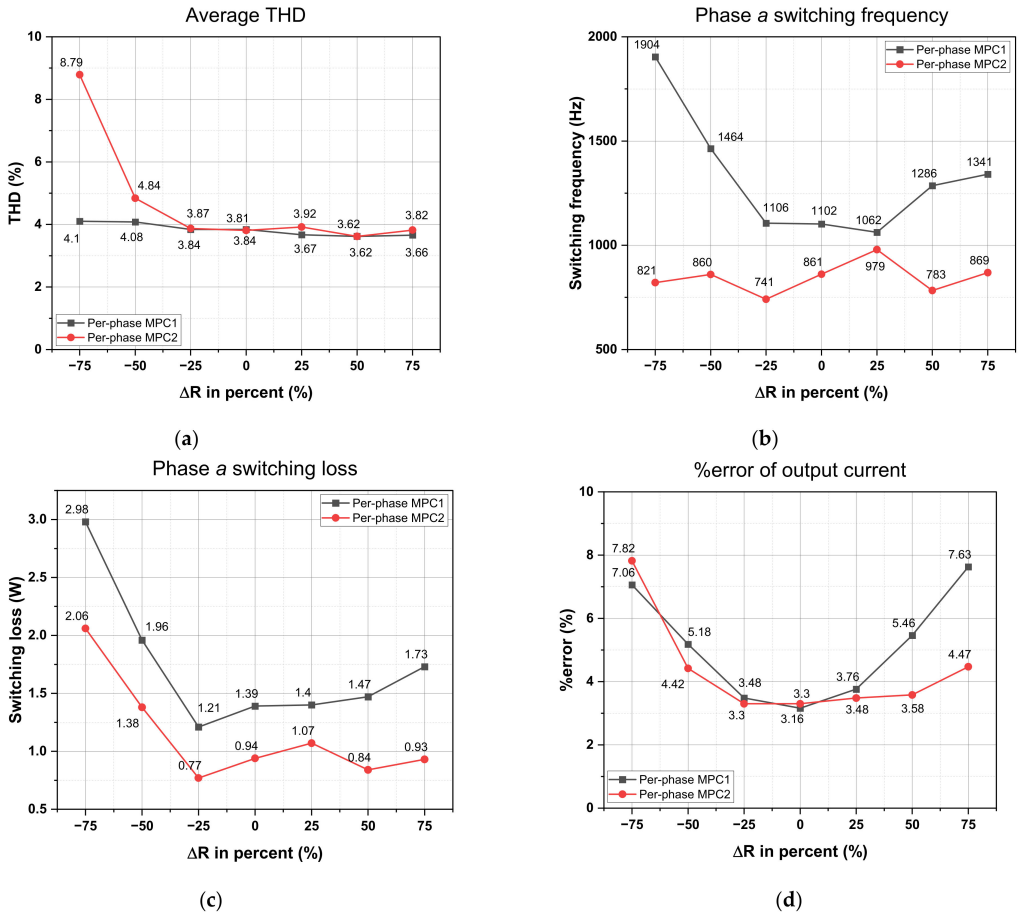


Figure 21. Performance comparison between per-phase MPC1 and per-phase MPC2 methods under load resistance parameter mismatch: (**a**) average THD of output current, (**b**) phase *a* switching frequency, (**c**) phase *a* switching loss, and (**d**) %error of load currents.

To comprehensively compare the performance of the per-phase MPC1 and per-phase MPC2 methods, two control schemes are conducted in the experiment. The per-phase MPC schemes are validated using a laboratory-scaled two-level three-phase VSI system. The structure of the two-level three-phase VSI system is presented in Figure 22. Meanwhile, the system parameters are similar to the simulation, as listed in Table 1. A Texas Instruments digital signal processor (DSP) TMS320F28335 is employed for implementing both of the per-phase MPC methods.

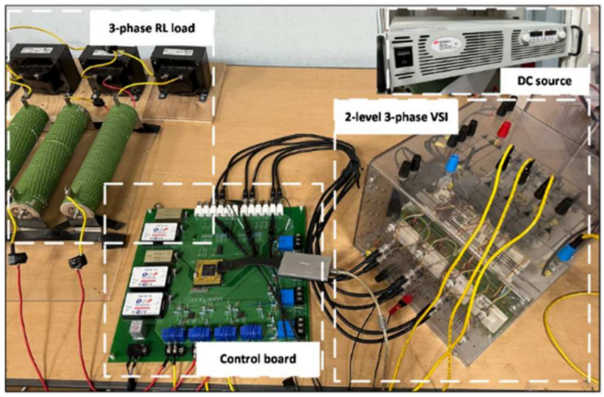


Figure 22. Overall experiment setup of 2-level 3-phase VSI.

Figure 23 presents the experiment results of the output current waveforms, the FFT of phase *a* current, and the switching signals at steady-state acquired by the per-phase MPC1 and per-phase MPC2 schemes. The output currents acquired with the two control methods have a sinusoidal form and an accurate phase and magnitude. In the per-phase MPC schemes, the FFT of the phase *a* output current has a wide range of frequencies. The FFT of the phase *a* output current is uniformly distributed across the frequency spectrum, reducing the individual harmonic component amplitudes.

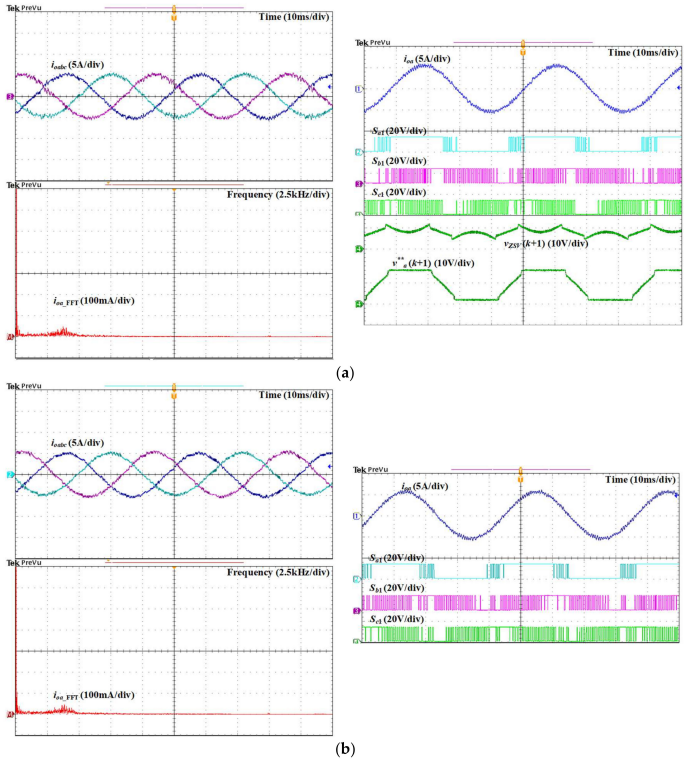


Figure 23. Experimental results of steady-state performance obtained with (**a**) per-phase MPC1 and (**b**) Per-phase MPC2 ("**" stands for modified reference).

On the right-hand side of Figure 23a, the waveforms of the phase a modified predicted reference voltages, predicted ZSV, and switching signal in one fundamental period obtained using the per-phase MPC1 method are presented. The modified predicted reference voltage of phase a consists of two clamping periods of 120° at positive and negative dc-link rails. This results in the power semiconductor device, S_{a1}, keeping its switching state for two-thirds of a fundamental cycle. In terms of per-phase MPC2, in Figure 23b, the power semiconductor device S_{a1}'s switching state contains a clamping period, which relates to the cases where the phase a reference voltage is determined as $v^*_{max}(k)$ or $v^*_{min}(k)$, as in experimental results shown in Figure 23b.

In terms of dynamic performance, Figure 24 illustrates the transient-state output current waveforms acquired by the per-phase MPC1 and per-phase MPC2 approaches. The magnitude of the reference current is increased from 3 A to 5 A to induce a transient state. This allows for an assessment of the dynamic behavior of the output current. In Figure 24, both the two per-phase MPC schemes have excellent dynamic performance. The waveforms of Figure 24a,b show that the system is highly stable since the current quickly follows the new reference value without any overshoot.

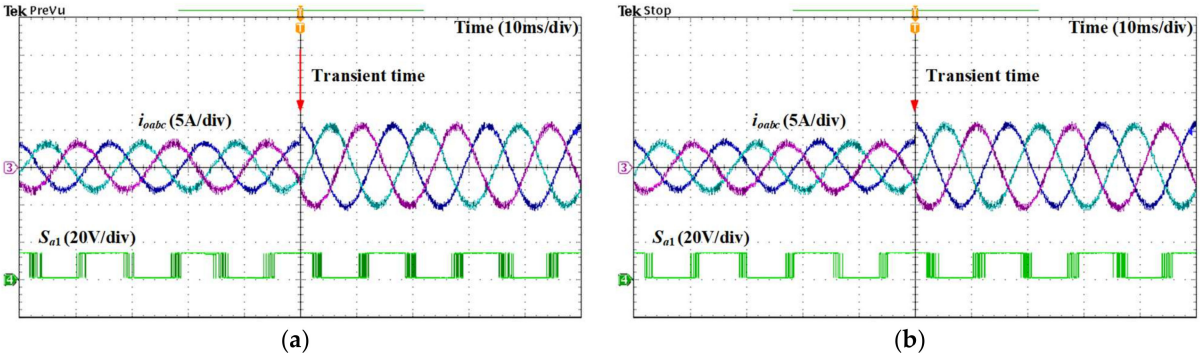


Figure 24. Experimental results of transient-state performance obtained with (**a**) per-phase MPC1 and (**b**) per-phase MPC2.

In the experiment implementation, the two per-phase techniques take different calculation times to execute the algorithm. The execution time for each of the algorithms was computed by measuring the elapsed time in the experimental setup, and the results are shown in Figure 25. It can be seen that per-phase MPC1 has the highest calculation time at 17.5 µs. This is because of the calculation time for all seven switching states and the zero-voltage vector selection of the considered per-phase MPC1 technique. Meanwhile, during the clamping period, the per-phase MPC2 method only needs to evaluate four switching states. Thus, its calculation time is lower than that of per-phase MPC1.

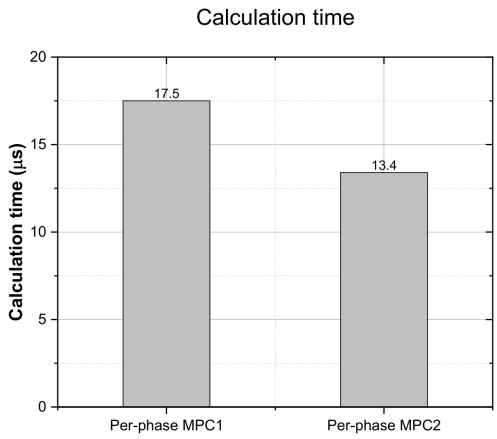


Figure 25. DSP calculation time comparison.

In addition to static load conditions, the simulation results obtained through two per-phase MPC for a VSI-fed three-phase induction motor are depicted in Figure 26. Here, phase *a* was still assumed to be the leg that has aged the most. In the simulation, the speed range control was evaluated while varying the rotor speed from −1200 r/min to 1200 r/min. The waveforms of the motor speed, output currents, and switching patterns are depicted in Figure 26. As can be seen in both Figure 26a,b, the motor speed correctly tracked the corresponding reference for both the two per-phase MPC methods. Meanwhile, the output currents have the correct sinusoidal form and magnitude. In terms of switching patterns, it can be observed that the phase *a* switching patterns obtained using the two per-phase MPC methods contain clamping regions as expected. This verifies the correctness of the two per-phase MPC methods used against the dynamic load (a three-phase induction motor).

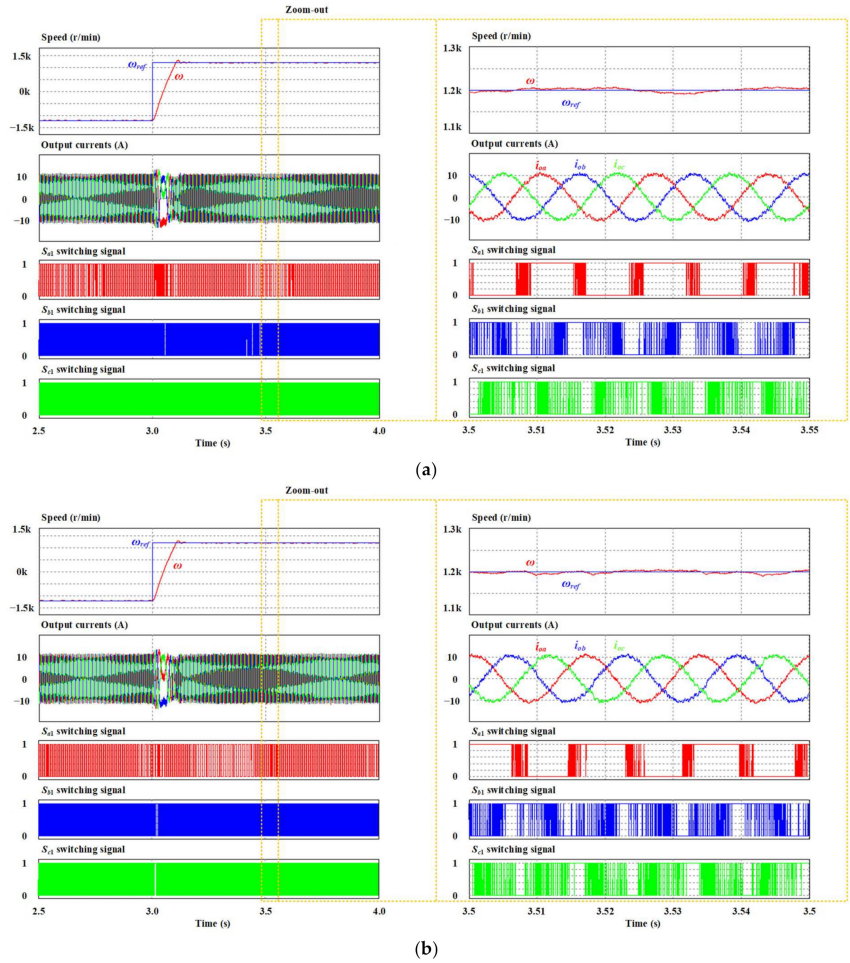


Figure 26. Simulation results of VSI-fed three-phase induction motor attained with (**a**) per-phase MPC1 and (**b**) per-phase MPC2.

Table 2 provides an overview of comparative findings derived from the simulations and experimental outcomes for the two per-phase MPC methods. Regarding output performance, the per-phase MPC1 method provides a lower output current THD than the per-phase MPC2 method. The two per-phase MPC techniques are good at lowering the switch loss in a specific leg. Among them, per-phase MPC2 reduces the switching frequency and switching loss in a specific phase the most, by about 20–30% lower than per-phase MPC1. In terms of dynamic response, the two per-phase MPC methods have superior performance. It is determined that the two per-phase MPC methods have differences in their parameter sensitivity. The load mismatches have a small effect on the performance of the per-phase MPC2 method but a great effect on the per-phase MPC1 method. Due to the per-phase MPC1 method having to calculate all the switching state cases of the VSI

for the considered cost function, the corresponding calculation time is higher than that of the per-phase MPC2 method by about 30%. Additionally, another drawback of the two per-phase MPC approaches is that the switching loss in the two remaining phases increases notably, though both per-phase MPC approaches can significantly reduce the switching loss in specific phase legs.

Table 2. Summary of comparison between two per-phase MPCs.

Performance	Method	
	Per-Phase MPC1	**Per-Phase MPC2**
Average THD of output currents	High	Highest
Per-phase switching frequency and loss reduction capability	High	Highest
Dynamic response	Fast	Fast
Effect of load inductance mismatch	High	Low
Effect of load resistance mismatch	High	Low
Calculation burden	High	Average

4. Conclusions

In this paper, two per-phase MPC methods for increasing the lifespan of VSIs by controlling the switching loss of the leg that has aged the most are compared. The theoretical background of the considered techniques is presented, followed by the simulation and experiment results to evaluate both steady-state, transient-state, and parameter mismatch performances among the two control techniques. Additionally, the operation of the two per-phase MPC methods against both a static load and a dynamic load is correctly verified. Both techniques considered give good results in terms of switching loss reduction capability, whereas the per-phase MPC2 method has the highest impact on reducing the switching loss in the most aged phase leg. In terms of steady-state performance, the two approaches have similar performance. The two per-phase MPC approaches have superior dynamic performance. Regarding uncertainty in the parameters, the per-phase MPC2 method is least affected compared to the per-phase MPC1 scheme. A disadvantage of the per-phase MPC methods is the high computational burden corresponding to the number of switching states evaluated.

Author Contributions: Conceptualization, S.K. and S.C.; methodology, S.K. and S.C.; software, M.H.N.; validation, M.H.N.; formal analysis, M.H.N.; investigation, M.H.N.; resources, S.K.; data curation, M.H.N.; writing—original draft preparation, M.H.N.; writing—review and editing, S.K. and S.C.; visualization, M.H.N.; supervision, S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

VSI	Voltage source inverter
SVPWM	Space vector pulse-width modulation
DPWM	Discontinuous pulse-width modulation
THD	Total harmonic distortion
MPC	Model predictive control
ZSV	Zero-sequence voltage
FFT	Fast Fourier transform

DSP	Digital signal processor
PI	Proportional–integral

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