# Dual Functions of V/SiO$_x$/AlO$_y$/p$^{++}$Si Device as Selector and Memory

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## Abstract

This letter presents dual functions including selector and memory switching in a V/SiO$_x$/AlO$_y$/p$^{++}$Si resistive memory device by simply controlling compliance current limit (CCL). Unidirectional threshold switching is observed after a positive forming with low CCL of 1 μA. The shifts to the V-electrode side of the oxygen form the VO$_x$ layer, where the threshold switching can be explained by the metal-insulation-transition phenomenon. For higher CCL (30 μA) applied to the device, a bipolar memory switching is obtained, which is attributed to formation and rupture of the conducting filament in SiO$_y$ layer. 1.5-nm-thick AlO$_y$ layer with high thermal conductivity plays an important role in lowering the off-current for memory and threshold switching. Through the temperature dependence, high-energy barrier (0.463 eV) in the LRS is confirmed, which can cause nonlinearity in a low-resistance state. The smaller the CCL, the higher the nonlinearity, which provides a larger array size in the cross-point array. The coexistence of memory and threshold switching in accordance with the CCL provides the flexibility to control the device for its intended use.

**Keywords:** Resistive switching, Selector, Memory, Nonlinearity, Silicon oxide, Vanadium

## Background

Resistive random-access memory (RRAM) is one of the promising candidates for the next-generation non-volatile memory technology due to its fast switching speed [1, 2], low-power consumption [3–8], multilevel capability [9–15], high scalability [16–20], and 3D stacking ability [21–25]. These properties are especially suitable for storage class memory (SCM) which can fill the performance gap between dynamic random-access memory (DRAM) as a main memory and solid-state-drive (SSD) as a storage memory. Even though RRAM device has made much progress in the past years [1–25], there remains, however, a major disadvantage: sneak current through neighboring cells occurs in a high-density cross-point array [26]. The memory device with the selector component should provide nonlinear current–voltage (I–V) characteristics to overcome this problem [26–35]. Until now, various devices with nonlinear concepts such as complementary resistive switching (CRS) [26], tunnel

barrier [27–33], Ag-based threshold switching [34], diode-type selector [35, 36], ovonic threshold switching (OTS) [37, 38], and metal-insulator-transition (MIT) [39–43] have been reported. VO$_x$ as one of the typical MIT materials could be widely used in potential applications as optical and electrical switching component [40–42]. SiO$_2$ is widely used as a passivation layer in the semiconductor industry. Moreover, Si-rich SiO$_x$ ($x < 2$) can be used as a resistance change layer in RRAM [44–55]. SiO$_x$ can be preferred over many other materials in terms of compatibility with CMOS processes and low cost. SiO$_x$-based RRAM devices have been reported to act as a mediator of the role of conducting bridges simply by using electrodes such as Cu and Ag with high diffusivity [44–47]. In another case, memory switching is induced by the valence change effect inside the SiO$_x$ layer, which can be explained by generation of oxygen vacancies or proton exchange model [48–55]. In the unipolar switching where a set operation precedes a reset, it is sensitive to the ambient atmosphere. The switching performance in the air is significantly degraded [48–53]. On the other hand, filamentary switching without backward-scan effects shows typical unipolar and bipolar switching in various SiO$_x$-based RRAM devices [52–54].

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Kim *et al. Nanoscale Research Letters* (2018) 13:252

Page 2 of 7

Here, we present the coexistence of threshold switching and memory switching in V/SiO$_x$/AlO$_y$/p$^{++}$Si device depending on compliance current limit (CCL). The device with silicon bottom electrode (BE) has several advantages compared to the conventional metal electrode. The RRAM device with memory or threshold switching is directly connected to the source or drain side in a transistor, which is a potential application for embedded memory and steep slope device. The overshoot current could be reduced due to the series resistance of Si BE. Moreover, nano-tip of silicon BE through wet etching and the adjustment of the doping concentration in silicon surface can improve switching performance. The AlO$_y$ layer, which is a large band gap with an insulated property, helps to lower the operating current during threshold and memory switching. The SiO$_x$ layer acts as memory switching layer at a high CCL, while it serves to supply oxygen to V TE at low CCL, which provides threshold switching.

## Methods

V/SiO$_x$/AlO$_y$/p$^{++}$Si device was fabricated as follows: Firstly, BF$_2$ ions were implanted with an acceleration energy of 40 keV and a dose of $5 \times 10^{15}$ cm$^{-2}$ into a Si substrate to heavily doped Si BE. The lattice damage was cured by the annealing process at 1050 °C for 10 min. Heavily doped Si BE had sheet resistance of 30.4 Ω/□. Next, a 1.5-nm-thick AlO$_y$ layer was deposited by an atomic layer deposition (ALD) system using H$_2$O and Al (CH$_3$)$_3$ and a 5.5-nm-thick SiO$_x$ layer underwent plasma-enhanced chemical vapor deposition (PECVD) by reacting 5% SiH$_4$/N$_2$ (160 sccm), N$_2$O (1300 sccm), and N$_2$ (240 sccm) at 300 °C. Subsequently, a 50-nm-thick vanadium (V) top electrode (TE) with a diameter of 100 μm was deposited by DC sputtering a V target with Ar gas (30 sccm). Finally, a 50-nm-thick Al as a protective layer was deposited by DC sputtering to prevent further oxidation of V TE. All electrical properties were characterized via the DC voltage sweep and pulse modes using a Keithley 4200-SCS semiconductor parameter analyzer (SPA) and a 4225-PMU ultra-fast current–voltage (I–V) module at room temperature, respectively. For device operation, the TiN BE was grounded and the Ni TE bias was controlled.
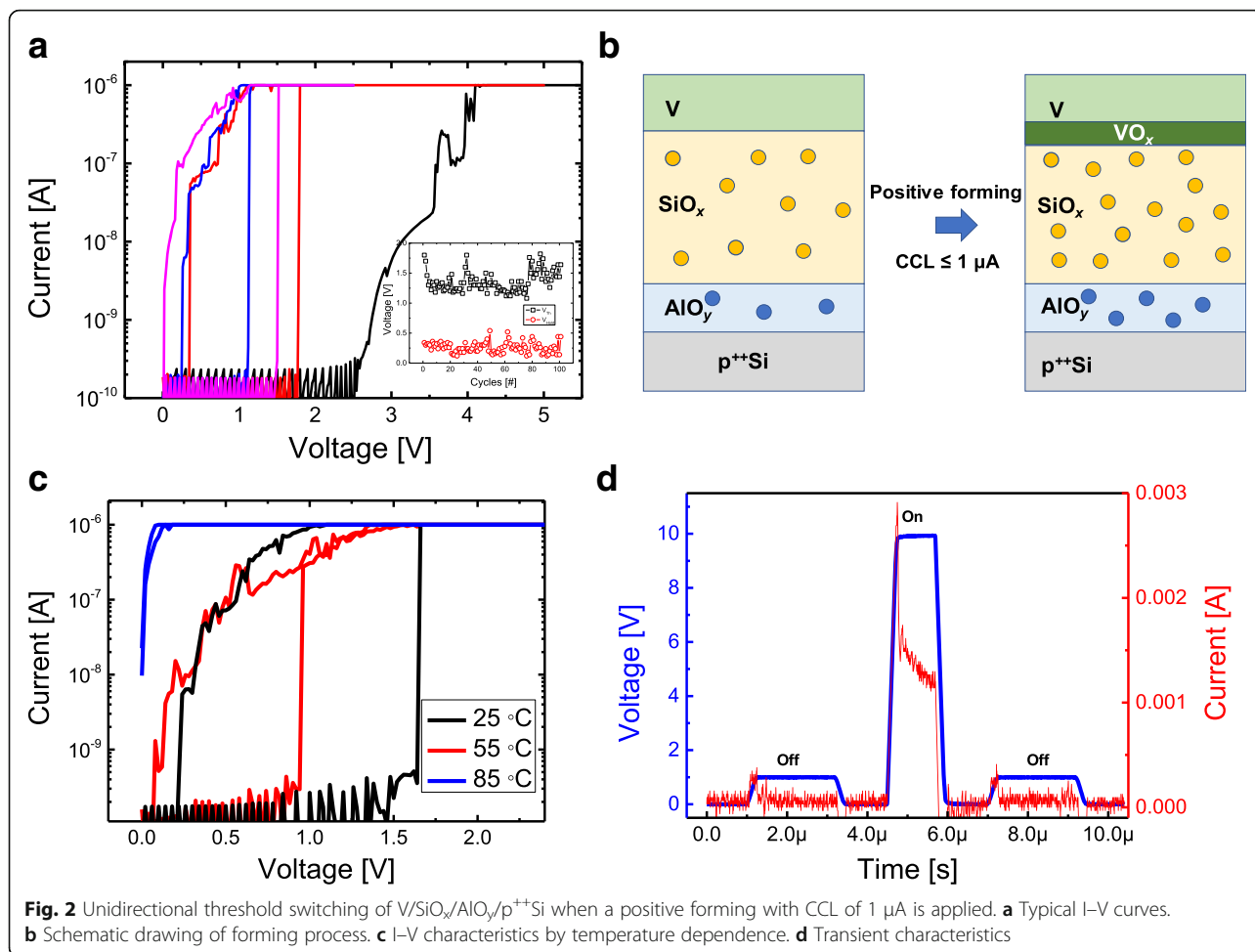
## Results and Discussion

Figure 1a shows the schematic structure of V/SiO$_x$/AlO$_y$/p$^{++}$Si device. Three amorphous V, SiO$_x$, and AlO$_y$ layers and single-crystalline Si layer are observed by a transmission electron microscopy (TEM) cross-sectional image as shown in Fig. 1b. The thicknesses of the SiO$_x$ and AlO$_y$ layers are 5.5 and 1.5 nm, respectively. To confirm the composition ratio of two dielectric films, XPS analysis was conducted (Additional file 1). The $x$
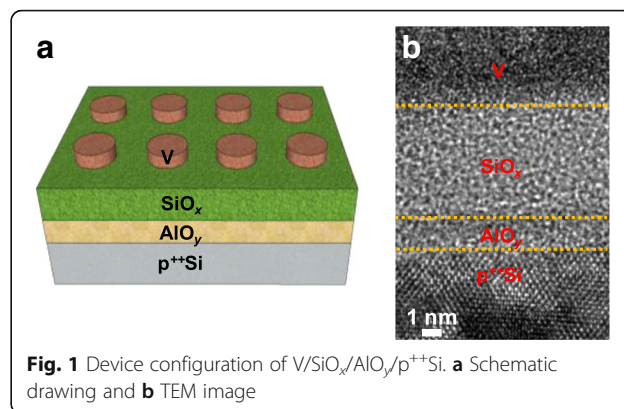


**Fig. 1** Device configuration of V/SiO$_x$/AlO$_y$/p$^{++}$Si. **a** Schematic drawing and **b** TEM image
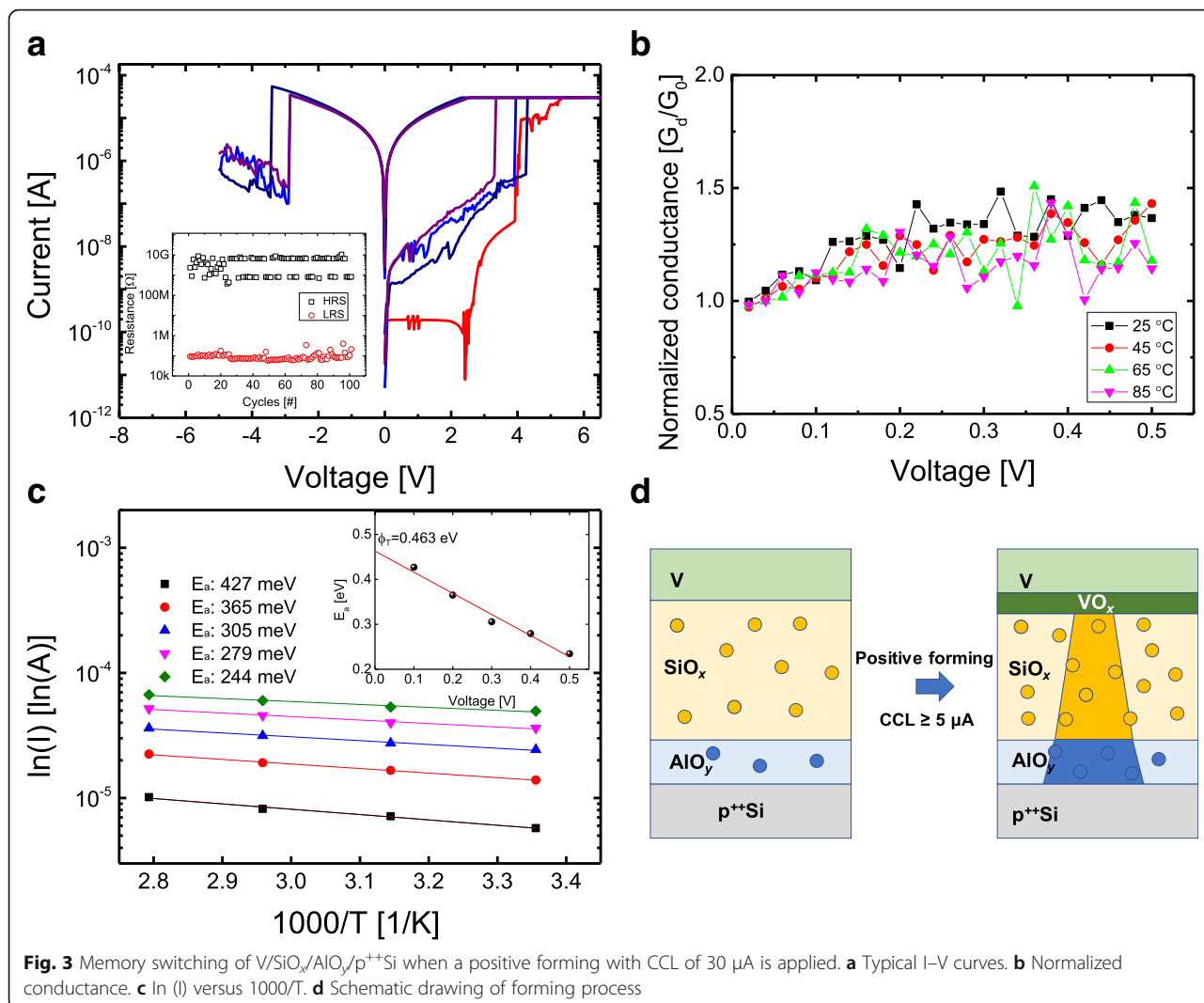
value of SiO$_x$ and the $y$ value of AlO$_y$ are 0.88 and 1.33, respectively. Our SiO$_x$ film using PECVD compared to SiO$_2$ deposited using dry oxidation is deposited at a much lower temperature and has much more defects, making them suitable for resistive switching at relatively lower voltages. Figure 2a shows typical threshold switching of V/SiO$_x$/AlO$_y$/p$^{++}$Si device. The initial switching with a positive forming process requires higher voltage than subsequent threshold switching since the dielectric layers have initially smaller defects. A CCL of 1 μA is applied to the device to avoid the formation of excessive conducting filaments in the SiO$_x$ layer. The leakage current is very low (100 pA at 1 V) compared with previously reported threshold switching of VO$_x$. This advantage is attributed to the Al$_2$O$_3$ with higher permittivity and thermal conductivity compared to the SiO$_2$. Off-state has the insulating property because the filaments are easily ruptured and then there are no remaining filaments. A possible mechanism for threshold switching is the oxidation of the V TE from the oxygen supplied from the SiO$_x$ layer during the positive forming process as shown in Fig. 2b. The electrical property of VO$_x$ between V TE and SiO$_x$ layer may change from insulating state to metallic state, causing a sudden change in resistance. A low CCL of 1 μA is not sufficient to cause efficient conducting filaments inside the SiO$_x$ film. Therefore, SiO$_x$ with insulating properties can be another cause to reduce the off-current. For a negative forming process of V/SiO$_x$/AlO$_y$/p$^{++}$Si device, a threshold switching is not observed (see Additional file 1). When the negative bias is applied to the V TE, the movement of the oxide moves toward the Si BE, so that the V TE can no longer participate in the threshold switching as VO$_x$. Inset of Fig. 2a exhibits the threshold voltage (V$_{th}$) and hold voltage (V$_{hold}$) during the 100 - cycles. The V$_{th}$ where the current sharply increases with nearly infinite slope is between 1.08 and 1.82 V, and V$_{hold}$ at which point the current return to a high-resistance state is between 0.12 and 0.54 V. Figure 2c shows the I–V characteristics in the on-current at different temperatures. At

Kim *et al. Nanoscale Research Letters* (2018) 13:252

Page 3 of 7



**Fig. 2** Unidirectional threshold switching of V/SiO$_x$/AlO$_y$/p$^{++}$Si when a positive forming with CCL of 1 μA is applied. **a** Typical I–V curves. **b** Schematic drawing of forming process. **c** I–V characteristics by temperature dependence. **d** Transient characteristics

25 °C and 55 °C, they show almost similar threshold switching, but I–V curve at a higher temperature of 85 °C loses the threshold switching property. It is well known that VO$_x$ loses its MIT at high temperatures. Thus, this result is another proof that VO$_x$ is the main cause of the threshold switching. Figure 2d shows the transient characteristics for threshold switching. The pulse with the amplitude of 1 V monitored the read current before and after writing pulse with width of 1 μs. The high current was monitored while the pulse with high amplitude is applied to the device, and then, the V/SiO$_x$/AlO$_y$/p$^{++}$Si device turned off the current immediately after the writing pulse was removed. The selector properties analyzed above can be used when combined with operation of memory elements below 1 μA [55, 56].

Figure 3a shows the bipolar resistive switching of V/SiO$_x$/AlO$_y$/p$^{++}$Si device after a positive forming with CCL of 100 μA. Then, the reset process with a rapid increase in resistance is performed by sweeping the negative voltage, and the device is switched to a high-resistance state (HRS). The set process with a rapid decrease in resistance then occurs at a positive bias

voltage, causing the device to turn back to a low-resistance state (LRS). In order to understand the properties of the conducting filament, we observe the normalized conductance and the temperature dependence. The conduction in the LRS is an important guideline to indirectly inform the properties of the conducting filament. Figure 3b shows the normalized conductance (G$_N$) which is defined as the dynamic conductance (G$_d$) divide by static conductance (G$_0$) for I–V curves of V/SiO$_x$/AlO$_y$/p$^{++}$Si device in the LRS with different temperatures. Regardless of the temperature, the G$_N$ value converges to 1 when the voltage is zero. This allows us to rule out the well-known conduction mechanism such as Schottky emission, Fowler-Nordheim tunneling, and Child's law (I~V$^2$) in space-charge-limited current (SCLC). Metallic ohmic conduction can also be excluded considering temperature dependence as shown in Fig. 3c. The decrease in resistance with increasing the temperature suggests that the conducting filament has a semiconducting property. Thus, we can exclude the penetration of V into the SiO$_x$ layer for the main conducting filament of V/SiO$_x$/AlO$_y$/p$^{++}$Si device in LRS. Therefore,

Kim et al. Nanoscale Research Letters (2018) 13:252

Page 4 of 7



**Fig. 3** Memory switching of V/SiO$_x$/AlO$_y$/p$^{++}$Si when a positive forming with CCL of 30 μA is applied. **a** Typical I–V curves. **b** Normalized conductance. **c** ln (I) versus 1000/T. **d** Schematic drawing of forming process

the bipolar memory operation of the V/SiO$_x$/AlO$_y$/p$^{++}$Si device is dominated by intrinsic switching of SiO$_x$. It is also confirmed that the positive and negative currents are not that much different suggesting that rather than an interface-type such as Schottky emission, it is dominated by bulk conduction. Taking into account the abovementioned normalized conductance, there are two possible bulk dominant conduction mechanisms. The first one is hopping conduction following the formula:
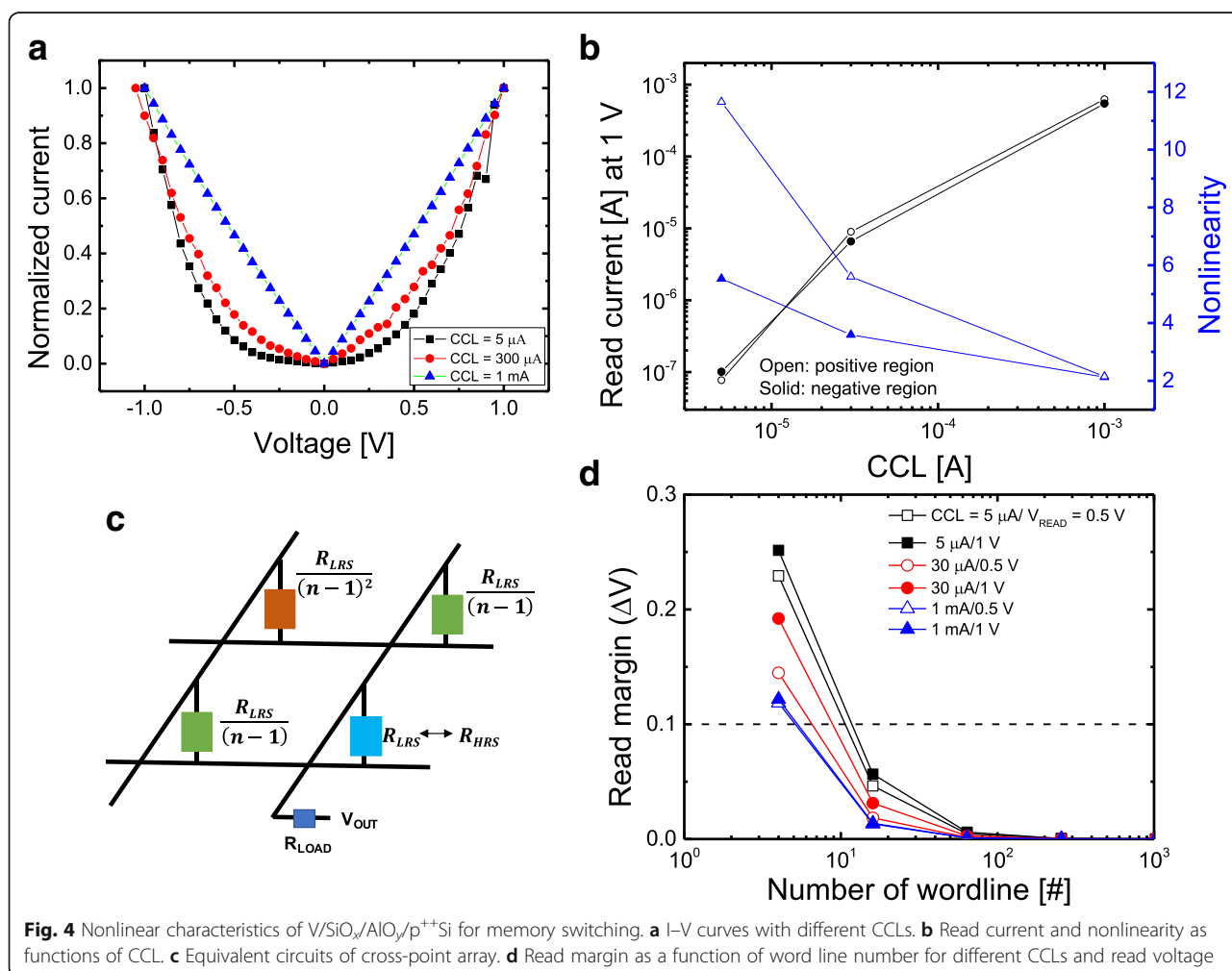
$$J = qnav_o e^{-q\varnothing_T/kT} e^{qaV/2dkT}$$

where $q$, $n$, $a$, $\varnothing_T$, $v_o$, and $d$ are the electric charge, concentration of space charge, mean of hopping distance, electron barrier height for hopping, intrinsic vibration frequency, and the thickness of dielectric film, respectively. The $\varnothing_T$ calculated from the slope of a linear plot of ln (I) versus 1000/T is 0.463 eV as shown in Fig. 3c. A

value calculated from the relationship between E$_a$ and V is 5.17 nm, indicating the conducting filament formed in the SiO$_x$ is not strong and is close to the HRS state. The other conduction mechanism, the Poole-Frenkel (P-F) emission, was covered in Additional file 1. Based on the above results, the conducting filament model in the memory operation of V/SiO$_x$/AlO$_y$/p$^{++}$Si device is depicted in Fig. 3d. In the positive forming process, the oxidation process proceeded on the V TE side, but due to the high CCL, a conductive filament can be formed inside the SiO$_x$ and AlO$_y$ due to the movement of the oxygen vacancies. During the reset process, the electric field opposite to the forming and set induces oxygen and recombination with the oxygen vacancy, resulting in the rupture of the conductive filament. It is noted that the selector and memory operations are observed in the same cell. Memory operation is possible after the threshold operation has occurred and then the switch is completely turned off. However, the reverse direction is not

Kim *et al. Nanoscale Research Letters* (2018) 13:252

Page 5 of 7

possible because the reset switching of the memory operation is not completely turned off.

Figure 4a shows normalized I–V curves in the LRS of V/SiO$_x$/AlO$_y$/p$^{++}$Si device at low-voltage regime (0~1 V) for different CCL conditions (5 μA, 30 μA, and 1 mA). Here, the normalized I–V curve is defined as the current at each voltage divided by the current at 1 V. Since the levels of the LRS current depending on the CCL are varied, we set the current value at 1 V to easily compare the nonlinearity. It can be observed that as the CCL decreases, the current is suppressed at lower voltage regime. In order to derive a more quantitative relation, nonlinearity is defined as the ratio of the current at V$_{READ}$ to that at the half of V$_{READ}$. Figure 4b shows the read current at 1 V and nonlinearity as a function of CCL for V/SiO$_x$/AlO$_y$/p$^{++}$Si device. The decrease in read current due to CCL reduction suggests that the conducting filament is becoming finer and then the nonlinearity increases. The intrinsic silicon oxide film exhibits high nonlinearity even in a single layer. The intrinsic nonlinear property is due to the bulk nature of the silicon oxide rather than the interface of the silicon. The smaller the CCL is, the less the degradation is generated in the SiO$_x$, so the lowering of the trap energy level in the LRS compared to that in the HRS can be minimized. Therefore, the higher energy barrier can maximize nonlinearity in the LRS state when lower CCL is applied to the device. Similarly, the conduction described by the P-F emission in the TaO$_x$/TiO$_y$ stack ensures high nonlinearity [57]. Another possibility is that because the dielectric constant of the oxide is smaller, more passes are made to the oxide film due to the concentration of the field. This can lead to the lowering of the trap energy level of the oxide layer, which can be expected to serve as a tunnel barrier for Al$_2$O$_3$. To obtain to the read margin (ΔV) in $n \times n$ cross-point array, we use the simplified equivalent circuit as shown in Fig. 4c. Considering the worst case, the adjacent cells are set to the LRS and the load resistance (R$_L$) to the LRS resistance. The ΔV was calculated from difference between V$_{OUT}$ at LRS and V$_{OUT}$ at HRS. Figure 4d shows the ΔV as a function of number of word lines ($n$) for V/SiO$_x$/AlO$_y$/p$^{++}$Si



**Fig. 4** Nonlinear characteristics of V/SiO$_x$/AlO$_y$/p$^{++}$Si for memory switching. **a** I–V curves with different CCLs. **b** Read current and nonlinearity as functions of CCL. **c** Equivalent circuits of cross-point array. **d** Read margin as a function of word line number for different CCLs and read voltage

Kim *et al. Nanoscale Research Letters* (2018) 13:252

Page 6 of 7

device. The smaller the CCL, the higher the ΔV because the nonlinearity increases. When 10% read margin is secured, the array can be expanded to about more than $10 \times 10$ for CCL of 5 μA and to $5 \times 5$ for CCL of 1 mA. The array size to withstand the sneak current is not sufficient, but it will help expand the array size when the device with selector function is connected in a V/SiO$_x$/AlO$_y$/p$^{++}$Si device. Compared to 0.5-V read in all CCLs, it has higher nonlinearity with read at 1 V. Although low V$_{READ}$ leads to low static power in the read operation, the value of nonlinearity becomes smaller, which is due to the fact that the electric field is less on the SiO$_x$/AlO$_y$ layer in smaller V$_{READ}$.

## Conclusions

In this work, a V/SiO$_x$/AlO$_y$/p$^{++}$Si device having both a selector and a memory function by simply controlling CCL is investigated. When a CCL of 1 μA or less is applied, unidirectional threshold switching is observed for selector application. Positive forming oxidizes the V electrode and the MIT phenomenon of VO$_x$ can induce threshold switching. The AlO$_y$ layer is able to achieve a high selectivity of $10^4$ by lowering the off-current. On the other hand, when a CCL of 5 μA or more is applied, memory switching is observed as effective conducting filaments are formed on the SiO$_x$ layer. The lower the CCL, the greater the nonlinearity, which helps to increase the size of the cross-point array.

## Additional File

**Additional file 1:** Supporting information. (DOCX 81 kb)

### Abbreviations
ALD: Atomic layer deposition; BE: Bottom electrode; CCL: Compliance current limit; CRS: Complementary resistive switching; DRAM: Dynamic random-access memory; HRS: High-resistance state; I–V: Current–voltage; LRS: Low-resistance state; MIT: Metal-insulator-transition; OTS: Ovonic threshold switching; PECVD: Plasma-enhanced chemical vapor deposition; P-F: Poole-Frenkel; RRAM: Resistive random-access memory; SCLC: Space-charge-limited current; SCM: Storage class memory; SPA: Semiconductor parameter analyzer; SSD: Solid-state-drive; TE: Top electrode; TEM: Transmission electron microscopy; V: Vanadium

### Availability of Data and Materials
All data and material are available.

### Authors' Contributions
In this work, KS prepared the samples and electrical measurements and wrote the manuscript. PBG and CYF designed the experiments. LCY, KMH, and KTH carried out the experiments. KMH, KH, and CYC helped in the analysis of the experimental results. All authors read and approved the final manuscript.

### Competing Interests
The authors declare that they have no competing interests.

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Kim *et al. Nanoscale Research Letters* (2018) 13:252

Page 7 of 7

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