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Capacitance–Voltage Fluctuation of Si_xN_y -Based Metal–Insulator–Metal Capacitor Due to Silane Surface Treatment

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Abstract: In this study, we analyze metal–insulator–metal (MIM) capacitors with different thicknesses of Si_xN_y film (650 Å, 500 Å, and 400 Å) and varying levels of film quality to improve their capacitance density. Si_xN_y thicknesses of 650 Å, 500 Å, and 400 Å are used with four different conditions, designated as MIM (N content 1.49), NEWMIM (N content 28.1), DAMANIT (N content 1.43), and NIT (N content 0.30). We divide the C–V characteristics into two categories: voltage coefficient of capacitance (VCC) and temperature coefficient of capacitance (TCC). There was an overall increase in the VCC as the thickness of the Si_xN_y film decreased, with some variation depending on the condition. However, the TCC did not vary significantly with thickness, only with condition. At the same thickness, the NIT condition yielded the highest capacitance density, while the MIM condition showed the lowest capacitance density. This difference was due to the actual thickness of the film and the variation in its k-value depending on the condition. The most influential factor for capacitance uniformity was the thickness uniformity of the Si_xN_y film.

Keywords: MIM; capacitors; metal–insulator–metal; electrical performance; Si_xN_y ; cap density; VCC; TCC



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1. Introduction

A metal–insulator–metal (MIM) capacitor is an analog integrated circuit (IC) configuration device with the advantages of low electrode resistance and parasitic capacitance [1–4]. MIM capacitors have high charge mobility and burst power characteristics that make them excellent energy-storage devices and potential auxiliary power sources.

IM capacitors have been applied to ICs such as high-power microprocessor units and dynamic random-access memory. However, with the development of wireless communication, their application to radio frequency (RF) devices has been actively studied [5–7]. As current RF devices require high operating frequencies, MIM devices also require high capacitance per unit area [8–11].

According to this demand, the design of the structure, thin-film deposition method, selection of the bottom and top electrode materials, insulator material, thickness of the electrode and insulator, dielectric constant of the insulator, and crystal structure of the insulator must be considered in depth to produce a high-performance MIM capacitor with a high capacitance [12–15]. In the evaluation of MIM capacitors, it is important to conduct a comprehensive analysis considering factors such as capacitance density (CD), leakage current density, charge storage density, and dielectric breakdown strength [16–19].

The choice of insulator material is a crucial factor in capacitors, and the CD relies heavily on the dielectric constant and thickness of the insulator. According to Equation (1),

the CD increases when the dielectric constant is higher, which is a natural property of the insulator, and when the thickness is lower [1,20]:

$$C = \frac{k\epsilon_0 A}{d} \rightarrow \frac{C}{A} = \frac{k\epsilon_0}{d} \quad (1)$$

where C denotes the capacitance (F), k is the dielectric constant, ϵ_0 is the permittivity of the vacuum (8.854×10^{-12} /m), and d is the thickness of the insulator (m).

Because of the abovementioned reasons, it is generally necessary to introduce a high- k material to increase the dielectric constant [21,22], which entails considerable investment and time because it requires equipment, facilities, and source replacement. In addition, according to Natori et al., the relative permittivity of the material (k) decreases as the insulator thickness of the capacitor decreases, and k tends to decrease significantly for high- k materials [13,23]. Therefore, the introduction of high- k materials is subject to many limitations. However, if the thickness of the currently used medium- k dielectric material, Si_xN_y ($k = 7$), can be reduced by considering the leakage aspect, the capacitance value can be increased without using a high- k material [24–26]. Yu et al. explained the performance of HfO_2 -based MIM capacitors deposited by the atomic layer deposition (ALD) method with respect to the thickness of the dielectric [27]. As the thickness of the HfO_2 insulator layer decreased, the CD and voltage coefficient of capacitance (VCC) increased [28–31]. In practice, GaAs-based MIM capacitors have been used in the past. In fact, for GaAs-based MIM capacitors, Si_xN_y is the most commonly applied material owing to its excellent electrical properties, compliant dielectric constant, high dielectric breakdown voltage, and low leakage current [28,32,33]. Moreover, the electrical properties can be improved by optimizing the deposition condition of Si_xN_y , which has the greatest effect on the electrical properties of MIM capacitors. Yota et al. confirmed that the stress, CD, breakdown voltage, and performance of MIM capacitors exhibited significant differences in each insulator layer, with a single layer or multiple layers of silicon nitride formed depending on the deposition conditions [34]. Therefore, the electrical properties of MIM capacitors can be improved by optimizing the deposition condition of Si_xN_y .

In this study, to develop an optimal condition for the deposition conditions of Si_xN_y that improves the insulator properties of MIM capacitors and secures feasibility, we fabricated MIM capacitors with different thicknesses of Si_xN_y and deposition conditions on M4 wiring and then evaluated the capacitance–voltage (C – V) characteristics, focusing on the evaluation of cap density uniformity, the dielectric temperature coefficient of capacitance (TCC), and the VCC.

2. Materials and Methods

Patterned 200 mm Si (100) wafers were used to measure the integration process steps. Several different cap dielectrics were investigated and deposited by PE-ALD. An Applied Materials MIRRA tool (Applied Materials, Gloucester, MA, USA) was used for the blanket. In this study, the density of MIM capacitors was considered to be $8 \text{ fF}/\text{m}^2$, and the capacitors were fully integrated using the 0.15 μm Al interconnect processes. The first single MIM capacitor was formed using metal 3 and metal 4 to minimize the effect of the parasitic coupling of the silicon substrates. In addition, the second single MIM capacitor was formed using metal 5 and metal 6. It is crucial for MIM capacitors to have a symmetric structure by having identical boundary conditions on both sides of the dielectric [8,35,36].

The bottom electrode of the MIM capacitor was prepared using Ti (100 Å)/Al–Cu (4500 Å)/Ti (50 Å)/TiN (600 Å) wiring, and the top electrode was prepared using TiN (1500 Å). The insulator was Si_xN_y . The capacitor fabrication process was as follows: bottom electrode deposition → bottom electrode scrub → insulator deposition → top metal deposition → MIM PH → MIM → TOP METAL etching → $((\text{CH}_3)_4\text{NOH}:\text{H}_2\text{O})$ cleaning 1 → MIM asher → $((\text{CH}_3)_4\text{NOH}:\text{H}_2\text{O})$ cleaning 2 → insulator etching → ACT 935 (wet PR strip solution including amine) → UVAS. MIM ET was performed using the endpoint detection method.

The top electrode layer was connected to the upper metal layer through a dense matrix of vias. All wafers mentioned in this paper were passivated using PE-ALD nitride and were annealed below 450 °C. To improve the voltage linearity, Interface plasma treatment was administered before and after the PE-ALD dielectrics. Further details of the interface plasma treatment and thickness ratio in each stack layer are listed in Table 1. The blanket film characteristics of PE-ALD dielectrics were evaluated by using an ellipsometer at 673 nm to measure the thickness, refractive index, and uniformity of the PE-ALD dielectrics. A Hg probe was used to measure the dielectric constant, and the deposition rate was calculated according to the thickness slope as a function of the cycle times [4].

Table 1. (a) Si_xN_y film properties and (b) corresponding process conditions.

(a)	MIM	NEW MIM 650	DAMA NIT	NIT
Dep. rate	~149 Å/s	~29 Å/s	~59 Å/s	88 Å/s
Within W/F unit (1σ)	1.14%	1.90%	2.34%	2.77%
W/F to W/F unit (1σ)	1.58%	2.21%	1.05%	2.30%
Stress	-2.23×10^9	-1.75×10^{10}	-2.34×10^9	
H content (N-H: Si-H)	12.7%: 8.5%	22.5%: 0.8%	10.5%: 7.3%	4.4%: 14.8%
N content (N-H/Si-H)	1.49	28.1	1.43	0.30
(b)	MIM 650	NEW MIM 650	DAMA NIT	NIT 650
Step end control	By time	By time	By time	By time
Maximum step time	4.4 s	22.8 s	11.0 s	
Endpoint selection	No endpoint	No endpoint	No endpoint	No endpoint
Pressure	Servo 4.25 Torr	Servo 4.25 Torr	Servo 4.2 Torr	Servo 4.5 Torr
RF power	690 W	690 W	420 W	425 W
Susc. temperature	400 °C	400 °C	400 °C	400 °C
Susceptor spacing	620 mils	620 mils	550 mils	475 mils
N ₂	3800 sccm	3800 sccm	2500 sccm	4000 sccm
NH ₃	130 sccm	50 sccm	38 sccm	60 sccm
SiH ₄	260 sccm	100 sccm	110 sccm	170 sccm

The C–V characteristics were measured manually using an LCR meter (HP4284A, Agilent, Santa Clara, CA, USA) under the conditions given in Table 2. The VRDB was performed based on the JESD35-A standard. The thickness analysis of Si_xN_y per condition was performed using transmission electron microscopy (CM200FEGTEM)/scanning transmission electron microscopy (STEM) operated at 300 keV with an energy-dispersive X-ray spectroscopy (EDS) SUTW-SiLi X-ray detector and a Gatan 666 parallel electron energy loss spectroscopy (PEELS) spectrometer (Philips, Eindhoven, Netherlands), and a focused ion beam (FIB). The via resistance and via chain yields were measured in dual-damascene structures. A wafer-level bias thermal stress (BTS) test was performed under different conditions to verify the effectiveness of the barrier layers. Failures were analyzed by scanning electron microscopy (SEM) and X-ray spectroscopy (EDX). (SIGMA, Carl Zeiss, Jena, Germany)

Table 2. C–V characterization measurement conditions.

Parameter	Setting
Display mode	Cp (parallel capacitor), D (dissipation factor)
Sweep voltage (V)	−5~5
Step (V)	0.5
Oscillation	0.025
Frequency (kHz)	100
Capacitor size (μm ²)	10 × 10, 15 × 15, 20 × 20, 25 × 25, 30 × 30, 50 × 50
Measurement points	Three points (top, center, and bottom)
Temperature (°C)	25, 50, 75, 100, 125

3. Results and Discussion

To understand the wafer-wide trend in CD, PCM measurements were performed with the split conditions given in Table 1; the corresponding results for a 25×25 cap size are presented in Figure 1.

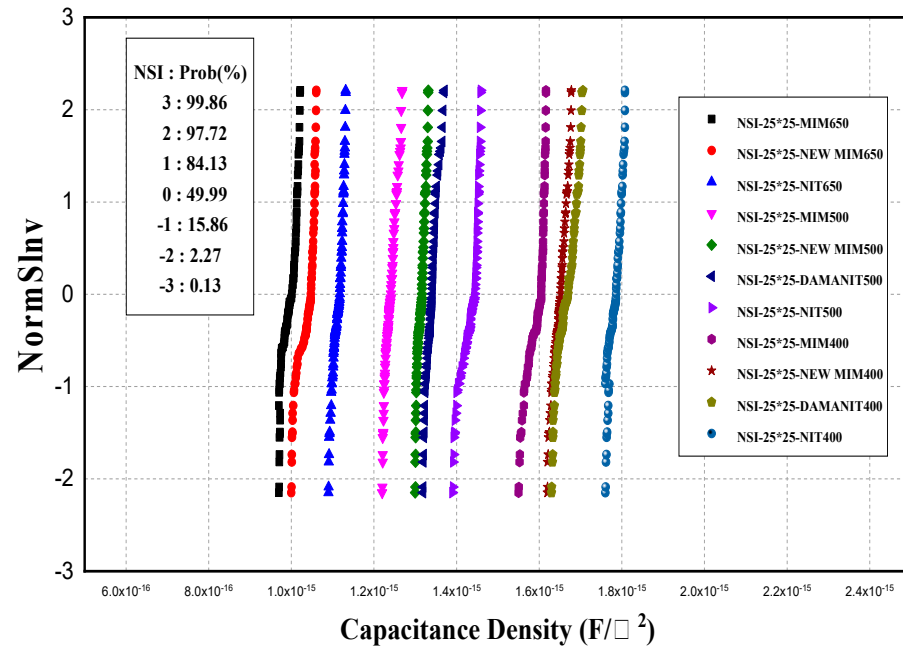


Figure 1. Accumulation curves for CD obtained from different thicknesses and conditions of SixNy films for MIM capacitors.

The CD varied depending on the split condition but was uniform within the wafer. For all conditions, the CD increased with decreasing thickness, and at the same thickness, it varied slightly between conditions. By examining the range of CD in relation to thickness, the following values were observed for thicknesses of 650, 500, and 400 Å, respectively: 0.983–1.1, 1.24–1.4, and 1.57–1.79 fF/μm². The difference in capacitance densities between conditions at the same thickness can be considered to be the difference between the actual thickness of the Si_xN_y film and the target thickness and the difference in the k-value of the deposited film by condition. To confirm this, 500 Å thick Si_xN_y films deposited under the different different conditions were analyzed by TEM; the corresponding results are shown in Figure 2.

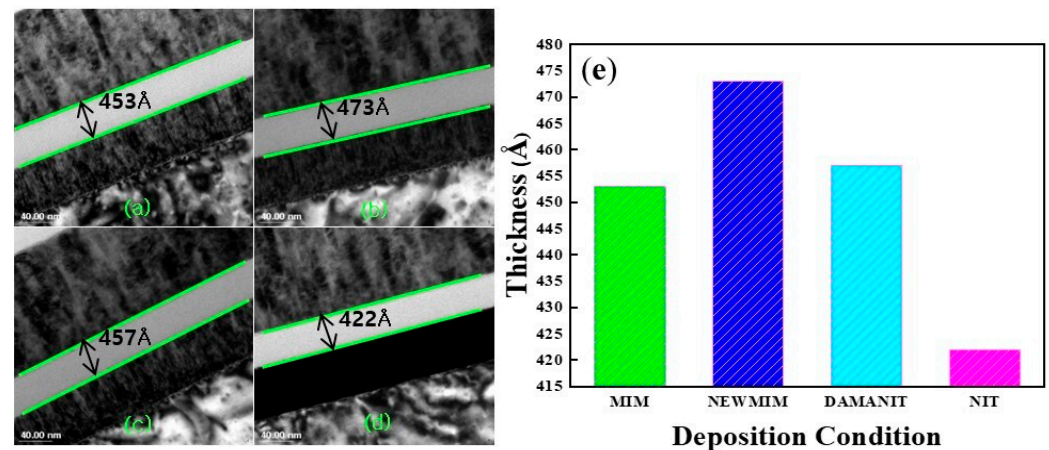


Figure 2. Cross-sectional TEM images of Si_xN_y films with (a) MIM, (b) NEWMIM, (c) DAMANIT, and (d) NIT. The thicknesses of the Si_xN_y films are presented in the (e) rod graph.

Figure 2a–d depict the cross-sectional TEM images of Si_xN_y films deposited under MIM, NEWMIM, DAMANIT, and NIT conditions, respectively, and Figure 2e shows a barplot of the thickness of Si_xN_y films obtained from the TEM images. The NIT condition showed the lowest thickness, while the NEWMIM condition showed the highest thickness. For accurate analysis, the k -value was calculated after matching the TEM analysis die and the PCM measurement die; the corresponding results are presented in Table 3.

Table 3. The k -values of the MIM capacitor with Si_xN_y conditions of MIM, NEWMIM, DAMANIT, and NIT.

Deposition Condition	MIM	NEWMIM	DAMANIT	NIT
CD ($\text{fF}/\mu\text{m}^2$)	1.3256	1.3203	1.3103	1.3606
Thickness (TEM, Å)	453	473	457	422
k -value ($\epsilon_0 \cdot \epsilon$)	6.00×10^{-17}	6.25×10^{-17}	5.99×10^{-17}	5.74×10^{-17}

In this experiment, we compared the capacitance densities of four materials with the same thickness (500 Å) and found that NIT afforded the highest CD, followed by NEWMIM, DAMANIT, and MIM. However, we noticed that the deposited thickness did not follow this trend. This indicates that thickness alone is not the only factor that affects the CD. The difference in the k -value according to the condition also appears to play a significant role in determining the CD. In general, the k -value is influenced by two primary factors, namely, the macroscopic electric field and the dipole moment per unit volume, as given by Equation (2) [2]:

$$K = 1 + \frac{4\pi P}{E} \quad (2)$$

where P is the dipole moment per unit volume and E is the macroscopic electric field.

Because the p -value is dependent on the electronic polarizability, it is affected by the bond conformation and bond strength [21]. The Si_xN_y films had different dipole moments due to the different values of Si-H/N-H (Table 4) depending on the deposition condition; therefore, the k -value was different for each condition.

Table 4. Properties of Si_xN_y films according to different conditions.

	MIM 650 DEP	NEW MIM 650 DEP	DAMA NIT 650 DEP	NIT 650 DEP
Deposition rate (Å/s)	~149	~29	~59	88
Within W/F unit (1σ, %)	1.14	1.90	2.34	2.77
W/F to W/F unit (1σ, %)	1.58	2.21	1.05	2.30
Stress	-2.23×10^9	-1.75×10^{10}	-2.34×10^9	-
H content (N-H:Si-H)	12.7%:8.5%	22.5%:0.8%	10.5%:7.3%	4.4%:14.8%

To check the variation in CD according to capacitor size, the capacitor density by thickness and condition was measured for 10×10 , 15×15 , 20×20 , 25×25 , 30×30 , and $50 \times 50 \mu\text{m}^2$ samples; it is plotted in Figure 3. In this case, the CD according to size was taken as the average value within the wafer.

It can be observed that the CD decreases as the size of the capacitor increases, regardless of the thickness and condition of Si_xN_y . After a certain point, the CD remains constant. This phenomenon can be attributed to the effect of fringe capacitance due to the perimeter/area ratio and the variation in fringe impedance CD (FICD) with respect to size. The difference between capacitor sizes of 10×10 and $20 \times 20 \mu\text{m}^2$ is more pronounced in the case of FICD variation, as it has a greater impact on smaller sizes [37].

In terms of device fabrication, the uniformity of the CD is closely related to the process capability index (C_p , C_{pk}), with Si_xN_y thickness uniformity being the most important factor.

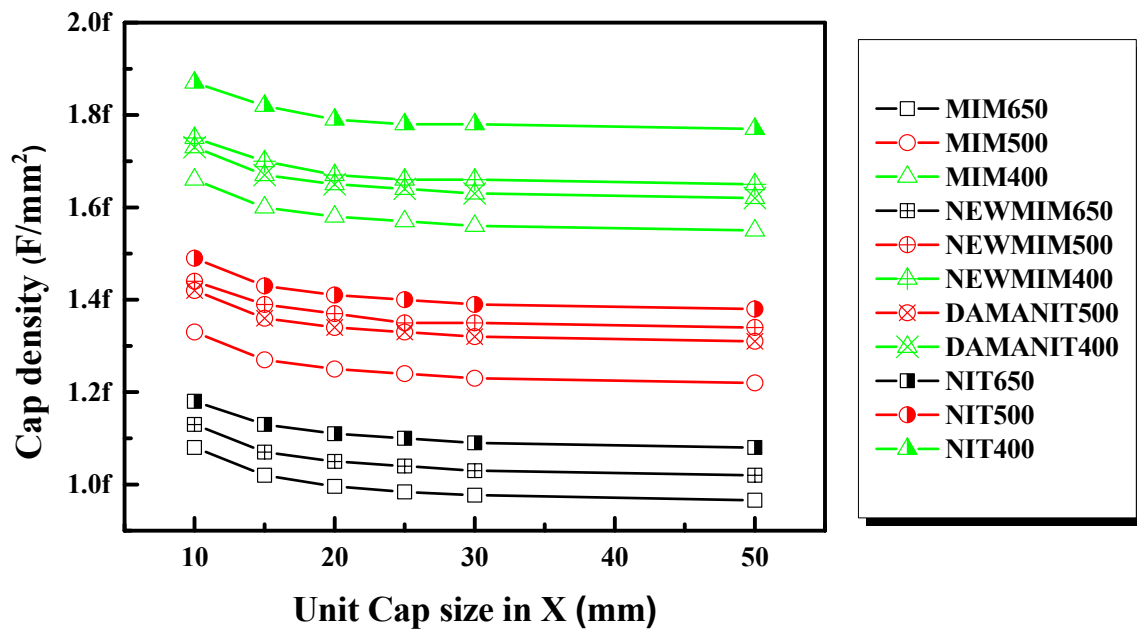


Figure 3. Effect of capacitor size on MIM CD with different Si_xN_y thicknesses and conditions.

As depicted in Figure 4, although there are a few points that deviate from the linear trend, a proportional relationship exists between Si_xN_y thickness nonuniformity and CD nonuniformity, with a slope of 1.04.

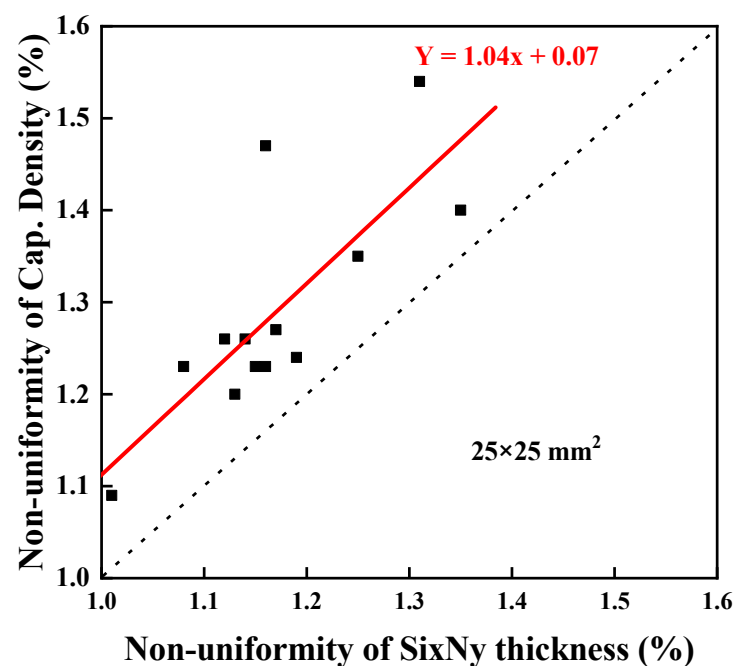


Figure 4. Relationship between nonuniformity of CD and Si_xN_y thickness.

Improving the uniformity of Si_xN_y thickness can result in an improvement in CD uniformity, which, in turn, can increase the values of C_p and C_{pk} on the device manufacturing side to 1.33 or above.

To measure the VCC, an index indicating the degree of change in capacitance with respect to voltage variations, measurements were taken at the top, center, and bottom of

the wafers according to the thickness of Si_xN_y and the conditions. The VCC is denoted by V_{cc1} (ppm/dV) and V_{cc2} (ppm/dV²), as expressed by Equation (3) [38]:

$$\frac{C(V) - C(0)}{C(0)} = V_{cc2}V^2 + V_{cc1}V + C \quad (3)$$

where $C(V)$ is the capacitance under variable voltage, $C(0)$ is the capacitance at 0 V, V_{cc1} and V_{cc2} are the VCCs, and C is a constant value.

The VCC graph was plotted by performing a polynomial fit with the voltage on the X-axis and the normalized ΔC on the y-axis, as described in Equation (3). As an example, the VCC graph for the Si_xN_y film processed with the NEWMIM condition at a thickness of 500 Å is depicted in Figure 5.

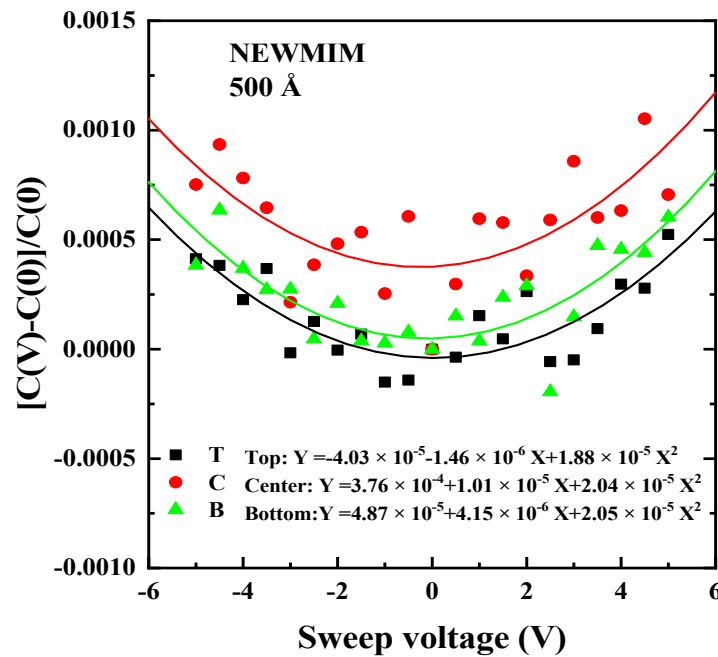


Figure 5. Normalized ΔC vs. voltage at the top, center, and bottom positions. The condition and thickness of the Si_xN_y film are NEWMIM and 500 Å, respectively.

The VCC graph results for the Si_xN_y films, which vary in thickness (650 Å, 500 Å, and 400 Å) and condition (MIM, NEWMIM, DAMANIT, and NIT), are summarized in Figure 6. Figure 6a displays the V_{cc1} values according to thickness, while Figure 6b illustrates the V_{cc2} values as a function of thickness. Both the V_{cc1} and V_{cc2} values showed an increasing trend as the thickness decreased, with the initial level and degree of increase varying according to the condition.

In the case of V_{cc1} , all conditions showed values below 60 ppm/dV at 650 Å, but they values increased as the thickness decreased, and only the MIM and NEWMIM conditions showed values over 60 ppm/V. V_{cc2} tended to increase as the thickness decreased; however, all other conditions except NIT could satisfy the value of 100 ppm/dV² or less when implementing a 2-fF/ μm^2 MIM capacitor.

To investigate the TCC characteristics of the MIM capacitors, the capacitance was measured at the center of the wafers with varying thicknesses and conditions of the Si_xN_y films while incrementally raising the temperature to 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C. The TCC was calculated using Equation (4) [39]:

$$\frac{C(T) - C(25)}{C(25)} = T_{cc}T + C \quad (4)$$

where $C(T)$ is the capacitance under variable temperature, $C(25)$ is the capacitance at 25 °C, T_{CC} is the TCC, and C is a constant value.

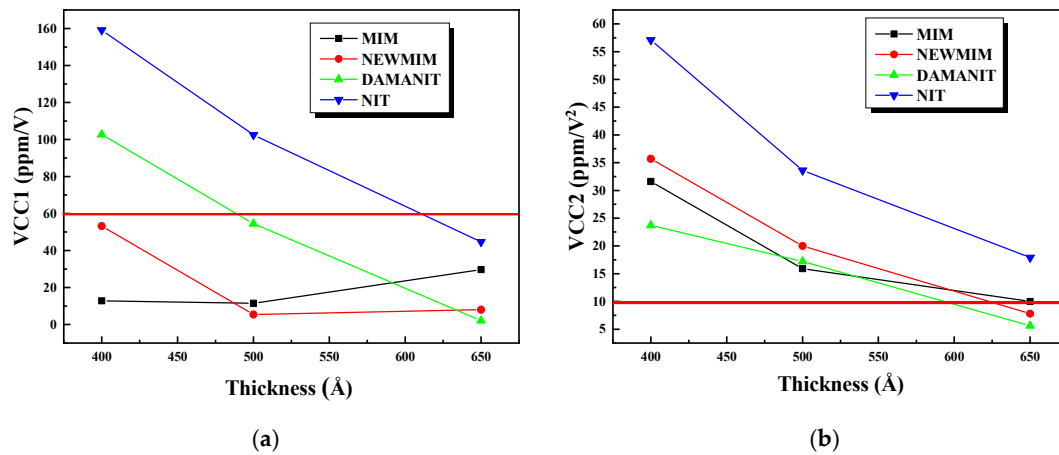


Figure 6. Graphs of (a) VCC1 and (b) VCC2 vs. thickness with Si_3N_4 conditions.

The TCC serves as an indicator of the degree of change in capacitance in response to temperature variations. Unlike the VCC, the TCC exhibits a linear relationship with temperature. Therefore, when the temperature is plotted on the X-axis and the normalized ΔC on the Y-axis, the slope value corresponds to the TCC value.

As an illustration, a TCC graph for Si_3N_4 films fabricated with the NEWMIM condition at thicknesses of 650, 500, and 400 Å is presented in Figure 7. Additionally, the results for the other conditions are presented to depict the variation in the TCC values according to thickness in Figure 8. Except for the NIT condition, the remaining conditions exhibited values below 50 ppm/dT, even as the thickness decreased. Moreover, the TCC values varied according to the condition at identical thicknesses.

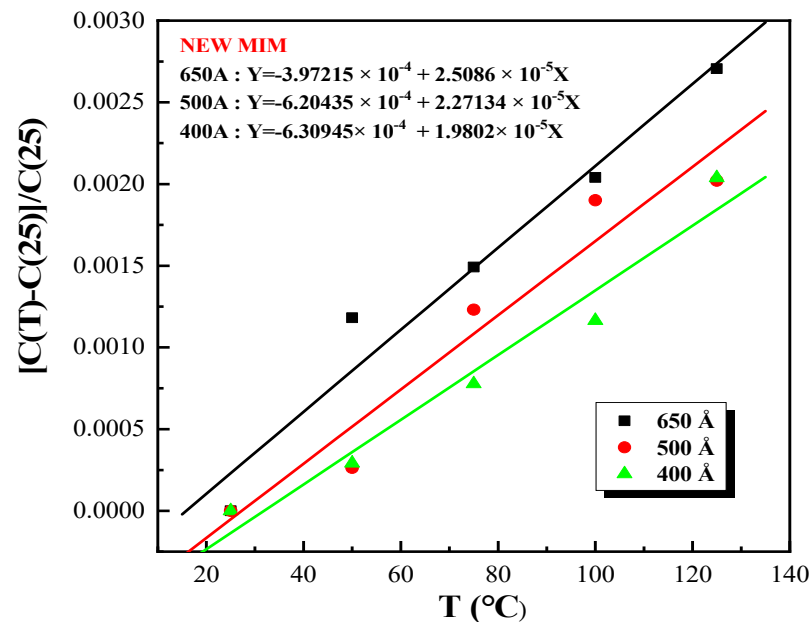


Figure 7. The TCC graph for Si_3N_4 films fabricated with the NEWMIM condition at thicknesses of 650, 500, and 400 Å.

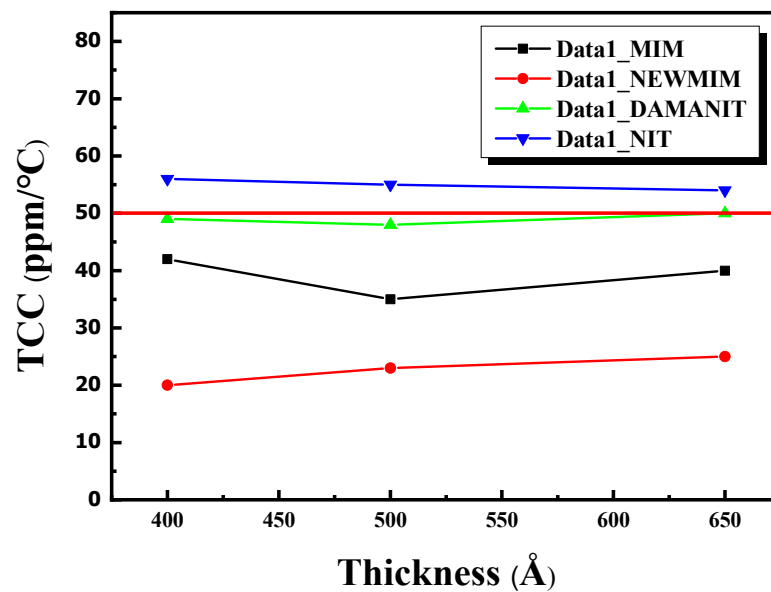


Figure 8. Graph of TCC1 vs. thickness with different Si_xN_y conditions.

As revealed by Table 4, the differences in Si_xN_y conditions are attributed to the N-H/Si-H ratio. To depict the changes in the TCC due to film quality, the N-H/Si-H vs. TCC values are plotted in Figure 9. The results indicate that as the N-H/Si-H ratio increased, the TCC values exhibited an exponential decay trend, confirming that the TCC values are influenced by the quality of the Si_xN_y film.

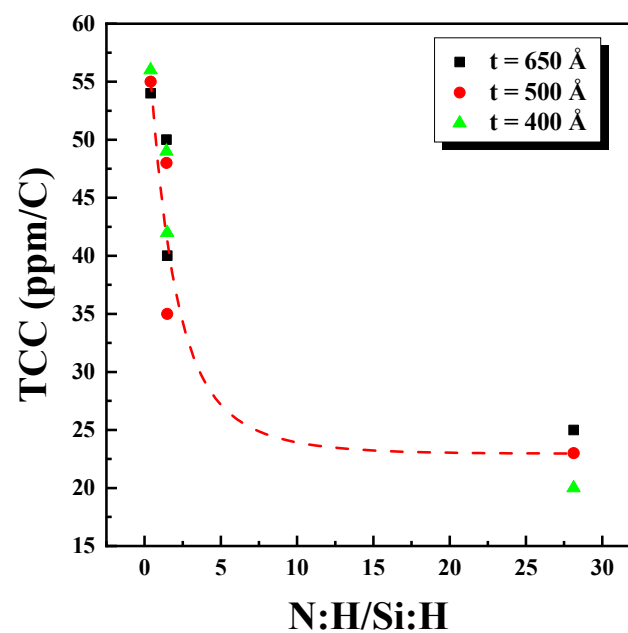


Figure 9. Graph of TCC vs. thickness with varying N:H/Si-H ratio.

4. Conclusions

An evaluation of the C-V characteristics was conducted for MIM capacitors based on the insulator (Si_xN_y) deposition thickness and deposition conditions. The CD values were in the ranges of 0.983–1.1, 1.24–1.4, and 1.57–1.79 $\text{fF}/\mu\text{m}^2$ for 650, 500, and 400 Å, respectively. Further, the CD increased as the thickness decreased, with variations across different conditions.

At the same thickness, the NIT condition exhibited the highest CD, while the MIM condition showed the lowest. This discrepancy is attributed to the effect of the actual thickness

and the difference in the k -value of the Si_xN_y film according to the condition. Additionally, the CD was observed to decrease with increasing capacitor size, possibly due to the influence of fringe capacitance, which increased in proportion to the perimeter/area ratio.

The thickness uniformity of Si_xN_y was found to be the most significant factor affecting capacitance uniformity. Improvements in thickness uniformity can enhance C_p and C_{pk} on the device side. Across all conditions, a general increase was observed in the VCC as the thickness decreased, although there were some variations between conditions. However, the TCC showed no significant difference with thickness, indicating that the variations were mainly due to the conditions.

In summary, from the perspective of C–V analysis, all conditions, except NIT, demonstrated superior characteristics. Implementing thin Si_xN_y film depositions with stable uniformity using conditions other than NIT could potentially provide MIM capacitors with CD values of less than 100 ppm/dV², aiming for the achievement of 2 fF/ μm^2 .

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Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

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References

- Xiong, L.; Hu, J.; Yang, Z.; Li, X.; Zhang, H.; Zhang, G. Dielectric Properties Investigation of Metal–Insulator–Metal (MIM) Capacitors. *Molecules* **2022**, *27*, 3951. [\[CrossRef\]](#) [\[PubMed\]](#)
- Karthik, R.; Manjusha, K.A. Metal Insulator Metal Capacitors-State of the Art. *J. Comput. Theor. Nanosci.* **2018**, *15*, 2346–2349. [\[CrossRef\]](#)
- Ding, S.-J.; Hu, H.; Zhu, C.; Kim, S.J.; Yu, X.; Li, M.-F.; Cho, B.J.; Chan, D.S.H.; Yu, M.B.; Rustagi, S.C.; et al. RF, DC, and reliability characteristics of ALD HfO_2 - Al_2O_3 laminate MIM capacitors for Si RF IC applications. *IEEE Trans. Electron Devices* **2004**, *51*, 886–894. [\[CrossRef\]](#)
- Choi, E.; Kim, A.; Kwon, S.H.; Pyo, S.G. Effect of Interface Treatment on the Voltage Linearity in 8 fF/ μm^2 High- k Dielectric and Combination Stacks on Metal Insulator Metal (MIM) Capacitor. *Sci. Adv. Mater.* **2018**, *10*, 467–470. [\[CrossRef\]](#)
- Hoa, P.T. High-K Dielectrics in Metal Insulator Metal (MIM) Capacitors for RF Applications. Ph.D. Thesis, National University of Singapore, Singapore, 2011.
- Pavunny, S.P.; Misra, P.; Scott, J.F.; Katiyar, R.S. Advanced high- k dielectric amorphous LaGdO_3 based high density metal-insulator-metal capacitors with sub-nanometer capacitance equivalent thickness. *Appl. Phys. Lett.* **2013**, *102*, 252905. [\[CrossRef\]](#)
- Ding, S.-J.; Hu, H.; Lim, H.; Kim, S.; Yu, X.; Zhu, C.; Li, M.; Cho, B.J.; Chan, D.S.; Rustagi, S.C. High-performance MIM capacitor using ALD high- k HfO_2 - Al_2O_3 laminate dielectrics. *IEEE Electron Device Lett.* **2003**, *24*, 730–732. [\[CrossRef\]](#)
- Sul, W.S.; Pyo, S.G. RF Characteristic Analysis Model Extraction on the Stacked Metal–Insulator–Metal Capacitors for Radio Frequency Applications. *IEEE Trans. Electron Devices* **2014**, *61*, 3011–3013. [\[CrossRef\]](#)
- Mu, J.; Chou, X.; Ma, Z.; He, J.; Xiong, J. High-Performance MIM Capacitors for a Secondary Power Supply Application. *Micromachines* **2018**, *9*, 69. [\[CrossRef\]](#)
- Li, W.; Lu, X.; Yang, R.; Liang, F.; Chen, W.; Xie, Z.; Zheng, J.; Zhu, J.; Huang, Y.; Yue, W.; et al. Highly sensitive and reproducible SERS substrates with binary colloidal crystals (bCCs) based on MIM structures. *Appl. Surf. Sci.* **2022**, *597*, 153654. [\[CrossRef\]](#)
- Jeon, S.; Sung, S.-K.; Jang, E.-H.; Jeong, J.; Surabhi, S.; Choi, J.-H.; Jeong, J.-R. Multilayer metal-oxide-metal nanopatterns via nanoimprint and strip-off for multispectral resonance. *Appl. Surf. Sci.* **2018**, *428*, 280–288. [\[CrossRef\]](#)
- Smitha, P.S.; Babu, V.S.; Shiny, G. Critical parameters of high performance metal-insulator-metal nanocapacitors: A review. *Mater. Res. Express* **2019**, *6*, 122003. [\[CrossRef\]](#)
- Sejas-García, S.C.; Torres-Torres, R.; Valderrama-B, R.; Molina, J. Complex Permittivity Determination of Thin-Films through RF-Measurements of a MIM Capacitor. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 805–807. [\[CrossRef\]](#)

14. Nam, M.; Kim, A.; Kang, K.; Choi, E.; Kwon, S.H.; Lee, S.J.; Pyo, S.G. Characterization of atomic layer deposited $\text{Al}_2\text{O}_3/\text{HfO}_2$ and $\text{Ta}_2\text{O}_5/\text{Al}_2\text{O}_3$ combination stacks. *Sci. Adv. Mater.* **2016**, *8*, 1958–1962. [\[CrossRef\]](#)
15. Jin Chung, J.; Hyuk Kim, T.; Ahsan Saeed, M.; Won Shim, J. Laminated indium-oxide/molybdenum-oxide nanocomposites for high-work-function electrodes in organic photovoltaics and capacitor devices. *Appl. Surf. Sci.* **2023**, *610*, 155526. [\[CrossRef\]](#)
16. Guo, Y.; Wang, S.; Du, X.; Liang, S.; Huang, S.; Peng, S.; Xie, Y.; Ma, M.; Xiong, L. Construction of ultrahigh capacity density carbon nanotube based MIM capacitor. *Energy Storage Mater.* **2023**, *63*, 103064. [\[CrossRef\]](#)
17. Ruhl, G.; Lehnert, W.; Lukosius, M.; Wenger, C.; Baristiran Kaynak, C.; Blomberg, T.; Haukka, S.; Baumann, P.K.; Besling, W.; Roest, A.; et al. Dielectric Material Options for Integrated Capacitors. *ECS J. Solid State Sci. Technol.* **2014**, *3*, N120–N125. [\[CrossRef\]](#)
18. Zheng, G.; He, Y.L.; Zhu, B.; Wu, X.; Zhang, D.W.; Ding, S.J. Improvement of Voltage Linearity and Leakage Current of MIM Capacitors With Atomic Layer Deposited Ti-Doped ZrO_2 Insulators. *IEEE Trans. Electron Devices* **2023**, *70*, 3064–3070. [\[CrossRef\]](#)
19. Park, Y.S.; Cho, S.-J.; Boo, J.-H.; Hong, B. Surface and electrical properties of organic–inorganic hybrid structure as gate insulator to organic thin film transistor. *Appl. Surf. Sci.* **2009**, *256*, 1023–1027. [\[CrossRef\]](#)
20. Wu, Y.-H.; Kao, C.-K.; Chen, B.-Y.; Lin, Y.-S.; Li, M.-Y.; Wu, H.-C. High density metal-insulator-metal capacitor based on $\text{ZrO}_2/\text{Al}_2\text{O}_3/\text{ZrO}_2$ laminate dielectric. *Appl. Phys. Lett.* **2008**, *93*, 033511. [\[CrossRef\]](#)
21. Xu, T.; Tekes, C.; Degertekin, F.L. CMUTs with high-K atomic layer deposition dielectric material insulation layer. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.* **2014**, *61*, 2121–2131. [\[CrossRef\]](#)
22. Sudheendran, K.; Pamu, D.; Ghanashyam Krishna, M.; James Raju, K.C. Determination of dielectric constant and loss of high-K thin films in the microwave frequencies. *Measurement* **2010**, *43*, 556–562. [\[CrossRef\]](#)
23. Holden, K.E.K.; Hall, G.D.R.; Cook, M.; Kendrick, C.; Pabst, K.; Greenwood, B.; Daugherty, R.; Gambino, J.P.; Allman, D.D.J. Dielectric Relaxation, Aging and Recovery in High-K MIM Capacitors. In Proceedings of the 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 21–25 March 2021; pp. 1–10.
24. Zhao, C.; Zhao, C.Z.; Werner, M.; Taylor, S.; Chalker, P. Dielectric relaxation of high-k oxides. *Nanoscale Res. Lett.* **2013**, *8*, 456. [\[CrossRef\]](#)
25. Ohshima, I.; Cheng, W.; Ono, Y.; Higuchi, M.; Hirayama, M.; Teramoto, A.; Sugawa, S.; Ohmi, T. Reliability of silicon nitride gate dielectrics grown at 400 °C formed by microwave-excited high-density plasma. *Appl. Surf. Sci.* **2003**, *216*, 246–251. [\[CrossRef\]](#)
26. Ma, T.P. Gate dielectric properties of silicon nitride films formed by jet vapor deposition. *Appl. Surf. Sci.* **1997**, *117–118*, 259–267. [\[CrossRef\]](#)
27. Yu, H.Y.; Li, M.F.; Kwong, D.L. ALD $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ high-k gate dielectrics for advanced MOS devices application. *Thin Solid Films* **2004**, *462–463*, 110–113. [\[CrossRef\]](#)
28. Lue, H.T.; Lai, S.C.; Hsu, T.H.; Du, P.Y.; Wang, S.Y.; Hsieh, K.Y.; Liu, R.; Lu, C.Y. Understanding barrier engineered charge-trapping NAND flash devices with and without high-K dielectric. In Proceedings of the 2009 IEEE International Reliability Physics Symposium, Montreal, QC, Canada, 26–30 April 2009; pp. 874–882.
29. Cockbain, A.G.; Harrop, P.J. The temperature coefficient of capacitance. *J. Phys. D Appl. Phys.* **1968**, *1*, 1109. [\[CrossRef\]](#)
30. Khaldi, O.; Jomni, F.; Gonon, P.; Mannequin, C.; Yangui, B. Investigation of electrical properties of HfO_2 metal–insulator–metal (MIM) devices. *Appl. Phys. A* **2014**, *116*, 1647–1653. [\[CrossRef\]](#)
31. Lee, A.J.; Kim, B.S.; Hwang, J.H.; Kim, Y.; Oh, H.; Park, Y.; Jeon, W. Controlling the crystallinity of HfO_2 thin film using the surface energy-driven phase stabilization and template effect. *Appl. Surf. Sci.* **2022**, *590*, 153082. [\[CrossRef\]](#)
32. Li, H.; Yun, H.; Liang, W.; Dong, A.; Miao, M.; Sundaram, K.B. Characterization of Dielectric Breakdown and Lifetime Analysis for Silicon Nitride Metal-Insulator-Metal Capacitors under Electrostatic Discharge Stresses. In Proceedings of the 2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 16–19 July 2018; pp. 1–5.
33. Kim, K.H.; Kim, K.S.; Ji, Y.J.; Kang, J.E.; Yeom, G.Y. Silicon nitride deposited by laser assisted plasma enhanced chemical vapor deposition for next generation organic electronic devices. *Appl. Surf. Sci.* **2021**, *541*, 148313. [\[CrossRef\]](#)
34. Yota, J. Effects of Deposition Method of PECVD Silicon Nitride as MIM Capacitor Dielectric for GaAs HBT Technology. *ECS Trans.* **2011**, *35*, 229. [\[CrossRef\]](#)
35. Iversen, C.-R. A high density MIM capacitor in a standard CMOS process. *JSTS J. Semicond. Technol. Sci.* **2001**, *1*, 189–192.
36. Bertaud, T.; Bermond, C.; Blonkowski, S.; Vallee, C.; Lacrevez, T.; Farcy, A.; Gros-Jean, M.; Flechet, B. Electrical Characterization of Advanced MIM Capacitors With ZrO_2 Insulator for High-Density Packaging and RF Applications. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2012**, *2*, 502–509. [\[CrossRef\]](#)
37. Sharp, K.A.; Honig, B. Electrostatic Interactions in Macromolecules: Theory and Applications. *Annu. Rev. Biophys.* **1990**, *19*, 301–332. [\[CrossRef\]](#)
38. Kittel, C. *Introduction to Solid State Physics*; Wiley: Hoboken, NJ, USA, 2004.
39. Kim, S.J.; Cho, B.J.; Li, M.-F.; Ding, S.-J.; Zhu, C.; Yu, M.B.; Narayanan, B.; Chin, A.; Kwong, D.-L. Improvement of voltage linearity in high- κ MIM capacitors using HfO_2 - SiO_2 stacked dielectric. *IEEE Electron Device Lett.* **2004**, *25*, 538–540. [\[CrossRef\]](#)

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