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A comprehensive review of multi-level inverters, modulation, and control for grid-interfaced solar PV systems

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With the significant development in photovoltaic (PV) systems, focus has been placed on inexpensive, efficient, and innovative power converter solutions, leading to a high diversity within power converters and new system configurations for grid-connected PV (GCPV) systems. During the last decade, multilevel inverter (MLI) designs have gained popularity in GCPV applications. This article provides a wide-ranging investigation of the common MLI topology in contrast to other existing MLI topologies for PV applications. Furthermore, the various modulation techniques used in MLI switching are elucidated and contrasted. The modulation strategies are reviewed with particular regard to their comparative suitability for the modulation of MLIs for PV applications. This article also provides a comparative analysis of available MLI control techniques and controllers for GCPV applications in recent times.

In recent times, the effective utilization of alternative energy sources, like solar, hydro, wind, and biogas energy, has seen a significant upsurge in fulfilling the growing energy requirements and mitigating the environmental impact associated with conventional energy generation. Solar energy, abundant and environmentally friendly, has been effectively used in both independent and grid-connected applications, establishing it as one of the top choices among renewable energy sources (RES). With more research being done on PV energy production methods and the price of PV panels going down, solar energy can be used for useful things like lighting and warmth that are driven by the sun, solar power plants that are tied to the grid, and home uses. Solar energy has had a notable increase in usage for power generation in off-grid and grid-connected industrial and residential sectors in recent[1–3]. Increases in electricity demand, technological advancements, a more favorable policy and regulatory framework, and growing environmental concerns have all contributed to a dramatic increase in PV's use for low-cost electricity generation in the past decade[4]. Whether PV is used in an islanding or grid-connected configuration, it has become an area of interest for academic research.

A power converter is crucial in the process of solar PV power conversion since it converts power generated from PV system into the required form. The PV system generates output in terms of DC voltage, which is intrinsically unstable and and may result in power quality issues. These concerns include voltage surges, flickers, sags and swells, outages, frequency deviations, unbalanced dc-link voltages, low power factor and electrical noise in its electricity generation PV applications[5–7]. These power quality problems troublesome for the operation of many sensitive types of equipment and other electric loads so need to be compensated and kept as per grid standards. To minimize the current and voltage harmonics generally shunt passive tuned LC filters, active power and high pass filters are utilized while power capacitors are deployed to improve the system's power factor. However, these conventional approaches have the drawbacks of fixed compensation, high cost, size, complexity and and the potential to induce resonance phenomena.

Efficient power electronic converters are necessary to address these power quality challenges[8]. Conventional two-level inverters have many drawbacks, including higher THD, significant switching losses, and high voltage stress on semiconductor switches within inverter. As a consequence, they are primarily utilized in medium power and low-voltage grid-connected applications. The existence of these disadvantages led to the development of the MLI idea[9,10].

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MLI firstly came into existence in 1975 and found suitable in high voltage utility grid. The so-called "Multilevel" begins with a three-level structure. The primary objective of the MLI general structure is to produce a sinusoidal output voltage by utilizing various voltage levels, often derived from capacitor voltages. The MLI can synthesize the higher output voltage even by employing the power devices of lower voltage rating. Furthermore, MLI structures enable the achievement of higher voltages while minimizing harmonic distortion, all without the need for transformers[11,12]. The multilevel waveform requires less passive filters. In comparison to a simple two-level inverter, MLI topologies have become popular because of their enhanced functionality, increased voltage tolerance, reduced voltage stress on the switches, practically sinusoidal voltage output form, and better harmonic spectra[10,13–15]. Hence, multilevel inverter (MLI) designs have gained popularity for GCPV applications during the last decade. In addition to conventional topologies some new and different MLI topologies such as hybrid, RDC, T-type, active-NPC, asymmetric and modular MLI can also use for grid-integrated PV applications[14,16–18]. In recent hybrid and RDC-MLIs are designed with a minimal number of elements, modular structure, high fault tolerance ability and transformer-less operation as well as non-initialization of the capacitor voltages that makes suits for HPFC and other custom PV power applications[19–22].

However, with the use of MLI there are some limitations like requirement of large no. of switching devices and complex switching strategies which are present in popular traditional topologies such as NPC or diode clamped, CHB, and FC that results in reduce reliability and sometime stability problems in grid- integrated applications. To address these problems, control mechanisms and measures are required for it when it is used with grid-integrated PV applications. Many developed control techniques by the researchers in recent times are compared[23–36]. Choosing the right triggering of semiconductor switches is an integral part of the MLI's process, It intends to produce an output voltage waveform with a sinusoidal shape across multiple stages. So suitable modulation schemes are required for efficient operation of MLI and keeping power quality of injected current and voltage as per grid standards and thus the study of modulation techniques becomes very important for researchers[16,37–39]. Many modulation techniques used for grid-integrated operation of PV are available in literatures. SVM, PWM, and SHE frequently used modulation approaches[26,37,40–47]. A comparison of available modulation techniques for PV applications perspective is also discussed in the present work.

This article provides novel contributions by giving a wide-ranging investigation of the common MLI topology in contrast to other existing Hybrid and RDC MLI topologies, particularly for PV applications. This article also provides a comparative analysis of recently published modulation strategies, MLI control techniques and controllers for GCPV applications. So, with the help of this study and by choosing a suitable MLI, modulation strategy and control approach can address several issues in GCPV systems.

Multilevel inverter (MLI) topologies for GCPV application

MLI topologies have gained popularity in the last decade and their adaptation in the GCPV operations are gradually increasing. MLI synthesize a sinusoidal voltage by using a no. of voltages level and results in a staircase waveform that approaches the sinusoidal waveform with least THD. Fundamentally, the synthesized output is dividing by splitting the dc-link voltage into a number of sections, with the purpose of every inverter phase leg may switch between several voltage levels. The MLI can synthesize the higher voltage even by employing the power devices of lower voltage ratings. MLI topologies have gained popularity in the power sector because to their favorable characteristics, such as increased voltage handling capacity, virtually perfect output voltage waveform with improved harmonic spectra, and reduced stress on switches in terms of $\frac{dV}{dt}$.

MLI topologies may be categorized according to factors such as modularity, structure, complexity, switches used, cost factor, level generation, switching losses, and total voltage blocking capability. However, in this study the MLI classification has been established on the quantity and configuration of used DC sources (PV) and their arrangements for the grid-integrated operations[16].

The NPC, CHB and FC are the commonly used MLI topologies for grid-tied PV applications. Also some new and different MLI topologies such as hybrid, RDC, T-type, and active NPC, asymmetric and modular MLI for this type of applications is developed recently[48]. This detailed classification is presented in Fig. 1.

Because of its compact size, modular design, few parts compared to other classical topologies, and ability to achieve high or medium power levels with low voltage rated switches, The CHB architecture is widely recognized as the most favored MLI configuration for GCPV systems[49]. Even though there exist many different MLI topologies, in this section only conventional important topologies NPC, FC, CHB along with T-type, active-NPC and hybrid MLI are explained in detail.

Neutral point clamped (NPC)-MLI

It is recognized as a first actual MLI which has been proposed in 1980's is the foundation of new MLI topologies. To achieve an infinite range of output voltage levels, this MLI is powered by only a single dc source (PV). This topology utilises clamping diodes and hence termed as DC-MLI[48]. The diodes that are linked across the dc-link capacitors are known as clamping diodes[9]. The neutral point is located in the center of the DC bus. The clamping diodes ensure that the switches can handle a maximum blocking voltage, which is equivalent to the voltage across one capacitor ($V_{dc}/4$), under steady circumstances. Due to the presence of symmetry, only one inverter leg of a three-phase five-level NPC-MLI for GCPV application is displayed in Fig. 2(a).

The five-level NPC-MLI is having eight switches (T_1, T_2,…T_8) and four dc-link capacitors. The total dc voltage (V_{dc}) is generally obtained from used RES with boost converter configuration. The switches (T_1, T_2, T_3*and* T_4) are utilized to get positive levels ($\frac{V_{dc}}{4}$, $\frac{V_{dc}}{2}$) in output voltage. Conversely, the (T_5, T_6, T_7*&* T_8) switches are used to acquire negative levels ($-\frac{V_{dc}}{4}$, $-\frac{V_{dc}}{2}$). The (T_3, T_4, T_5*and* T_6) switches are switched on to get the zero-voltage level. This topology is useful for three and five level MLI operation as its arrangement is simple, more efficient, requires simple control scheme and also it is having the advantage of using only single voltage source to get numerous voltage levels and lower THD output voltage waveform is attained that results in less use of bulky

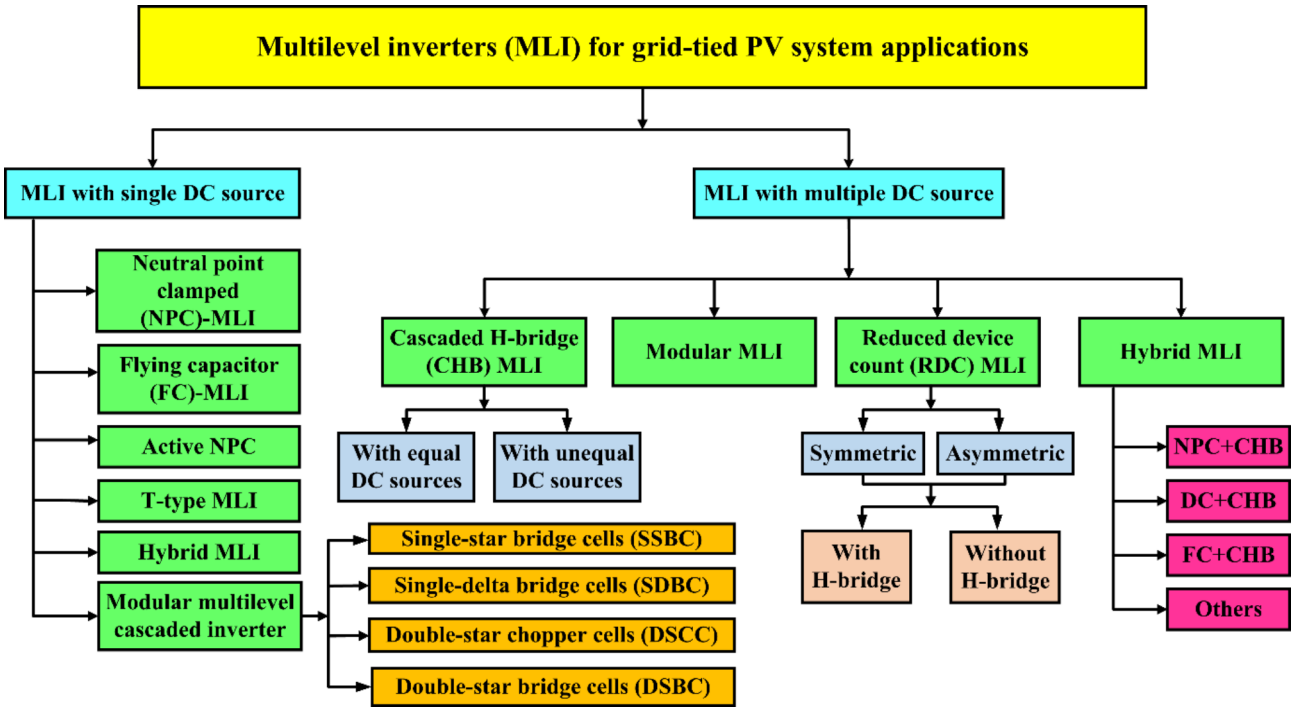

Fig. 1. MLI categorization according to the quantity of DC sources utilized.

filters. The NPC-MLI founds it application in medium voltage industrial drive and low frequency applications. However, NPC-MLI having some major drawbacks that makes this topology unattractive for higher voltage levels like necessity of large no. of dc-link capacitors and clamping diodes, different reverse voltage blocking for clamping diodes, difficulty in balancing of dc-link capacitors and lack in modularity.

Flying capacitor (FC)-MLI

This structure comes into existence in the year of 1992. FC-MLI topology is quite alike to DC-MLI; instead of using clamping diodes, floating capacitors are used as the only distinction. FC-MLI has a switching robustness within a phase, which may be used to equalize the FC voltages and evenly distribute the losses incurred during switching and conduction of switches[46,47]. The circuit configuration of a five-level FCMLC for GCPV application is shown in Fig. 2 (b).

This MLI employs a single dc source (RES) to achieve a multitude of voltage levels in the output. This structure having several advantages like modularity in structure, huge number of capacitors enhances the ride-through capabilities in the event of a power interruption, the switching state redundancy provides more flexibility for the design of the switching pattern and natural balancing of capacitor voltages. However, for having some disadvantages of requirement of many bulky storage capacitors for high voltage levels, difficult to package, more expensive, complex control circuitry and capacitors voltages have to be pre-charged at start up to a value, which are close to their nominal values.

Cascaded H-Bridge (CHB)-MLI

The CHB configuration is the most favored option for high and medium voltage PV applications among all MLI configurations. This structure showed up first in 1988, developed during the 1990s and increased more consideration after 1997[48]. The construction of this system relies on connecting in series a specific number of isolated DC power supplies with single-phase H-bridge inverters. The system comprises of $2(m-1)$ & $\frac{m-1}{2}$ power switches and dc voltage sources (PV) respectively to achieve an output waveform with 'm' voltage levels. The number of levels, represented as 'm', is directly related to the number of isolated HBC, according to formula ($m = 2n + 1$). Compared to NPC and FC MLI, this architecture requires fewer components due to the absence of capacitors and clamped diodes.

Figure 2 (c) illustrates a GC PV application using a single-phase five-level CHB-MLI. As displayed in diagram CHB-MLI consists of two isolated PV sources, which are connected to individual HBC through individual dc-links. Through the use of these two HBC output voltages, it is possible to accomplish the desired output voltage, hence makes it more suitable and flexible for any type of RES. Its compact and modular structure for any number of voltage level also makes it use more preferable in high power transformer less industrial applications. The simplicity and flexibility in inverter design of this topology allow for easy expansion to higher levels. However, the deployment of this structure is constrained in certain scenarios because of the necessity for numerous separate DC sources.

Multiple voltage source CHB-MLI depending upon the equality of dc sources classified as:

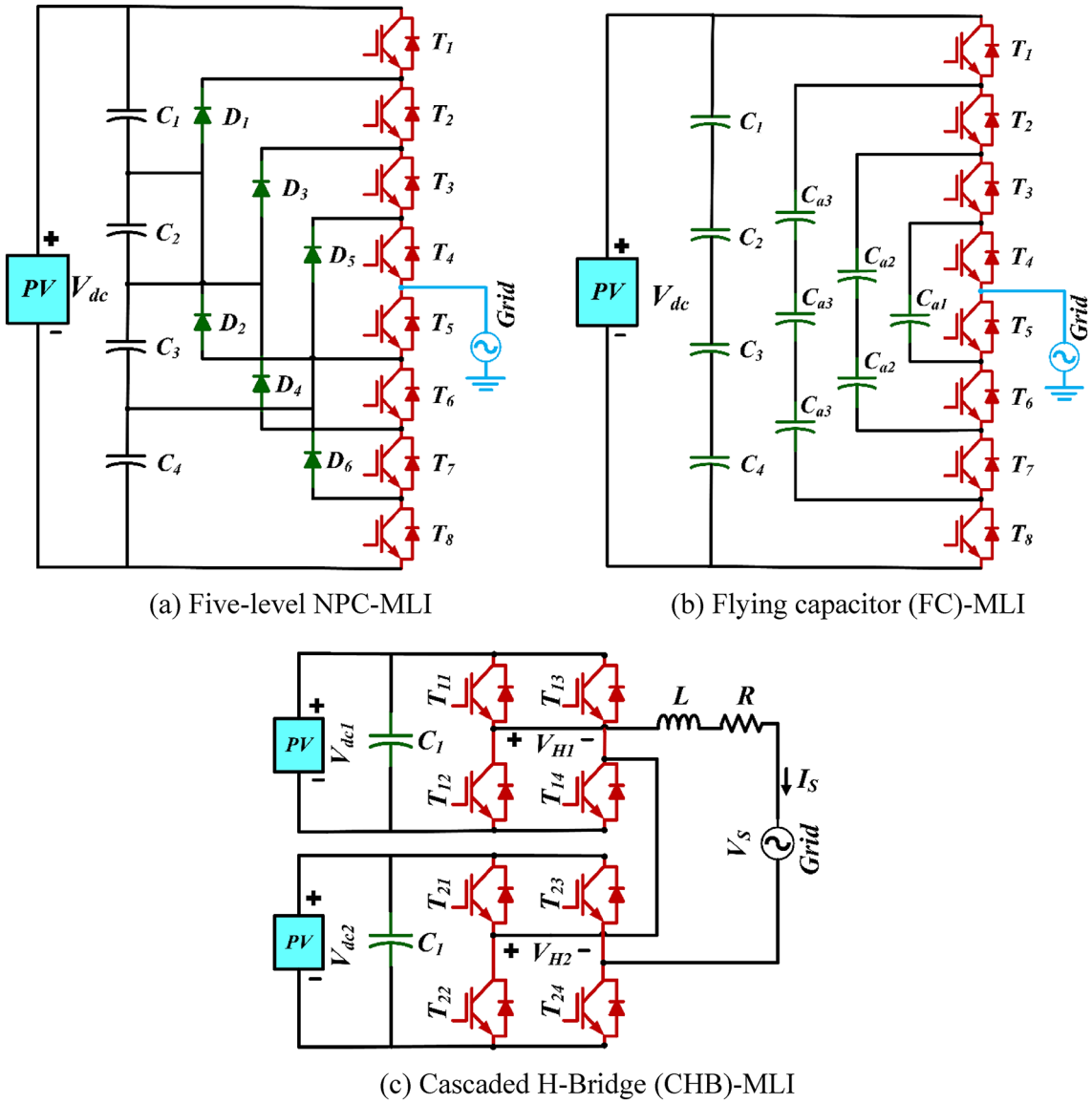

Fig. 2. Conventional MLI Topologies.

1. Symmetric CHB-MLI or CHB-MLI with equal dc sources
2. Asymmetric CHB-MLI or CHB-MLI with unequal dc sources

(a) ***CHB-MLI with equal dc sources***.

As the name suggests, CHB-MLI is characterized as symmetric or unary considering isolated DC sources have identical voltage levels. In Fig. 2 (c) if the values of voltages V_{dc1} and V_{dc2} obtained from respective isolated PV arrays are equal it is called as symmetric CHB-MLI with multiple dc source. This configuration found very few utilization or implementation for energy conversion in grid-tied RES applications. As it is not compulsory that environmental conditions and nature of source for a particular PV array remain to be same. However, if identical similar rating PV under similar environmental conditions are assumed for each HBC, the issue of balancing the dc-link capacitors is not present in this particular configuration.

(b) ***CHB-MLI with unequal dc sources***.

The multiple dc source voltages obtained from respective PV in the previous section are identical in nature. However, in actual, the environmental conditions like solar irradiation may be different. In PV system, this variation in solar irradiation conditions may be due to presence of partial shading, PV panel rating mismatching, cell fractures, dust and soiling, bubble formation, corrosion, bond deterioration, and variations in ambient variables including temperature and pressure. Because of these conditions, different voltages are obtained from used PV arrays, and supplied to respective individual connected HBC of used CHB-MLI. Hence, the voltage

values are unequal for MLI in nature. For example in Fig. 2 (c) if the values of voltages V_{dc1} and V_{dc2} are not equal, CHB-MLI in this type of application called as asymmetric inverter. The structure is displayed in Fig. 2 (c) which is made up of two single-phase HBCs linked in series. This configuration is capable of producing five output voltage levels. However, by using two distinct switching patterns that correspond to various combinations of the HBC output voltages, the same topology may create seven output voltage levels. By appropriately regulating the switches of each HBC, it is possible to get an output voltage with seven distinct values. However, if unequal voltage rating isolated PV are assumed for multiple HBC, the issue of dc-link capacitor balancing is present in this type of structure. In addition, modularity in structure lost, switching scheme becomes difficult and also the power quality control by using control techniques becomes complex. As a result, used for limited industrial applications. Hence, these above stated problems are need to be deal in an efficient way for the proper utilization of such type of MLI in distinct applications.

Hybrid-MLI

Recently, many combinations of various distinct MLI topologies have been designed by extracting their advantages, resulting in growth of new and more efficient structures of MLI topologies called hybrid MLI. Although these hybrid MLIs having various advantages, but some drawbacks like control complexity and less modular structure are also evident. Some examples of hybrid MLI topologies are reported in[16,17,33,50–57]. The suggested MLI shown in Fig. 3(a)[58] integrates a T-Type inverter with an H-Bridge module composed of sub-switches. This study includes the design and modeling of the proposed RDC-MLI utilizing the staircase PWM technique, which was evaluated with various combinations of loads and showed stability under nonlinear loads, making it very appropriate for FACTS and GC-MLI applications. Also, Fig. 3 (b) and (c) show two hybrid-MLI topologies.

Active NPC-MLI

NPC is a conventional and well known MLI topology for RES applications. However, it has voltage unbalance problem among the capacitors and additional hardware is required for voltage balancing. Another issue with NPC is that semiconductor devices have an uneven distribution of losses[59]. To keep equal distribution the active-NPC is proposed and this topology serve as an alternative of NPC-MLI. Due to equal loss distribution among switches, this MLI topology is very attractive in PV applications. However, this topology requires passive filters to keep harmonic content in output within prescribed limits. Figure 3(d) displays a five-level ANPC-MLI for GCPV. A 9-level RDC ANPC MLI is proposed in[60] which is an upgrade to the conventional 5-level ANPC MLI.

T-Type-MLI

This MLI consists of a T-type leg and a standard two-level leg. Figure 3(e) represents the circuit of a a grid-connected RES application using a single-phase five-level transformer-less T-type MLI[61]. The T_1 and T_3 switches on each leg of a T-type MLI are linked to dc-link at leg's midpoint via a bidirectional switch. This topology is asymmetrical in nature.

Modular cascaded-MLI

The single-phase modular cascaded MLI for grid-connected RES[62,63] is represented in Fig. 3 (f). The MLI comprises several sub-modules (SM). All of SMs are equivalent to half-bridges, and they are all linked to the RES. It also consists of an inductor and a resistor in both arms of inverter. This MLI is most suitable for high voltage applications.

Reduced device count (RDC) -MLI

For RES[22], presents RDC-MLI topology as shown in Fig. 3(g). With the use of 10 power switches, this layout can effectively control a total of 25 voltage levels from two separate DC sources. Furthermore, this topology is used to suggest two generalized MLI setups that provide more design flexibility. The lower component count compared to other existing MLI topologies is an advantage of the proposed technique. An enhanced asymmetrical MLI featuring 15 output voltage levels is shown in Fig. 3(h)[64]. The topology features fewer switches, is cost-effective, and improved reliability compared to newly introduced topologies with same voltage levels. Three distinct extensions of the proposed circuit also presented. For solar PV power conversion systems, the research in[65] suggests a new MLI topology called Dual-Source MLI (DSMLI) that uses fewer power switches shown in Fig. 3(i). No cascade is necessary for its operation in either symmetric or asymmetric modes. Consequently, fewer switching components are needed to generate multiple levels of the voltage waveform for the staircase. To drive high voltage levels with few switches in tandem with traditional topologies[66], presents a novel asymmetric operating structure in Fig. 3(j). 10 distinct algorithms for calculating voltage magnitude are evaluated for their efficacy, and a multicarrier PWM approach controls the complexity of the suggested topology. A novel transformer-less step-up switched capacitor topology is presented in Fig. 3(k)[67]. This topology employs twelve switches to generate nine distinct voltage levels. Most notably, the suggested topology has zero leakage current, boost capability, lower voltage stressors, and the fewest switching components. Also, there's no need for an additional circuit to accomplish capacitor self-balancing because the capacitors already have such qualities. Some other RDC-MLI topologies are documented in[68–71].

Comparative evaluation of MLI

The choice of individual inverter topologies as a HPFC in PV applications depends on their performance, cost, size and implementation factors. Table 1 gives the comparison of power component required per phase-leg for the above-discussed MLI topologies. From Table 1, it is evident that the CHB-MLI demonstrates the lowest need for power components.

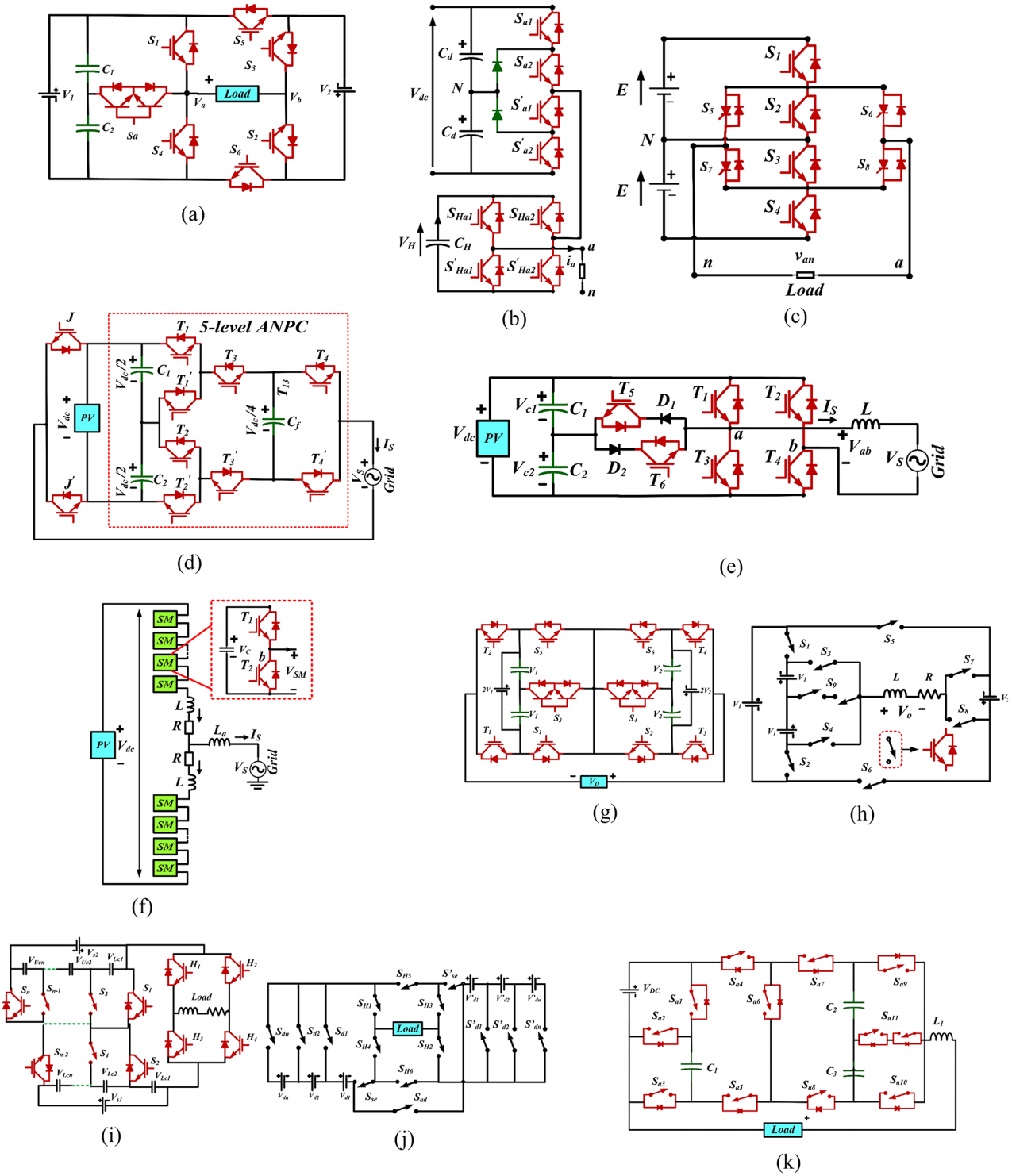

Fig. 3. (a) Hybrid T-Type inverter with an H-Bridge[58](b) NPC-HB hybrid MLI[56], Fig. 3(c) Symmetrical Hybrid MLI[57](e) Five-level transformer-less T-type MLI for grid-connected RES[61](d) Five-level ANPC-MLI for grid-connected RES[60](f) Single-phase modular cascaded MLI for grid-connected RES[62](g)-(k) RDC-MLI topologies[22,64–67].

Table 2 gives the MLI topologies comparison based on their implementation factors. Even though FC-MLI have a natural capacitor voltage balancing operation and modular structure, but its application as a HPFC and in PV applications is restricted owed to the necessity of a substantial quantity of capacitors and their initialization process (pre-charge). Alternatively, the CHB-MLI and DC-MLI topologies appears to be most appropriate for

MLI topology for (m-voltage levels)	Anti-parallel diodes	Main switches	DC-link capacitor	Clam-ping diodes	Isolated dc sources	Floating capacitors
DC-MLI [9]	*2(m-1)*	*2(m-1)*	*(m-1)*	*(m-1)× (m-2)*	*1*	*0*
FC-MLI [9]	*2(m-1)*	*2(m-1)*	*(m-1)*	*0*	*1*	*((m-1)× (m-2))/2*
Active–NPC [61]	*m/2*	*m/2*	*2*	*0*	*1*	*(m-3)/2*
T-type MLI [73]	*((m-1)× (m-2))/2*	*((m-1)× (m-2))/2*	*(m-3)*	*(m-3)*	*1*	*0*
CHB-MLI [21,74]	*2(m-1)*	*2(m-1)*	*(m-1)/2*	*0*	*(m-1)/2*	*0*
NPC-HB hybrid MLI [57]	*2(m-1)*	*2(m-1)*	*(m-1)/2*	*(m-1)/2*	*(m-1)/4*	*(m-1)/4*
Symmetrical Hybrid MLI [58]	*2(m-1)*	*2(m-1)*	*(m-1)/2*	*0*	*(m-1)/2*	*0*
Cascaded hybridized RDC-MLI [75]	*(m + 1)*	*(m + 1)*	*(m-1)/2*	*(m-1)*	*(m-1)/4*	*0*
Improved PWMSVS-MLI [76]	*M*	*m*	*0*	*m*	*(m-1)/2*	*(m-1)/4*

Table 1. Multilevel converter topologies for PV applications.

	Inverter topology				
Implementation factor	**DC-MLI**	**FC-MLI**	**CHB-MLI**	**Hybrid- MLI**	**ANPC-MLI**
Particular specifications	Clamping diodes	Floating capacitors	Isolated DC sources	Dependent on proposed topology	ANPC DC-Link capacitors
Modularity	Low	High	Very high	Low	Low
Complexity associated with the design and execution	Low	Medium	Least (with transformer-less applications)	High	High
DC source requirement	Single dc source	Single dc source	Single or multiple dc source	Single or multiple dc source	Single
Issues related to control	Voltage balancing	Voltage setup	Power sharing, voltage balancing	Power switching and voltage balancing	Active voltage balancing control
Fault tolerance	Difficult	Easy	Easy	Difficult	Easy
Cost	Low (3-level), High (>=4-level).	Medium (3 level), High (>=4 level).	Very low (transformer-less applications), High (with transformer applications).	Dependent upon proposed topology	Medium

Table 2. MLI topologies comparison based on their implementation factors.

HPFC in PV applications. However, the concerns of capacitor voltage unbalance at large number of levels is to be considered. DC-MLI requires a significant quantity of clamping diodes and dc-link capacitors.

The requirement of least number of components, high fault tolerance ability, modular structure and transformer-less operation as well as non-initialization of the capacitor voltages makes CHB-MLI suits for HPFC and other custom PV power applications. However, the unbalance of dc-link voltages must be considered while operated in PV applications. If the stability of the dc-link voltages is no longer guaranteed, a group of switching devices experiences a higher voltage across their terminals and extra distortion may also takes place in the injected voltages and currents. Therefore, the prime issue in devising the control schemes for CHB-MLI should be to minimize the harmonic content in injected grid current while simultaneously maintaining instantaneous dc-link capacitor voltage balancing.

Modulation techniques for grid-connected MLI

To produce a staircase-like output voltage with several levels, considerable quantity of power switches are necessary in a MLI. To minimize THD and power quality in output waveform, the duration and sequence to operate these switches plays very important role. So suitable modulation schemes are required for efficient operation of MLI and keeping power quality of injected voltage and current as per grid standards[16,37,38]. Many modulation strategies used for grid-integrate operation of MLI in RECS. The Fig. 4 shows the modulation techniques that are available in literatures.

The PWM, SVM and SHE are the most commonly used modulation techniques[37,40–43]. As the power dissipation across the switches is the main concern in MLI based high power grid-tied PV application, so to enhance the efficiency of MLI the multicarrier sinusoidal PWM schemes are primarily used. Here, the discussion is confide to only on the switching techniques, which are suitable for grid-connected CHB-MLI for PV applications.

Fundamental switching frequency modulation approaches

(a) Selective Harmonic Elimination (SHE):

SHE-PWM was developed to reduce lower order harmonics and minimize THD of inverter output voltage waveform. The output waveform was previously modified by adding unknown switching angles and zeroing them. Subsequently, the Fourier series method was used to depict output voltage waveform and eliminate the undesired harmonic elements, while maintaining fundamental component at the same level as reference

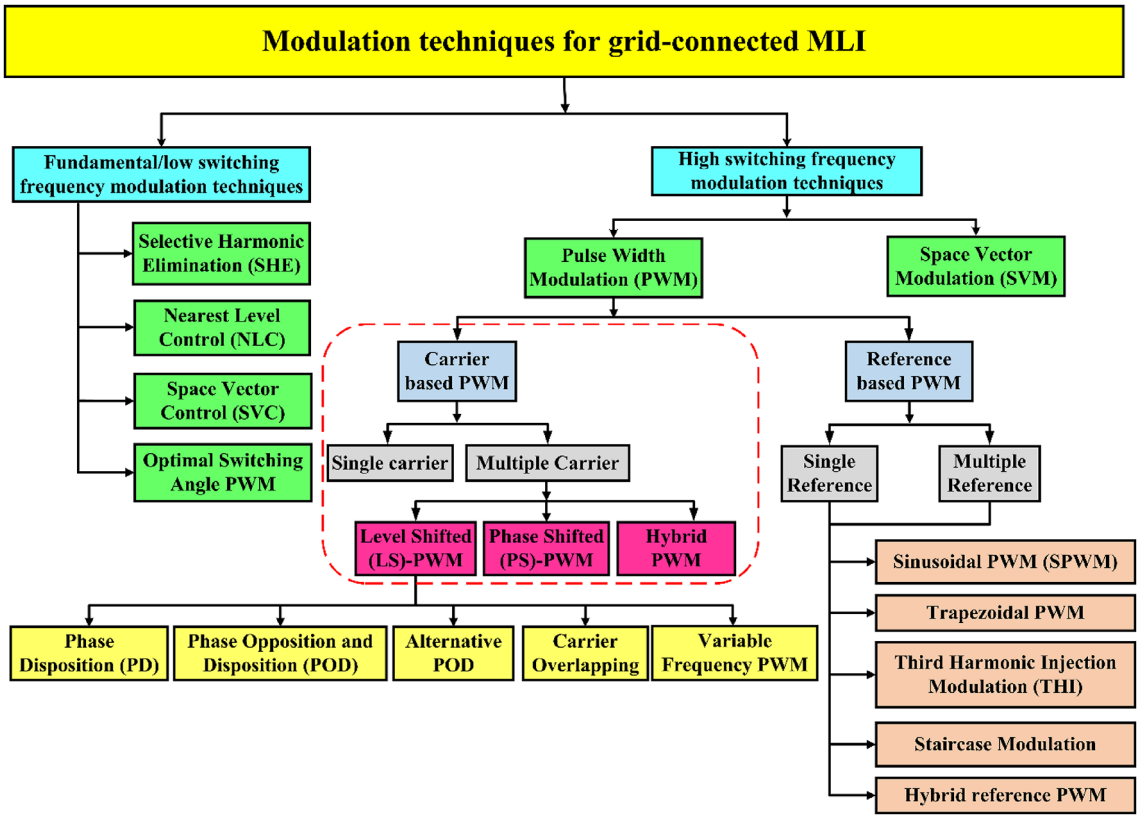

Fig. 4. Modulation techniques for grid-connected MLI.

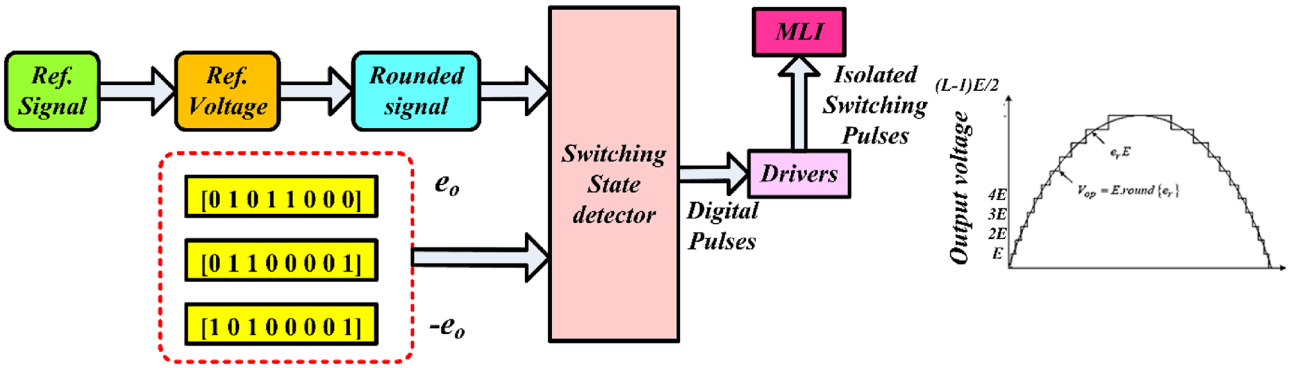

Fig. 5. Nearest Level control (NLC).

value. This technique is attractive for high-power converters with three levels and a low switching frequency. This approach exhibits reduced losses in switching and interference from electromagnetic waves compared to SPWM, since to its lower switching frequency. SHE-PWM struggles to solve nonlinear transcendental equations with trigonometric terms that have many solutions and need lookup tables.

(b) Nearest Level control (NLC).

This approach involves comparing the sinusoidal reference with the MLI output voltage to determine the optimal voltage level. Figure 5 depicts the few stages of NLC required to produce the output voltage waveform. NLC is well-suited for high-power inverters since it simplifies finding the voltage level closest to the load, improves the output voltage quality and reduces load current ripple.

High switching frequency modulation techniques

LS-PWM and PS-PWM are two types of carrier-based multilevel PWM methods[75]. Both of these carriers based PWM schemes used for MLI are explained as follows:

(a) Phase-shifted PWM (PSPWM).

Within this technique, (m-1) triangular carrier signals (CS) with identical frequency and amplitude are evenly phase shifted across a single switching period. Two nearest CS's phase shifts (Φcr) are calculated by applying Eq. (1):

$$\Phi_{cr} = 360^{o}/(m-1) \tag{1}$$

The sinusoidal modulating signals frequency and amplitude are adjustable in nature. The amplitude modulation index (m_a) in this method allows for control over the inverter's fundamental-frequency component of output voltage. It is calculated using the formula (m_a=V_m/V_{cr}). V_m and V_{cr} represents peak value of modulating and carrier voltage signal respectively. Gate signals for the power switches are produced by assessing modulating signals with phase-shifted CS. Both the upper and lower switches of HBCs are active when the modulating signal is greater than CS.

Figure 6 (a). shows the PSPWM scheme principle for a five-level CHB-MLI. To produce a five-level inverter output voltage four triangular carrier signals with an equal phase shift of 90° are required. Due to symmetry of phases, the modulating scheme is shown only for single phase. For simplicity the gate signals for only upper switches of HBCs are shown as second switch in each leg is complementary in nature. One of the primary benefits with the PSPWM modulation strategy is that it maintains the duty cycles of the cells approximately equal and therefore maintains an even power distribution among HBC which naturally balances the capacitor voltages of the inverter. This feature makes the PSPWM as a dominant PWM method for CHB-MLIs.

(b) Level-shifted PWM (LSPWM).

The (*m-1*) triangle carrier signals are necessary to produce an '*m*' level inverter output waveform, much as the PSPWM technique and these carrier signals having same frequency and magnitude are level-shifted i.e. (are placed vertically disposed) with each other over one switching period. The frequency modulation index (m_f= f_{cr}/f_m) stays same compared to PSPWM, however the amplitude modulation index (m_a) differs and given as {m_a=V_m/ V_{cr}(m-1)}. By continuously comparing the modulating signals with these level-shifted carrier signals switching pulses for the power switches are generated. Based on the phase relation between individual carrier's signals, LSPWM scheme is categorized into APOD, PD, and POD. Figure 9(b) shows the PD-LSPWM scheme principle for a five-level CHB-MLI.

Among these LSPWM schemes, in PD strategy all carrier signals are vertically disposed but are in phase with each other and results in lowest voltage THD. Nevertheless, the frequency at which the device switches is not the same as the frequency of the carrier. Moreover, the switching frequency varies across devices in various HBCs. The varying times of device conduction lead to reduced market penetration, even in applications that do not need transformers, such as PV power conversion and APFs. Additionally, this variation affects the discharging and charging of DC bus capacitors and results in uneven power distribution in the used MLI.

(c) **Hybrid PWM switching strategy**.

Figure 7 illustrates a hybrid PWM switching approach, in which the modulating signals 'm_{a1}' and 'm_{a2}' are derived from their corresponding control systems. In Fig. 6(c), the symbols 'cr_1' and 'cr_2' denote the level-shifted triangular carriers used to produce firing pulses for switches in relation to the reference 'm_{a1}'. The triangle carriers 'cr_3' and 'cr_4' are generated by phase-shifting 'cr_1' and 'cr_2' correspondingly. These carriers are responsible for providing firing pulses for switches in relation to 'm_{a2}'. The figure clearly illustrates that the hybrid PWM results the AC side of the converter to produce five distinct levels of phase voltage.

(d) **Space Vector Modulation (SVM)**.

The SVM technique is suitable for all types of MLI for high power RES applications. SVM includes features such as reduced current ripple, easy hardware deployment and optimal dc-link voltage utilization[76]. The SVM is beneficial in PV applications because it provides a lower component size, the highest gain for every modulation index, and a somewhat broader range of modulation indices. This approach employs the SVM reference signal, with the modulation index serving as an extra reference signal. The supplementary reference signal is compared with the triangle carrier signal to produce the ST pulse. The SVM reference signal is contrasted with a triangular carrier signal to produce a PWM signal. Ultimately, both PWM signals are combined to activate the inverter switches. A comprehensive study of the SVM scheme, beginning with fundamental concepts, is presented here, demonstrating its potential as an effective solution for PV systems. SVM is a discrete control technique frequently implemented digitally with high-frequency PWM. The sampled analog signal computes the state vector of the system's reference output voltage, subsequently determines the corresponding voltage space vector discretely, and employs the digital signal controller to produce a high-frequency PWM signal. This enables switch control through the suitable duty cycle and frequency of the PWM, resulting in the output voltage waveform comprising three symmetrical sine waves. In conventional modulation method, the SVM scheme initiates with the production of the reference voltage vector (V_{ref}) in the $\alpha\beta$ plane. Understanding the position of V_{ref} is essential, as the inverter's switching sequence is contingent upon its placement. The inverter has a total of 3^3 switching states, resulting in 27 space vectors, as illustrated in Fig. 7[77].

The switching sequences in SVM can be comprehensively analyzed by the space vector diagram depicted in Fig. 7, which comprises 6 sectors (A, B, C, D, E, F), with each sector including 4 regions. For clarity, let us assume that V_{ref} is situated in region 2. The switching sequence varies for each location. Since the Vref is located in sector A (region 2), the switching sequence can be executed; however, the turn-on duration for switches in each phase has not been computed. The turn-on time for switches to produce the PWM signal is calculated by a series of successive steps.

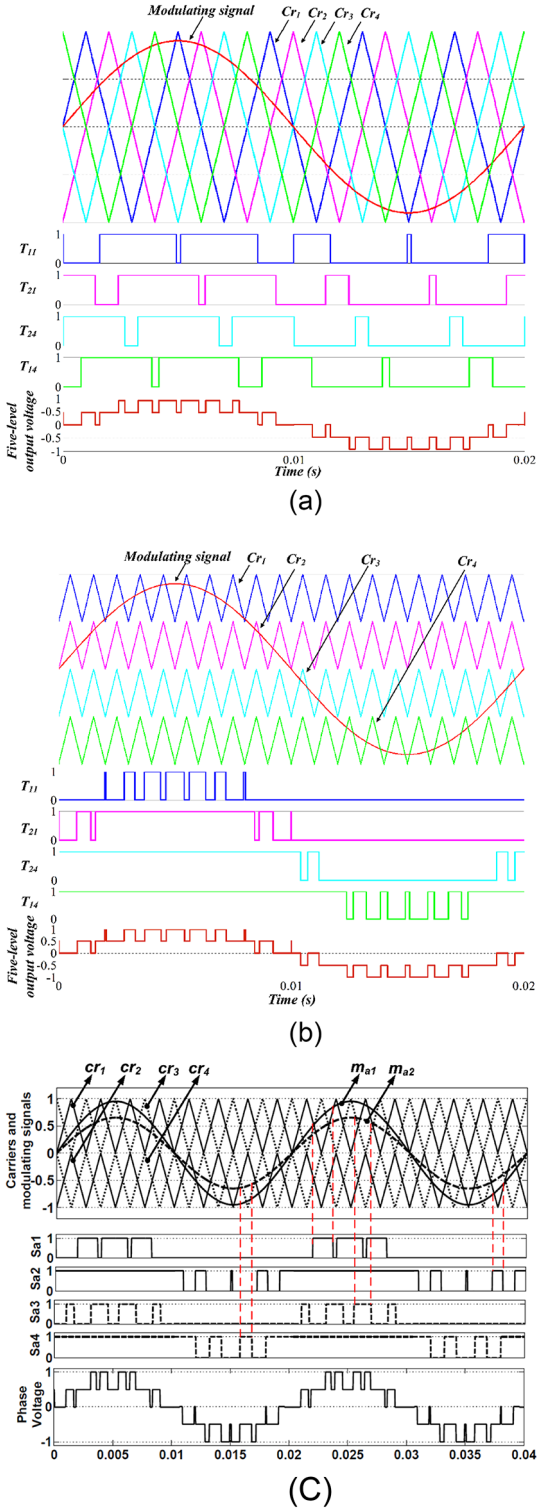

Fig. 6. (a) PSPWM scheme for **f**ive-level CHB-MLI (m_f=5, f_m=50 Hz, m_a=0.9 and f_{cr}=250 Hz)(b). LSPWM scheme for **f**ive-level CHB-MLI (m_f=20, f_m=50 Hz, m_a=0.9 and f_{cr}=1000 Hz)(c) Hybrid PWM switching strategy.

Comparative performance evaluation of carrier based PWM strategies

The performance of PSPWM and LSPWM schemes are studied for the application of CHB-MLI in RES. Table 3 depicts the comparative performance of LSPWM and PSPWM schemes. In LSPWM scheme, device conduction times are varying, therefore power loss and heat distribution within the MLI may not become uniform, making HBC capacitor voltage balancing impossible. PSPWM having main advantages to maintain the duty cycles of

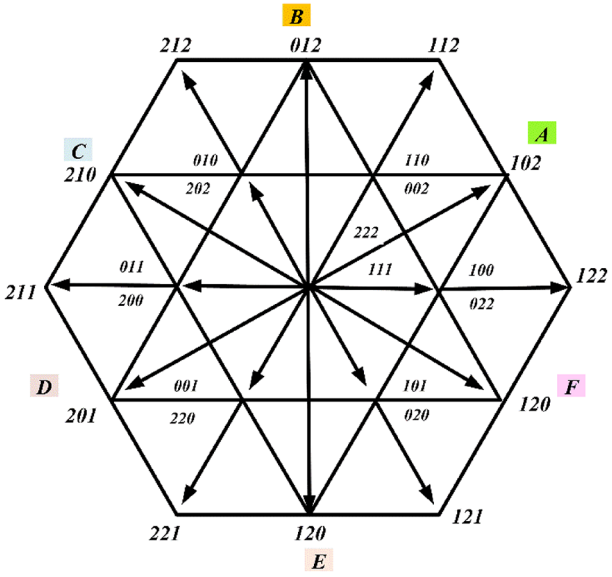

Fig. 7. SVM space vectors diagram, 1 indicates positive state, 2 indicates negative state, and 0 indicates zero states[77].

Important aspects	LSPWM	PSPWM
Device switching frequency	Different	Uniform across all devices
Is the conduction period of the device same?	No	Yes
Converter topology	Topology independent	FCMLC, CHBC
Line-to-line voltage THD	Better	Good
Natural capacitor voltage balancing	Not possible	Voltage balancing achieved
Controller design	Complex	Easy

Table 3. Comparative performance of LSPWM and PSPWM schemes.

the cells approximately equal and therefore maintains an even power distribution among HBC, which naturally balances the capacitor voltages of the inverter.

However, in LSPWM scheme the THD of inverter output injected voltages is less compared to PSPWM scheme. The supply side power quality aspects remain nearly same in both the schemes. The efficacy of a modulation approach relies on duration of device conduction periods, the chosen topology, and their respective performances.

Control techniques for grid-connected MLI

Precise control techniques are often required of grid-connected cascaded MLIs, to inject pure sinusoidal current that is in phase with grid voltage and maintains the UPF. It is important to ensure that all active power produces by PV gets transmitted directly to grid, with the dc-link voltage being greater than the grid's peak voltage. Furthermore, for cascaded MLIs with several PV strings, the controller should optimize power extraction from each array by independently regulating the dc-link voltages. Variations in temperature, irradiation, and wind speed are just a few examples of external factors that the controller has to be able to maintain system stability under. In order to minimize power quality issues and maximize power extraction from PV, several control systems and power conditioning schemes have been described in the literature[23–34]. However, dc-link voltage unbalance in cascaded MLI based grid-integrated solar energy conversion systems is still the long-standing problem and special measures are required to ensure dc-link capacitor voltage balancing or to employ a closed-loop voltage control in the cascaded MLI topologies.

Control techniques for single voltage sourced grid-connected MLIs

Figure 8 shows the schematic of a modular multilevel PV inverter's control block, which illustrates how a PI controller compares the reference dc-link voltage (U_{dcref}) with the actual voltage (U_{dc}) to produce the active reference current (i_{dref}). I_{qref} represents the reference current that is responsive to changes. Decoupled control allows for the acquisition of the reference voltage and the application of the compensation signal for suppressing circulating current. The dynamic balancing of the system capacitor voltage may now only be achieved by PWM adjustment, rather than by producing a balance compensation signal. This strategy improves system stability by preventing excessive compensating signal interference, suppressing circulating current, and maximizing DC

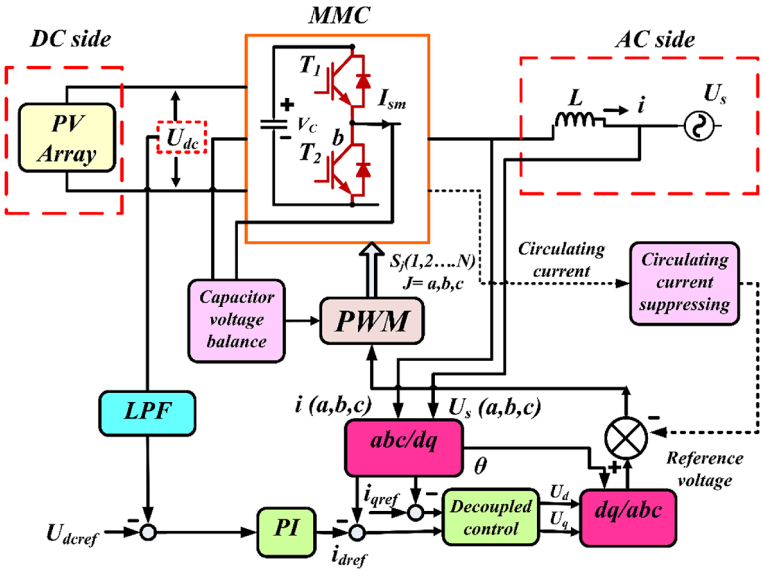

Fig. 8. Modulation Method for Photovoltaic Grid-Connected Generator[62].

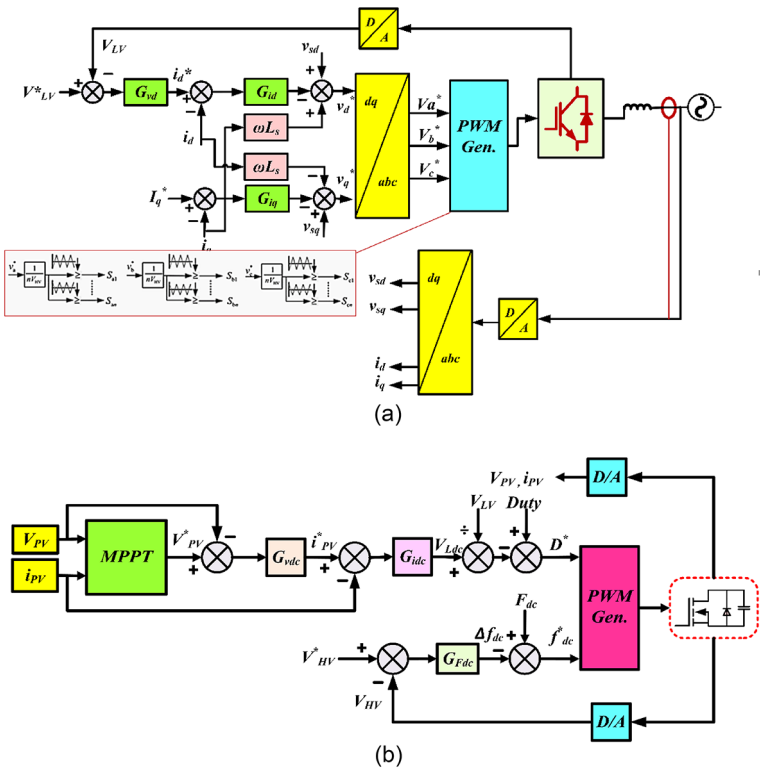

Fig. 9. (a) Control strategy for CHB grid-integrated converter[78](b) Control strategy for IB-FBLLC converters[78].

voltage use. Due to its ability to easily identify the closest voltage level compared to the NVC method, resulting in improved output voltage and load current ripple[62].

Figure 9 shows a three-phase CHB-based PV system with an CHB inverter and a dc-dc converter called an IB-FBLLC. Figure 9(a) illustrates the three primary components of CHB control system: modulation level, reactive and active current references, and feedforward decoupling control mechanism. The cross-current feedforward structure segregates the currents along q- and d-axes in the d-q reference frame. The voltage loop PI controller is denoted by G_{vd}, whereas the current loop PI controllers are denoted by G_{id} and G_{iq}. To improve grid current quality, the modulation stage makes use of the phase-shifted modulation method (PS-SPWM).

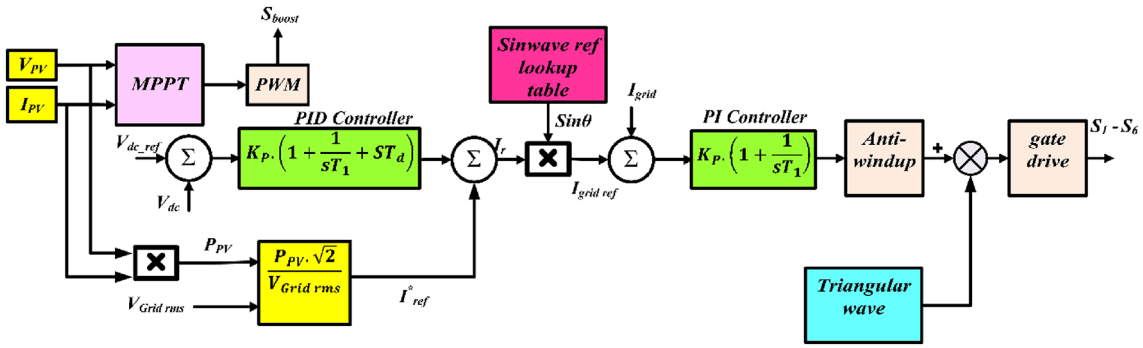

Fig. 10. Seven-level inverter with closed-loop control algorithm[30].

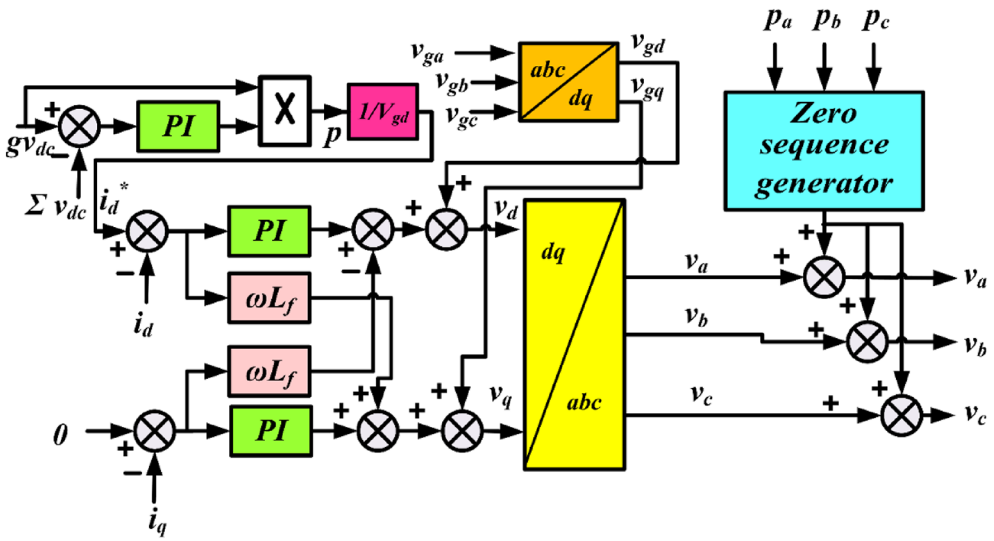

Fig. 11. Decoupled conventional control using dq rotational frame[24].

However, the CHB control method must be enhanced to achieve power balance. The H-bridge dc-link voltage (v_{HV}) is under the control of the traditional voltage loop, while the common dc voltage (v_{LV}) is under the management of the suggested method. Figure 9(b) demonstrates that the IB-FBLLC converters control the H-bridge dc-link voltage. Figure 9(b) demonstrates that, for any certain phase, different H-bridge cells display the same modulation waveform. Similarly, when we get to phases A, B, and C, we see that the modulation waveforms have identical magnitude and a shift-phase angle of 2/3. This prevents modification of the waveforms to accomplish dc-link voltage balancing in a single phase, as was previously suggested.

A current controller, reference-current generator, dc-bus voltage controller, and MPPT algorithm make up the control system depicts in Fig. 9(b). The primary functions of control system are to optimize the energy transfer from PV to grid and to provide sinusoidal current with minimal harmonic distortion, regardless of presence of harmonics in grid voltage.

The perturb-and-observe (P&O) approach is often utilized in MPPT at the proposed inverter because of its straightforward design and small number of observed parameters. At regular intervals, it compares PV output power to power produced during the previous perturbation cycle and either raises or lowers the voltage at the array terminals. The direction of the perturbation should remain unchanged in the subsequent cycle if power is increasing; otherwise, it will reverse. Since each MPPT cycle affects the voltage at the array's terminals, the P&O strategy will begin to loop around the achieved MPP as represented in Fig. 10[30].

Due to the unpredictable fluctuations in temperature, irradiance, and other variables, the three phases are expected to have distinct power levels The power imbalance state causes unforeseen issues with this architecture, which was originally intended to function under balanced power circumstances. The research suggests three innovative zero-sequence injection (ZSI) approach as an extension to traditional ZSI approach to address this issue. It employs a standard decoupled control scheme predicated on the dq rotational frame as shown in Fig. 11. The total of capacitor voltages is adjusted to the reference by making error signal amplified and establishing it as direct axis current reference. The disclosed approach generates the zero sequence v_0 and adds it to the converter output voltages based on three-phase power production p_a, p_b, p_c[24].

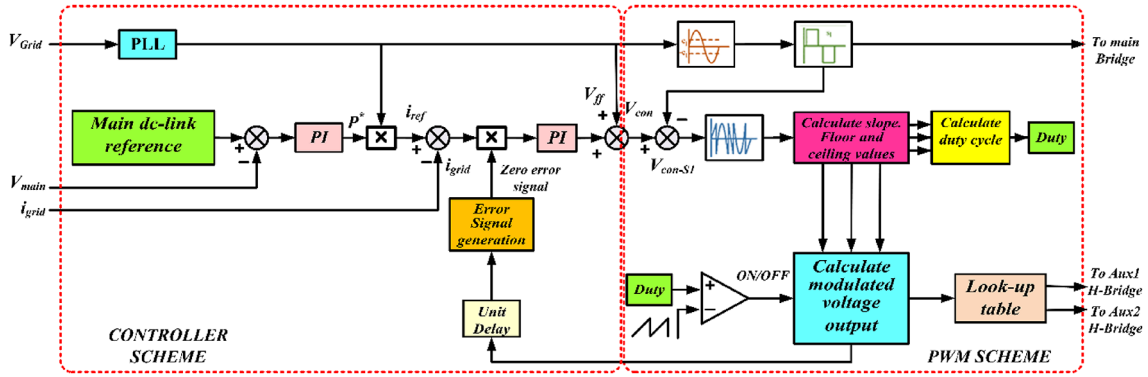

Fig. 12. Hybrid PWM technique with control approach for 27-level inverter[79].

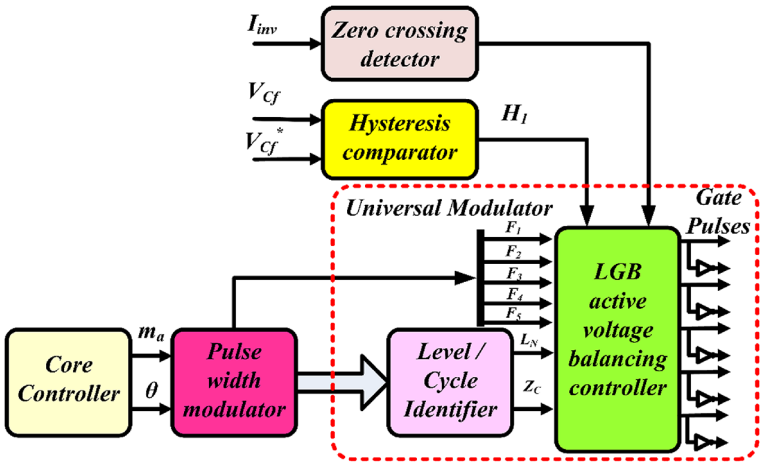

Fig. 13. FC active voltage balancing with LGB control system[60].

A closed-loop hybrid-switching method is presented to regulate the trinary asymmetrical 27-level inverter utilized in a PV system in[79]. A two-loop control strategy for a grid-connected PV system is shown in Fig. 12. While the internal current loop maintains a power factor of one, the external voltage control loop regulates the main H-bridge voltage. The ceiling, floor and slope values are obtained from the auxiliary H-bridge modules to execute right and left justified timer approach as outlined. Figure 12 illustrates the stable operation that occurs when a zero-error signal is added into a closed-loop control system.

To keep the flying capacitor voltage constant, independent of power factor and load current, an equation-based active voltage balancing method has been developed. The direction of the load current can be determined with the use of a zero-crossing detector. In Fig. 13A hysteresis controller used to indicate the state of FC voltage variation. The core controller supplies the reference modulation index, which is then utilized by a PWM to generate a multistep reference signal. The PWM uses methods including sinusoidal PWM, SHE, and others to generate a multistep reference waveform. Inverter output voltage levels are the only data needed by the level identifier, which is why this subsystem is called a universal modulator[60].

Control techniques of multiple voltage source grid-connected MLI

The study[80] demonstrates a power transfer control system as displayed in Fig. 14 is a novel technique for the CHB-MLI based SECS and can also balance the dc-link capacitors with each HBC of CHB-MLI under partial shade or varying environmental conditions. The control component of bidirectional power flow may be studied with this approach, allowing for individual HBC regulation and the adaptable extraction of power from dc-links. Thus, dc-link capacitor balancing is achieved in spite of environmental mismatch in panel matching.

The control mechanism of the five-level Modular FC Multilevel Converter (MFCMLC) is displayed in Fig. 15, illustrating the self-governing control used to establish the reference dc-link voltages (Vdcx1 and Vdcx2) for two separate isolated HBC. Since the voltage of each HBC and its capacitors can be independently controlled, this control method makes MPPT applicable to wind and PV systems alike. In addition, the MFCMLC, equipped with a control system and switching approach, effectively handles the power imbalances occur both between and within cells of a phase,, under different environmental conditions[81].

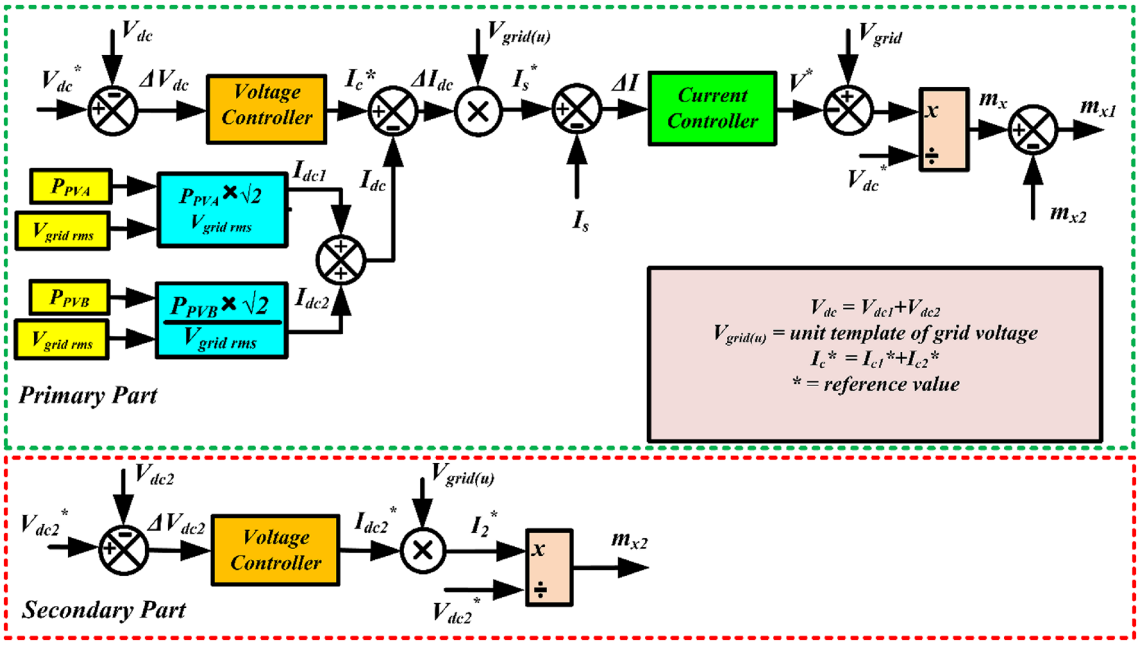

Fig. 14. Control scheme for CHB-MLI[80].

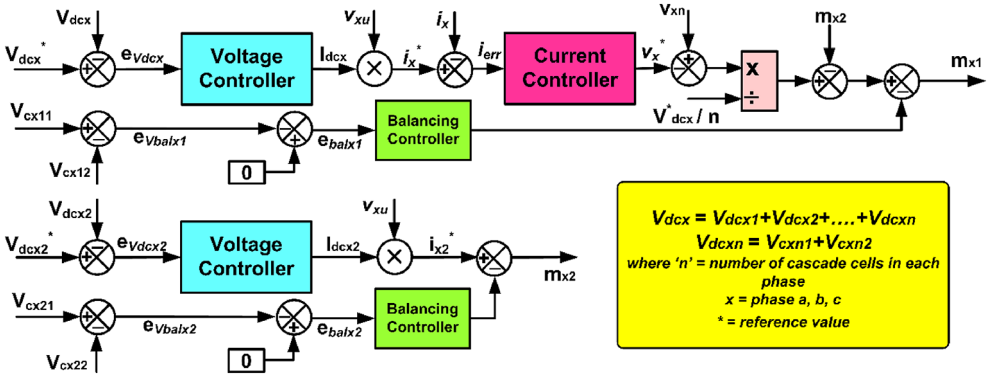

Fig. 15. Control Scheme for MFCMLC[81].

A controller has been developed represented in Fig. 16for a single-phase CHB converter that uses 'n' no. of modules[21]. The controller consists of a single internal current loop to produce a sinusoidal reference current with UPF and 'n' outer voltage loops for maintaining constant voltages across the DC links.

Figure 17shows the CHBMLI's energy balancing controller's conventional control strategy, which is based on a model[82], of energy-sampled PV system data. The closed-loop dynamics of the kth inverter-bridge's energy-balance controller will be regulated by a PI controller. The design requirements guarantee a rapid and responsive reaction, achieve local stability for controller, and have zero steady-state error at the tracking frequency. Unfortunately, direct connection of the PV arrays to the specific converter module was not possible since the control algorithms offered for high-voltage, large-scale PV system applications failed to account for the difficulties caused by leakage current.

In order to regulate the DC buses of a single-phase H-bridge-based multilevel active rectifier[83] provide PI-based control techniques in Fig. 18. The poor regulation of the grid current by the two solutions causes the instability. Unfortunately, the dc-link settles in more than 2 s (slow response) using the third option offered, which was constructed with voltage and current controls.

According to[84], low-cost controllers that use the d-q reference frame as their control method presented in can maximize power extraction from integrated RES while preserving power quality in a variety of situations. However, the suggested system simply employs a single DC-DC converter that is linked to a shared DC bus and is managed only by a PV array's MPPT algorithm. As a result, it is impossible to perform separate control and tracking of the two PV. In terms of THD, there is space for advancement of grid current, which is currently below the acceptable limits. Figure 19 provides the comprehensive diagram of Hysteresis controller. The hysteresis

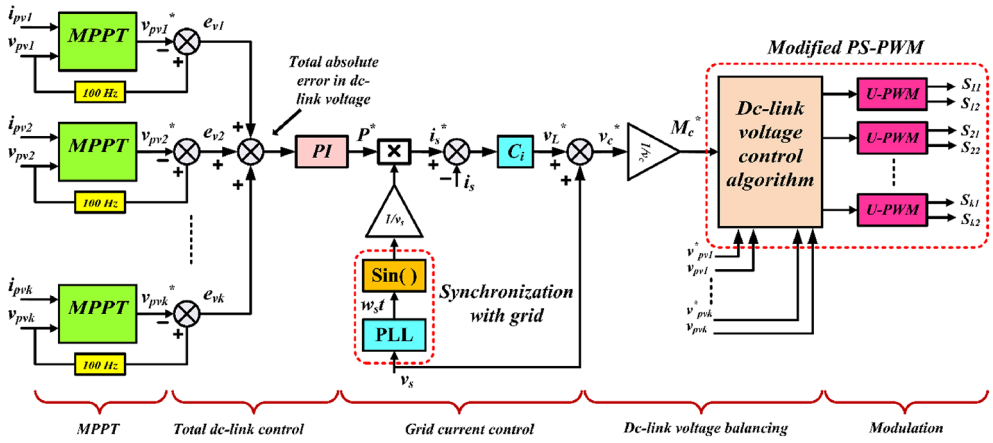

Fig. 16. Control Scheme for cascaded MLI[21].

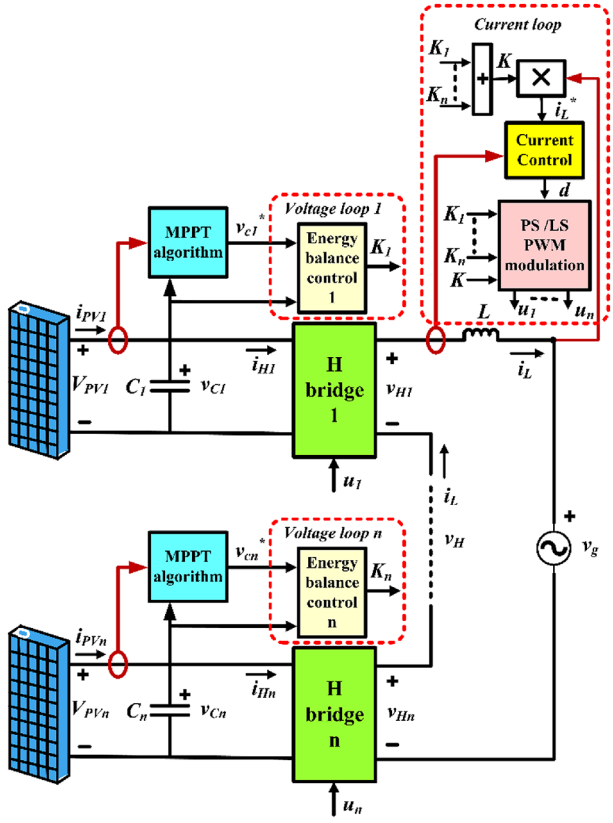

Fig. 17. CHBMLI's energy balancing controller[82].

current controller is constructed using high-frequency operational amplifiers (specifically, the LM-318). The microcontroller's inbuilt ADC module digitizes the current transducers' sensing of I_{PV} and I_b.

As seen in Fig. 20, a dc voltage controller is described in[85] that employs two proportional-integral (PI) controllers, namely sigma and delta controllers, to maintain a standard reference voltage (V^*_{dc}), equal to two three-phase, two-level inverter bridges (V_H and V_L) dc link voltage. The inverter and grid-reference current that it injects into grid via the transformer's open-end winding are both generated by the sigma controller. To do this, a voltage feed-forward current controller is used. An SVM variation is used to generate the MLI gate pulses. The controller works effectively in any environment and can handle temperature and irradiance swings with ease. Unfortunately, the control mechanism is ineffective for MLIs with more than two inverter bridges.

The control technique shown in Fig. 21for the MLI-based GCPV system requires a total of (n + 1) controllers when n no. of H-bridges are coupled in a cascaded fashion[86]. The individual and overall DC-link capacitor voltages are controlled by 'n' voltage controllers, among others. The remaining controller is responsible for

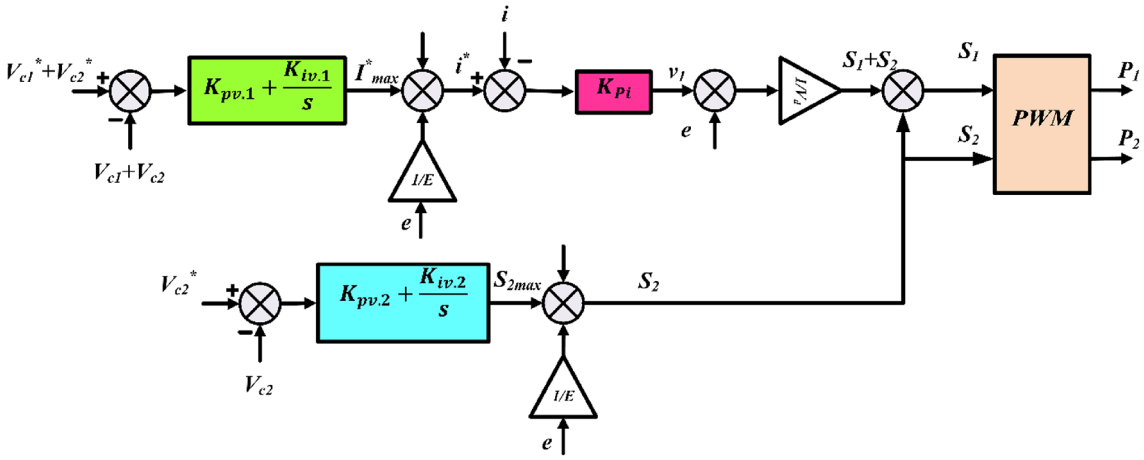

Fig. 18. PI-based control techniques for multilevel active rectifier[83].

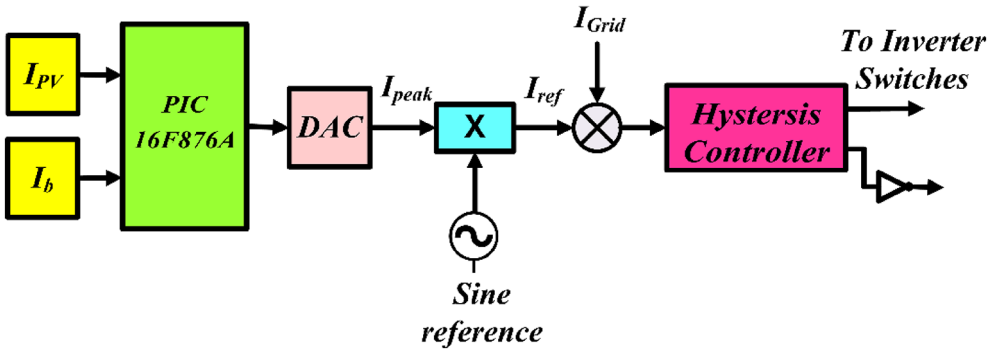

Fig. 19. Current reference generator with a Hysteresis controller[84].

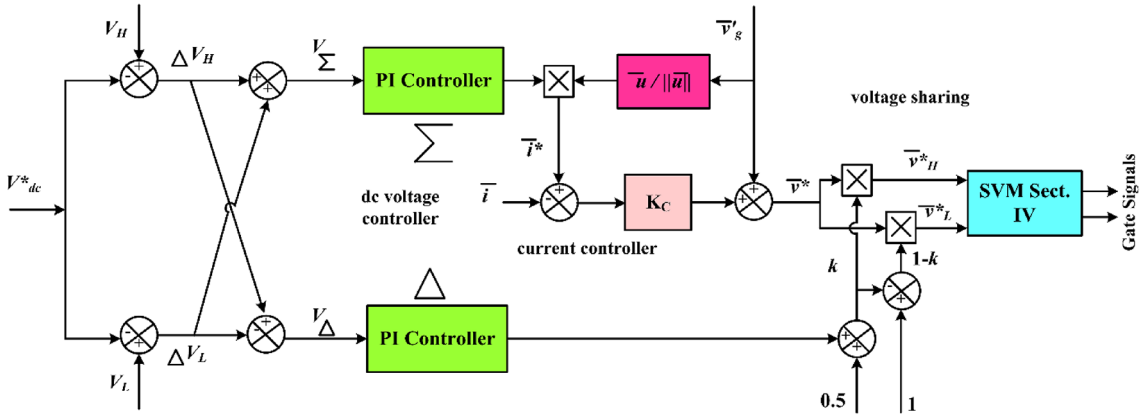

Fig. 20. Dual inverter topology converter control[85].

optimizing the H-bridges inverter current injected into grid (Ig) as a sinusoid at near UPF, matching the reference grid current (Ig*) determined by the voltage controllers.

Figure 22 depicts the architecture of the control system, with V_{dc1}- V_{dcN}represent the obtained DC voltages of the cells[87]. This paper employs a two-stage cascaded controller to accomplish the control objectives. The outer loop controls the overall voltage of capacitors using a standard PI controller. To adjust the grid's active power absorption or alternating current amplitude, the PI controller generates a direct current signal. The internal loop regulates the input current such that it is sinusoidal and in sync with grid voltage. Due to its simplicity and low steady-state amplitude and phase error, the proportional-resonant (PR) controller is used in this research.

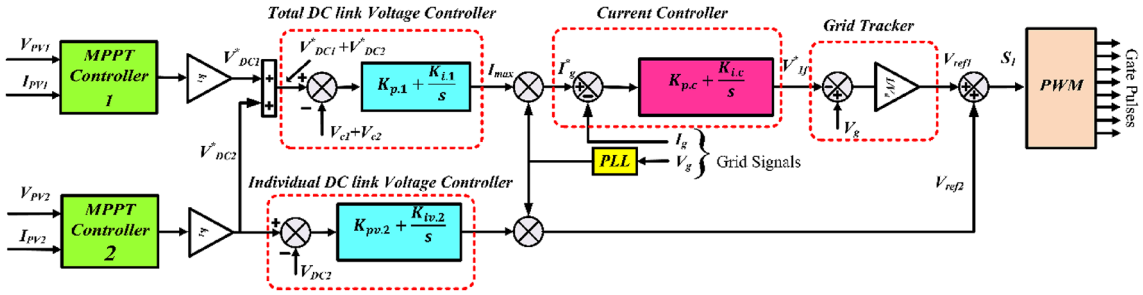

Fig. 21. Control of asymmetrical cascaded MLI[86].

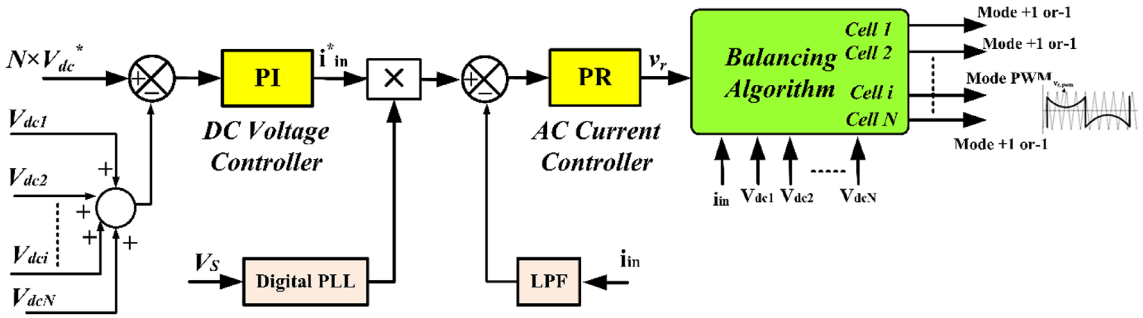

Fig. 22. Extended operating zone voltage balancing approach for CHB converters[87].

GCMLIs controllers comparative analysis for PV applications

A review of multiple grid control approaches presented in the previous research for distinct GCMLIs is conducted, as outlined in Table 4. The analysis is conducted based on various grid current control approaches, DC bus voltage control methods, and the modulation strategies used in the application for a grid-connected system. Furthermore, for a better visualization of the system's performance, we have included the key elements of the controllers suggested for the different GCMLIs.

Conclusions

In this study, the classification of MLI is explained and an extensive review of available MLIs for GCPV applications is successfully presented. The better characteristics of MLIs compared to conventional two-level inverters are leading to their increased utilization. Using asymmetrical voltage sources for the MLI leads to significant enhancements in voltage characteristics and a decrease in multiple components. Additionally, the MLI has no difficulty to matching the precise grid codes required for grid interface. The PWM and other modulation strategies for the GCMLIs are categorized in depth based on their switching frequencies. The choice of modulation technique determines the switching frequency, which in turn affects the presence of ripples and harmonics in the MLI voltage waveform. The control strategies for different PV-GCMLIs have been categorized according to the controlling approaches and MLI types. This work has successfully demonstrated the potential of control techniques for GCPV applications. The control scheme and modulation strategies have been presented for different MLI topologies. So, with the help of this study and by choosing a suitable MLI, modulation strategy and control approach can address several issues in GCPV systems.

Categories of MLI	Reference	Topology of MLI	No. of levels & phase	Modulation Scheme & switching frequency	DC bus voltage controller	Control Scheme	Outcomes
Single-voltage sourced GCMLI	88	NPC	3, 3-ph	SVPWM, 5 kHz	PQ and FLC	VOC	Limited to three-level output voltage.
	89	NPC	m, 3-ph	SVPWM, 5 kHz.		DCC	Ensures precise control of line current.
	90	NPC	m, 1-ph	Nearest three virtual SV-PWM, 5 kHz	PI controller, comparator & sensor	Control of DC-link voltage, modulator loop & unbalanced control	Eliminates the need for transformers to step-up voltage by lowering the devices voltage ratings.
	(Wang et al., 2013)	FC	7, 1-ph	Phase-shifted PWM, 10 kHz.	PI	Predictive current control method	Balances the DC link voltage and improves the generated reference signals' accuracy without using feedback control.
	91	ANPC	5, 1-ph	Voltage injection using a carrier- based PWM with zero sequence, 2 kHz		Neutral point potential balancing method.	The FC voltage needs to be regulated to quarter of the input DC voltage.
	92	ANPC-CHB	5, 3-ph	Novel PWM strategy, 20 kHz	PI controller with decoupling voltage source	FC reference generator & Neutral point voltage balancing approach	Produces a balanced voltage across the dc-link capacitor without limiting the flying capacitor voltage.
	21		m, 1-ph	PS-PWM & 5 kHz	PR controller	Dual-loop control	Mismatch in active power among modules might result in unsymmetrical output voltage, power quality degradation and over-modulation.
	93	DC with capacitive divider	m, 1-ph	PS & LS PWM, 5kHZ.	Digital PI controller	Energy balance controller	Faster dynamics, local stability and negligible steady-state error
	94,95	Cascaded Dual	m, 3-ph	Hysteresis control & 1 kHz	Digital PI controller	SMC	Reduced system order, Robust and suitable for ON-OFF operation of power switches.
	67	Transformer-less MLI with RDC	1-ph	PD-PWM	-	PWM Control	topology has zero leakage current, boost capability, lower voltage stressors, and the fewest switching components.
	96	Cascaded dual two level inverter	m, 3-ph	Improved SVM, 20 kHz.	Digital PI	Closed-loop control	The system can function as active filter, providing load balancing, reactive power injection and harmonic compensation capabilities.
Multiple voltage-sourced GCMLI	97	Cascaded inverter with T-type circuit	m, 1-ph	Dual reference PS-PWM, 3 kHz.	Digital PI	Dual- loop control	Mismatch in active power among modules might result in unsymmetrical output voltage, power quality degradation and over-modulation.
	98	Modified Cascaded	5, 1-ph	Reusable PWM	PR controller	Closed-loop current control	Effective for large-scale GCPV systems.
	62	Modular CHB	m, 3-ph	Modulation compensation PWM, 1.5 kHz.	PI	Closed-loop distributed MPPT control approach	The PV system's overall flexibility and efficiency have been enhanced.
	99	Trinary and Binary CHB	7 & 9; 1-ph	LS PWM, 12 kHz.		Continuous power theory (CPT) based controller	The controller provides effective voltage regulation and rapid dynamic responses.
	100,101	Trinary CHB	27, 1-ph	Modified Hybrid PWM in H bridge and jumping Modulation in auxiliary circuit, 30 kHz.	PI controller	Hybrid control approach & control platform containing DSP.	By incorporating a zero-error signal into the closed-loop control, steady-state operation was guaranteed.
	102	Cascaded Full-bridge inverter with a FC	9, 1-ph	Novel PWM approach with use of low-cost DSP	PI controller	Hysteresis-based control.	Reduces ground leakage current and enhances system efficiency.
	100,103,	Hybrid PUC	7, 1-ph	Optimized switching angle	PI controller	model predictive control (MPC), Finite control set (FCS)	Fast transient response with stable and accurate tracking of reference current at steady state
	57	Symmetrical hybrid	5, 1-ph, 3-ph	sinusoidal unipolar PWM,1.5 kHz, Space-vector PWM, 1.5 kHz	-	-	Low-frequency switches can handle the entire dc-link voltage, while fast-switching semiconductors are capable of withstanding half of it.
	60	Active NPC-RDC inverter	9, 1-ph	Multicarrier PWM, 2 kHz		LGB active voltage balancing controller	The technique is feasible in real-time with an inexpensive processor.
	22	T-Type converters with RDC	1-ph	staircase modulation	PI controller	-	This topology have less components and and have more design flexibility.
	64	Asymmetrical RDC-MLI	1-ph	NLC modulation	-	-	The topology features fewer switches, is cost-effective, and improved reliability compared to newly introduced topologies with same voltage levels.
	66	Asymmetric H-6 Structured MLI	1-ph	multicarrier PWM	-	-	Proposing a novel asymmetric H-6 structured MLI topology Utilizing a series of discrete DC input sources on both sides of the H-6 inverter to generate varying voltage levels
	78	Interleaved-boost full-bridge LLC (IB-FBLLC) and CHB multilevel converters		PS-SPWM, 2 kHz	PI controller	Input port and HVS voltage control	Minimizing input current ripple and adjusting the switching frequency band can enhance the optimization of magnetic components and PV power extraction.

Table 4. GCMLIs controllers comparative analysis for PV applications.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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Author contributions

Bhupender Sharma: performed the experiments, analyzed and interpreted the data, wrote the paperSaibal Manna: analyzed and designed the experimentsVivek Saxena: performed the experimentsPraveen Kumar Raghuvanshi: analyzed tools or data and interpreted the data, materialsMohammed H. Alsharif: analyzed the experiments, contributed reagentsMun Kyeom Kim: conceived and designed the experiments, contributed reagents.

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Declarations

Competing interests

The authors declare no competing interests.

Additional information

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