A 2.16-μW Low-Power Continuous-Time Delta–Sigma Modulator With Improved-Linearity G_m for Wearable ECG Application

Jaedo Kim, *Graduate Student Member, IEEE*, Quanzhen Duan, *Member, IEEE*, Jihun Choi, *Graduate Student Member, IEEE*, Chiho Song, *Graduate Student Member, IEEE*, and Jeongjin Roh, *Senior Member, IEEE*

***Abstract*—This brief presents a 2.16 μW low-power third-order single-bit continuous-time delta-sigma modulator (CTDSM) for electrocardiogram (ECG) signal acquisition application. The proposed CTDSM uses an active-RC (A-RC) integrator as a first integrator and an improved linearized G_m-C integrator for the second and third integrators, respectively. The mixed-integrator structure helps to mitigate the trade-offs between power consumption and resolution. Moreover, a source-degenerated auxiliary differential pair circuit is used for the G_m-C integrators to improve their linearity. By using A-RC and G_m-C integrators together along with an improved-linearized G_m block, the total power consumption was measured as 2.16 μW with a peak signal-to-noise ratio of 80.1 dB, signal-to-noise, and distortion ratio of 78.4 dB, and a dynamic range of 81.4 dB with a bandwidth of 250 Hz. Furthermore, a real-time ECG signal was successfully captured in an ECG acquisition system that consisted a heart-rate sensor and a signal acquisition circuit, including the proposed CTDSM.**

***Index Terms*—Continuous-time delta-sigma modulation, weak inversion, G_m-C structure, operational transconductance amplifier, and low-power consumption.**

I. Introduction

RECENTLY, electrocardiogram (ECG) monitoring has become one of the most prominent requirements in portable/wearable devices in modern medical diagnosis. An ECG acquisition system primarily consists of a heart-rate sensor and a signal acquisition circuit, including an analog-to-digital converter (ADC). To ensure high performance with an ECG signal bandwidth, continuous-time delta-sigma modulator (CTDSM) is mostly preferred in ECG acquisition systems since it provides high resolution at a low power consumption. More importantly, it is more cost-effective than other counterpart ADCs. A CTDSM can be implemented either by active-RC (A-RC) integrators or G_m-C integrators. As shown in Fig. 1(a), an A-RC integrator with a load from the A-RC integrator can be used in an A-RC integrator-based CTDSM. Generally, the A-RC integrator-based CTDSM requires high-power two-stage operational transconductance amplifiers (OTAs) to drive resistance loads [16]. From Fig. 1(b), a G_m-C integrator with a load of G_m-C integrator is used in G_m-C integrator-based CTDSMs. Owing to the infinite load, a much more power-efficient OTA can be implemented for G_m-C integrators in G_m-C integrators-based CTDSMs. However, poor linearity occurs in these integrators because of its open-loop configurations, which causes distortion. Therefore, in this brief, a mixed-integrator structure for CTDSM comprising an A-RC integrator for the first integrator (INT1) and two G_m-C integrators for the second and third integrators (INT2 and INT3) is proposed to reduce the trade-off

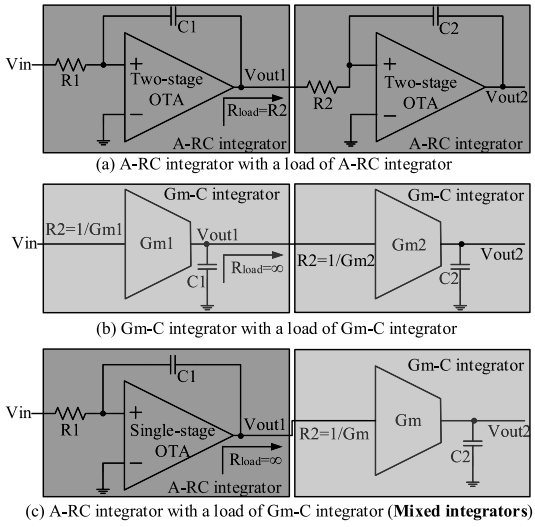

Fig. 1. (a) Active-RC integrators-based structure used in the conventional CTDSM. (b) G_m-C integrators-based structure used in an other conventional CTDSM. (c) Mixed integrator used for the proposed low-power CTDSM.

Manuscript received 14 May 2022; accepted 3 July 2022. Date of publication 7 July 2022; date of current version 28 October 2022. This work was supported in part by the Korea Institute for Advancement of Technology (KIAT) Grant funded by the Korea Government (MOTIE, Competency Development Program for Industry Specialist) under Grant P0012451; in part by the Technology Innovation Program (Development of Ultra Low Power High Resolution Analog IP Module for Healthcare Sensors) funded by the Ministry of Trade, Industry & Energy, (MOTIE), South Korea, under Grant 20016379; and in part by the National Research Foundation of Korea (NRF) Grant funded by the Korea Government (MSIT) under Grant 2019R1A2C2085189. This brief was recommended by Associate Editor U. Guler. *(Corresponding author: Jeongjin Roh.)*

Jaedo Kim, Jihun Choi, Chiho Song, and Jeongjin Roh are with the Department of Electrical Engineering, Hanyang University, Ansan 15588, South Korea (e-mail: jroh@hanyang.ac.kr).

Quanzhen Duan is with the School of Integrated Circuit, Sun Yat-sen University, Shenzhen 510275, China.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2022.3188793.

Digital Object Identifier 10.1109/TCSII.2022.3188793

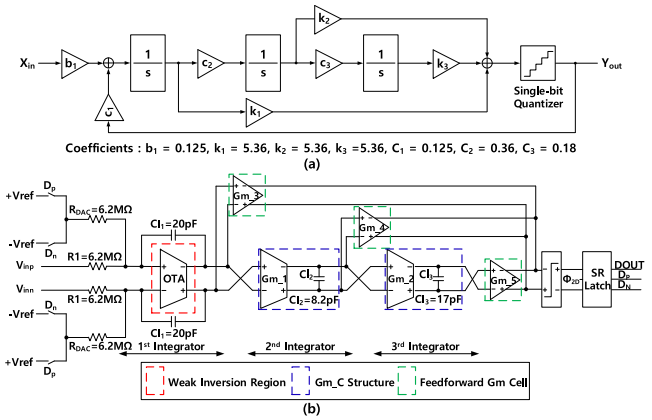

Fig. 2. (a) The proposed third-order CIFF single-bit CTDSM structure. (b) Schematic implementation of the proposed CTDSM.

between power consumption and resolution [1], as shown in Fig. 1(c). The reason behind choosing an A-RC integrator for INT1 is to alleviate the linearity problem caused by the large input signal swing. In an A-RC based CTDSM, the succeeding integrator input resistance in between two consecutive A-RC integrators behaves as the load for the preceding integrators, which affects the OTA gain of the preceding stage. Thus, in the proposed CTDSM, the large input impedance of the G_m-C integrator for INT2 behaves as a large output impedance for the OTA of INT1, which allows the use of an efficient single-stage OTA operating in the weak inversion region instead of the two-stage OTA for INT1 to achieve low power [2]. In addition, fast and easy tuning of the G_m-C integrators for INT2 and INT3 are also implemented to achieve further power reductions. However, the coefficients of the integrator are determined by G_m and the capacitance, which vary with the input voltage swing, thus causing a nonlinearity problem. Therefore, to mitigate this issue, a source-degenerated auxiliary differential pair (SDADP) was used to improve the linear range of G_m, which improved the performance of the CTDSM proposed in this brief. The simulation results in [10] successfully verified this SDADP structure after implementation in a continuous-time filter. Upon successful simulation verification, this SDADP structure was further applied to a high resolution delta-sigma modulator to complete the chip test.

II. Circuit Design and Implementation

A. The Proposed CTDSM Structure

Fig. 2(a) presents the MATLAB representation of the proposed third-order cascade-of-integrators with a feedforward (CIFF) single-bit CTDSM structure. Since the CIFF structure with an input-feedforward path only processes the quantization noise in the loop and has a small output swing for each integrator output, less power consumption is required for the OTA [3]. Meanwhile, this greatly reduces the design requirement of G_m-C integrators for INT2 and INT3. Based on the MATLAB/Simulink modeling in Fig. 2(a), the coefficients of the proposed CTDSM are determined, and its noise transfer function (NTF) is expressed as follows:

$$NTF = \frac{s^3}{s^3 + 0.6703s^2 + 0.2442s + 0.0440}, \tag{1}$$

where the gain of NTF over the whole frequency range should be 1.5 or lower to ensure stability of the CTDSM. The NTF gain was set to 1.5, and the NTF was obtained using the Delta-Sigma Toolbox in MATLAB [3], as shown in Equation (1). The proposed CTDSM uses Gm-C integrators for the remaining integrators INT2 and INT3, except for INT1. Therefore, NTF was calculated by reducing the coefficient to reduce the output swing of each integrator in consideration of the Gm linearity. Fig. 2(b) illustrates the overall schematic of the proposed CTDSM, which includes an A-RC integrator as INT1, two G_m-C integrators for INT2 and INT3, and G_m cells (G_{m3}, G_{m4}, and G_{m5}) for the feedforward paths. As already discussed, the A-RC integrator is used to alleviate the nonlinearity of the first integrator. The transconductance of the low-power OTAs designed for the G_m cells is determined using the equation below:

$$G_m = \frac{1}{R}. \tag{2}$$

A resistive feedback circuit was implemented for the single-bit digital-to-analog converter path, where the feedback logic signals (Dp and Dn) were generated from the block of "SR Latch". The values of the resistor, capacitor, and G_m in Fig. 2(b) were determined using the coefficients obtained from the MATLAB simulation in Fig. 2(a). Excess loop delay (ELD) is a well-known nonideality of high-speed continuous-time delta-sigma modulators. Unlike an ideal modulator, which instantaneously performs sampling, quantization, and digital-to-analog conversion, real modulators always exhibit a time delay in the signal processing chain. The delay arises from the non-zero switching time of the transistors in the comparators of the quantizer and the digital-to-analog converter. However, in low-speed applications, the one clock period is sufficiently long, and the time delay accounts for a very small portion of one clock period, so the ELD is not a serious issue in low-speed CTDSMs. Table I shows the simulation results according to PVT variation [4] of the proposed CTDSM.

TABLE I
Summary of SNR/SNDR With Simulation Results According to PVT Variation of the Proposed CTDSM

Temperature	FF	TT	SS
–40 °C	87.1/86.8	87.1/86.7	85.8/85.4
27 °C	85.8/85.0	86.1/85.4	84.7/83.8
125 °C	83.5/83.4	83.4/83.0	82.6/82.5

B. Single-Stage OTA Working in the Weak Inversion Region

Fig. 3(a) shows the OTA schematic used in INT1. As mentioned, owing to the large input impedance of G_m of INT2 in the proposed mixed-integrators CTDSM, a single-stage class-AB OTA [5] operating in the weak inversion region instead of a two-stage OTA in INT1 was used to improve the power consumption. In the delta-sigma modulator, the OTA of the first integrator is particularly important [6]. Moreover, for a given

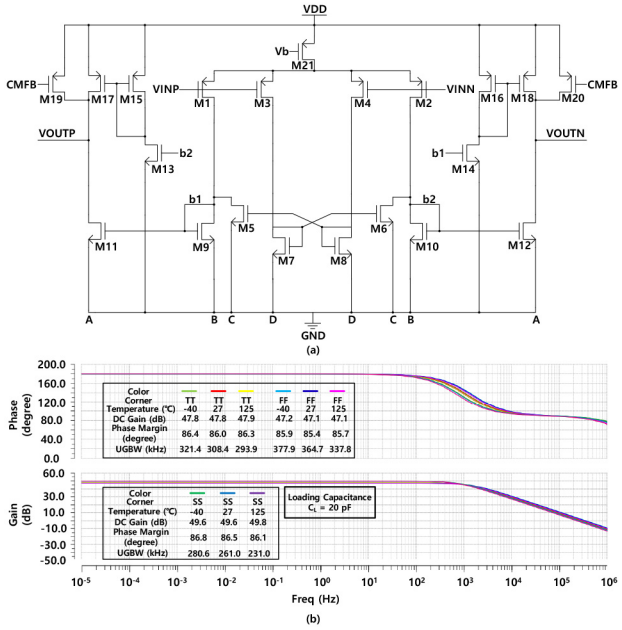

Fig. 3. (a) Schematic of a class-AB OTA working in a weak inversion region. (b) Open-loop AC simulation results of the adopted OTA.

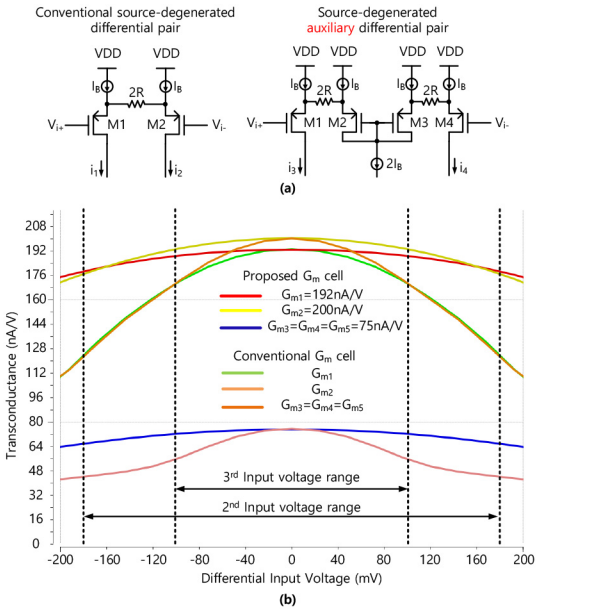

Fig. 4. (a) The conventional source-degenerated differential pair structure and the adopted SDADP structure. (b) Simulated results of the conventional source-degenerated differential pair structure and the adopted SDADP structure.

transistor, the channel length modulation effect is the same for both weak and strong inversions, and r_{ds} changes according to the drain current [7]. The channel-length modulation factor λ is equal to the reciprocal of the initial voltage and is a function of the channel length. Therefore, r_{ds} increases both as the drain current decreases and as the operation decreases from strong inversion to weak inversion. The designed class-AB OTA gain can be calculated, as $A_v = G_m \times R_{out}$, where its transconductance G_m and equivalent output resistance R_{out} are indicated in [5]. Fig. 3(b) shows the open-loop AC simulation result of the designed class-AB OTA with an equivalent load capacitor of 20 pF. The DC gain and unity-gain bandwidth (UGBW) are 47 dB and 230 kHz, respectively, and the phase margin obtained is approximately 85 degrees under different process corners (TT, FF, and SS) and temperatures (−40, 27, and 125 °C). For the typical case (process: TT, temperature: 27 °C), a DC gain of 47.8 dB, UGBW of 308.4 kHz, phase margin of 86.0 degrees, and a unity-gain bandwidth (UGBW) of 308.4 kHz were obtained. The input resistance of the proposed CTDSM was determined as 6.2 $M\Omega$ by considering the thermal noise of 4kTR [8]. The input-referred noise of the weak inversion OTA of the first integrator was calculated through the noise simulation of the Spice simulation. The input-referred noise of the proposed CTDSM is 2.90 nV^2/Hz. Considering the noise of the proposed CTDSM, the SNR was calculated as 84 dB using the SNR formula [9]. The noise of these components is sufficiently low to achieve the target SNR of the ADC.

C. The High-Linearity G_m-C Implemented by an Auxiliary Differential Pair OTA

Fig. 4(a) illustrates the conventional source-degenerated differential pair structure and the SDADP structure used in the proposed CTDSM. Fig. 4(b) shows the linear range comparison of the conventional source-degenerated differential pair structure and the SDADP structure obtained from the simulation. Compared to the conventional source-degenerated differential pair structure, the SDADP structure has a much wider linear range with low harmonic distortion [10]. Therefore, this SDADP structure was used to implement all G_m cells in the proposed low-power CTDSM, as shown in Fig. 2(b). Fig. 5 shows the schematic of G_m implemented in the proposed CTDSM, where R1 and R2 are the degenerated resistors (R1 = R2), transistors M3-M6 are biased using IB, and a current of 2IB flows into the tail current source transistor M13. Transistors M11 and M12 operating in the deep triode region were used for common-mode sensing, and since it does not require an additional biased current, it benefits by lowering the current to some extent. SDADP has been designed with a different bias current to match the input swings of different G_m cells in this proposed CTDSM. Consequently, nearly

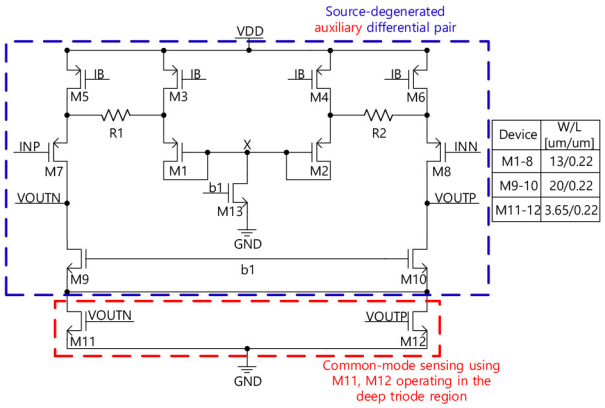

Fig. 5. Schematic of G_m implemented in the proposed CTDSM.

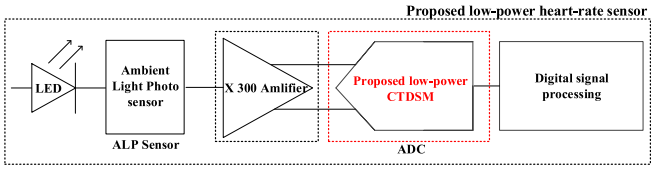

Fig. 6. Block diagram of an ECG acquisition system using the proposed CTDSM.

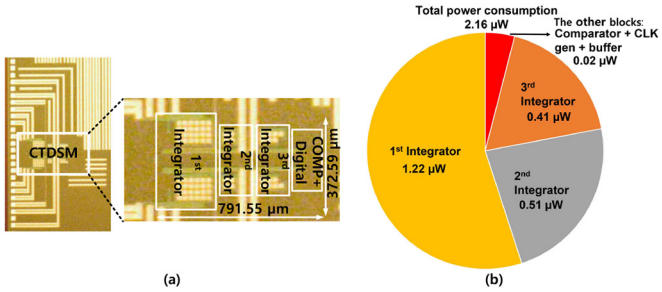

Fig. 7. (a) Chip microphotograph. (b) Power consumption of the proposed CTDSM.

constant coefficients were obtained for the proposed CTDSM with optimized power consumption.

D. ECG Acquisition System Using the Proposed CTDSM

The proposed low-power CTDSM was implemented on an ECG acquisition system to verify its performance, as shown in Fig. 6. The ECG acquisition system comprised a heart-rate sensor including a light-emitting diode (LED), an ambient light photo (ALP) sensor, an amplifier, the proposed CTDSM, and digital signal processing (DSP). The LED in the ECG continuously emits light, and the ALP sensor measures the amount of LED light reflected by the capillaries. The amount of returned light decreases when blood flowing in the capillaries increases and the amount of light reflection increases when the blood flowing in the capillaries decreases. Accordingly, ECG signals are successfully detected by the heart-rate sensor. Furthermore, the detected ECG signals are amplified by an amplifier with a gain of 300 before being processed by the proposed low-power CTDSM, as shown in Fig. 6. Finally, an ECG waveform is obtained using DSP, which consists of Arduino and MATLAB tools.

III. Measurement Results

A. Measurement Results of the Proposed CTDSM

Fig. 7(a) shows a microphotograph of the proposed low-power CTDSM with a total area of 0.29 mm^2. The power consumption distribution of the proposed low-power CTDSM is shown in Fig. 7(b), where the total power consumption is 2.16 μW with a 1.8 V supply voltage. The OTA of INT1 is the most important block that determines chip performance, so 55% of the total chip power is used by INT1. Fig. 8(a) shows the measured digital output FFT spectrum of the proposed low-power CTDSM chip. A signal-to-noise ratio (SNR) of 80.1 dB and an SNDR of 78.4 dB were achieved. The FFT points of 65536, the input signal frequency of 51.757 Hz, and the signal bandwidth of 250 Hz were used during chip

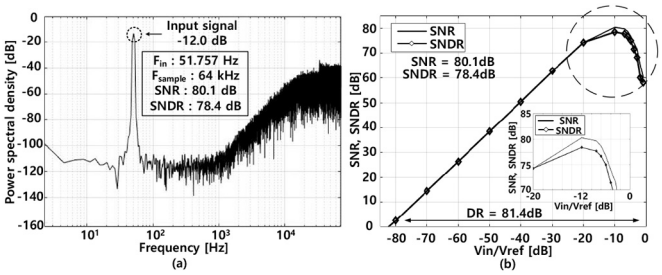

Fig. 8. (a) Measured output FFT spectrum of the proposed CTDSM chip. (b) Dynamic range spectrum of the proposed CTDSM chip.

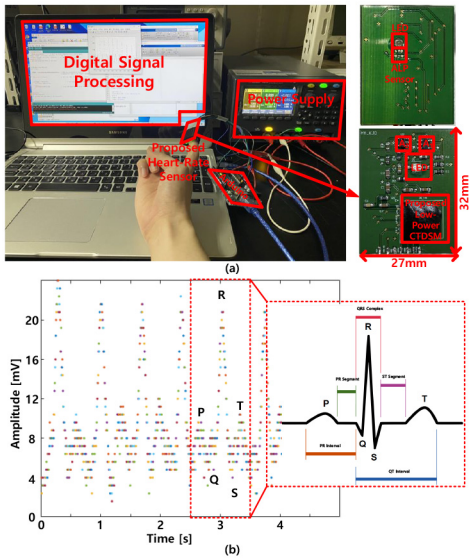

Fig. 9. (a) Test bench of the ECG acquisition system with the proposed low-power CTDSM. (b) Measured real-time ECG waveform of the ECG acquisition system.

testing. Owing to the proposed mixed-integrator structure and improved linearized G_m using the SDADP circuit, there were no visible harmonics, as shown in Fig. 8(a). The measurement result is lower than the simulation results because of the extra parasitic component and noise of the chip and the PCB. Fig. 8(b) shows the measured dynamic range (DR) of 81.4 dB for the proposed low-power CTDSM at a signal bandwidth of 250 Hz. The general figure of merit (FoM_W) [3] is used for a performance comparison with other state-of-the-arts methods. The experimental results of the proposed CTDSM and other studies are summarized in Table II. It can be observed that the proposed low-power architecture has a significant reduction in power consumption and exhibits a good FoM_W compared to other delta-sigma modulators with similar low-bandwidth application.

B. Measurement Results of a ECG Acquisition System With the Proposed CTDSM

Based on the block diagram of an ECG acquisition system in Fig. 6, a test bench was generated as shown in Fig. 9(a). The PCB of the ECG acquisition system was 27 mm × 32 mm. The sensor supply voltage was 3.3 V, which is different from the supply voltage of the proposed CTDSM (1.8 V). The

TABLE II
SUMMARY OF THE CTDSM MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

Parameter	ACCESS'20 [6]	VLSI'18 [11]*	TCASII'18 [12]	JSSC'19 [13]*	VLSI'19 [14]	TCASI'22 [15]	TCASI'20 [16]	ACCESS'20 [17]*	This Work
Architecture	DT	CT	CT	CT	CT	DT	CT	CT	CT
Structure	–	G_m-C	A-RC	G_m-C	G_m-C	–	A-RC	G_m-C	A-RC+G_m-C
Process	0.18-μm	0.18-μm	0.13-μm	0.18-μm	0.18-μm	90-nm	0.18-μm	65-nm	0.18-μm
Supply(V)	1.8	1	0.6	1.8	0.3	1.2	1.8	1.2	1.8
BW(kHz)	25	0.3	100	0.25	0.062	0.25	24	0.001	0.25
Power(μW)	1900	6.5	130.41	23.04	0.037	30	1330	15	2.16
SNR/SNDR(dB)	90.7/90.1	–/84.3	69.6/60.3	–/78	54.7/53.3	93/91	91.7/84.9	–/78	80.1/78.4
FoM_W(pJ/Conv.)	1.45	0.81	0.77	7.1	0.79	2.07	1.85	1155	0.63

1. *Structure with IA, 2. FoM$_W$ $= Power/(2^{(SNDR-1.76)/6.02} \times 2 \times BW)$.

experiment was conducted in a dark environment to measure the amount of light reflected from the capillaries using LEDs, as mentioned in Section II. Fig. 9(b) presents the final measured real-time ECG waveform, where the PQ interval is approximately 0.20 s, and the lowest change in R voltage is from 2 to 25 mV. Evidently, the ECG acquisition system operated correctly and the performance of the proposed CTDSM was successfully verified using the fabricated ECG acquisition system.

IV. CONCLUSION

A 2.16 μW low-power third-order single-bit CTDSM for ECG signal acquisition is presented in this brief. The proposed low-power CTDSM uses a mixed-integrator structure and an improved-linearity G_m block. The proposed mixed structure consists of an A-RC integrator for the INT1 and G_m-C integrators for INT2 and INT3 to reduce the power consumption. Owing to the large input resistance of the second integrator, a single-stage OTA working in the weak inversion region is used in the first integrator to reduce power consumption, instead of a conventional two-stage OTA. Overall, it was verified that the proposed single-bit CTDSM uses less power.

ACKNOWLEDGMENT

The chip fabrication and EDA Tools were supported by the IC Design Education Center (IDEC).

REFERENCES

[1] P. Crombez, G. Van der Plas, M. S. J. Steyaert, and J. Craninckx, "A single-bit 500 kHz-10 MHz multimode power-performance scalable 83-to-67 dB DR CT$\Delta\Sigma$ for SDR in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1159–1171, Jun. 2010.

[2] M. Honarparvar, J. M. de la Rosa, and M. Sawan, "A 0.9-V 100-μW feedforward adder-less inverter-based MASH $\Delta\Sigma$ modulator with 91-dB dynamic range and 20-kHz bandwidth," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 3675–3687, Nov. 2018.

[3] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta–Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2017.

[4] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. New Delhi, India: Pearson, 2015.

[5] H. Roh, H. Kim, Y. Choi, J. Roh, Y.-G. Kim, and J.-K. Kwon, "A 0.6-V delta–sigma modulator with subthreshold-leakage suppression switches," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 825–829, Nov. 2009.

[6] J. Kim, S. Song, and J. Roh, "A high slew-rate enhancement class-AB operational transconductance amplifier (OTA) for switched-capacitor (SC) applications," *IEEE Access*, vol. 8, pp. 226167–226175, 2020.

[7] D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS Op Amps," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 1, pp. 8–14, Jan. 2004.

[8] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill, 2017.

[9] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*. Hoboken, NJ, USA: Wiley, 2012.

[10] T. B. Kumar, S. K. Kar, and D. Boolchandani, "A wide linear range CMOS OTA and its application in continuous-time filters," *Anal. Integr. Circuits Signal Process*, vol. 103, pp. 283–290, May 2020.

[11] J.-S. Bang, H. Jeon, M. Je, and G.-H. Cho, "6.5μW 92.3dB-DR biopotential-recording front-end with 360mVpp linear input range," in *Proc. IEEE Symp. VLSI Circuits*, Oct. 2018, pp. 239–240.

[12] P. C. C. de Aguirre and A. A. Susin, "A 0.6-V, 74.2-dB DR continuous-time sigma–delta modulator with inverter-based amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 10, pp. 1310–1314, Oct. 2018.

[13] A. Nikas, S. Jambunathan, L. Klein, M. Voelker, and M. Ortmanns, "A continuous-time delta–sigma modulator using a modified instrumentation amplifier and current reuse DAC for neural recording," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2879–2891, Oct. 2019.

[14] T. Kulej, F. Khateb, and L. H. C. Ferreira, "A 0.3-V 37-nW 53-dB SNDR asynchronous delta–sigma modulator in 0.18-μm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 2, pp. 316–325, Feb. 2019.

[15] A. Boni, L. Giuffredi, G. Pietrini, M. Ronchi, and M. Caselli, "A low-power sigma–delta modulator for healthcare and medical diagnostic applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 207–219, Jan. 2022.

[16] R. S. A. Kumar and N. Krishnapura, "Multi-channel analog-to-digital conversion techniques using a continuous-time delta-sigma modulator without reset," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 3693–3703, Nov. 2020.

[17] J. Aymerich *et al.*, "A 15-μW 105-dB 1.8-Vpp potentiostatic delta-sigma modulator for wearable electrochemical transducers in 65-nm CMOS technology," *IEEE Access*, vol. 8, pp. 62127–62136, 2020.