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A Novel 3D 2TnC FeRAM Architecture and Operation Scheme with Improved Disturbance for High-Bit-Density Dynamic Random-Access Memory

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Abstract: In this paper, we proposed the development of stackable 3D ferroelectric random-access memory (FeRAM), with two select transistors and n capacitors (2TnC), to address scaling limitations for bit density growth and the complicated manufacturing of 3D dynamic random-access memory (DRAM). The proposed 3D FeRAM has a 3D NAND-like architecture, with stacked metal–ferroelectric–metal (MFM) capacitors serving as memory cells in a unit string. A similar manufacturing process is used to achieve a cost-effective process and high bit density for next-generation DRAM applications. The two access transistors, string–select–line (SSL) and ground–select–line (GSL), are perfect string selections. We confirmed that the grounded back gate (GBG) of the proposed architecture can significantly improve the worst disturbance case compared to a floating back gate (FBG) like the 1TnC structure. Also, we confirmed the feasibility of performing the random-access operation during the read operation regardless of the data pattern of the selected string.

Keywords: 3D DRAM; 3D NAND Flash; 2TnC; non-volatile memory; disturbance

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1. Introduction

The demand for RAM devices has increased explosively with the development of data centers, cloud computing, artificial intelligence, autonomous driving, and social network services (SNSs) [1,2]. To achieve high-density random-access memory, 2D dynamic random-access memory (DRAM) was scaled down continuously. However, it finally encountered scaling challenges like sensing margin degradation, due to scaled-down cell capacitance, and reliability issues, such as data retention by the leakage current [3]. As shown in Figure 1a, 3D DRAM is one of the realistic candidates for next-generation DRAM applications to address these issues. However, it has several challenges, such as high manufacturing costs and the scaling limitations of the cell [4,5]. Several next-generation memory technologies have been introduced as alternatives to overcome the limitations of DRAM, including Capacitor-less 1T DRAM, resistive random-access memory (ReRAM), and magnetoresistive random-access memory (MRAM). Capless 1T DRAM [6,7] faces reliability issues, such as the degradation of data retention. ReRAM [8,9] is constrained by device variability and challenges in fabrication processes, while MRAM [10,11] suffers from high power consumption and the complexity of its manufacturing requirements.

Hafnia-based FeRAM is a promising candidate for achieving high speeds and low power, possessing non-volatile memory characteristics [6]. FeRAM is highly suitable for DRAM applications. To identify stored data, FeRAM uses a destructive read-out method, which senses the charge flow to the bit line (BL) by polarization switching during the read operation [12,13]. However, the charge-based sensing has a clear limitation in that sufficient areas and polarization charges are needed to ensure a definite sensing margin, and this

means that scaling for bit density growth is limited [3]. Recently, stackable 3D FeRAM with multi-capacitors configurations and ternary content addressable memory (TCAM) for in-memory computing neuromorphic applications involving metal–ferroelectric–metal oxide semiconductor (MFMOS) structures have also been reported [12,14–19]. However, they still have reliability issues, in which unintentional polarization switching occurs, called 'disturbance', in unselected memory cells during array-level operations. The reported structures share the metal storage electrodes with other cells, which are connected in parallel to MFM capacitors and the plate line (PL) used as the shared electrodes of the memory cells.

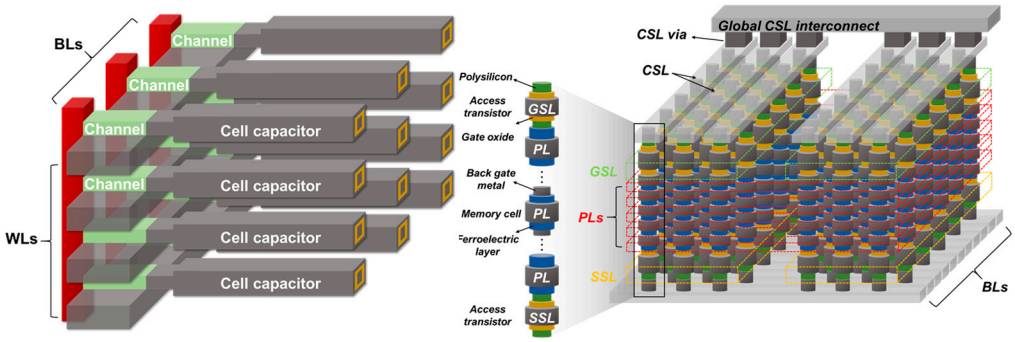


Figure 1. A bird's eye view of the (**a**) 3D VS-DRAM array and the (**b**) proposed 3D 2TnC FeRAM cell array.

To address these issues, a novel approach is required from architectural and operational perspectives. In this paper, we proposed a stackable 3D 2TnC FeRAM with a 3D NAND-like architecture to improve bit density while reducing manufacturing costs for the DRAM application, as shown in Figure 1b. The architecture has a staggered memory pillar structure, and each memory pillar has a stacked gate-all-around (GAA)-type MFM capacitor for memory cells. The 3D DRAM architecture in Figure 1a requires more area per layer due to its horizontally arranged capacitors. In contrast, the proposed 3D 2TnC FeRAM structure in Figure 1b vertically stacks the capacitors, maximizing spatial efficiency and achieving a higher integration density within the same area, thus making its use more cost-effective during the manufacturing process. We confirmed the feasibility of the read/write operation as the array-level simulation of the proposed architecture using Sentaurus Technology computer-aided design (TCAD) simulations. We further investigated the alleviated critical disturbance case in inhibited strings. This occurs at the memory cells that the share selected PL (PLSEL) with the grounded common source line (CSL) through a GSL transistor. This structure eliminated the floating state of the back gate storage node. Finally, to perform the clear identification of the multi-bit RAM with cell stacking, we proposed a read operation scheme for the proposed structure.

2. Three-Dimensional 2TnC FeRAM Architecture

Figure 2 illustrates detailed 3D images of the 3D 2TnC FeRAM architecture and its schematic diagram. As shown in Figure 2a, there are cell arrays, staircases, and various interconnections in the proposed architecture. In Figure 2b, we provide a 3D schematic diagram of the proposed architecture, and there are interconnections for PL, SSL, GSL, and CSL. PL and CSL are shared with the strings in a unit block. The cross-sectional view of the cell array region is illustrated in Figure 2c. The SSL and GSL transistors are located at the top and bottom of the strings. The 3D NAND architecture has separated GSL and SSL transistors. Memory cells are parallel-connected MFM capacitors formed with PLs, a ferroelectric layer, and a metal-based back gate. The back gate serves as the storage node of the 1T1C DRAM, and it is shared with the whole memory cell in the unit string. Figure 2d shows a detailed cross-sectional view of the staircase. The interconnections to the

peripheral circuit are produced through hybrid bonding. Finally, the top cross-sectional views of each CSL plane and BL plane on the cell array region are illustrated in Figure 2e,f. As shown in Figure 2e, CSL is shared with whole strings in the unit block. The GSLs (GSL_1 and GSL_2) are isolated using a GSL slit for the string selection's connection to the CSL. The top view of the bit line (BL) direction is shown in Figure 2f. Three BLs pass through the top of a memory hole, and each BL is connected with different memory holes. The BLs are shared with several strings in the other blocks and the SSL activates the selected string. To identify the selected string for a read/write operation, the SSLs (SSL_1 and SSL_2) are isolated with SSL slits.

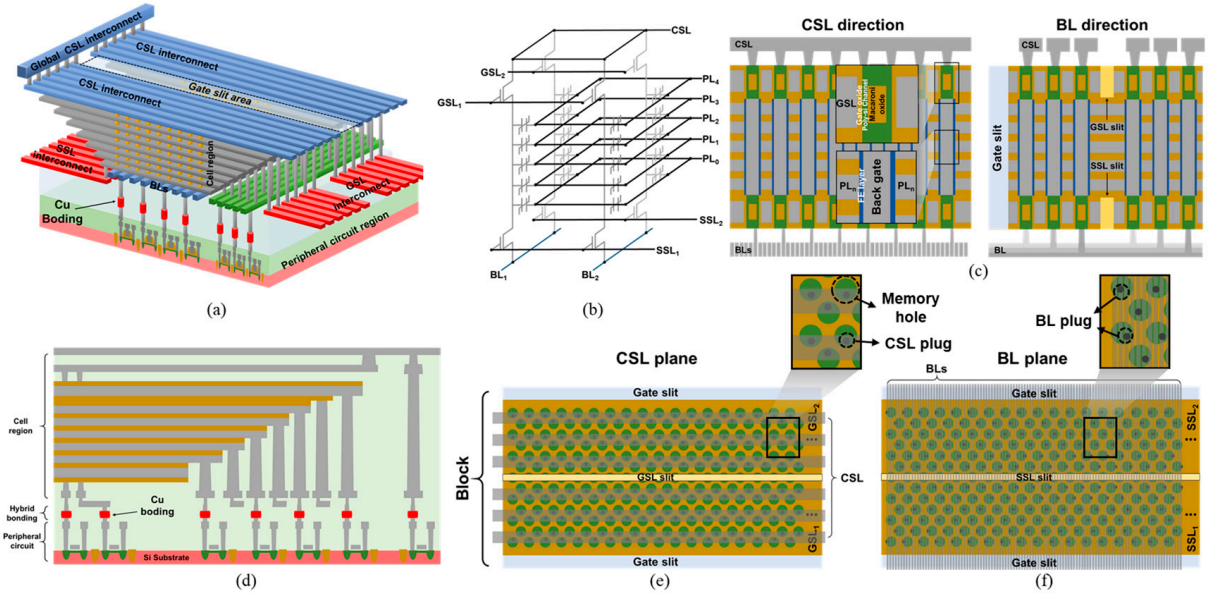


Figure 2. Various views of the proposed architecture. (**a**) A bird's eye view of the proposed architecture; (**b**) a schematic diagram of 3D 2TnC FeRAM; (**c**) cross-sectional views of the cell array region; (**d**) a cross-sectional view of the staircase in the proposed architecture; a top view of (**e**) the CSL plane; the (**f**) BL plane in the cell array.

Figure 3 shows the manufacturing process flow of the proposed architecture. First, oxide–nitride (ON) stacking for the GSL and hole etching with polysilicon deposition are executed. In contrast to the 3D NAND Flash process, the ON stack is etched by GSL cutting, the GSL slit is filled with oxide, and the CMP is executed. After the GSL formation process ends, multiple ON layers used for memory cells are deposited above the GSL. Next, memory holes are etched, the ferroelectric layer is deposited, and the back gate metal is inserted into the memory hole. SSL is then formed by repeating the same process on the memory cell stacks. After these processes, gate slit etching, gate oxide oxidation, and gate replacement processes are required, just as in 3D NAND Flash. CSL metal interconnections are formed after hybrid bonding and CMP are used to access the back side for further processing. Cost-effective manufacturing can be achieved with this 3D NAND-like process flow and architecture.

Since the memory cells used in this 3D NAND-like architecture are vertically aligned within pillars, and as the SSL and GSL lines are only selectively placed on essential layers, the manufacturing process used in this work maintains a consistent number of lithography steps regardless of the number of layers. This enables maximal spatial efficiency in the cell array structure, resulting in a reduction in the overall costs associated with the lithography process.

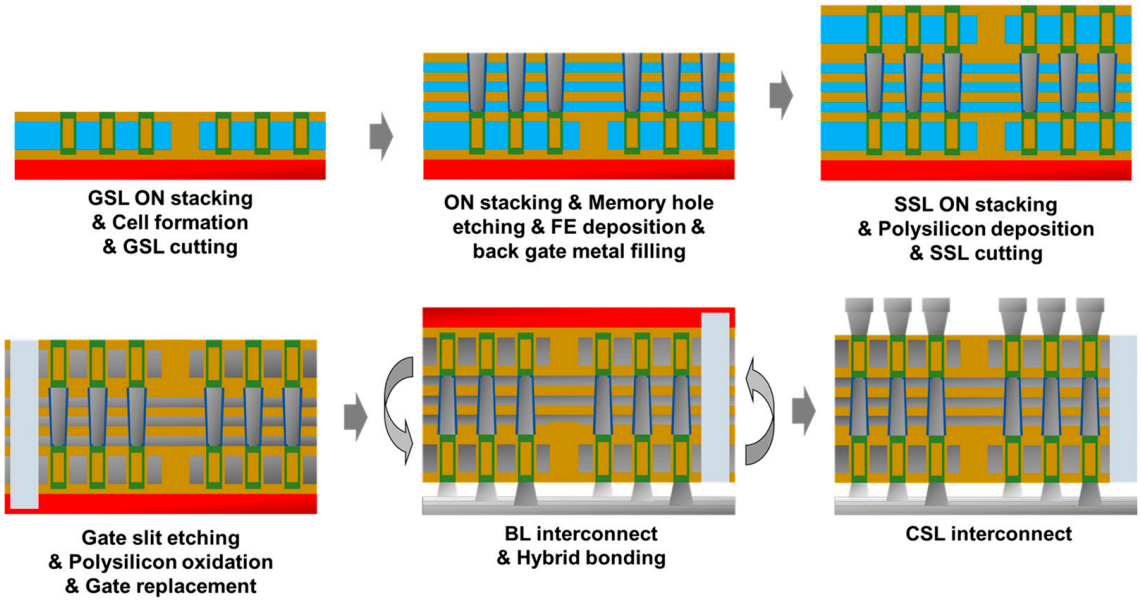
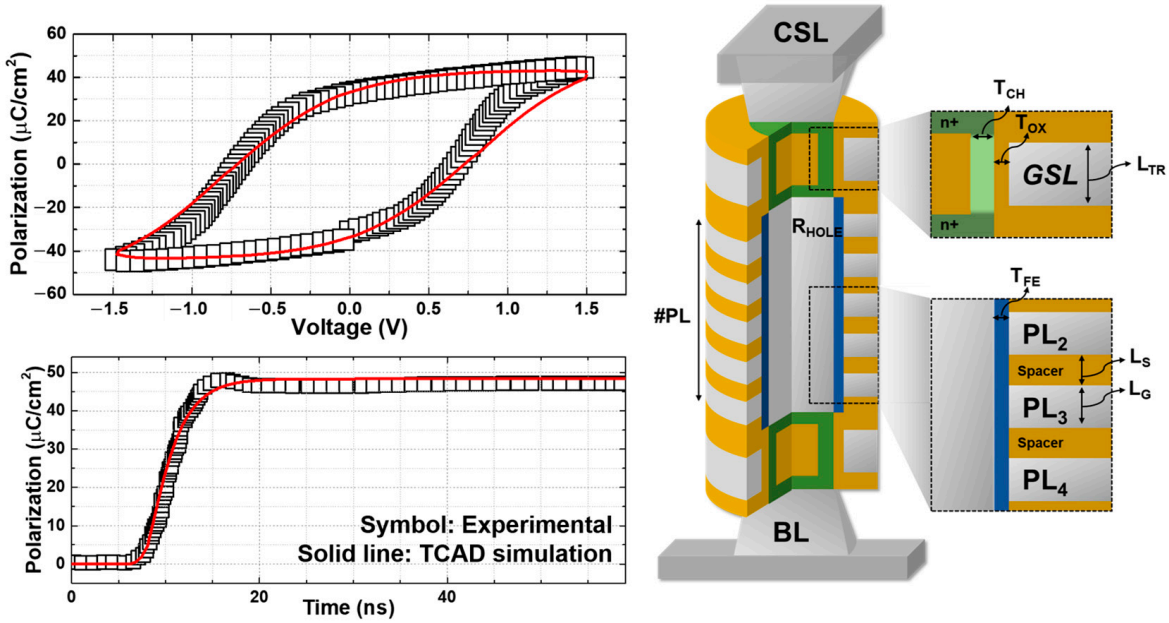


Figure 3. The manufacturing process of the 2TnC 3D FeRAM.

3. TCAD Simulation Setup

To simulate the proposed architecture, the material parameters were derived from a previous study on $Hf_{0.5}Zr_{0.5}O_2$ [18]. As shown in Figure 4a, the experimental polarization–electric field (P-E) hysteresis curve and switching kinetics of the previous study were calibrated with an MFM (TiN-HZO-W) capacitor. Material parameters, calibrated based on measurement data, are listed in Table 1. The device simulation for the P-E curve with the MFM capacitor was performed by using a Preisach model for the ferroelectric material to represent multi-domain switching [20,21].



(**a**) Experimental: Ramaswamy et al. (2023) (**b**)

Figure 4. (**a**) Polarization–voltage (P-V) curve and the switching dynamic curve of the experimental measurement [18] and the TCAD simulation calibration result. (**b**) The cross-sectional view of the unit string structure and the parameters used in TCAD simulation.

Table 1. Material and design parameters used in TCAD simulation.

	Parameter (Symbol)	Value (Unit)
Material parameter	Saturation polarization (Ps)	54 ($\mu C/cm^2$)
	Remnant polarization (Pr)	38 ($\mu C/cm^2$)
	Coercive field (Ec)	1.3 (MV/cm)
	Relaxation time (τ)	2 (ns)
	Dielectric constant (ε_{FE})	25 (ε_0)
	Doping concentration of polysilicon	1×10^{20} (cm^{-3})
Design parameter	Number of PL	5
	Selected PL	2
	Gate length of the memory cell (L_G)	100 (nm)
	Spacer length (L_S)	60 (nm)
	Ferroelectric layer thickness (T_{FE})	5 (nm)
	Radius of memory hole (R_{HOLE})	100 (nm)
	Gate length of access transistor (L_{TR})	150 (nm)
	Gate oxide thickness of access transistor (T_{OX})	5 (nm)
	Polysilicon channel thickness (T_{CH})	20 (nm)

Figure 4b shows a cross-sectional view of 3D 2TnC FeRAM, which is used in TCAD simulation. The proposed structure incorporates GAA-type transistors and MFM capacitors, with their design parameters detailed in Table 1. To confirm the cell's characteristics, we used the cylindrical computing method in the TCAD simulation [22]. The cell had a 100 nm memory hole radius (R_{HOLE}), a 100 nm gate length (L_G), and 5 nm ferroelectric layer thickness (T_{FE}). These were the design parameters used for calculating the sensing margin of the 3D FeRAM [15]. The polysilicon contact regions with the BL plug, CSL plug, and the back gate metal must be heavily doped with an n-type dopant to form ohmic contacts; however, channel regions of the GSL and the SSL consist of undoped polysilicon. The 2T5C FeRAM structure, consisting of 5 stacked memory cells, was simulated to confirm the read/write operation, with the 2nd PL serving as the target cell. For the polysilicon channel in the SSL and GSL transistors, the Shockley–Read–Hall (SRH) recombination model and the drift–diffusion model were adopted to calculate carrier transport. Additionally, the Hurkx band-to-band tunneling model was employed to evaluate the leakage current [22].

4. Simulation Results and Discussion

4.1. Basic Operation Characteristics

Figure 5a shows the array operation scheme of the proposed architecture. During the operation, V_{ON} (=2 V) and V_{OFF} (=−2 V) are applied to each selected SSL (SSL_{SEL}) and each selected GSL (GSL_{SEL}) to select a string for use in the memory array. On the other hand, V_{OFF} and V_{ON} are applied to inhibit SSL (SSL_{Inh}) and inhibit GSL (GSL_{Inh}), respectively. The operation voltage ($\pm V_{DD}$), which induces polarization switching in the target cell, is applied separately to BL and PL. The V_{DD} in our simulation is 1.5 V, which aligns with values reported in recent studies on 3D FeRAM, ranging from 1.5 V to 2 V [14,23]. Thus, power consumption from the operation voltage is expected to be comparable to that achieved in recent studies. That is, $\pm 2/3 V_{DD}$ and $\mp 1/3 V_{DD}$ are applied to each BL and each selected PL (PL_{SEL}). Unselected inhibited PLs (PL_{Inh}) are applied at $\pm 1/3 V_{DD}$ under coercive voltage. In the case of the read operation, $-V_{DD}$ and GND are applied to PL_{SEL} and selected BL (BL_{SEL}), respectively, to fully switch the polarization of the target cell. Figure 5b shows the 3D schematic diagram of the proposed architecture in relation to the voltage condition during each operation. Because the SSL_{SEL} is turned on and the GSL_{SEL} is turned off, the electrostatic potential of the back gate in the selected string increased to the voltage of the BL_{SEL}.

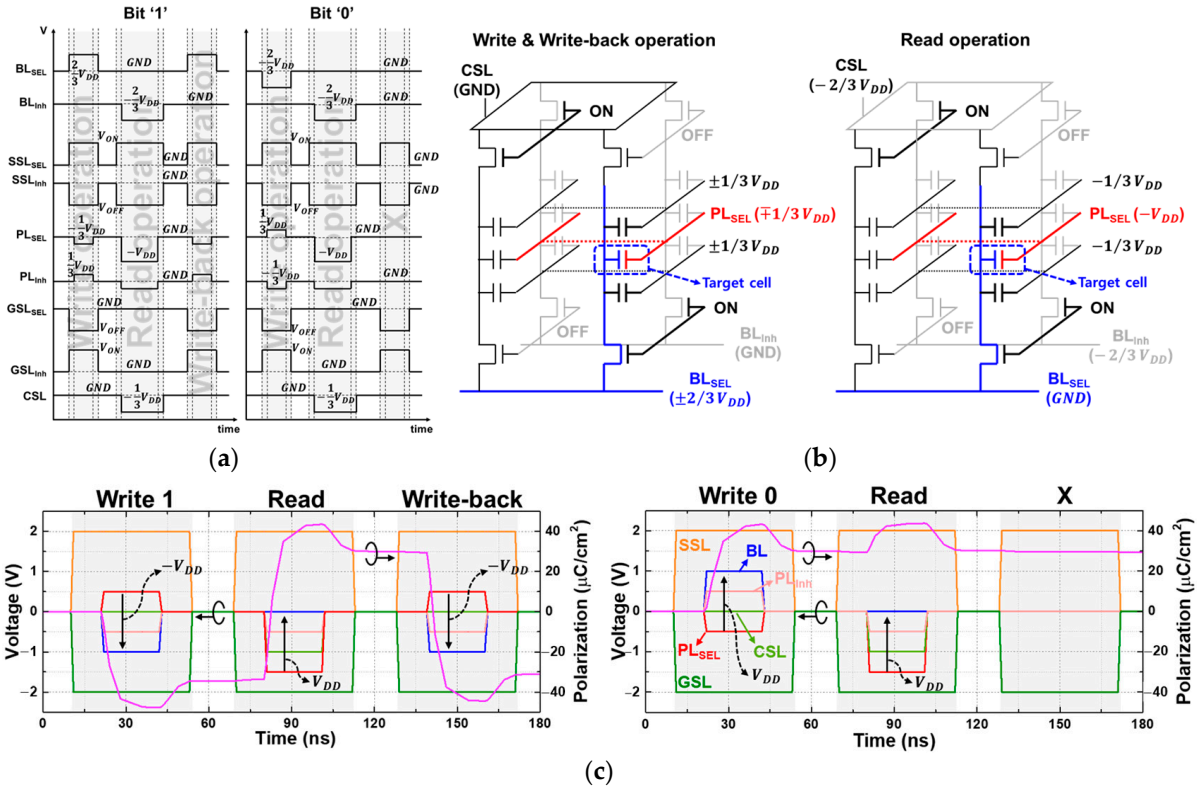


Figure 5. (**a**) The timing diagram of write/read/write back operation of the proposed structure. (**b**) Three-dimensional array schematic diagram, showing the voltage condition of the proposed architecture, for random-access operations. (**c**) The polarization density of write/read/write back operation in the selected string.

However, the other back gates are successfully configured, potentially through BL_{Inh} and CSL, to prevent the operation via these inhibited strings. As a result, Figure 5c shows the polarization density according to each operation in the target cell in the selected string. The operation speed in our simulation, which is the read/write time (50 ns as shown in Figure 5c), is faster compared to the write/read operation time reported in [24]. In the case of writing bit 0, the polarization density switches to +Ps and finally relaxes to +Pr after the operation ends. On the other hand, in the case of writing bit 1, the target cell exhibits a polarity opposite to that of bit 0. During the read operation, the polarization of bit 1 in the target cell is fully switched to +Ps and then relaxed to +Pr, the same as with bit 0. For bit 1, the fully switched polarization after the read operation necessitates a 'write-back' operation to restore the previous data.

4.2. Disturbance in Array-Level Operation

The inevitable sharing of PL with unselected memory cells induces an unintentional electric field by applying the stress voltage ($V_{Disturb}$) across the FE layer. Thus, the disturbance must be considered during the operation of the proposed 2TnC FeRAM because it has a NAND-like architecture. Thus, we must minimize $V_{Disturb}$ [25]. With the proposed operation in Figure 5, we can control $V_{Disturb}$ to be under $\pm 1/3 V_{DD}$. Figure 6a shows two disturbance cases, similar to those in 3D NAND Flash memory, that exist in 3D 2TnC FeRAM. First, we investigated program (PGM) disturbance, which occurs at cells sharing SSL_{SEL} in inhibited strings with X/Y/XY modes. Second, pass disturbance occurs at unselected cells in the whole string in the block that shares unselected PL. To investigate the disturbance in inhibited strings, we used the back gate with two states to compare the disturbance.

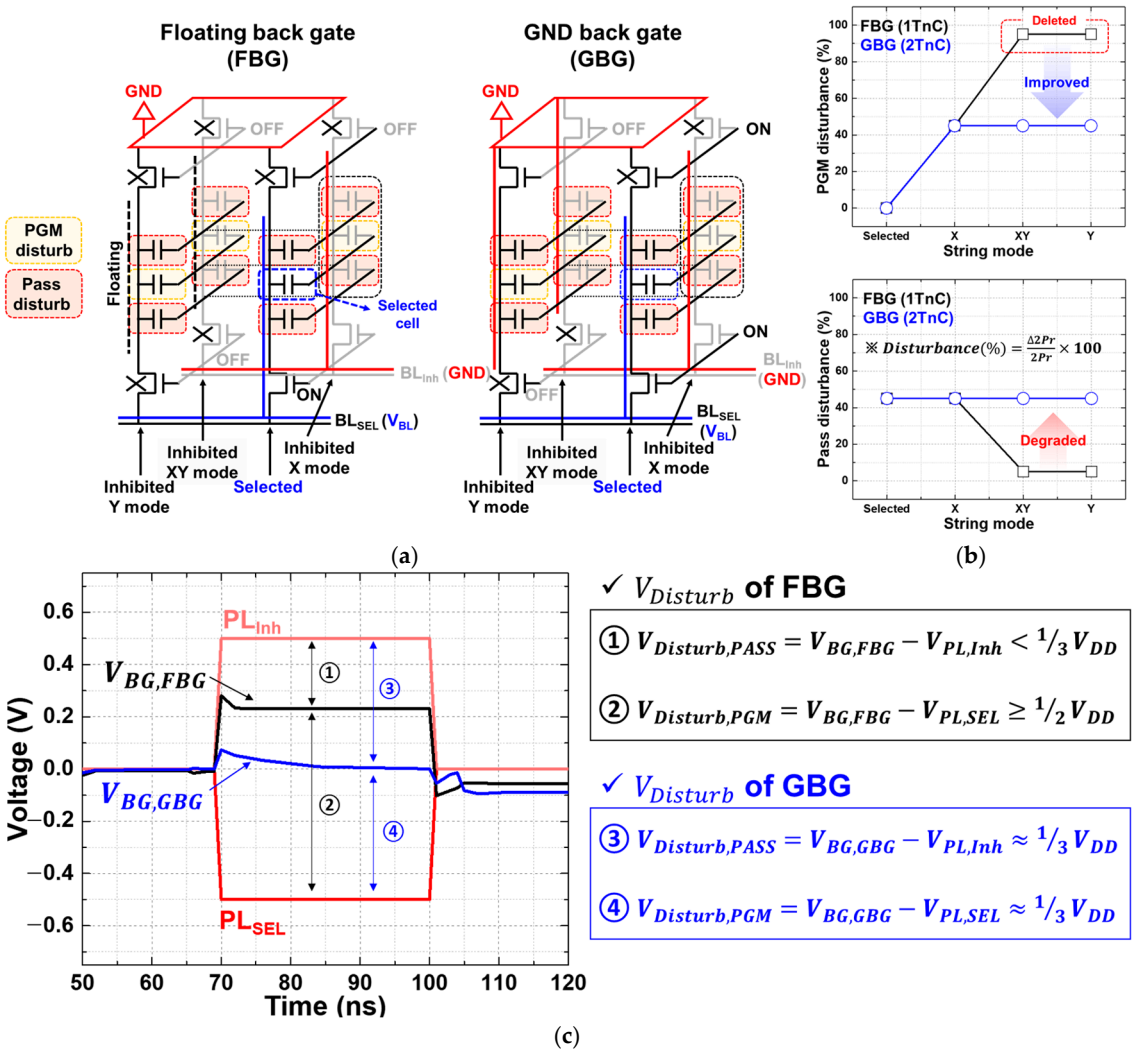


Figure 6. (**a**) Back gate states during the read/write operation of the proposed structure. (**b**) Two types of disturbance cases, with the single stress pulse depending on the back gate state. (**c**) Back gate potential transfer curve during a writing operation in the inhibited Y/XY mode.

We used the back gate with the floating state in Y/XY modes (FBG), in which the GSL and the SSL are turned off to float the back gate, the same as occurs in 1T1C FeRAM. The second case is the grounded back gate (GBG), which is connected to the grounded CSL of this proposed architecture. As shown in Figure 6b, ΔPr, which means the degradation of the polarization, is compared to previous Pr values during pass and PGM disturbance is confirmed. The pass disturbance of FBG is degraded (below 5%), and it has immunity to pass disturbance. However, the PGM disturbance of FBG is severely degraded, being nearly 95% at Y/XY modes.

This severe reliability issue in FBG must be addressed. In the case of GBG, PGM disturbance and pass disturbance are uniformly degraded by less than 45%. As shown in Figure 6c, we investigated the potential impact of the back gate metal (V_{BG}) on disturbed states through simulation results. Because of the high-k ferroelectric material, the V_{BG} of FBG increased to a value close to the voltage of the PL_{Inh} via capacitive coupling with PLs and the small electric field formed across the FE layer between the back gate and PL_{Inh} in Y/XY mode strings [25]. Thus, pass disturbance in the Y/XY mode is improved by boosted V_{BG}. However, PGM disturbance is severely degraded by the large electric field across the FE layer of the cells, which shares PL_{SEL} in the Y/XY mode. In the case of GBG, PGM disturbance is improved by controlling $V_{Disturb}$ using the grounded back gate.

4.3. Data Sensing with Multi-Capacitors

FeRAM identifies the stored data with voltage sensing similar to that of a conventional DRAM. During the read operation in Figure 5c, different amounts of charge from polarization switching flow to the BL, inducing a rise in BL voltage, and this charge flow can be confirmed as a BL current [22]. Figure 7a shows the current transfer curve corresponding to the target memory cell of the 2T1C FeRAM. Current peaks are used to identify the stored data, and offsetting the current peaks is a standard of the sensing margin. However, 3D FeRAM with parallel-connected capacitors still suffers from unintended charge flow induced by the pass disturbance during the read operation. This noise current, which means that the ΔBL current between 'Number of bit 1' = 0 and 4 (except for the stored data in target cell), must be considered to ensure the reliability of the proposed architecture. Figure 7b shows the BL current of each stored data in the target cell depending on the data pattern in Table 2. The BL current of each bit, 1 and 0, increased with the increasing the number of bit 1 in the selected string, and the minimum sensing margin was significantly degraded by the pass disturbance.

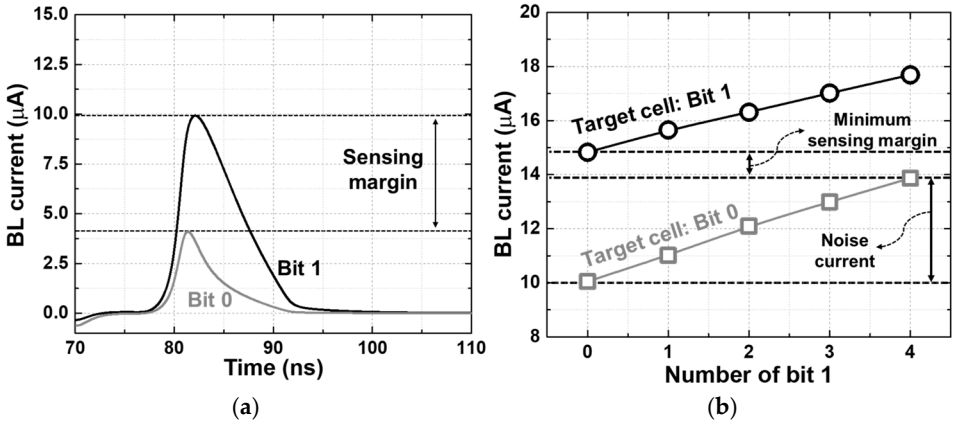


Figure 7. (**a**) The BL current of FeRAM during the read operation. (**b**) The BL current peak depending on the data pattern in the selected string of the 2T5C FeRAM.

Table 2. Data pattern stored in a selected string.

Number of Bit 1	Data Pattern in Selected String (PL_4-PL_3-PL_2-PL_1-PL_0)	Target Cell (PL_2)
0	00x00	0 or 1
1	00x01, 00x10, . . ., 10x00	
2	00x11, 01x01, . . ., 11x00	
3	01x11, 10x11, . . ., 11x10	
4	11x11	

To mitigate the charge flow from the unselected cells, we proposed the use of a read operation scheme using a dummy pulse in Figure 8a. GSL is activated to connect the back gate to the CSL with biasing at PL_{Inh}, referred to as the 'dummy pulse'. As soon as the dummy pulse ends, SSL is turned on to connect the back gate to the BL. This is the main read pulse used to detect the charge flow resulting from the polarization switching of the target cell. The current paths during the dummy pulse and the read pulse of the proposed read operation are shown in Figure 8b. During the dummy pulse, the current path of noise induced by pass disturbance is directed to the CSL instead of the BL, while the charge from the target cell flows to the BL during the read pulse. Based on the proposed read operation, Figure 9a shows the BL current for each operation scheme according to the data pattern shown in Table 2. The total BL currents of both bit 0 and 1 are reduced compared to the 'without (W/O) dummy pulse' read scheme. However, the BL current of the proposed 'with the (W) dummy pulse' read scheme is uniform and independent of

the data pattern. These results mean that the BL current from unselected memory cells is successfully eliminated, resulting in improved reliability. Consequently, the sensing margin of the proposed structure improved, as shown in Figure 9b. Notably, the noise ratio improved by up to 94% compared to the W/O dummy pulse read scheme, confirming that the proposed W dummy pulse read operation is suitable for the 3D 2TnC FeRAM in terms of achieving multi-bit sensing.

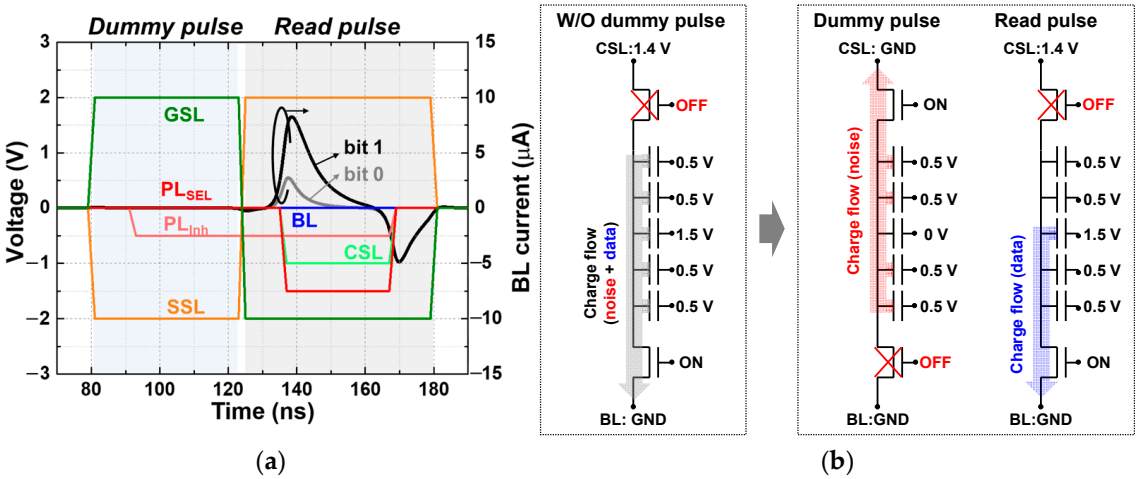


Figure 8. (**a**) The timing diagram of the proposed read operation scheme with dummy pulse. (**b**) The current paths used during read operation.

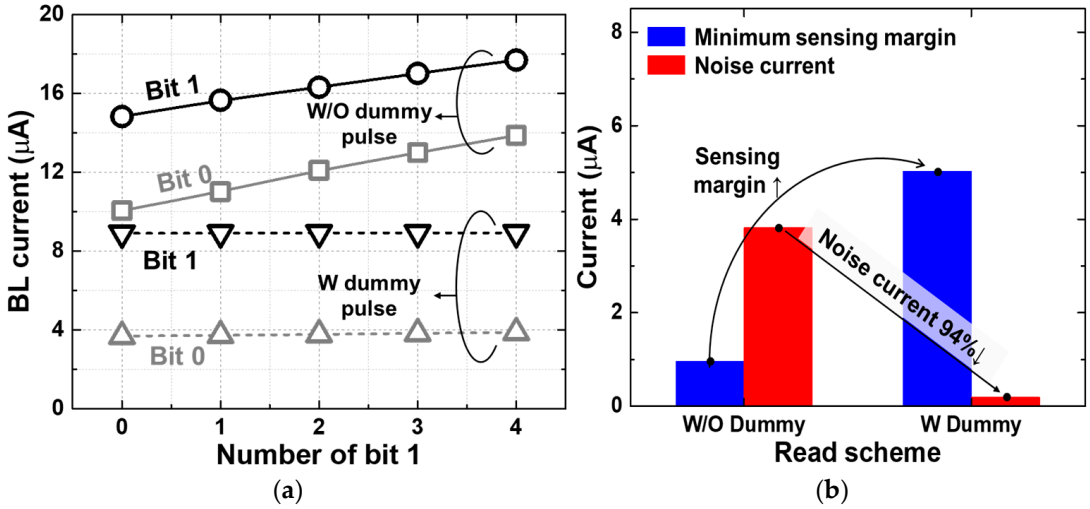


Figure 9. (**a**) BL current of the without (W/O) dummy pulse (solid line) and with (W) dummy pulse (dash line) according to the data pattern shown in the selected string. (**b**) The sensing margin and noise current of each read scheme.

5. Conclusions

In this paper, we proposed a stackable 3D 2TnC FeRAM architecture to increase bit density and lower manufacturing costs. We confirmed that the disturbance was suppressed compared to the FBG of 1TnC with the GBG state during operations. Also, the proposed read operation with a dummy pulse led to the successful n-bit sensing of the parallel connected MFM capacitors in the unit string without affecting the data pattern in the selected string. Based on these simulation results, we confirmed the feasibility of the proposed architecture and noted that it may be an emerging candidate for high-bit-density DRAM applications.

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