IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

IEEE POWER & ENERGY SOCIETY SECTION

Received 3 March 2025, accepted 30 March 2025, date of publication 1 April 2025, date of current version 10 April 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3556936

RESEARCH ARTICLE

Fault Current Limiter and Mechanical DC CB-Based Protection Against Valve-Side SPG Faults in HB-MMC Bipolar System

MUHAMMAD USMAN, YU-JIN KWAK, AND BANG-WOOK LEE, (Senior Member, IEEE)
HVDC Electric Power Laboratory, Department of Electrical and Electronic Engineering, Hanyang University, Ansan 15588, South Korea

Corresponding author: Bang-Wook Lee (bangwook@hanyang.ac.kr)

This work was supported in part by Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by Korean Government of the Ministry of Trade, Industry, and Energy (MOTIE) through the DC Grid Energy Innovation Research Center under Grant 20224000000160; and in part by KETEP of Republic of Korea under Grant 20225500000150.

ABSTRACT Valve-side single-phase-to-ground (SPG) faults are atypical yet critical for the operation of half-bridge (HB) Modular Multilevel converter (MMC) bipolar or asymmetrical monopolar systems. For the impacted converter station, these faults may result in non-zero crossing currents on the connected AC grid and cause significant overvoltage on upper arm submodule (SM) capacitors. This article presents an SPG valve-side fault mitigation strategy using a power electronic (PE) fault current limiter (FCL) installed at the grounded terminal of the MMC converter, along with a mechanical DC breaker on the DC transmission line. The FCL transfers converter ground current to a resistive branch during the SPG fault, resulting in zero crossing currents on the AC side of the grid, thus ensuring fault current clearance by grid-side AC circuit breakers. Moreover, the proposed topology limits the fault current magnitude, reducing the impact of SPG valve-side faults on the AC grid. The discontinuous DC line current is cleared by a fast mechanical DC circuit breaker, halting the charging of the upper arm SM capacitor and limiting the overvoltage stress on converter insulation. In addition, the severity of upper arm SM overvoltage in case of SPG fault in long distance HB-MMC bipolar links has been assessed, and the prospect of a passive oscillation DC circuit breaker to curb such overvoltage has been demonstrated. The effectiveness of the protection topology has been verified through PSCAD/EMTDC software and compared with previously proposed SPG fault clearance methods.

INDEX TERMS MMC-HVDC bipolar links, dc circuit breaker, passive oscillation dc circuit breaker, single-phase valve-side MMC fault, PSCAD/EMTDC program.

I. INTRODUCTION

The goal of bulk power transmission through long-distance DC interconnections has attracted the attention of energy subsidiaries and researchers toward bipolar VSC-HVDC links, in contrast to the existing systematic monopolar scheme [1], [2]. Such links can be operated as an asymmetric monopole during single-pole maintenance, ensuring reliable power supply [3], [4]. Currently, NORDLINK, rated at ±525kV/1.4 GW, is one of the world's latest bipolar systems in service [5], [6]. Transformer/valve-side single-phase-to-ground (SPG) faults are rare but peculiar issues in MMC-VSC bipolar converters that have gained attention in recent years [7], [8], [9], [10], [12], [13], [14], [15].

An SPG fault in a half-bridge (HB) MMC station with low-impedance grounding results in non-zero crossing currents on the AC grid, which cannot be cleared by grid-side AC circuit breakers (ACCB) [9]. Issue of non-zero crossing grid-side currents could be resolved by utilizing full-bridge (FB) MMC topology at the expense of additional power electronic components [8], [10], [14]. Additionally, MMC upper arm submodules (SM) experience capacitor charging during the blocked state, which results in upper arm overvoltage, straining the insulation of the converter station. Permanent or temporary SPG faults between the converter valve and transformer occur due to insulation failure or flashover at

The associate editor coordinating the review of this manuscript and approving it for publication was Dragan Jovcic.

wall bushings that separate them [8]. Corrosion or water infiltration in valve cables could also lead to SPG faults.

Various methods to resolve the above-discussed internal HB-MMC converter fault have been devised in [9], [11], [12], [13], [14], [15], and [22]. These methods can be classified into three categories: dedicated equipment-based methods, auxiliary converter-circuitry based methods, and hybrid MMC converter methods (combination of half-bridge submodules (HBSM) and full-bridge submodules (FBSM). Dedicated equipment methods, as the name implies, consist of protection equipment on either the AC or DC side of the converter station. For example, the Skagerrak HVDC transmission system utilizes earthing breakers on the grid-AC side [11], artificially converting valve-side SPG faults into three-phase faults to produce zero-crossing currents at the grid-side. However, slow AC circuit breaker (CB) operation, coupled with prospective voltage drops, might compromise the stability of the AC grid. Similarly, [9] proposes an RL grounding circuit for MMC converters to achieve zero-crossing current on the grid-side. However, a large inductor in the RL circuit is required to guarantee continuous zero-crossing currents on the grid-side until the ACCBs can clear SPG fault, which results in a higher magnitude of post-SPG fault valve-side voltage on healthy phases, ultimately worsening upper arm submodule (SM) overvoltage, as empirically demonstrated in [9]. Additionally, a larger RL inductor would result in a higher transient overvoltage across it during fault conditions and would raise the insulation cost of the grounded pole. Double-thyristor and anti-parallel thyristor-pair/damping-submodule based methods deploy additional circuitry with SM modules to mitigate SPG faults [12], [13]. These schemes respond faster since they utilize power electronic components. Similar to the auxiliary ACCB method, the double-thyristor method produces a three-phase fault at the converter valve side, which worsens the fault current flowing through the lower arm's power electronic equipment and the converter transformer. The latter method creates discontinuous conduction intervals in the lower arm currents through the damping modules in the MMC converter, which are ultimately cleared by the anti-parallel thyristor-pair module. However, the number of thyristor pairs required to withstand post-fault line voltage stress is high, leading to significant steady-state power losses [13]. In the hybrid SM method [14], a high FBSM-to-HBSM ratio in the lower arm is required to avoid lower arm SM overvoltage, which diminishes the economic advantage offered by the hybrid-MMC [16]. In [15], a grounded thyristor loop is introduced in a Hybrid-MMC station (with reduced FBSMs) to clear SPG faults However, an SPG fault in such a scheme cannot be cleared until the DC-side fault current is cleared which depends on the blocking of the remote converter station. Additionally, the inclusion of extra circuitry within the MMC converter increases its vulnerability to further faults.

This article proposes a ground-side fault current limiter (FCL)-based SPG fault mitigation method. The utility of FCLs in suppressing the rate-of-rise of fault current during conventional DC pole-to-pole and pole-to-ground faults has been demonstrated previously, assisting HVDC converter stations or DC circuit breakers in clearing such faults [17], [18], [19], [20], [21], [22]. During steady-state operation, FCLs do not restrict current flow, having negligible influence on the power grid. However, once a fault is detected, the FCL resists the flow of fault current, assisting in fault current clearance. Depending on the fault current limiting mechanism, FCLs can be primarily classified as resistive or inductive types [17], [18]. The scope of this paper is to assess the application of FCLs on the converter ground for SPG valve-side fault mitigation, which has not been investigated previously. It is not intended to devise a novel FCL topology in this manuscript. As implied from [12] and [13], induction-type FCLs would not be suitable for converter station grounding. Resistive-type FCLs can be further classified as power electronic (PE) resistive FCLs and superconductive FCLs (R-SFCL) [19], [20], [21]. Here, a PE-FCL is utilized to mitigate SPG valve-side faults in HB-MMC bipolar systems.

Recent researches address the upper arm SM capacitor charging by blocking it utilizing anti-parallel thyristor pair [13], [14]. Although high-speed DC circuit breakers (5)-10 ms) could prevent upper arm SM capacitor charging, they are not considered a viable solution for such overvoltage faults due to their high cost and on-state losses (in the case of hybrid DC CBs) [22]. However, because of the discontinuous nature of line current and the relatively slower progression of SM capacitor charging in the case of blocked faulty HB-MMC converter station under an SPG fault, mechanical DC CBs and passive oscillation-type DC circuit breakers could be utilized for upper arm overvoltage prevention. These DC CBs have a fault clearance time of 14-30 ms but are more economical compared to state-of-the-art DC CB topologies [23], [24]. The clearance of conventional DC-side faults through the coordinated operation of DCCBs and hybrid-MMC converter station blocking has been investigated previously [25], [26]. The utility of mechanical DC CBs in conjunction with blocked faulty converter station in preventing severe SM overvoltage has been investigated in this manuscript.

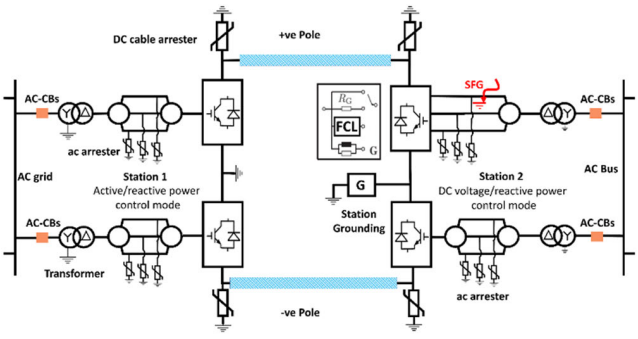

FIGURE 1. General model of an HVDC HB-MMC point-to-point bipolar link.

Salient contribution of this manuscript include:

- Assessment of converter grounding PE-FCL in limiting and clearing non-zero-crossing grid-side fault currents caused by SPG valve-side faults in a bipolar MMC converter station.
- Evaluation of the utility of a mechanical DC CB in suppressing upper arm SM overvoltage, with and with-out the blocking of the remote converter station.
- Challenge of upper SM overvoltage suppression for long-distance overhead (OH) transmission line due to non-zero crossing line current under SPG valve-side fault have been investigated.
- Prospect of passive oscillation-type DC CBs to curb SM overvoltage for long-distance OH MMC bipolar link have been assessed, especially in cases where remote converter stations are unlikely to be blocked due to commutation delays or failures.
- A comparison of the proposed SPG valve-side fault mitigation technique with the existing solutions have been presented.

This paper is further organized as follows. Section II provides a brief description of the considered ±320 kV bipolar VSC-MMC link, along with an empirical analysis of the impact of SPG valve-side fault on the upper and lower converter arms. In Section III & IV, FCL and DC CB method is employed to resolve issues caused by SPG fault, while Section V compares the presented methods with previous ones. Finally, Sections VI and VII provide a generalized evaluation and conclusion, respectively.

II. HB-MMC TOPOLOGY DESCRIPTION

Assessment of SPG valve-side fault is carried out in a ±320kV OH HB-bipolar link as depicted in Fig. 1, with system parameters provided in Table 1. The bipolar converter station can be solidly grounded, grounded through a resistor, or use RL grounding method. In a converter station with high-resistive grounding, the grid-side current exhibits zero-crossing behavior, as negligible fault current flows through the lower arm of the converter [12]. However, to avoid higher insulation costs and the need for increased air clearance at the grounding pole, ideally, both converter stations should be solidly grounded. For a point-to-point HVDC link with one high-impedance grounding MMC station, the other converter station has to be either low-resistive or solidly grounded so that earth current can flow during normal operation [27]. In a high-impedance grounded converter station, the advantage of a low-rated earthing pole is lost. Furthermore, the steady-state post-fault voltage on the healthy pole could reach up to 2 p.u., while detection and clearance of ground faults are difficult for high-impedance grounding [27], [28]. In low-resistance or solidly grounded systems, SPG faults result in a distinct grid-side current. Given the advantages of low-resistive grounding, this study considers solidly grounded HB-MMC converters.

Each pole of the bipolar configuration can operate as an independently controlled asymmetric monopolar link; hence, only the +ve pole of the HVDC system is investigated in this section. A frequency-dependent transmission line model is used in PSCAD/EMTDC software to accurately simulate the transient response of a 400 km long transmission line. The AC side of the grid is modeled as an R/L-L equivalent circuit with a short-circuit ratio of 2.6 @ 85.9° [29]. Transmission line parameters are presented in Appendix of this manuscript.

TABLE 1. Parameters of HB-MMC bipolar DC link.

Parameters	Converter station 1st (Active power control) & 2nd (V_{dc} control)
Power rating per pole	750 MW
DC rated voltage	±320 kV
Submodules per arm	40
Transformer leakage reactance	0.1 p.u.
Transformer ratio (kV/kV)	230/175
Submodule capacitor	5.1 mF
AC frequency	60 Hz
Arm inductance (L_{arm})	50mH
Arm resistance (R_{arm})	0.2Ω
Pole reactor	50 mH
Modulation Index (m)	0.89

A. SPG FAULT CHARACTERISTIC AT UPPER ARM

Fig. 2 depicts the +ve pole of considered HB-MMC converter system. The converter transformer is in a Y/Δ configuration, which eliminates zero-sequence currents on the valve side of the MMC converter [7]. When an SPG fault occurs, a large fault current flows through the MMC SMs, causing the SM capacitors to discharge. As a result, the converter station is immediately blocked after fault detection (within 2ms). Once the converter station is blocked, the upper arm SMs behave differently from the lower arm SMs due to the current's direction [12]. The impact of valve-side SPG on lower arm is discussed in the next section. In case of HB upper arm SMs, fault current could traverse from +ve pole towards the valve-side via SM capacitors and diode path. Equivalent model of upper arm SMs is shown in Fig. 2 (a). The maximum cumulative voltage across upper arm SMs (u_{ux}), assuming the lower arm current is blocked, can be expressed as:

$$u_{ux} = V_{dc} - L_{arm}\frac{\mathrm{d}i_{x\_upper}}{\mathrm{dt}} - R_{arm}i_{x\_upper} - u'_x(x = a, b, c) \tag{1}$$

where, V_{dc} is +ve pole voltage, L_{arm} and R_{arm} and arm inductance and resistance respectively. While u'_x is post-fault valve-side ac voltage and i_{x_upper} is arm current. If valve-side SPG fault occur on phase 'a', the post-fault valve-side phase voltages can be expressed as follows: $u'_a = 0$, $u'_b = -u_{AB}$ and $u'_c = u_{CA}$. From (1), it can be inferred that the upper arm SMs charge only when the potential difference across them exceeds the SM voltage capacitors. The maximum upper arm overvoltage (u_{ux_max}) after periodic charging of SM capacitor can be estimated as:

$$u_{ux\_max} = V_{dc} + max\,|u_x| + \Delta V_{dc} = (1 + 0.866m)\,V_{dc} + \Delta V_{dc} \tag{2}$$

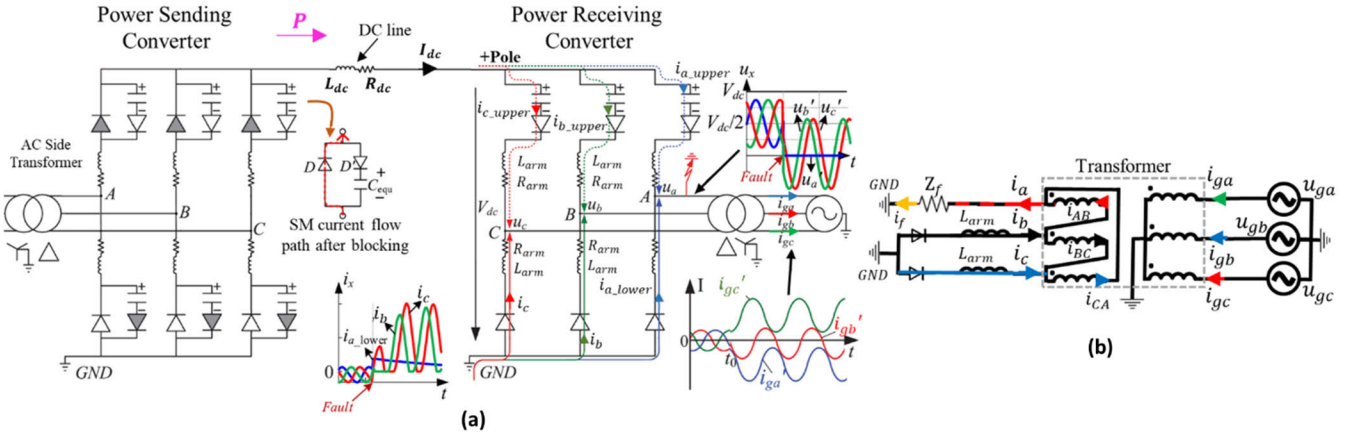

FIGURE 2. (a) Equivalent circuit of +ve pole of a bipolar link in the case of SPG valve-side fault at phase 'a' of power receiving converter. (b) SPG fault equivalent circuit on AC side of the converter station.

ΔV_{dc} represents the change in dc voltage due to transients after the converter enters the blocking state. The maximum valve-side voltage ($max\,|u_x|$) is $\sqrt{6}$ times the valve-side pre-fault phase voltage U_x, which is related to V_{dc} and modulation index 'm' as:

$$U_x = mV_{dc}/2\sqrt{2} \quad (0 \le m \le 1) \tag{3}$$

For the considered transmission system, m is estimated to be 0.89. Thus, from (2) & (3), $u_{ux\_max} \geq 1.77V_{dc}$ for healthy phases (b and c). For faulted phase (a), u_{ua_max} equals $V_{dc}+\Delta V_{dc}$.

In the event of communication failure or delay during SPG valve-side fault, the opposite/remote converter station might not be blocked. If the SPG fault occur at DC voltage and reactive power (V_{dc}-Q) controlling converter, unblocked active power controlling remote converter (RC) would rapidly rise transmission line voltage, resulting in upper arm SM overvoltage of about 2 p.u. for healthy valve-side phases [14]. Therefore, either HB-MMC converter insulation should be designed to withstand such faults or an effective protection scheme is needed to be implemented.

B. SPG FAULT CHARACTERISTIC AT LOWER ARM

The fault current from the converter ground is fed into the transformer delta winding through the lower arm freewheeling diodes of phases b and c, ultimately flowing out of phase a to the fault location, forming a current loop, as illustrated in Fig. 2(b). The fault ground resistance (Z_f) is considered zero to emulate worst-case scenario. During an SPG valve-side fault, the blocked lower arm conducts the fault current in a single direction through the submodule (SM) diode only (without involving the capacitor), thereby preventing capacitor overvoltage. The insignificant lower arm current (i_{a_lower}) of faulty phase a, due to arm inductance, decays to zero, as shown in Fig. 2(a). During the fault condition, the following relationship between healthy valve-side phase voltages and lower arm phase currents (i_b and i_c) can be deduced:

$$\begin{cases} u_b = u_{AB} = L_{arm}\frac{\mathrm{d}i_b}{\mathrm{dt}} + i_b R_{arm}, \\ u_c = u_{CA} = -L_{arm}\frac{\mathrm{d}i_c}{\mathrm{dt}} - i_c R_{arm}, \end{cases} \tag{4}$$

The initial condition for healthy lower arm currents for (4) can be estimated as:

$$i_x\,(0+) = i_x\,(0-) = I_x, \quad (x = b, c) \tag{5}$$

By substituting (5) into (4), lower-arm currents can be expressed as (6):

$$\begin{cases} i_x = A_x \sin(\omega t + \varphi_x) - B_x \cos(\omega t + \varphi_x) + C_x e^{-\frac{R_{arm}}{L_{arm}}t} \\ A_x = \frac{R_{arm}U_n}{R_{arm}^2+(\omega L_{arm})^2} \\ B_x = \frac{\omega L_{arm}U_n}{R_{arm}^2+(\omega L_{arm})^2} \\ C_x = I_x + B_x \cos(\varphi_x) + A_x \sin(\varphi_x) \end{cases}, \tag{6}$$

Due to delta configuration, post-fault valve-side phase voltage (u'_x) can be expressed as line voltages: $u'_x = U_n \sin(\omega t + \varphi_x)$ during SPG fault [9]. Where, U_n is the peak line voltage, ω is AC system frequency, and φ_x is the post-fault phase angle of the healthy phase. Since R_{arm} is negligible, A_x can be ignored, while B_x can be approximated as $\sqrt{2}\,U_x/\omega L_{arm}$. Thus, the healthy-phase lower-arm current can be presented as a combination of aperiodic and periodic components, as expressed in equation (7) and in [13]. From equation (7), i_b and i_c can be estimated as follows:

$$i_x = \left(I_x + \frac{U_n}{\omega L_{arm}}\cos(\varphi_x)\right) e^{-\frac{R_{arm}}{L_{arm}}t} - \frac{U_n}{\omega L_{arm}}\cos(\omega t + \varphi_x) \tag{7}$$

R_{arm} and L_{arm} are estimated to be 0.2Ω and 0.15H respectively. The aperiodic DC component $\left[I_x + (\sqrt{2}U_x/\omega L_{arm})\ cos\,(\varphi_x)\right]$ in (7) does not decay significantly for several hundred milliseconds, clamping the lower-arm current. The lower-arm current remains +ve due to the continuous unidirectional nature of the free-wheeling diodes, which

almost conduct current throughout the entire AC cycle. The ground fault current, i_f can be expressed as shown in (8).

$$i_b + i_c = i_f, \tag{8}$$

From Fig. 2(b), the relationship between converter transformer's valve-side phase and line currents can be formulated as (9), Where, i_{AB}, i_{BC} and i_{CA} are line currents on transformer delta side.

$$\begin{cases} i_a = i_{AB} - i_{CA}, \\ i_b = i_{BC} - i_{AB}, \\ i_c = i_{CA} - i_{BC}, \end{cases} \tag{9}$$

The grid-side of the transformer is in wye formation with a turn ratio K. Therefore, current transformer delta-side line currents could be expressed in terms of grid-side phase currents ($i'_{ga}, i'_{gb}\&i'_{gc}$) as:

$$\begin{cases} i_{AB} = Ki'_{ga}/\sqrt{3}, \\ i_{BC} = Ki'_{gb}/\sqrt{3}, \\ i_{CA} = Ki'_{gc}/\sqrt{3}, \end{cases} \tag{10}$$

The grid-side phase current waveforms can be estimated in terms of valve currents i_b and i_c from (9) & (10).

$$\begin{cases} i'_{ga} = -K/\sqrt{3}(2i_b + i_c), \\ i'_{gb} = K/\sqrt{3}(i_b - i_c), \\ i'_{gc} = K/\sqrt{3}(i_b + 2i_c), \end{cases} \tag{11}$$

From (11), It can be inferred that i'_{ga} and i'_{gc} would have a non-zero crossing waveform due to aperiodic components in i_b and i_c. while, i'_{gb} exhibits a zero-crossing behavior during an SPG valve-side fault.

III. GROUND FCL BASED VALVE-SIDE SPG FAULT MITIGATION

As analyzed in Section **II**, if the DC offset of i_b and i_c can be quickly attenuated, the grid-side currents can be clamped to a zero-crossing value during a valve-side SPG fault, which can be cleared by ACCBs. This can be done by resistive damping of the lower arm of MMC converter station. Additionally, from (6), resistive damping would result in reduction of B_x, which dictates the magnitude of periodic element in i_b and i_c. This could limit the magnitude of grid-side fault current i'_{ga} and i'_{gc} and curb the impact of SPG fault on the connect AC grid.

This paper proposes power electronic fault current limiter being installed at the MMC station ground 'G' (where RL circuit or ground resistance is placed) as shown in Fig 3. The

FCL consists of main power electronic branch, resistive branch and surge arrester branch. The PE branch is in on-state before fault inception thus offering negligible resistance to ground current during normal operation. Once the SPG fault is discriminated the PE branch is blocked. This cause the ground fault current i_f to be commutated into the resistive branch which ultimately produce zero-crossing current on all three phases at AC-grid side which can be cleared by ACCBs with in 100ms after SPG fault detection.

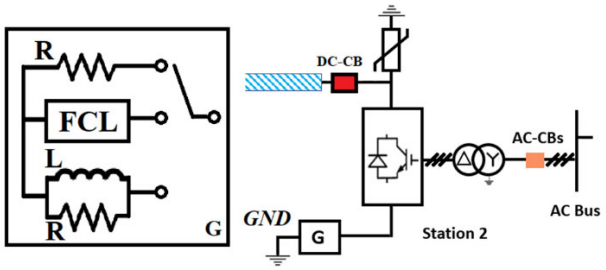

FIGURE 3. Various grounding methods depicted at single pole of MMC substation in bipolar transmission link.

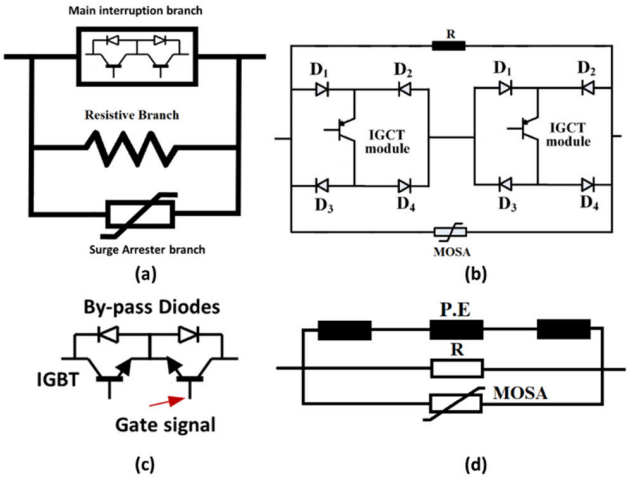

FIGURE 4. (a) Basic Model of Power electronic FCL. (b) FCL consisting diode-bridge & IGCT based PE module. (c) IGBT-diode bi-directional PE module. (d) Depiction of multiple PE module FCL.

The basic structure of FCL model is depicted in Fig. 4(a). The PE branch module is composed of two series connected IGBT modules in opposite direction along with anti-parallel diodes for bi-directional current conduction as shown in Fig. 4(c). Furthermore, FCL module with reduced cost and less full-controlled switches can be composed by bridge-type PE branch consist of diodes D_1-D_4 and an Integrated Gate-Commutated Thyristor (IGCT) or IGBT as shown in Fig. 4(b). The diode bridge would conduct current only when IGBT/IGCT is in on-state. The PE branch, based on FCL voltage rating, can be devised as a series combination of multiple PE modules as depicted in Fig. 4(d).

From (6) and (8), it can be estimated that i_f initially contains a large DC component, which is damped within 1–2 AC cycles due to the FCL resistance. Consequently, a surge arrester branch is installed across the FCL to restrict the initial overvoltage across the PE branch. This measure significantly lowers the required withstand voltage across the PE branch, resulting in a reduction of on-state losses. The FCL is installed at the converter station grounding, which is typically designed with a low basic insulation level (BIL). That is advantageous in terms of ground-side equipment costs, such as lower insulation costs of arm inductor and

air clearance. The upper limit of the FCL and surge arrester voltage rating is thus defined by the grounded pole BIL. For a ±320 kV bipolar link, a practical example of a switching impulse protection level (SIPL) of 150kV@10kA for ground-side surge arrester is presented in preview literature [7].

From (6), the damped i_b and i_c (after the aperiodic component has decayed swiftly) due to the FCL resistance can be estimated as shown in (12).

$$i_x = -\frac{\omega L_{arm} U_n}{(R_{equ})^2 + (\omega L_{arm})^2} \cos(\omega t + \varphi_x) \, (x = b, c) \quad (12)$$

Here, R_{equ} is the resistance, which constitute of equivalent

FCL resistance on each healthy lower arm. From (11) and (12), the magnitude of the grid-side fault current can be estimated. The PE branch voltage rating can be calculated as $i_f R$.

A. SIMULATION VERIFICATION

The impacted converter station is blocked 2ms after SPG fault inception, assuming that the converter fault detection system or blocking mechanism can be triggered within this period, as suggested in the previous literature [12]. However, to discriminate an SPG fault, zero-sequence current on the valve side of the converter station, which is zero under nominal conditions due to balanced upper and lower arm currents, can be utilized [30]. This balance is lost during an SPG fault due to different in fault current conduction in the upper and lower arms of the faulty converter station, as explained in Section II, which can be exploited for SPG fault detection. The FCL PE branch is blocked 1.5ms after the MMC converter station is blocked to account for the added delay in discriminating the SPG fault. PSCAD/EMTDC simulations are conducted without a DC pole reactor to emulate the maximum ground current before the MMC converter is blocked. Empirical investigation of the grid-side and valve-side currents during an SPG fault in a low-impedance grounded bipolar system is validated by the waveforms depicted in Fig. 5.

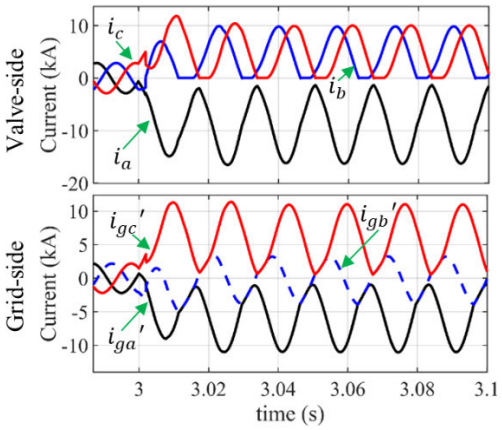

FIGURE 5. Valve and grid-side current waveforms during an SPG valve-side fault at low impedance grounded MMC converter station.

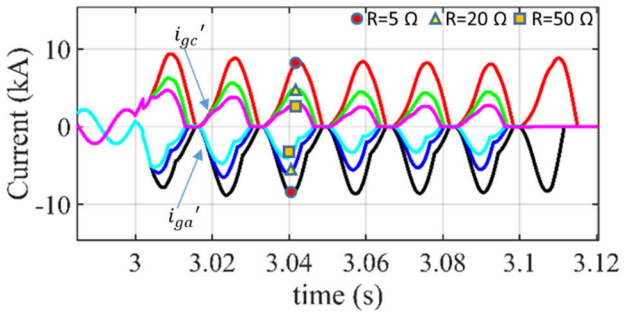

FIGURE 6. Grid-side current (i_{ga}' & i_{gc}') w.r.t varying FCL resistance.

Fig. 6 depicts impact of variance in FCL branch resistance on grid-side current. It is observed that zero-crossing grid current can be achieved from FCL resistance as low as 5Ω. However, higher FCL branch resistance of 20Ω & 50Ω restrict the peak grid-side fault current to 2 and 1.2 times the steady state respectively as assessed by (12). This curbs the impact of the SPG valve-side fault on the connected AC system until it is cleared by the grid-side ACCBs. Fig. 7 depicts that the FCL branch resistance is inversely related to MMC ground-side current during an SPG fault. Although the freewheeling diodes in the lower arm of the MMC converter are designed to withstand the peak current and heat losses incurred during an SPG fault [12], higher FCL branch resistance would further reduce the lower arm diode current for the healthy phase, ultimately reducing the diode's heat loss (I^2t). However, a large resistance FCL could increase the insulation requirements on the converter station's ground side. For instance, with a 50Ω FCL, the peak overvoltage reaches up to 178kV, as depicted in Fig. 8. Therefore, a tradeoff between the converter ground-side BIL and grid-side AC current restriction during an SPG fault would have to be made. Nevertheless, for an FCL resistance branch of 20Ω, the ground-side overvoltage remains below the SIPL of the surge arrester and the converter's ground-side BIL, for a practical ±320kV bipolar HVDC system as discussed earlier.

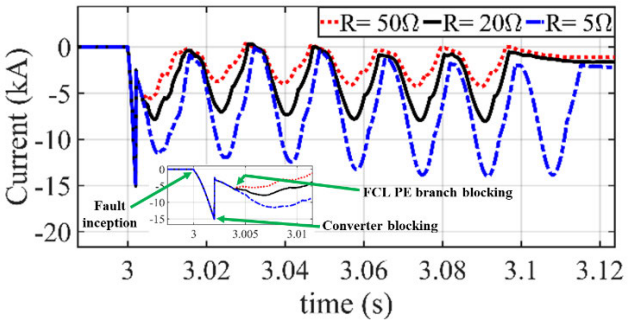

FIGURE 7. Ground-side current at faulty MMC converter station w.r.t varying PE-FCL resistance.

The surge arresters' VI characteristics in PSCAD, with maximum continuous operating voltages (MCOV) of 62kV, 132kV, and 162kV, are utilized for 5Ω, 20Ω and 50Ω FCL,

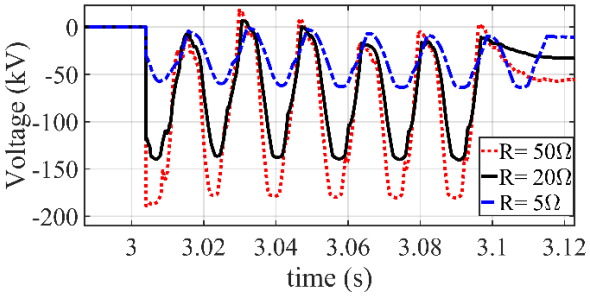

FIGURE 8. Prospect of voltage across FCL with varying branch resistance during an SPG-valve-side fault.

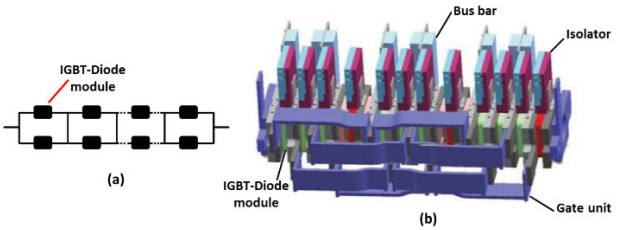

FIGURE 9. (a) P.E branch topology (b) Stack design for P.E branch.

respectively, and are tabulated in Table 2. The total energy absorbed by the FCL surge arrester during an SPG fault is depicted in Table 3.

B. PARAMETRIC DESIGN OF P.E. AND RESISTANCE BRANCH

It can be inferred that the P.E. branch is required to conduct ground-side current during steady-state operation. Thus, the designed P.E. branch must be able to carry the continuous grounded pole current and reliably withstand the thermal stress associated with it under normal conditions. For the HVDC system described in Section II, with an estimated ground current of 2.34 kA, the IGBT-diode P.E. branch, as depicted in Fig. 4(c), can practically be modeled using a series combination of 4.5kV/3kA StakPak IGBT-diode modules (5SNA3000K452300) [32]. Since the peak ground current could exceed 3kA during SPG fault, a parallel combination of StakPak IGBT modules would be utilized for higher current handling capability. For instance, a 20Ω FCL with a surge arrester rated at 132 kV requires 31 units of 5SNA3000K452300 modules. As the post-SPG fault ground current reaches a peak magnitude of 4-5 kA before it is cleared/commutated by the P.E. branch, two parallel semi-conductor modules would be utilized, as depicted in Fig. 9(a). The cooling system for power electronic systems is designed based on power losses incurred due to continuous DC ground pole current. The conduction/power losses (P_{ce}) associated with each IGBT can be approximated by considering the IGBT's on-state zero-current collector- emitter voltage (v_{ce0}) as the DC source voltage, with a collector-emitter on-state resistance (R_{ce0}) in series [33].

$$P_{ce} = v_{ce} i_{ce} = v_{ce0} i_{ce} + R_{ce0} i_{ce}^2, \tag{13}$$

TABLE 2. Ground-side FCL surge arrester parameters.

FCL Resistance: 5Ω, 20Ω, 50Ω Arrester MCOV: 62kV, 132kV, 162kV	
I, kA	***Voltage (p.u.)***
0.003	1
0.03	1.0271
0.1	1.0296
0.2	1.0332
0.38	1.0396
0.65	1.0493
1	1.0618
3	1.1333
12	1.2042
30	1.2604
200	1.7917

TABLE 3. Energy absorbed by FCL surge arrester during SPG fault.

FCL Resistance (Ω)	Energy Absorbed (kJ)
5	402
20	1344
50	3673

where, v_{ce} and i_{ce} are the nominal collector-emitter voltage and current, respectively. Similarly, the power losses across the diodes (P_D) can be estimated using the diode's on-state resistance (R_{on}) and forward voltage drop (v_{FVD}).

$$P_D = v_D i_D = v_{FVD} i_D + R_{on} i_D^2, \tag{14}$$

v_D and i_D are the instantaneous voltage drop and diode current, respectively. According to [32] and [33], the P.E. branch (depicted in Fig. 9(a)), with a fault current handling capability of 6kA, incurs steady-state power losses of 2.54kW and 2.44kW in each current-conducting IGBT and diode, respectively, for the nominal pole-ground current. These losses must be managed by the thermal management system of the P.E. branch. A practical P.E. branch would be a compact structure consisting of a busbar, isolators, a gate unit, and semiconductor modules, with a cooling mechanism to account for on-state power losses, similar to the load commutation switch in a hybrid DCCB, as shown in Fig. 9(b) [34]. The configuration of power electronic module used in P.E. branch as well as thermal losses associated with them (as estimated here) dictate the physical size/foot print of the P.E branch. A similar assessment could be carried out to devise an IGCT-diode-based P.E. branch depicted in Fig. 4(b). As discussed in Section **III-A**, higher FCL resistor would require more power electronic modules with more thermal management requirement overall i.e. for a fault current handling capability of 6kA for 50Ω FCL with an MCOV of 162kV require 40 × 2 StakPak IGBT.

The turn-off time for the StakPak IGBT module is 5.13μs, which is accounted for within the SPG fault discrimination and P.E. branch turn-off time delay (1.5 ms) considered in Section III-A. The rate of rise of the ground fault current is

limited by the transformer impedance. Therefore, the turn-off time delay of the StakPak IGBT has an insignificant impact on the peak P.E. branch current before it is commutated. Furthermore, to curb the rate of rise of the fault current in case the turn-off time delay of a power electronic module is significantly high, a ground pole reactor could be installed.

The FCL resistive branch is not required to conduct ground pole current during the pre-fault condition and thus does not require a cooling mechanism to handle steady-state losses. Consequently, it can be modeled as a Neutral Earth Resistor (NER) [35]. The physical size and thermal management requirements for such a resistor would be similar to those of an RL grounding NER, which does not conduct current during steady-state conditions [9]. However, the NER should be able to withstand the energy dumped (tRi_f^2) in the resistor during SPG valve-side fault mitigation.

HVDC NER's can be manufactured from high-temperature stainless steel alloys, offering fast cooling and stable resistance over the device's lifespan as compared to liquid resistors that cool down slowly [35]. For example, RP resistors are constructed from a continuous stainless steel strip wound edgewise into oval coils. These coils are supported by rigid ceramic insulators and can handle high temperatures of up to 1100°C without strain. Such material is also efficient at packing large resistor mass into a compact space. As the FCL branch can be modeled using versatile off-the-shelf power system equipment, its exact dimensions and footprint depend on the power electronic components used, as well as its thermal management system and resistive branch material. This section only analyzes the necessary constraints and properties that need to be assessed to devise a practical grounding FCL.

IV. SM OVERVOLTAGE SUPPRESSION BY MECHANICAL DC CB

As discussed in section **II**, the upper arm SMs capacitor of the faulty converter station get charged after it is blocked. For the considered modulation index (m), the upper arm SM overvoltage could reach to 2 p.u. if the remote active power controlling converter station is not blocked, as estimated by (2). The charging process won't terminate until the grid-side ACCBs isolate the fault or until the SM capacitors charge to their maximum limit. Therefore, it is crucial to terminate this charging process before the insulation of the MMC converter station is compromised.

Fig. 10 depicts the nature of the current in the faulty converter station during an SPG fault after the station is blocked. It is observed that the DC line current falls to zero after several milliseconds. This occurs because the charging of the upper arm SM capacitors in the impacted converter is a periodic process; the SM capacitors are charged only during the negative half-cycle of the valve-side voltages. Furthermore, the charging duration is reduced with each AC cycle due to the high SM voltage from the previous cycle. As a result, the current conduction duration is also reduced, as observed at the +ve converter pole. For the considered 400km transmission line, the pole current reaches its first zero-crossing at approximately 30ms and 48ms for the blocked and unblocked remote converter, respectively. The remote converter would be blocked either by local protection mechanisms or by a blocking signal from the faulty converter. A remote converter blocking delay of 5ms is included to emulate communication delay. It is inferred that the pole reactance has an insignificant impact on the time required to reach the first zero-crossing of the pole current. A pole reactance of 50mH was chosen for comparison in Fig. 10.

From [13], the change in SM capacitor voltage, ΔV_{dc}, can be estimated as:

$$\Delta V_{dc} = \frac{P\Delta t}{3V_{dc}C_{SM}} \tag{15}$$

where, Δt is the time period between the power-receiving converter blocking and when the SM capacitor charging stops. C_{SM} is the equivalent arm capacitor. The higher the power transmitted (P) and Δt, higher the SM capacitor voltage ($\geq 1.866mV_{dc}$). Its inferred from Fig. 10 that the pole arm current can be cleared using a mechanical breaker when it reaches zero-crossing, preventing further aggravation of SM overvoltage. Fig. 11 depicts the upper arm SM capacitor overvoltage for three combination of protection strategies:

- RC blocked and mechanical DC CB operation.
- Remote converter unblocked and DC CB operation.
- Unblocked RC without DC CB

Upper SM capacitor reach voltage up to 1.88 p.u. for the healthy arm until the fault is cleared by the grid-side ACCBs after 100ms in the 3rd protection strategy. In the case where a mechanical interrupter clears the fault with the remote converter station blocked, the maximum SM capacitor overvoltage is 1.3 p.u., significantly lower compared to the estimated overvoltage without any protection scheme. The mechanical DC CB in PSCAD is modeled as an ideal switch that can only interrupt fault current when it reaches zero-crossing, after 30ms of fault inception. Furthermore, it has been noted that even without the RC station being blocked, the mechanical DC CB limits the SM voltage to 1.68 p.u. of the steady-state SM voltage. From a design point of view, the converter station should be designed to withstand an SM overvoltage of at least 2 p.u.; thus, the mechanical DC CB method would effectively limit SM overvoltage during an SPG valve-side fault, especially for a blocked remote power-controlling converter.

A. IMPACT OF TRANSMISSION LINE LENGTH ON SM OVERVOLTAGE

The length of the transmission line is expected to play a crucial role in shaping the transient response of the line current (affecting ΔV_{dc}), as a longer transmission line would have higher line inductance. For the considered bipolar system, the length is varied between 100 and 1000 km, and its effect on the upper arm SM overvoltage in healthy phase C is assessed with mechanical DC CB protection, as shown in Fig. 12. It is observed that for relatively shorter transmission

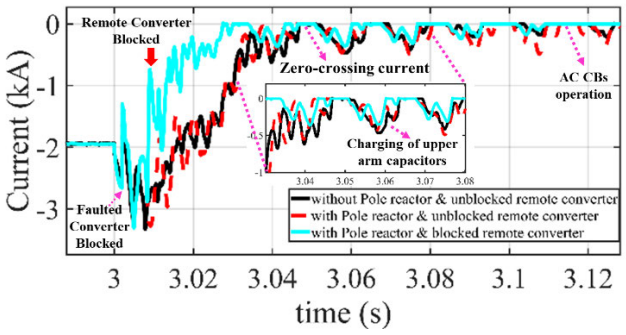

FIGURE 10. +ve Pole current during an SPG fault flowing from power-receiving MMC converter to power-sending converter.

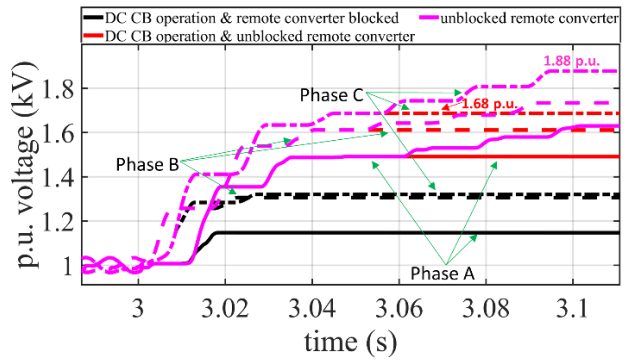

FIGURE 11. Overvoltage prospect of upper arm SM overvoltage with and without remote converter blocked and DC CB operation.

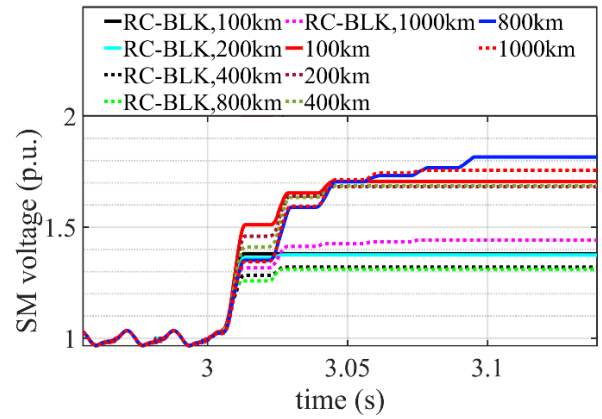

FIGURE 12. Prospect of upper arm SM overvoltage w.r.t variation in transmission line length and mechanical DCCB based protection implemented.

lengths (100-400 km), the mechanical DC CB effectively limits Δt, which ultimately reduces ΔV_{dc} whether the remote converter is blocked (RC-BLK) or not. However, for longer transmission lines, due to the higher line inductance, the pole current takes more time to reach zero- crossing, making a mere mechanical interrupter less effective in limiting SM overvoltage. SM capacitor overvoltage is most severe when the remote converter is not blocked, reaching up to 1.81 p.u. for an 800 km transmission line. It is also noted that for a 1000km DC line, SM capacitor charging is interrupted earlier than for the 800 km line when the remote converter is unblocked. This uncertainty in DC CB operation can be attributed to the shorter zero-crossing period of the pole current. In the case of RC-blocked, although it takes longer to clear the DC line current using the DC CB, SM overvoltage remains below 1.45 p.u. Thus, for very long-distance bipolar ptp system, a different upper arm SM overvoltage suppression strategy should be adopted to limit SM overvoltage during an SPG fault.

B. PASSIVE OSCILLATION DCCB BASED SM OVERVOLTAGE MITIGATION

For a multi-terminal DC system (MTDC), it is expected that the remote power sending converter station might not be blocked to ensure a redundant power supply to healthy converter stations [13]. Additionally, the higher the transmitted power (P) and the longer the transmission line, the less effective the mechanical DC CB-based SM overvoltage mitigation technique will be. In such scenarios, passive oscillation-type DC CBs could be utilized to clear the pole current within 20-30 ms. These DC CBs consist of an LC branch and a surge arrester branch in parallel to a mechanical interrupter (S_1), as depicted in Fig. 13. The LC branch produce artificial current zero-crossing in S_1 during the current interruption process. After current zero has been generated in the S_1, current is completely commutated into LC branch while S_1 transitions to an open-state. This result in rise in LC branch capacitor (C_p) voltage, which is clamped by the parallel surge arrester branch. Once DC CB interrupts the fault current, a residual breaker (S_2) is utilized to clear any residual current.

Previously, many passive oscillation type DC CB have been devised [23]. In this manuscript, CIGRE passive oscillation-type DC CB have been analyzed to clear DC line current during an SPG fault. The LC branch resonance frequency is 14.5 kHz. Further DC CB specifications are shown in Table 4. modeling depth for the DC CB concerning system-level studies in EMT software represents a trade-off between computational burden and the required accuracy of results. For system-level analysis, the mechanical interrupter is usually modeled as an ideal switch, meaning it does not account for internal physical phenomena and breaks current on demand. Similarly, critical internal data like current commutation and LC capacitor voltage stress are not required in system-level studies. Moreover, detailed internal phenomena are assessed during the DC CB design process in EMT software with appropriate time steps. Thus, a simplified model of the considered DC CB has been utilized in a bipolar HVDC system [31]. S_1 and S_2 are modeled as an ideal switch in PSCAD/EMTDC software, while the LC branch is simplified by removing the inductance as shown in Fig. 13. This setup can estimate the voltage waveform and energy absorbed by metallic oxide surge arrester branch (MOSA) during DC CB interruption process.

TABLE 4. Passive oscillation type DC CB specification [23].

Type	I* (kA)	Volt** (kV)	L (μH)	C (μF)	f (kHz)	Commutation time (ms)
SF_6	2.2	500	40	3	14.5	14

*Current, **Voltage rating

Once the current is interrupted by the mechanical branch, the LC branch capacitor charges, dictating the rate of rise of voltage across the DC CB before it is clamped by the MOSA. It should be noted that the considered simplified model has a slight margin of error in estimating initial transient interrupt

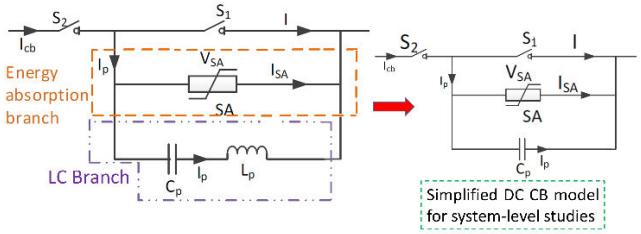

FIGURE 13. Depiction of a passive oscillation-type DC circuit breaker and its simplified model for large DC network simulation.

voltage, as explained in [31]. However, for a large network simulation, it reasonably estimates the transient interrupt voltage, DC CB current, and surge arrester energy. Current and voltage waveforms, as well as energy dumped in the surge arrester branch for the considered DC CB at the faulty converter station of an 800 km long point-to-point (ptp) bipolar system, are shown in Fig. 14. S_1 interrupts at 16 ms after fault inception. The energy absorbed by the surge arrester is around 2.5 MJ, which is relatively lower than in conventional applications of DC CBs, as the line current at the time of interruption is 0.5kA (1/4 of the steady-state current) during an SPG fault. After line current is interrupted, S_2 is actuated to clear any residual line current at 25ms. The pole current clearance limits arm SM overvoltage to a safe limit (1.35 p.u.) for healthy phases in the 800 km long-distance HVDC bipolar system as shown in Fig. 15. The voltage-current characteristics of the surge arrester utilized in PSCAD/EMTDC are shown in the Appendix.

V. COMPARISON WITH OTHER SPG FAULT MITIGATION SCHEMES

A. SPG FAULT MITIGATION SCHEMES

The proposed mechanical DCCB-FCL strategy is compared with previously proposed methods. Thus SPG fault is instigated at the +ve pole of the power-receiving active power-controlling converter station (rather than V_{dc}-Q controlling converter) within a 400 km HB MMC bipolar link. As a result, the estimated upper arm SM overvoltage would be less severe compared to the one discussed in Section IV.

Valve-side and grid-side currents, upper arm SM capacitor voltage, and DC line voltage are assessed and depicted in Fig. 18 for the FCL-DCCB method, LR grounding method [9], auxiliary ACCBs on the grid side [11], double thyristor-based protection [12], mixed-SM methods [14], Thyristor-pair/damper module method [13] and grounded thyristor with hybrid MMC method [15]. An FCL branch resistance of 30Ω is utilized with a surge arrester rating of 170@10kA. To ensure current zero-crossing on the grid side for 100ms in the RL method, R and L are set to 20Ω and 0.75H, respectively. Location of RL circuit in MMC converter station is depicted in Fig. 3. In case of auxiliary breaker method, the grid side is connected with grounding ACCBs with a series resistance of 10Ω on each phase. During an SPG valve-side fault, these auxiliary ACCBs are closed before the grid-side ACCB operates, i.e., the auxiliary branch closes at 100ms after fault inception, producing a three-phase grid-side fault, after which the ACCB clears the fault at 200ms. For double-thyristor method, the converter's SPG fault is converted into an artificial three-phase valve-side fault within 2.5ms (after fault discrimination) by triggering the double-thyristor modules in each lower arm. As discussed in [14], to avoid lower arm overvoltage during SPG fault mitigation in a mixed-SM converter strategy, at least m86.6% of the lower arm bridge modules should be full-bridge. Therefore, 31 out of 40 SMs are taken to be FBSMs for mixed-SM method.

For the thyristor-pair and damper module method [13], depicted in Fig. 16, the lower arm is equipped with a resistive damper module, which restricts the lower arm current and creates a non-conduction interval while the converter station is blocked; subsequently, the anti-parallel thyristor pair clears the SPG fault. Here, the damper resistor is set to 5Ω. The upper arm consists only of anti-parallel thyristor modules, as the negative voltage from the SM capacitor generates zero-crossing, as explained in Section II-A. During normal converter operation, the thyristor-pair/damper modules are in the on-state, conducting the arm current. However, once the SPG fault is discriminated from conventional faults, the power electronic components of these modules are blocked. The recently proposed grounded thyristor loop-based hybrid MMC [15], reduces the required number of FBSMs to 7% of the total SM to clear the SPG fault. The thyristor loop when triggered creates a short circuit-loop across upper and lower arms of the MMC, in addition to a temporary three-phase short circuit on valve-side of the transformer. The DC-side current is first interrupted using mechanical switches (S_1 and S_2, as depicted in Fig. 17) after the RC is blocked. Subsequently, the valve-side thyristor loop is blocked, which clears the three-phase valve-side current at the first current zero-crossing. For this study, the DC-side mechanical breakers are set to clear the fault 18 ms after its inception, after which the thyristor loop is blocked 0.5 ms later.

SPG fault protection mechanisms are investigated either with or without the remote converter being blocked. All the studied methods achieve zero-crossing currents on the grid side of the MMC converter (see Fig. 18). For the proposed method, it can be seen that the grid-side current achieves zero

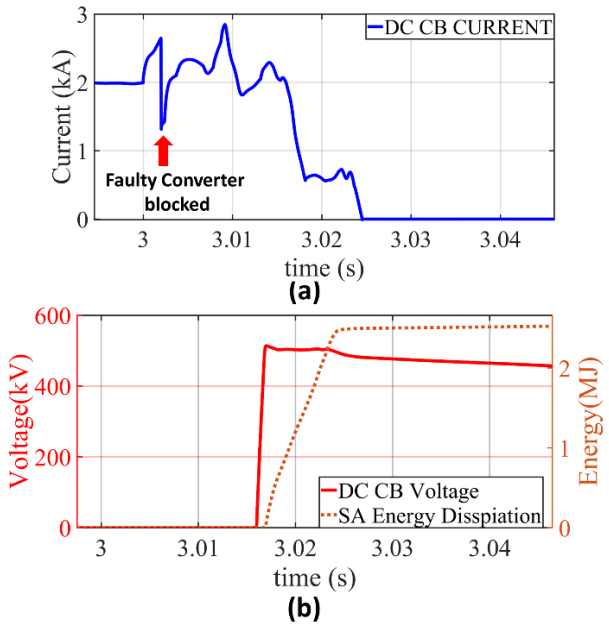

FIGURE 14. (a) Current waveform (b) voltage waveform and SA energy of passive oscillation DC CB during upper arm overvoltage mitigation under SPG valve-side fault in an 800km HVDC ptp bipolar link.

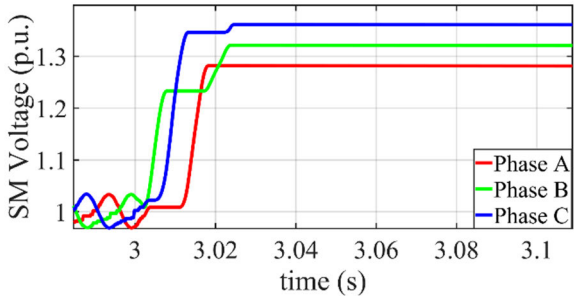

FIGURE 15. Upper arm SM voltage at faulty converter station for an 800km long bipolar link, utilizing passive oscillation DC CB mitigation method.

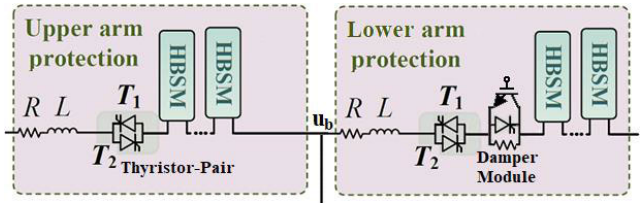

FIGURE 16. Anti-parallel thyristor/damper module depiction on upper & lower arms of phase b in HB-MMC converter, as presented in [13].

crossing and is limited to 1.6 p.u. of steady-state magnitude before being cleared by the ACCBs. However, in the case of an RL circuit, the grid-side fault current rises above 3 p.u., which may severely impact the voltage of the connected AC grid before being cleared by the ACCBs at 100 ms. Moreover, the current zero crossing in the case of an RL circuit is not uniform, and large inductance could further elevate the upper arm overvoltage (to 1.71 p.u.), as seen in Fig. 18(b). In the case of the auxiliary ACCB and double thyristor method, the upper submodule (SM) overvoltage is limited to 1.27 p.u. and 1.25 p.u., respectively, when the remote converter is blocked. However, an artificial three-phase fault further elevates the grid and valve-side fault current magnitude (to 4-5 p.u.), which could damage lower arm power electronic devices and the converter transformer.

The mixed-SM MMC converter effectively clears or limits the grid-side current once faulty converter station is blocked. However, with this method, if the remote converter station is not blocked, the upper arm SM overvoltage can reach up to 2 p.u. Thus, for such a scheme, a separate upper arm overvoltage mitigation technique must be deployed.

For the Thyristor-pair/damper module method, SM overvoltage is restricted to 1.49 p.u. even with the RC unblocked, and the grid and valve-side currents are cleared within 20 ms. In the case of a hybrid MMC with a grounded thyristor loop, SM overvoltage remains below 1.2 p.u., with the SPG fault cleared within two AC cycles. However, if the remote converter station is not blocked on time, the current interruption time of the DC mechanical switches increases, which can lead to premature blocking of the thyristor loop, rendering it ineffective in clearing the artificial three-phase fault. Furthermore, if the lower mechanical switch fails to clear the fault, the voltage across the lower arm FBSMs could rise to as high as 5 p.u., as shown in Fig. 19, severely impacting the MMC station.

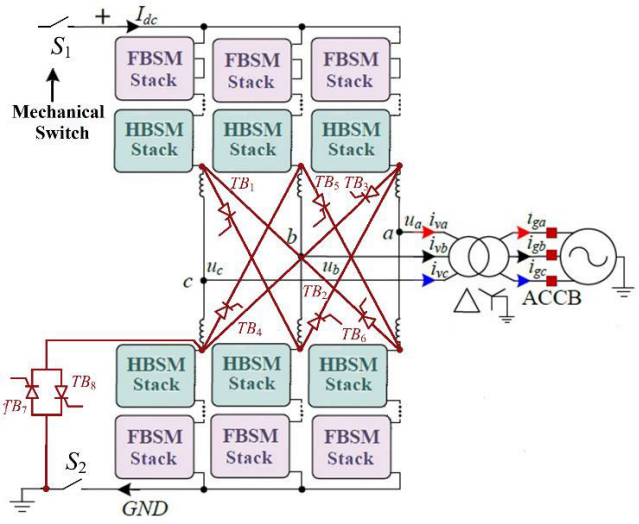

FIGURE 17. Depiction of grounded thyristor loop & hybrid MMC based SPG fault mitigation method [15].

For the compared methods, the upper SM module overvoltage cannot be suppressed reliably unless the remote converter station is blocked, except for the FCL-DCCB and Thyristor-pair/damper module method. In general, blocking the remote converter station results in a larger overvoltage surge on the healthy (-ve) pole of the bipolar system compared to when the remote converter is unblocked.

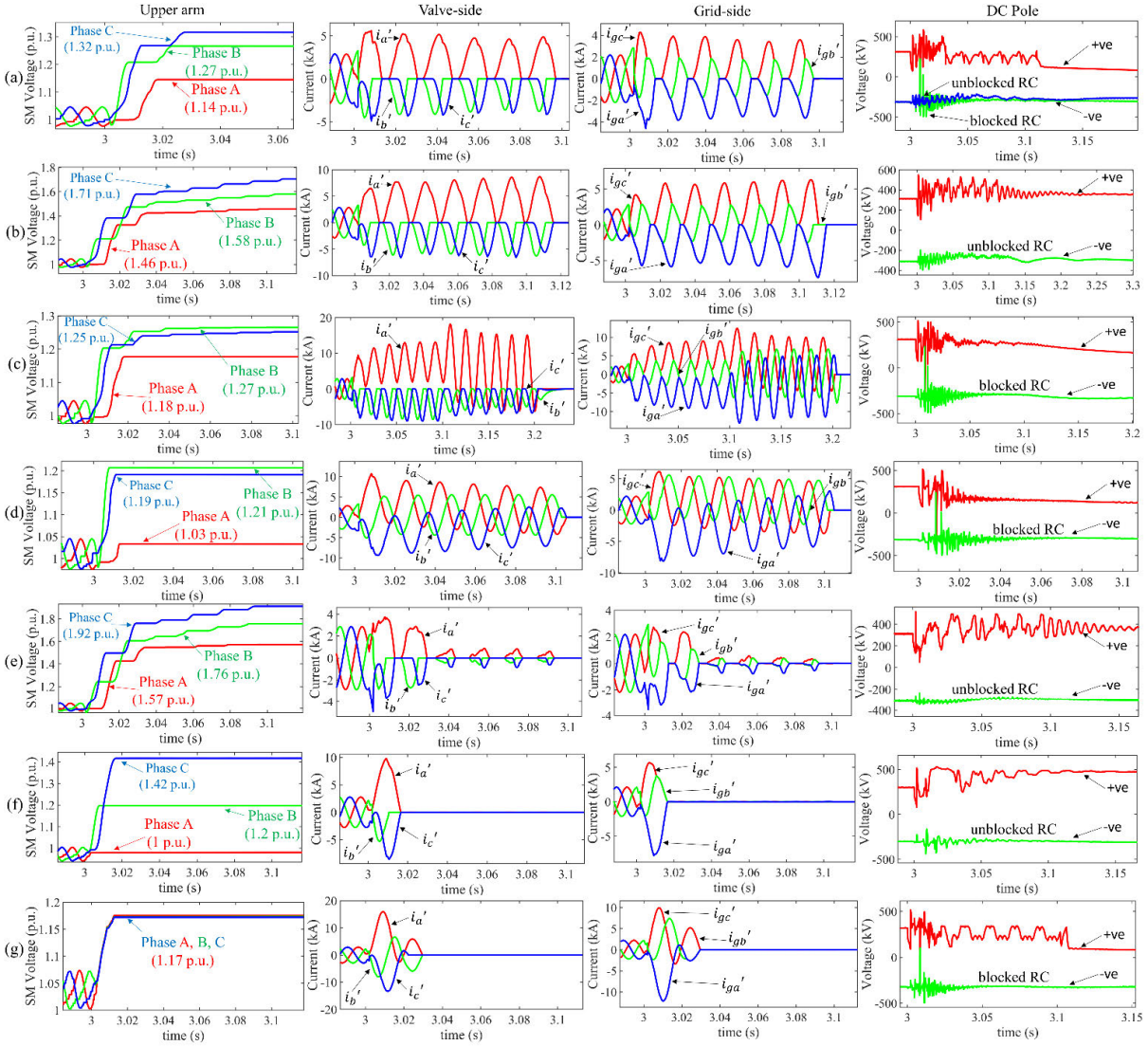

FIGURE 18. Results of implementing the seven considered protection methods. (a) FCL and DC CB method. (b) The LR-circuit method. (c) The auxiliary ACCB based method. (d) The double-thyristor based method. (e) The mixed-SM based method. (f) Thyristor-pair & damper module method. (g) Grounded thyristor loop with hybrid MMC.

Although the proposed FCL-DCCB method requires assistance from the ACCB on the grid side to clear SPG faults, it is both economical and less prone to additional faults, in contrast to the costly or complex fast SPG fault mitigation techniques proposed in [13], [14], and [15]. Additionally, it limits the grid-side fault current, reducing its impact on the AC grid, the converter transformer, and the power-electronic components of the MMC lower-arm healthy phases before SPG fault is cleared.

B. ON-STATE POWER LOSES COMPARISON OF FCL-DC CB AND THYRISTOR-PAIR/DAMPER MODULE METHOD

The proposed FCL-DCCB method and the thyristor-pair/damper module method both restrict the lower arm current to clear the SPG fault. However, damper modules are used only to create a current-zero interval in the latter method, assisting the anti-parallel thyristor in clearing the fault. Thus, the anti-parallel thyristor has to withstand the post-fault side voltage. The required number of upper and lower arm thyristor modules (N_{TU} & N_{TL}) can be estimated as (16) and (17) respectively [13].

$$(V_{diff} + U_n)/N_{TU} < U_{THY} \tag{16}$$

$$U_n/N_{TL} < U_{THY} \tag{17}$$

Here, V_{diff} is voltage difference between V_{dc} and upper arm SM capacitor voltage (u_{ux}), while U_{THY} is maximum thyristor withstand voltage. The damper module in the lower arm of the MMC consists of an IGBT and a thyristor connected in parallel with a resistive branch (as depicted in Fig. 16). The number of IGBTs/Thyristors required for the damper modules depends on the maximum voltage applied across them during SPG fault mitigation. From (7),

damper modules must withstand a cumulative voltage of: $\left[I_x + (2\sqrt{2}U_x/\omega L_{arm})cos(\varphi_x)\right] R_D$, where R_D is the damper resistance. For the case studied in section **V-B**, a damping resistance of 5Ω requires a damper voltage rating of 44 kV in each arm. For instance, if 4.5kV/3kA thyristor from Zhangbei project were utilized [13], 10 dampers in series with a resistance of 0.5Ω would have to be required.

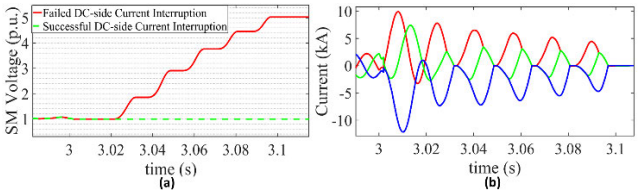

FIGURE 19. Prospect of (a) lower arm FBSM voltage and (b) grid-side current for the grounded thyristor loop & hybrid MMC method w.r.t the failed interruption of DC-side current by mechanical switches.

In the case of the FCL-DCCB, upper arm SM voltages during an SPG fault are suppressed using a mechanical DC CB, which typically does not incur steady-state power losses. Power losses due to the solid-state FCL depend on the number of IGBTs or other power electronic components used in its PE branch. For a 30Ω FCL, the post-fault current reaches up to 5.14 kA during SPG fault mitigation. The PE branch should be rated at ≥155 kV with a surge arrester rated at 170kV@10kA. It can be inferred that required IGBT module of a 30Ω FCL is similar to that of a 5Ω damper installed on each lower arm of the HB-MMC converter in thyristor pair/damper module method. Additionally, the FCL-DCCB method eliminates the need for a large number of thyristor pairs required to clear SPG faults in HB-MMC converter stations.

Following are the distinguish features of the proposed FCL-DCCB method as compared to pre-existing methods:

- In contrast to pre-existing SPG valve-side fault mitigation methods, the FCL-DCCB method suppresses MMC grid (i'_{ga}, i'_{gb}&i'_{gc}) and valve-side currents (i'_a, i'_b&i'_c) before they are cleared by the ACCBs. This approach limits the impact of the SPG fault on the connected AC grid and MMC converter station equipment e.g. lower arm diodes.
- The proposed method limits the upper arm SM overvoltage (up to 1.32 p.u.) utilizing mechanical DCCB which do not incur steady-state losses in contrast to pre-existing thyristor-pair based upper arm SM voltage suppression method.
- The FCL-DCCB method does not necessitate modifications to the converter station topology, thereby minimizing the risk of additional converter station faults, unlike the hybrid MMC approach with a grounded thyristor loop, as presented in Fig. 19.
- Compared to the thyristor-pair/damper module method, the proposed FCL-DCCB method eliminates the requirement for thyristor-pairs in the upper and lower arms of the converter station for SPG fault clearance, thereby have lower steady-state power losses.

In summary, the grounding FCL and DC CB methods perform well in suppressing and mitigating SPG grid-side fault currents and upper arm overvoltage, especially when compared to conventional auxiliary equipment-based methods. Although the proposed method requires a grid-side ACCB to ultimately clear the SPG valve-side fault, it can help avoid high on-state losses associated with fault current clearing thyristor pairs on each upper and lower arm of MMC converter in thyristor-pair/damping module topology. Furthermore, techniques that involve implementing additional circuitry within the converter station, such as the grounded thyristor-loop with hybrid MMC, are more prone to additional internal faults.

VI. GENERALIZED EVALUATION

To assess the efficacy of the proposed grounding FCL and DCCB-based SPG valve-side fault protection at the MMC converter station in a bipolar transmission system, extensive time-domain simulations and empirical investigations have been conducted.

Following are the salient assessments of this article:

- DC offset in Grid side currents (i'_{ga} & i'_{gc}) under an SPG valve-side fault can be attenuated within a single AC cycle with grounding FCL resistance as low as 5Ω. Thus, zero-crossing grid-side currents can be effectively cleared by ACCBs.
- Higher FCL resistance can limit the grid-side fault current magnitude in addition to attenuating the aperiodic component, thus reducing the fault's impact on the connected AC grid. For example, in the considered bipolar system, 20Ω resistance could limit the fault current magnitude to 2 times the nominal value. However, the upper limit of FCL resistance depends on the ground-side BIL of the MMC converter station.
- Exploiting the discontinuous nature of the pole current during an SPG fault, mechanical DC CB have been proposed to limit upper arm SM overvoltage, keeping it below 1.5 p.u., if the remote converter station is blocked (for the studied 400km, ±320kV bipolar transmission line).
- This paper analyzed the impact of transmission line length on upper arm SM capacitor charging. A longer transmission line, due to its larger line inductance, tends to have a longer duration of non-zero-crossing pole currents after the faulty converter station is blocked. Consequently, mere mechanical DC CB cannot effectively terminate SM overvoltage if the remote converter station is not blocked. Furthermore, the previously proposed anti-parallel thyristor pair method [13], [14] would also take longer time to clear such fault.
- The utility of cost-effective passive oscillation DC circuit breakers (DC CBs) for upper arm SM overvoltage suppression has been demonstrated for long-distance

TABLE 5. VI characteristic of the considered DC CB surge arrester.

Discharge current (kA)	Voltage (kV)
0.01	483
0.1	494
2	526
6	555
8	563
10	570
14	581
20	590

HVDC bipolar lines or situations where the remote converter station cannot be blocked (such as in MTDC transmission systems). These DC CBs can clear line current within 25-30 ms, limiting the upper SM overvoltage to 1.4 p.u., as estimated from the simulated case of an 800 km line. The energy absorbed by the DC CB's surge arrester is notably lower compared to conventional pole current fault interruption, because the pole current is already attenuated due to pre-charged SM capacitors. Thus, the cost of such DC CBs can be further reduced for SPG fault clearance application.

The proposed ground FCL and DC CB are effective in clearing and limiting the impact of the SPG valve-side fault on converter station peripherals without altering the MMC converter topology.

Future research is required to assess alternative resistive FCL topologies, such as superconducting FCLs, for their application in converter station grounding to mitigate single-phase-to-ground valve-side faults and other internal converter faults.

VII. CONCLUSION

Worldwide interest in bulk power transmission has led to the development of HB-MMC HVDC bipolar systems. However, a single-phase-to-ground fault at the converter station valve results in AC grid-side current with a large DC offset in such transmission systems, which conventional ACCBs cannot clear. Additionally, such internal converter faults lead to severe voltage in upper arm sub-modules. In this manuscript, a dedicated grounding FCL and mechanical DC CB-based SPG fault mitigation strategy is proposed. The presented protection topology, assessed using PSCAD/EMTDC software, can effectively limit SPG grid-side fault current as well as upper arm SM overvoltage, compared to other equipment-based strategies. Furthermore, the proposed technique can be integrated into conventional bipolar systems without altering the converter station topology. Mechanical and passive oscillation-type DC CBs ensure upper arm SM overvoltage suppression without incurring steady-state power losses. Although FCL incur on-state power losses, these are less severe compared to the previously proposed thyristor-pair/damper module method.

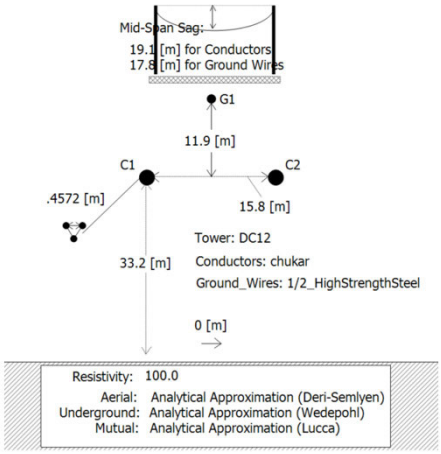

FIGURE 20. Overhead transmission line dimensions and configuration in PSCAD.

APPENDIX

Dimensional aspects of the OH line used in this manuscript are shown in Fig. 20. The SA branch VI characteristic in the passive oscillation DC CB is tabulated in Table 5.

ACKNOWLEDGMENT

The authors express their gratitude to Korea Institute of Energy Technology Evaluation and Planning (KETEP).

REFERENCES

[1] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular multilevel converters: Recent achievements and challenges," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 224–239, 2021.

[2] C. Hirsching, M. Goertz, S. Wenig, S. Beckler, M. Suriyah, and T. Leibfried, "On control and balancing of rigid bipolar MMC-HVdc links enabling subsystem-independent power transfer," *Electric Power Syst. Res.*, vol. 189, Dec. 2020, Art. no. 106768.

[3] S. Jiang, Y. Xin, G. Li, and L. Wang, "A novel DC fault ride-through method for wind farms connected to the grid through bipolar MMC-HVDC transmission," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2937–2950, Dec. 2020.

[4] M. Enomoto, K. Sano, J. Kanno, and J. Fukushima, "Reconfiguration of bipolar HVDC system for continuous transmission under DC line fault," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 8622–8633, Jul. 2024.

[5] Ø. Sagosen, A. Craig, R. Poole, and R. Paradine, "Need, design and business case for building the north Sea link," in *Proc. CIGRE Gen. Meeting*, Aug. 2018, pp. 1–9.

[6] O. Vestergaard and P. Lundberg, "Maritime link the first bipolar VSC HVDC with overhead line," in *Proc. AEIT HVDC Int. Conf. (AEIT HVDC)*, May 2019, pp. 1–4.

[7] M. Goertz, S. Wenig, S. Beckler, C. Hirsching, M. Suriyah, and T. Leibfried, "Analysis of cable overvoltages in symmetrical monopolar and rigid bipolar HVDC configuration," *IEEE Trans. Power Del.*, vol. 35, no. 4, pp. 2097–2107, Apr. 2019.

[8] G. Li, J. Liang, C. E. Ugalde-Loo, F. Ma, H. Liang, and Z. Song, "Protection for submodule overvoltage caused by converter valve-side single-phase-to-ground faults in FB-MMC based bipolar HVDC systems," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2641–2650, Dec. 2020.

[9] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of Single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444–2453, Mar. 2019.

[10] H. Zhou, W. Yao, K. Sun, X. Ai, J. Wen, and S. Cheng, "Characteristic investigation and overvoltage suppression of MMC-HVDC integrated offshore wind farms under onshore valve-side SPG fault," *IEEE Trans. Power Syst.*, vol. 39, no. 1, pp. 1346–1359, Jan. 2023.

[11] J. P. Kjærgaard, K. Sogaard, S. D. Mikkelsen, T. Pande-Rolfson, A. Strandem, and B. Bergdahl, "Bipolar operation of an HVDC VSC converter with an LCC converter," in *Proc. Conf. Internationale des Grands Reseaux Electriques Colloq. High Voltage Direct Curr. Power Electron. Syst.*, 2012, pp. 1–7.

[12] G. Li, W. Liu, T. Joseph, J. Liang, and Z. Song, "Double-Thyristor-Based protection for valve-side Single-Phase-to-Ground faults in HB-MMC-Based bipolar HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5810–5815, Jul. 2020.

[13] X. Liu, G. Li, T. Zheng, X. Yang, and J. M. Guerrero, "Thyristor-pair- and damping-submodule-based protection against valve-side single-phase-to-ground faults in MMC-MTDC systems," *IEEE Trans. Power Del.*, vol. 37, no. 4, pp. 3257–3269, Aug. 2022.

[14] P. Sun, G. Li, H. Wang, J. Liang, and G. Konstantinou, "Valve-side single-phase-to-ground fault analysis in bipolar MMC-HVDC systems with hybrid SMs," *IEEE Trans. Power Del.*, vol. 39, no. 5, pp. 3001–3004, Oct. 2024.

[15] H. Li, F. Deng, J. Tian, Y. Lu, G. Li, and J. Lin, "Grounded thyristor loop-based hybrid MMCs for valve-side single-phase-to-ground faults in bipolar HVdc systems," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6298–6311, May 2024.

[16] Y. Tian, H. R. Wickramasinghe, P. Sun, Z. Li, J. Pou, and G. Konstantinou, "Assessment of low-loss configurations for efficiency improvement in hybrid modular multilevel converters," *IEEE Access*, vol. 9, pp. 158155–158166, 2021.

[17] Z. Dai and Y. Li, "A dual-stage solid-state fault-current limiter for flexible DC distribution networks," *IEEE Trans. Power Del.*, vol. 39, no. 5, pp. 2920–2931, Oct. 2024.

[18] P. Wang, Y. Zhou, W. Wei, X. Hao, Z. Mao, W. Wang, and D. Xu, "A DC solid-state current limiter with adaptive current-limiting ability," *IEEE Trans. Ind. Appl.*, vol. 59, no. 1, pp. 970–980, Jan. 2023.

[19] Z. Cao, S. Yan, L. Ren, Y. Xu, Y. Tang, J. Shi, and J. Li, "Experimental analysis of flux-coupling-type superconducting fault current limiter prototypes," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, pp. 1–5, Nov. 2021.

[20] Y. Nikulshin, A. Kafri, Y. Yeshurun, and S. Wolfus, "Energy storing and fault current limiting in a unified superconducting magnetic device," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 5, pp. 1–5, Aug. 2023.

[21] B. Xiang, Z. Yuan, L. Li, M. Yang, Q. Zhang, Z. Liu, Y. Geng, and J. Wang, "Electromagnetic thermal analysis on variable resistive-type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 34, no. 8, pp. 1–5, Nov. 2024.

[22] S. Sarkar and A. Das, "Fault limiting circuit based protection for DC and AC faults in HB-MMC HVDC systems," in *Proc. IECON – 47th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2021, pp. 1–6.

[23] C. Franck and R. Smeets, "Technical requirements and specifications of state-of-the-art HVDC switching equipment," CIGRE WG A3/B4.34, Paris, France, Tech. Rep. 683, 2017.

[24] C. G. A. Koreman, H. Ito, S. Xu, C. Zou, Z. Yuan, Z. Yu, and W. D. Zhou, "HVDC circuit breakers," in *High Voltage DC Transmission Systems: HVDC*. Cham, Switzerland: Springer, 2023, pp. 1–67.

[25] Y. Liu, Y. Jin, Z. Li, Y. Liu, B. Li, and Z. Duan, "Mechanical DC breakers and hybrid MMC based coordinated strategy for MMC-HVDC DC fault riding through," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 4, pp. 3705–3714, Apr. 2021.

[26] C. Liu, F. Deng, Q. Heng, X. Cai, R. Zhu, and M. Liserre, "Crossing thyristor branches-based hybrid modular multilevel converters for DC line faults," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9719–9730, Oct. 2021.

[27] W. Leterme, P. Tielens, S. De Boeck, and D. Van Hertem, "Overview of grounding and configuration options for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2467–2475, Dec. 2014.

[28] M. Goertz, C. Hirsching, S. Wenig, K. M. Schäfer, S. Beckle, J. Reisbeck, M. Kahl, M. Suriyah, and T. Leibfried, "Analysis of overvoltage levels in the rigid bipolar MMC-HVDC configuration," in *Proc. 15th IET Int. Conf. AC DC Power Transmiss. (ACDC)*, Feb. 2019, pp. 1–6.

[29] A. H. G. Holthe, "Analysis of a multi-infeed HVDC system in the Norwegian power system," Master's thesis, Dept. Electr. Power Eng., Institutt Elkraftteknikk, Trondheim, Norway, 2024.

[30] S. Xue, C. Gu, B. Liu, and B. Fan, "Analysis and protection scheme of station internal AC grounding faults in a bipolar MMC-HVDC system," *IEEE Access*, vol. 8, pp. 26536–26548, 2020.

[31] F. Page, K. Kuroda, R. Uda, S. Tokoyoda, T. Minagawa, H. Ito, and M. Popov, "Mechanical circuit breaker modelling for system level real time protection system simulations," in *Proc. CIGRE Winnipeg Colloq. Exhib.*, Sep. 2017, p. 30.

[32] ABB Semiconductor, Lenzburg, Switzerland. (Feb. 2025). *5SNA3000K452300 Data Sheet*. [Online]. Available: http://www.abb.com

[33] Dynex Semiconductor. (Feb. 2021). *AN6156: Calculating Power Losses in an IGBT Module, Application Note*. [Online]. Available: https://www.dynexsemi.com

[34] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.

[35] Cressall Resistors Ltd., Leicester, U.K. (2024). *Industrial Power Resistors*. [Online]. Available: https://www.cressall.com/

MUHAMMAD USMAN was born in Multan, Pakistan, in March 1998. He received the bachelor's degree in electrical engineering from the University of Engineering and Technology (UET), Lahore, Pakistan, in 2019. Currently, he is pursuing the combined M.S. and Ph.D. degree with HVDC Electric Power Laboratory, Hanyang University, Ansan, South Korea.

His research interests include power electronics, insulation coordination studies for dc grids, protection systems, and switchgear design for HVDC and MVDC systems.

Mr. Usman is a Student Member of Korean Institute of Electrical Engineers (KIEE) and a member of Pakistan Engineering Council.

YU-JIN KWAK was born in Seoul, South Korea, in August 1996. She received the bachelor's degree in electronic systems engineering from Hanyang University, Ansan, South Korea, in 2021, where she is currently pursuing the combined M.S. and Ph.D. degree with the HVDC Electric Power Laboratory. Her research interests include power system analysis and devices for HVDC systems. She is a Student Member of KIEE.

BANG-WOOK LEE (Senior Member, IEEE) was born in Jeju, South Korea, in June 1968. He received the bachelor's, master's, and Ph.D. degrees in electrical engineering from Hanyang University, Seoul, South Korea, in 1991, 1993, and 1998, respectively.

He was a Senior Research Engineer with LS Industrial Systems, South Korea. In 2008, he joined the Department of Electronic System Engineering, Hanyang University, where he is currently a Professor. His research interests include high-voltage insulation design, high-voltage dc (HVDC) protection systems, and development of electrical equipment, including transmission line structures for HVDC and HVAC power systems.

Prof. Lee is the Scholar Director and a member of the HVDC Research Committee of the KIEE, the Power Cable Experts Committee of Korean Agency for Technology and Standards, and CIGRE.