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Time-multiplexed test access architecture for stacked integrated circuits

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Abstract: Due to ever-increasing gap between (1) the tester-channel and scan-shift frequencies, and (2) the wafer-level and package-level test frequencies, the tester-channel frequency is underutilized for stacked-ICs. Thus, we present a novel time-multiplexed test access architecture for SICs that complies with P1838 and it significant reduces test time, which reduction is observed on a synthetic SIC based on ITC'02 benchmark SoCs.

Keywords: 3D test access architecture, design-for-testability, stacked-ICs

Classification: Circuits and modules for electronic instrumentation

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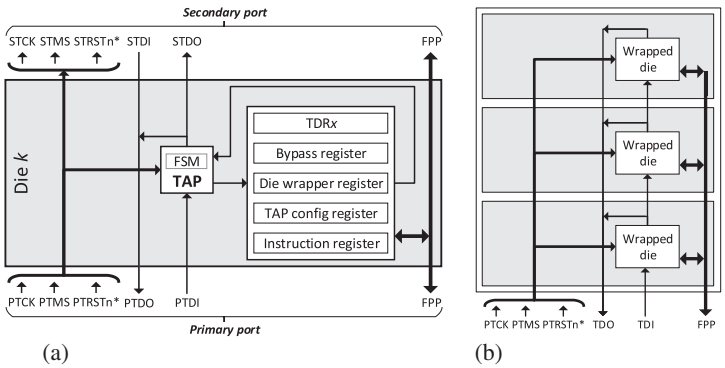
1 Introduction

Unlike 2D-ICs, stacked integrated circuits (SICs) go through various test stages [1], which contribute to the test cost and complexity. IEEE P1838 [2] has proposed a test access architecture for 3D-SICs that supports modular testing. Recent research on different test issues related to SICs has considered compatibility with IEEE P1838 [3, 4]. Fig. 1(a) illustrates an IEEE P1838 complied die-wrapper, which suggests that each die has a TAP and its controller along with the corresponding registers. Fig. 1(b) illustrates an example stack of three dies compatible with P1838. All wrapped dies are daisy-chained with respect to serial test access mechanism (TDI–TDO) and the control signals (TCK, TMS and TRSTn) are broadcast to all wrapped dies. For high bandwidth test access, a flexible parallel port (FPP) is proposed and its width is user defined. The configurable options of each lane of the flexible parallel test bus include direction (In, Out or BiDir) and edge of clock for sending output (positive or negative).

Generally, besides a sequential test access to each die, the test access optimization schemes can result in daisy-chained and/or parallel accesses [5, 6, 7]. Even though there is a separate TAP controller on each die of P1838 complied stack, all wrapped dies stay in a common state, e.g., shift, capture, update, because control signals are broadcast to them. Therefore, we cannot independently control each die wrapper, which may unnecessarily prolong the shift-state of some dies due to a longer shift-state of a die. Thus, during a parallel test of multiple dies, the test time of some cores might be increased, which potentially increases the test time of the corresponding SIC.

Moreover, the tester-channel frequency is underutilized due to ever-increasing gaps between (1) the tester-channel and scan-shift frequencies, and (2) the wafer-level and package-level test frequencies [8].

Thus, we present a novel time-multiplexed test access architecture for SICs that is compatible with IEEE P1838. It reduces the test cost of SICs by leveraging



(a) (b)

Fig. 1. P1838 complied (a) die-wrapper and (b) example stack.

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the tester-channel frequency at both the wafer-level and package-level tests. The proposed architecture accesses multiple dies in a time-division manner with a higher tester-channel frequency, and significantly reduces the absolute test time at each test stage of an SIC.

2 Time-multiplexed test access architecture for SICs

The proposed architecture is based on time-division multiplexing (TDM). Fig. 2(a) illustrates a die equipped with the proposed architecture that is compatible with the P1838. Each die wrapper is accessed in a time-division manner with a higher tester-channel frequency. The number of time-slots is equal to the ratio of the tester-channel frequency to the scan-shift frequency.

For example, the scan-shift frequency for each die of a three-die stack is 50 MHz. Thus, a tester-channel frequency of 150 MHz can be used to test three dies with TDM. Fig. 2(b) illustrates a timing diagram for this example. It shows three non-overlapping clocks, one for each die; thus, the test peak-power of the stack-under test is associated to only one die. Each die samples the test data on a common 3D TAM in the corresponding time-slot. For the tester-channel frequency f, the scan-shift frequencies can be in the range of $f/2^n$ where n is a positive integer. For example, for a stack of four dies, TDM can be implemented with scan-shift frequencies of 40, 20, 10 and 10 MHz with tester-channel frequency of 80 MHz.

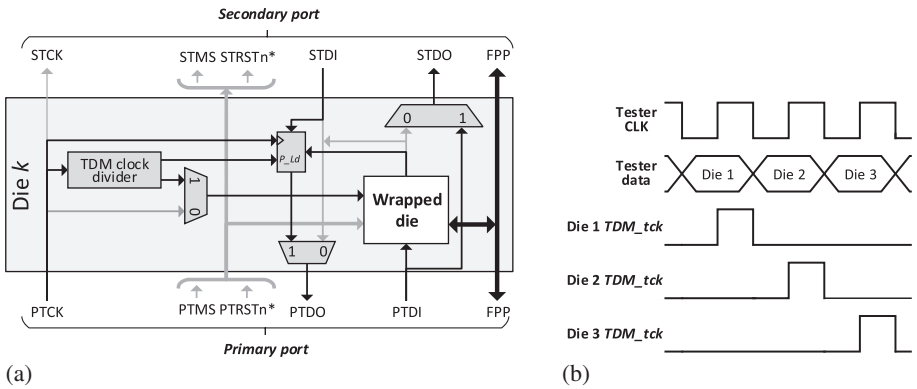
Fig. 2(a) shows that on each stack tier, there is a wrapped die and a simple proposed configurable logic to enable 3D-TDM. The configurable logic for each die includes:

(1) multiplexing logic for configuring either the proposed TDM-based architecture or the conventional P1838 architecture, which is important for diagnosability.

(2) a TDM clock divider that divides the test clock to generate *TDM_clk* for the corresponding die wrapper.

(3) a logic block for the test data output from the wrapped die. These logic blocks from all dies constitute a parallel-in serial-out shift register across the stack. This shift register loads in parallel from all wrapped dies with TCK if parallel load *(P_Ld)* signal is HIGH otherwise it serially shifts-out.

The FPP lanes for scan data in and out are respectively configured in the same way as TDI and TDO paths are configured. The proposed architecture connects all



(a) (b)

Fig. 2. (a) IEEE P1838 complied wrapped die for TDM-based test access and (b) timing diagram of TDM for a three-die stack.

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of the test data/control lines to each die wrapper in parallel, unlike the conventional P1838 architecture.

The configurable logic is controlled by an additional test data register of a die wrapper (the 3D-TDM test data register) and it can be selected with a dedicated instruction. It has four segments: *TDM_mode*, *TDM_clk_EN*, *No. of time-slots*, and *Allocated time-slot*, as shown in Fig. 3 (upper block). The *TDM_mode* segment controls all multiplexers illustrated in Fig. 2(a). The *TDM_clk_EN* segment controls the TDM clock divider. The pattern in the *No. of time-slots* segment limits the counting range of the counter, in other words, this segment defines the number of time-slots for a stack. The pattern in the *Allocated time-slot* segment defines the allocated time-slot to the corresponding die.

TDM clock divider is a configurable block and it generates (1) the desired number of time-slots, (2) the *TDM_clk* pulse at the allocated time-slot for the corresponding die wrapper, and (3) the *P_Ld* signal for loading the output of the die wrapper into the corresponding logic block of parallel-in serial-out shift register. *P_Ld* signal is asserted after the shift operation for all time-slots is completed, i.e., when the counter's output is '00'. The configurability relaxes the optimization and test access scheduling for each test stage from the knowledge of the number of dies to be stacked and their hierarchical tier. Thus, we can configure the number of time-slots according to the test frequency limits imposed by the wafer-level and package-level tests. Moreover, we can allocate one or more time-slots to a stacked die.

TDM clock divider is comprised of a comparing logic and a counter, which operates at the negative edge of TCK. Fig. 3 (lower block) illustrates an example of a 2-bit configurable TDM clock divider. It compares the contents of the *No. of time-slots* segment of 3D-TDM test data register with the counter's output to generate a reset signal for the counter that is a synchronous reset. Hence it recursively counts 0, 1 and 2, or generates three time-slots.

Furthermore, TDM clock divider compares the contents of the *Allocated time-slot* segment with the output of the counter, if matched, the successive TCK pulse is passed to the corresponding die wrapper through *TDM_clk* line. The example TDM clock divider in the figure allocates the 2nd time-slot to the corresponding stacked die. The counter is enabled or disabled with the *TDM_clk_EN* signal. The counter can be disabled when the test operation of the corresponding die is finished or when it needs to be paused due to the test schedule.

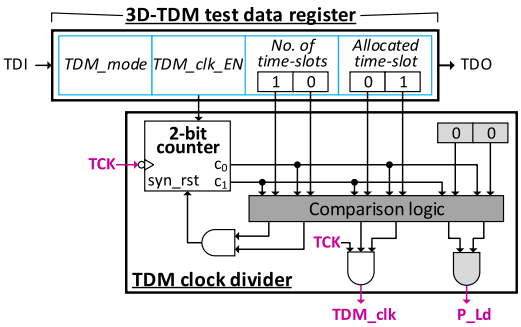

Fig. 3. 3D-TDM test data register (upper block) and an example 2-bit configurable TDM clock divider (lower block).

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A non-overlapping clock to each die-wrapper allows applying separate TMS signal for each wrapped die. The TMS signal streams of multiple TAP controllers is merged in such a way that each die wrapper samples the corresponding TMS signal during its allocated time-slot. Thus, the state of the TAP controller of each die is independent of each other, unlike the conventional P1838 architecture.

Hence, as the proposed architecture independently accesses multiple dies in a time-division manner with faster tester-channel frequency and with full test bandwidth, the absolute test time is significantly reduced compared to the sequential test of all stacked-dies.

Besides, the functional paths for the TDM logic on a die, see Fig. 2(a), can be tested with the integrity test of the other test logic. First, 3D-TDM-TDR can be tested by shifting a stream of alternative 0s and 1s. For testing the remaining TDM logic, select bypass register, load both the *TDM_mode* and *TDM_clk_EN* segments with '1', and load the segments associated to the TDM clock divider to generate only two time-slots. Assign one time-slot to the corresponding wrapped die. Apply a test data stream on PTDI and STDI and observe through the wrapper-cells of PTDO and STDO. Thus, following functional paths are tested: PTDI → STDO, PTDI → PTDO, SDTI → PTDO and clock-associated paths.

Most of the DFT of recent SoCs include scan compression techniques to cope with the ever-increasing test data volume to reduce the test cost and improve the test quality. Scan compression reduces the number of scan-in pins that reduces the parallel 3D TAM width of the corresponding die. Thus, a scan compression based dies can further improve the test time.

Moreover, at-speed test is also adopted for recent SoCs in which the launch and capture are performed with functional clock. Therefore, to implement at-speed test with the proposed architecture, TDM mode can be surrendered during capture state of TAP controller. This approach may increase the capture power due to simultaneous capture operation on multiple dies. This issue can be tackled by incorporating capture power reduction techniques, e.g., clock-gating based approach [9].

3 Experimental results

We evaluate the time-multiplexed test access with a synthetic SIC with five SoCs from the ITC'02 benchmark set [10], i.e., p93791, p34292, p22810, f2126 and d695, which are respectively stacked from bottom to top. Each SoC is considered a separate die. We assumed that all cores are soft cores; thus, all cells (boundary and scan) of a core are evenly distributed among TAM wires, i.e., $\lceil \frac{total\ cells}{TAM\ width} \rceil$, and the assumed TAM width is 16 wires. The number of cells of each module of benchmark SoCs and the number of test vectors are specified in [10]. All cores of an SoC are considered in a single design level rather than hierarchical levels.

An assumed test architecture for each die is defined as follows. Each core is tested sequentially with the full TAM width, i.e., one core at a time. The scan-shift frequency is 50 MHz, and the test frequency limits at the wafer-level and package-level tests are 100 MHz and 1 GHz, respectively. Thus, the upper bounds of the number of time-slots at the wafer-level and package-level tests are 2 and 20, respectively. We have calculated the absolute test time for the sequential and time-

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multiplexed test accesses. In the sequential test access of dies, one die is tested at a time.

Total test time of an SIC is the sum of test times at all its test stages. For example, three known good dies are to be stacked into a single SIC, its test stages include:

1) A stacked test of two dies with TDM at 100 MHz; this test can be represented as *TDM(1,2)*.
2) A stacked test of three dies in which two dies are tested with TDM at 100 MHz and, and sequentially, one die is tested at 50 MHz. This test can be represented as TDM(1,2), 3.
3) A packaged test of three dies in which three dies are tested with TDM at 150 MHz, and is represented as TDM(1,2,3).

The comparison in Table I reveals that the time-multiplexed test access significantly reduces the total absolute test time of SIC compared to the sequential test access to each die because it leverages the test frequency limits. Since the test time of all dies is not same, dummy bits are transmitted until all stacked dies are tested. However, an efficient optimization and test access scheduling can further improve the test time, and it is an open issue for future work.

Table I. Absolute test time comparison of a synthetic SIC

Test stage	Test schedule	Test freq. (MHz)	Absolute test time *(ms)*	
			Sequential test access	Time-multiplexed test access
2-die stack	*TDM(1,2)*	100	60.49	38.24
3-die stack	*TDM(1,2), 3*	100	70.80	48.55
4-die stack	*TDM(1,2), TDM(3,4)*	100	77.48	48.55
5-die stack	*TDM(1,2), TDM(3,4), 5*	100	78.39	49.46
Packaged	*TDM(1,2,3,4,5)*	250	78.39	38.24
Total absolute test time of SIC (milli-seconds)			**365.55**	**223.04**
Total percentage reduction (%)			—	***38.99***

4 Conclusion

We have presented a time-multiplexed test access architecture, compatible with IEEE P1838, for stacked ICs. It leverages the tester-channel frequency at each test stage and significantly reduces the absolute test time of an SIC. The results showed that the test time is significantly reduced with respect to the sequential test access to each die.

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