Sputter-grown GeTe/Sb_2Te_3 superlattice interfacial phase change memory for low power and multi-level-cell operation

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The multi-level feature of GeTe/Sb_2Te_3 interfacial phase change memory was achieved by applying a designed voltage-based pulse. It stably demonstrated five multi-level states without interference for 90 cycles by varying the pulse width. GeTe/Sb_2Te_3 interfacial phase change memory demonstrated retention time of $> 1.0 \times 10^3$ s, presenting the significantly low drift coefficient (ν) of < 0.009, indicating no resistivity drift due to the structure relaxation of glass. In addition, the reset energy consumption of GeTe/Sb_2Te_3 interfacial phase change memory was reduced by more than 85% compared to conventional $Ge_2Sb_2Te_5$ phase change memory at each bottom electrode contact size. Multi-level-cell operation mechanism and gradual increase in conductance value of GeTe/Sb_2Te_3 interfacial phase change memory was explained by a partial resistance transition model where phase transition occurred partially in all layers. The result of the GeTe/Sb_2Te_3 interfacial phase change memory performance is expected to bring great advantages to the next-generation storage class memory industry that requires low energy and high density.

Introduction: Phase change memory (PCM), which stores data as reversible phase transitions between an amorphous and crystalline state, has been considered as a promising candidate for the next-generation storage class memories (SCM) due to its simple structure, fast switching speed, low power consumption, high density, and CMOS compatibility [1]. Among chalcogenide phase change materials, the $Ge_2Sb_2Te_5$ (GST) alloy has been extensively studied in optical and electronics applications [2]. The switching of the GST alloy creates a conductive state by applying a current or voltage pulse at a temperature higher than 150°C, which is called SET operation. The amorphous state with high resistance is formed by melting temperature higher than 625°C in a crystalline material subsequently quenching, which is called the RESET operation. The difference in resistance between the SET and the RESET is determined by the chemical bonding of phase change materials. The crystalline GST has a six-fold coordinated resonant bonding with a long bond length. Conversely, the amorphous GST has a covalent bonding aligned with the 8-N rule with a relatively short bond length [3]. However, since the phase transition of the GST alloy is three-dimensional, a huge amount of entropy loss occurs, leading to high energy consumption and heat dissipation, especially during RESET operation [4]. To overcome this weakness, interfacial phase-change memory (iPCM) has emerged in which van der Waals (vdW) gap is located between alternately deposited GeTe/Sb_2Te_3 ultrathin layers, forming a superlattice structure [5]. In iPCM structure, Ge atoms located in between two-dimensional Sb_2Te_3 films in the iPCM structure drifted along with the vdW gap by electrical or optical excitation. Depending on the motion of Ge atoms, the stacking sequence of the superlattice film varies, which is expected to produce a reversible transition from high-resistance state (i.e., inverted Petrov phase) to low-resistance state (i.e., Ferro, Petrov phase) and vice versa [6]. Even though the underlying switching mechanism of iPCM device is still controversial, as switching of iPCM is a non-melting process, the iPCM produced lower entropy than the GST PCM resulted from the movement of Ge atoms limited within the GeTe layer. Therefore, the superlattice structure has strength in reliability and fast switching characteristics based on a crystalline-to-crystalline state in the Ge-Te bonding state [7]. The iPCM mechanism realized a fast operating speed and reduced power consumption by restraining an atomic movement. Although some researches on the operation of iPCM have been reported, researches on the multi-level-cell (MLC) operation and its mechanism are still insufficient [8].

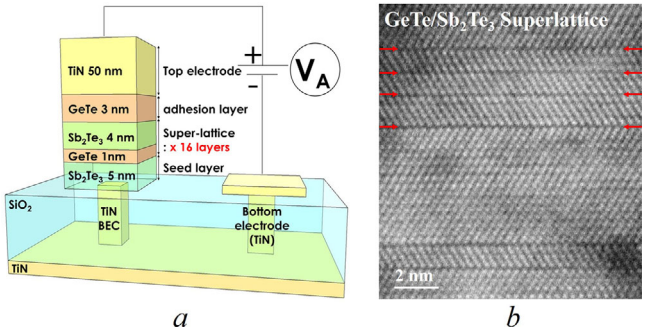

Fig. 1 *Fabricated the GeTe/Sb_2Te_3 iPCM device. (a) Schematic of the GeTe/Sb_2Te_3 iPCM. (b) HR-TEM image of GeTe/Sb_2Te_3 superlattice structure (the red arrow represents the van der Waals gap between thin films)*

In this study, we fabricated the poly-crystalline GeTe/Sb_2Te_3 films with vdW gap by using a sputtering system and investigated the dependence of crystalline of the GeTe/Sb_2Te_3 films on deposited temperature. In particular, MLC operation (five multi-level states) and low power switching of iPCM were demonstrated by a simple voltage-based electrical pulse scheme and increased step pulse programming (ISPP). Lastly, the mechanism for the MLC operation of iPCM was discussed in detail using a partial resistance transition model.

Methods: An approximately 30-nm-thick SiO_2 film was deposited on a TiN/SiO_2 wafer by chemical vapour deposition (CVD) and nano-holes ranging from 34 to 1921 nm were patterned by photo lithography and dry etching. Interconnected ~ 50-nm-thick plug-type TiN bottom electrodes were fabricated by TiN-film deposition on the nano-holes and subsequent chemical mechanical planarization (CMP). Afterwards, all the films were fabricated by multi-chamber cluster sputtering system without vacuum breaking under a high vacuum of $< 1 \times 10^{-8}$ torr. The GeTe and Sb_2Te_3 thin films were deposited by a two-step growth method [9]. To ensure the formation of highly (00l) oriented superlattice films, a 5-nm-thick amorphous Sb_2Te_3 seed layer was deposited at room temperature and annealed at 270°C for an hour on the TiN which serves as a bottom electrode contact (BEC). Afterwards, GeTe/Sb_2Te_3 superlattice films were deposited by alternately sputtering the alloy targets of GeTe and Sb_2Te_3 at 270°C, in which the thickness of GeTe and Sb_2Te_3 was fixed at 1 and 4 nm, respectively. GeTe/Sb_2Te_3 superlattice films were repeatedly deposited for 16 cycles, resulting in a total thickness of 80 nm. A 3-nm-thick GeTe film was deposited as an adhesion layer right before depositing a top electrode. GeTe/Sb_2Te_3 superlattice films were naturally cooled down to room temperature in the vacuum ambient. Lastly, a TiN film was deposited, which served as a top electrode contact (TEC). The schematic structure of fabricated iPCM was illustrated as shown in Figure 1a. In addition, the cross-sectional structure of GeTe/ Sb_2Te_3 superlattice was observed by a high resolution transmission electron microscopy (HR-TEM, JEM-2100F), as shown in Figure 1b. Furthermore, the crystallinity of Sb_2Te_3 seed layer and grown superlattice structure were analysed by X-ray diffraction (XRD). Cu-Kα (= 0.1542 nm) radiation was used in a Bragg–geometry (θ-2θ symmetric scans) for out-of-plane orientation (Smart lab, Corp.). In addition, $Ge_2Sb_2Te_5$ PCM was fabricated on a TiN bottom electrode patterned wafer with the identical BEC size for comparison. The resistance-voltage (R-V) characteristics and conductance values of iPCM was measured using Keithley 4200A-SCS parameter analysers.

Results: It was necessary to determine the temperature conditions for sputtering superlattice film before depositing the superlattice structure, because the superlattice films of GeTe/Sb_2Te_3 iPCM must be highly oriented to perform a crystalline-crystalline transition. Note that the

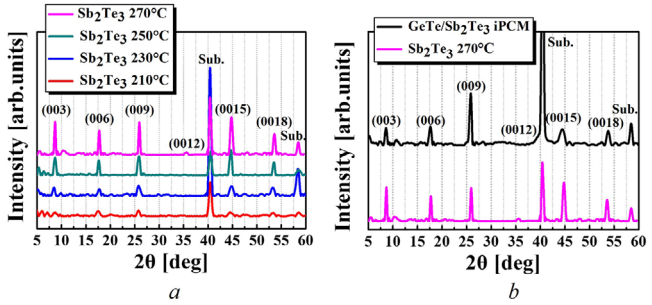

Fig. 2 *Analysis on crystallinity of the Sb_2Te_3 seed layer and the GeTe/Sb_2Te_3 superlattice thin film. (a) Crystallinity of Sb_2Te_3 thin film varying with annealing temperature. (b) Comparison of crystallinity of GeTe/Sb_2Te_3 superlattice thin film and Sb_2Te_3 thin film annealed at 270°C*

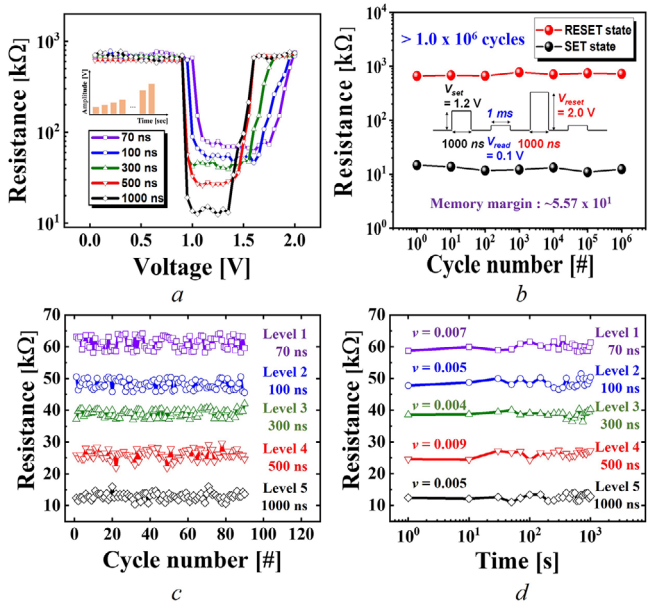

Fig. 3 *Non-volatile memory cell performance of GeTe/Sb_2Te_3 iPCM. (a) GeTe/Sb_2Te_3 iPCM unipolar switching characteristic. (b) Single-level operation of the GeTe/Sb_2Te_3 iPCM. (c) Multi-level operation of the GeTe/Sb_2Te_3 iPCM. Level 1, 2, 3, 4 and 5 are corresponding to pulse width of 70, 100, 300, 500 and 1000 ns, respectively. (d) Multi-level retention of the GeTe/Sb_2Te_3 iPCM*

crystallinity of the Sb_2Te_3 seed layer determines the crystalline quality of the GeTe/Sb_2Te_3 iPCM, because the subsequently deposited thin films are self-aligned with the first deposited Sb_2Te_3 film which is called a seed layer. The crystallinity of Sb_2Te_3 thin films annealed at different temperatures was demonstrated as shown in Figure 2a. It indicates that all thin films annealed at 210 to 270°C have a hexagonal (00*l*) peak in the *c*-axis. Among them, the Sb_2Te_3 thin film annealed at 270°C has the most highly-oriented structure. In other words, the Sb_2Te_3 thin film has the largest crystal grain size at 270°C. Furthermore, it presented a peak position similar to the optimum Sb_2Te_3 thin film as shown in Figure 2b. Comparing the XRD peaks of the GeTe/Sb_2Te_3 superlattice films in detail, they are relatively broad or slightly deviated from (00*l*) compared to the peaks of the Sb_2Te_3 thin films annealed at 270°C. It can be inferred that these results were due to the applied strain caused by the repeated deposition of ultra-thin GeTe/Sb_2Te_3 superlattice films. Although it is difficult to understand the exact arrangement of atoms in the superlattice structure, it was confirmed that iPCM composed of highly (00*l*) oriented GeTe/Sb_2Te_3 superlattice films could be fabricated under optimal condition.

The electrical switching characteristics of GeTe/Sb_2Te_3 iPCM was investigated by applying voltage-based AC square pulse designed with the pulse scheme of ISPP in which the pulse width was fixed and the amplitude of the voltage was increased by 0.05 V, as shown in Figure 3a. The five R-V curves for the iPCM samples in Figure 3a exhibited RESET and SET process in one polarity. Afterwards, the reliability (i.e., write/erase

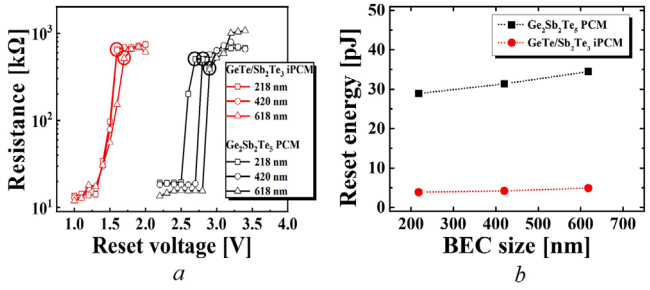

Fig. 4 *Comparison of RESET operation and RESET energy of GST PCM and GeTe/Sb_2Te_3 iPCM. (a) Resistance versus reset voltage of GST PCM and GeTe/Sb_2Te_3 iPCM with different BEC size of 218, 420 and 618 nm. (b) RESET energy of GST PCM and GeTe/Sb_2Te_3 iPCM with different BEC size*

endurance cycle) of iPCM sample using pulse width of 1000 ns was measured. It demonstrated the endurance cycles of $> 10^6$ cycles, sustaining the memory margin of $\sim 5.57 \times 10^1$, as shown in Figure 3b. Furthermore, it should be noted that the shorter the pulse width, the lower the on/off ratio and wider the voltage range to persist the SET state. This implies that multi-level cell characteristics can be achieved by implementing an intermediate resistance resulting from the change in the pulse width. Based on the ISPP with various pulse width conditions, five intermediate resistance states sustaining 90 cycles were obtained, as shown in Figure 3c. It should, however, be noted that this multi-level feature is difficult to be implemented in the case of a GST PCM as it is difficult to control the uniformity of the thermal distribution applied to the phase change material. In addition, since the major obstacle of data retention in multi-level GST PCM is the resistance drift caused by structural relaxation of amorphous GST, the resistance drift coefficient was calculated by using Equation (1), where R_0 is the initial resistance at t_0, and ν is the fitted resistance drift coefficient to confirm the unique operation mechanism of iPCM [10]:

$$R(t) = R_0 \left(\frac{t}{t_0}\right)^{\nu} \tag{1}$$

The multi-level retention characteristics of iPCM was evaluated, as shown in Figure 3d. It demonstrated the multi-level retention time of $> 1.0 \times 10^3$, presenting the low drift coefficient (ν) of < 0.009. Therefore, this suggests that the operation mechanism of iPCM is intrinsically different from the GST PCM.

The RESET operation of GeTe/Sb_2Te_3 iPCM samples were investigated by characterizing R-V curves of three GeTe/Sb_2Te_3 iPCM with different BEC size, as shown in Figure 4. Regardless of BEC size, all GeTe/Sb_2Te_3 iPCM exhibited significantly lower RESET voltage than the GST PCM, that is, 1.8 V for iPCM and 2.8 V for GST PCM, respectively, as shown in Figure 4a. The RESET energy of GST PCM and GeTe/Sb_2Te_3 iPCM samples was extracted at the point (the black and the red circles in the R-V curve) where the resistance became a high resistance state as the pulse was applied. Since the current value is not a constant value during the phase transition, the energy consumption for the RESET operation was roughly calculated by using the Equation (2), where E_{RESET} is the energy consumption for the RESET operation, V_{RESET} is the voltage at the point where the high resistance was achieved and *t* is the time of the applied pulse:

$$E_{RESET} = \left(\frac{V_{RESET}^2}{R_{RESET}}\right) \cdot t \tag{2}$$

The RESET energy of both GST PCM and GeTe/Sb_2Te_3 iPCM increased with BEC size. However, the RESET energy of GeTe/Sb_2Te_3 iPCM was significantly lower than that of GST PCM. That is, the RESET energy of the GeTe/Sb_2Te_3 iPCM was reduced by 85% compared with that of the GST PCM at the same BEC size, as shown in Table 1. In particular, by comparing the slope of the reset energy change depending on the BEC size, it was found that the GeTe/Sb_2Te_3 iPCM had a weaker dependence on heat than the GST PCM, as shown in Figure 4b. This was due to the less effect of heat concentration in GeTe/Sb_2Te_3 iPCM than in GST PCM, resulting from lower V_{RESET} of the GeTe/Sb_2Te_3 iPCM

Table 1. Relative energy reduction of iPCM compared with PCM

BEC (nm)	218	420	618
Energy reduction	86.57%	86.64%	85.57%

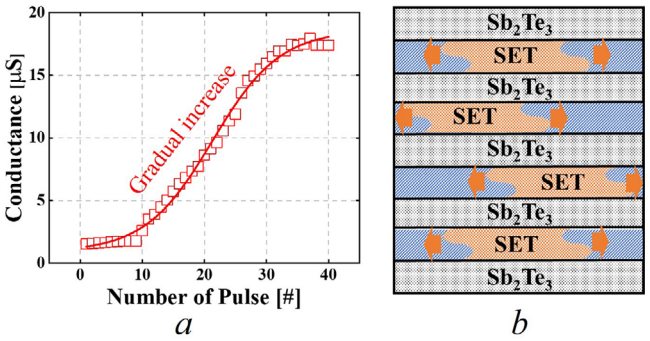

Fig. 5 *Demonstration of intermediate resistance mechanism of the GeTe/Sb_2Te_3 iPCM. (a) The gradual conductance characteristic of GeTe/Sb_2Te_3 iPCM. Apply 70 ns, 0.8 V pulse. (b) Model of partial resistance transition model in GeTe/Sb_2Te_3 iPCM*

than the GST PCM. Therefore, unlike GST PCM, operated by a melting-quenching mechanism, GeTe/Sb_2Te_3 iPCM is more likely to operate by a mechanism such as charge injection.

Although several researches on MLC operation of iPCM have been reported, the mechanism for the MLC operation of iPCM has not clearly been elucidated. In particular, the mechanism for MLC operation of the GeTe/Sb_2Te_3 iPCM can be explained by the gradual conductance characteristic. As shown in Figure 5a, when a number of identical set pulse with an amplitude of 0.8 V and width of 70 ns was applied to the GeTe/Sb_2Te_3 iPCM, the conductance value gradually increased. From this result, the mechanism for MLC operation of GeTe/Sb_2Te_3 iPCM can be suggested through the partial model, as shown in Figure 5b. Although several mechanisms on iPCM operation have been proposed, it has not been elucidated clearly. Nevertheless, it is clear that the atomic structure change due to the movement of Ge atoms located within the GeTe thin film of the GeTe/Sb_2Te_3 iPCM is the main cause of the transition of resistance. Therefore, it can be assumed that the movement of Ge atoms located within the GeTe thin films in a superlattice play an important role in GeTe/Sb_2Te_3 iPCM. We assume a partial model in which the resistance states of all GeTe thin films are partially changed. If the resistance state of GeTe thin film is changed one-by-one, the resistance must be changed discretely while the electrical pulse is applied. However, the GeTe/Sb_2Te_3 iPCM clearly demonstrated 40 conductance states, which gradually increased. In other words, it may be reasonable to suppose that the resistance transition of the iPCM does not change for each layer. The gradual change in conductance is clear evidence that the MLC operation of GeTe/Sb_2Te_3 iPCM can be explained by the partial model in which resistance partially changed in all layers. The lower the applied energy, the smaller the area of resistance change of all GeTe films in the GeTe/Sb_2Te_3 iPCM. It is speculated that the difference in the total energy applied by the pulse width seems to control the partially changing area of the GeTe/Sb_2Te_3 iPCM. These results are consistent with previous research demonstrating the thermal distribution and gradual electrical characteristics of iPCM when the electrical pulse is applied [11,12]. As a result, it is evident that the on/off ratio can be changed by varying the applied pulse width. In the case of the GST PCM, however, the phase transition occurs based on a melting-quenching mechanism. Therefore, in the RESET process, the resistance increases more rapidly than that of the iPCM. The difference in electrical characteristics between the GST PCM and GeTe/Sb_2Te_3 iPCM may contribute to artificial synaptic applications that require a gradual increase in conductance in future works.

Conclusion: In conclusion, we demonstrated fundamental electrical memory characteristics based on GeTe/Sb_2Te_3 iPCM. We have presented the possibility of MLC operation of the iPCM varying the pulse width through electrical pulse scheme design. In addition, it was confirmed that, compared to the GST PCM, the RESET energy consumption was reduced about 85% by atomic movement restraint. Furthermore, we explained the electrical characteristics of the iPCM through a partial model, since it demonstrated gradual increase in conductance as electrical pulse was applied. In conclusion, this work presents great potential for GeTe/Sb_2Te_3 iPCM to become one of the most promising candidates for storage class memory applications.

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