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Impact of Residual Stress on a Polysilicon Channel in Scaled 3D NAND Flash Memory

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Abstract: The effects of residual stress on a tungsten gate in a polysilicon channel in scaled 3D NAND flash memories were investigated using a technology computer-aided design simulation. The NAND strings, with respect to the distance from the tungsten slit, were also analyzed. The scaling of the spacer thickness and hole diameter induced compressive stress on the polysilicon channel. Moreover, the residual stress of polysilicon channel in the string near the tungsten slit had greater compressive stress than the string farther away. The increase in compressive stress in the polysilicon channel degraded the Bit-Line current (I_{on}) due to stress-induced electron mobility deterioration. Moreover, a threshold voltage shift (ΔV_{th}) occurred in the negative direction due to conduction band lowering.

Keywords: 3D NAND; hole profile; mechanical stress; polysilicon channel; scaling; TCAD

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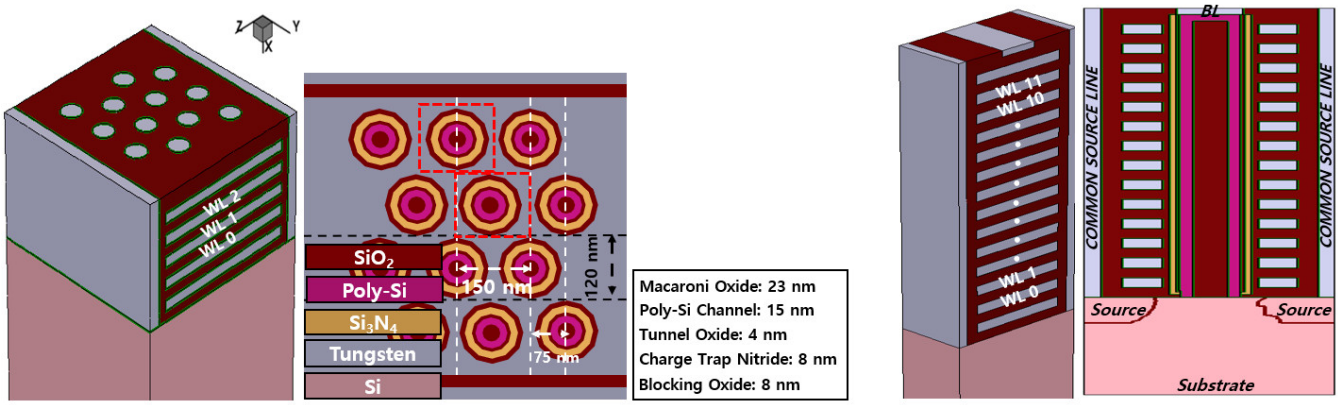
1. Introduction

The memory market, originally driven solely by the mobile device industry, has expanded because of the emerging artificial intelligence and automobile industries. The explosive growth of data generated by these industries demands an increase in the storage capacity of 3D NAND. This demand has been met by increasing the number of stacking gate layers (WL), which reached 128 levels in 2019 [1,2]. As the number of WL layers increases, the difficulties in fabrication, such as hole etching and control of mechanical stress, have increased [3,4]. Therefore, vertical scaling is necessary to achieve 3D NAND technology with 200 levels and beyond, because the thickness of the total chip is limited to approximately 25 μm for stacking 16 chips [5]. Moreover, lateral scaling, such as of the hole diameter, is another way to achieve a higher density [6]. In our previous work, the annealing temperature, channel hole angle, and tungsten intrinsic stress were parameters that changed the residual stress of the polysilicon channel in 3D NAND, and the change in stress distribution of the polysilicon channel affects the electrical characteristics, degrading the 3D NAND BL current [7]. Furthermore, residual stress generates the dangling bond, which increases the trap site, leading to deterioration of the interface properties. Therefore, cell characteristics, such as the leakage current and memory window, were degraded [8]. Although there are various studies on mechanical stress in 3D NAND, the impact of vertical and lateral scaling on the residual stress of the polysilicon channel has not been studied. This work investigated the residual stress of the polysilicon channel according to the spacer oxide thickness and hole diameter and its impact on the I_{on} and V_{th} of 3D NAND. The distribution of threshold voltage was also analyzed using TCAD simulation.

2. Materials and Methods

The simulations were conducted on two types of 3D NAND structures to investigate the residual stress of films and the stress-induced effects on the electrical characteristics, respectively, and to minimize simulation time. Figure 1a shows the structural and stack

details of the 3D NAND device for stress analysis simulation. Twelve strings, with each string comprising 3 WLs with a string select line (SSL) and a ground select line (GSL), were considered. The diameter of the vertical hole was 120 nm with 150 nm of cell string pitch. Two strings along with the red square dotted box were selected for the stress simulation in order to investigate the position of strings relative to the common source line. The string located near the center and the common source line of 3D NAND will be called the center and slit string, respectively. The structure for the stress-induced effects simulation consisted of 12 WLs, as shown in Figure 1b. The thickness of the macaroni oxide, polysilicon channel, tunnel oxide, charge trap nitride, and blocking oxide were identical for both structures.



(**a**) (**b**)

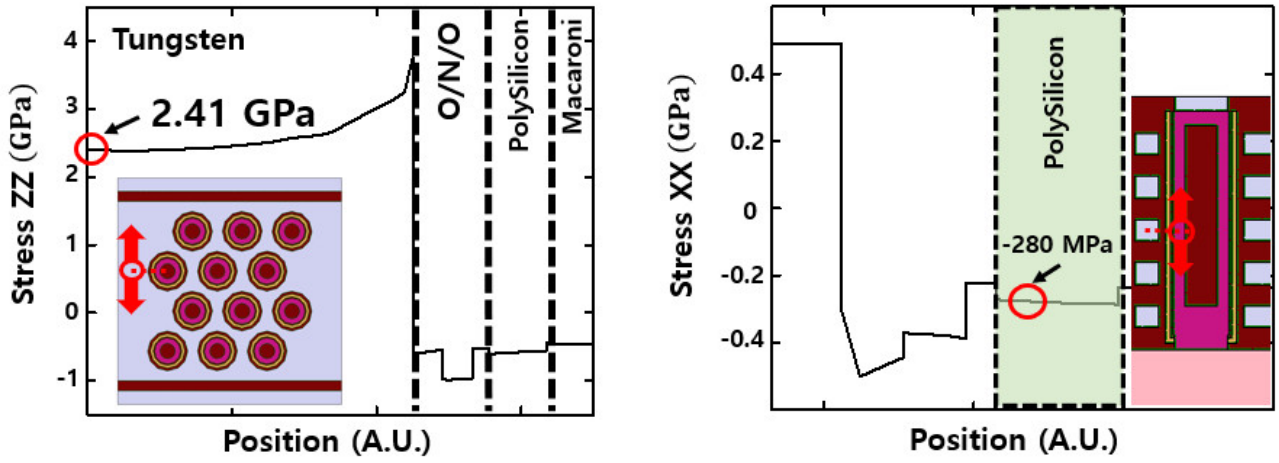
Figure 1. 3D NAND model used for stress simulation and material parameters. 3D simulation model of 3D NAND used in (**a**) the stress simulation and (**b**) the stress-induced electrical characteristics variation simulation.

To accurately analyze the impact of scaling on the residual stress of films, the internal stress of tungsten films was tuned to match the industrial devices. As shown in Figure 2a, the residual stress of the tungsten films after the tungsten replacement gate process was approximately 2.41 GPa, which matches reported experimental data [9]. The residual stress of the polysilicon channel at the final structure in the simulation, as shown in Figure 2b, was −280 MPa, which is also similar to the reported data [10]. The distribution of the residual stress of the polysilicon channel in 3D NAND was then analyzed when scaled. The residual stress was calculated using the Maxwell model, which takes dilatational and deviatoric stress into consideration [11]. The mechanical parameters used in this study are summarized in Table 1.

Table 1. Mechanical parameters used in the 3D NAND simulation. The Young's modulus (YM), bulk modulus (BM), shear modulus (SM), Poisson's ratio (PR), and coefficient of thermal expansion (CTE) were used to calculate the mechanical stress simulation.

Materials	YM [GPa]	BM [GPa]	SM [GPa]	PR	CTE
Silicon Oxide	70	39	29	0.20	1.37
Polysilicon	160	99	65	0.23	3.00
Silicon Nitride	270	196	106	0.27	3.20
Tungsten	410	311	160	0.28	4.60
Silicon	130	98	51	0.28	3.00

To accurately investigate the impact of residual stress on the electrical characteristics, the BL current and threshold voltage were calibrated by tuning the doping and interface trap parameters of polysilicon to match the reported data, as shown in Figure 3 [12]. Moreover, the deformation potential (minimum, ekp, and hkp) and subband (doping, effective mass, and scattering) model were incorporated in the TCAD device simulations.



(**a**) (**b**)

Figure 2. TCAD calibration with the reported experimental data. The residual stress of (**a**) the tungsten film after the tungsten replacement gate process and (**b**) the polysilicon channel in the final structure.

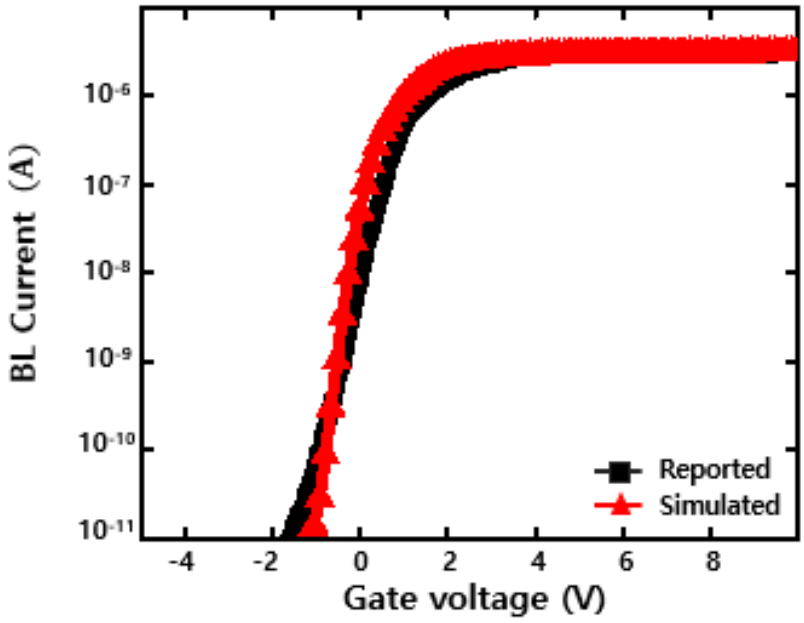


Figure 3. TCAD calibration for the initial state I_d-V_g characteristics of the memory transistor with the reported data [12].

3. Results and Discussion

Impact of Scaling on the Residual Stress of the Polysilicon Channel

The residual stress of the polysilicon channel in two strings was considered for analyzing the impact of tungsten films in a common source line. As shown in Figure 4a, the polysilicon channel in the string closest to the common source line had greater compressive residual stress than that in the string closest to the center. When the thickness of the spacer oxide was scaled from 30 nm to 25 nm and 19 nm, with the hole diameter fixed to 120 nm, the channel stress increased in the compressive direction due to the adjacent tungsten gates, which had greater tensile stress than the other films because of their proximity [7]. When the hole diameter was scaled from 120 nm to 100 nm by 10 nm, with the spacer thickness fixed to 30 nm, the channel stress was also increased during compression because of the increase in volume of the tungsten gates surrounding the hole. Figure 4b shows the channel stress when the spacer thickness and hole diameter were both scaled. The channel stress

nearly doubled during compression from −260 MPa to −620 MPa in the string closest to center, and from −340 MPa to −660 MPa in the string closest to the common source line, when scaled.

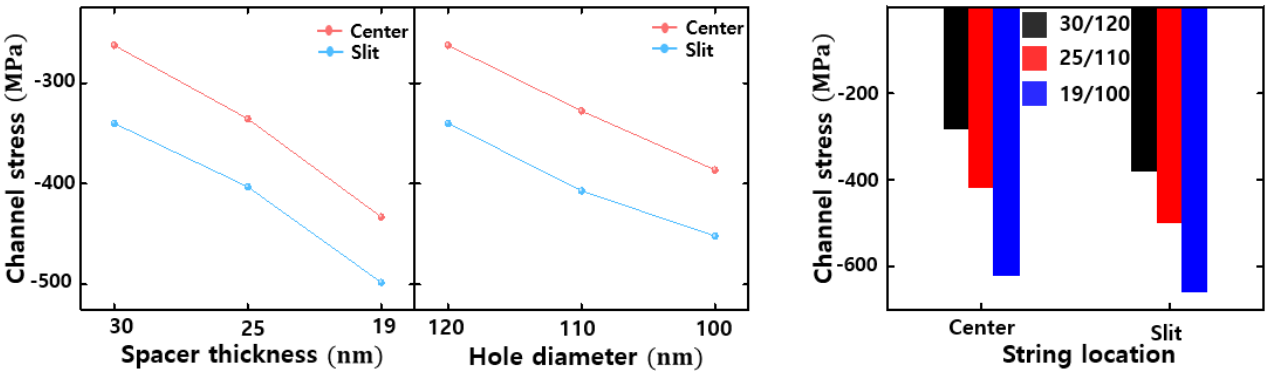
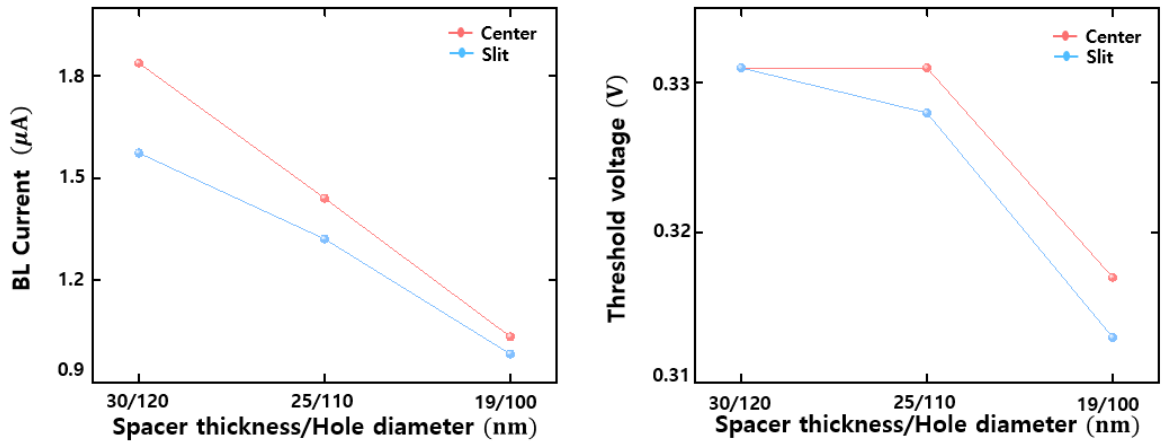


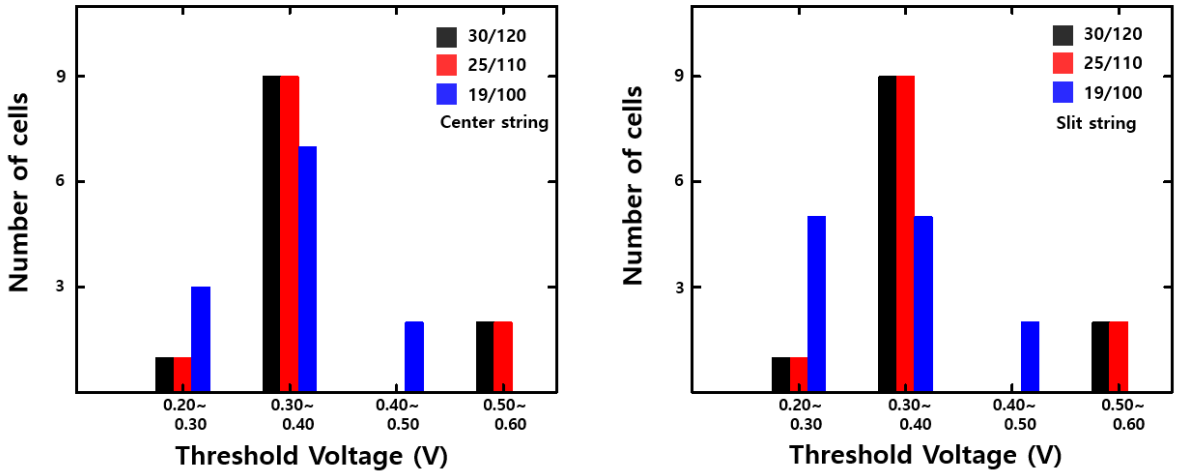
Figure 4. The channel stress of the two strings with respect to the distance from the common source line. The channel stress of two strings when the spacer thickness and hole diameter were (**a**) individually scaled and (**b**) both scaled.

Electrical characteristics, such as BL current (I_{on}) and threshold voltage (V_{th}), are affected by the residual stress of the channel region in 3D NAND [13,14]. The compressive channel stress decreases the I_{on} value due to the degradation of electron mobility caused by the piezo-resistance effect [15]. Furthermore, V_{th} is negatively shifted, with increasing compressive channel stress due to the lowering of the conduction band [16,17]. The electrical characteristics of the scaled structure are affected by the stress factors and scaling factors. To analyze the impact of only the stress factors, the structure shown in Figure 1b was used, and the residual stress of the polysilicon channel was modulated by depositing tungsten film with different internal stresses to match the simulation data of the channel stress shown in Figure 4b. The BL current and threshold voltage were measured on WL5. Figure 5 presents the BL current and threshold voltage as a function of spacer thickness and hole diameter with the string location. As shown in Figure 5a, the BL current of the string located near the center degraded from 1.84 μA to 1.44 μA and 1.03 μA, with scaling. Moreover, the BL current of the string located near the slit deteriorated from 1.57 μA to 1.32 μA and 0.98 μA. The degradation of the BL current in the two studied strings was attributed to the deterioration of electron mobility caused by increased compressive residual channel stress with scaling [18]. The threshold voltage was shifted negatively in both strings with scaling, as shown in Figure 5b, which can be attributed to conduction band lowering due to the increased channel compressive stress. Therefore, the scaling of the spacer thickness and hole diameter deteriorates the BL current and negatively shifts the threshold voltage of 3D NAND. Figure 6 shows the histogram of threshold voltage of cells in the string located near the center and common source line. When the spacer thickness and hole diameter were scaled to 25 nm and 110 nm, the distribution of the threshold voltages of cells showed no change on either string. However, the negative shift of threshold voltage distribution occurred on both strings by the scaling of spacer thickness and hole diameter to 19 nm and 100 nm, respectively.



(**a**) (**b**)

Figure 5. (**a**) BL current and (**b**) threshold voltage of two strings on WL5 when the spacer thickness and hole diameter are both scaled.



(**a**) (**b**)

Figure 6. Distribution of initial threshold voltages of cells when the spacer thickness and hole diameter are both scaled on the string located near the (**a**) center and (**b**) common source line.

4. Conclusions

The impact of scaling on the residual stress of a polysilicon channel on two strings in 3D NAND was investigated using TCAD simulation. When the spacer thickness and hole diameter were scaled, the residual polysilicon channel stress was increased during compression, causing detrimental effects to the electrical characteristics. Moreover, the polysilicon channel stress of the string located closer to the common source line was greater than that of the string located closer to center. Compressive residual channel stress degraded the BL current due to the deterioration of electron mobility, and a negative shift of V_{th} was induced because of the reduced conduction band energy of the polysilicon channel.

This study implies that the residual compressive stress of tungsten must be controlled to prevent degradation of the BL current and the negative shift of the threshold voltage. Further studies are necessary for investigating the impact of stress-induced channel residual stress on the memory characteristics of 3D NAND.

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resources, J.L. and D.-G.Y.; data curation, J.L. and D.-G.Y.; writing—original draft preparation, J.L.; writing—review and editing, Y.-H.S.; visualization, J.L. and D.-G.Y.; supervision, Y.-H.S.; project administration, J.L.; funding acquisition, Y.-H.S. All authors have read and agreed to the published version of the manuscript.

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