energies

MDPI

Article

One-Cycle Control of Three-Phase Five-Level Diode-Clamped STATCOM

In Wha Jeong and Tae Hyun Sung *

Department of Electrical Engineering, Hanyang University, Seoul 04763, Korea; jeongi@uci.edu
* Correspondence: sungth@hanyang.ac.kr

Abstract: This paper presents a new multilevel one-cycle control (OCC) technique for a five-level diode-clamped multilevel converter (DCMC)-based static VAR compensator (STATCOM). The OCC algorithm in combination with multi-carrier level-shifted PWM control is used in the proposed five-level DCMC-based STATCOM. The automatic dc link voltage balance is simply realized by four voltage compensators presented as the part of the OCC controller. In this paper the OCC principle of a two-level converter-based STATCOM is reviewed and extended to the five-level DCMC-based STATCOM. The proposed multilevel OCC control method of the five-level DCMC-based STATCOM in steady-state and dynamic operation modes is verified by simulation and experimental results.

Keywords: one-cycle control; static VAR compensator; dc-link voltage balance; reactive power compensation

check for updates

Citation: Jeong, I.W.; Sung, T.H. One-Cycle Control of Three-Phase Five-Level Diode-Clamped STATCOM. *Energies* **2021**, *14*, 1830. https://doi.org/10.3390/en14071830

Academic Editor: Teuvo Suntio

Received: 5 February 2021
Accepted: 20 March 2021
Published: 25 March 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

To meet the future energy needs and to address environmental concerns, it is necessary to utilize renewable energy resources and minimize the usage of fossil fuel. There has been an extensive growth and development of the renewable energy resources in recent years. Integration of the renewable energy resources into existing power system presents many technical challenges such as voltage stability, power quality problems. Today, more than 340,000 wind turbines are installed all over the world [1]. With fixed speed wind turbine, all the fluctuations in the wind speed are transmitted as fluctuations in the mechanical torque into electrical power in the grid, which causes severe voltage fluctuations. As a result, curtailment is often in order as a necessary measure to reduce the grid impact.

Traditionally, switched capacitors and/or compensation inductors have been applied to the power grid to provide reactive power compensation for voltage support, which can reduce voltage fluctuations in the transmission line. However, these passive compensators, switched capacitors and inductors are not effective for voltage support since their response time is slow, they may produce either over-compensation or under-compensation. They are discrete in nature and less VAR is available when the voltage is low. To overcome these shortcomings, static synchronous compensator (STATCOM) has been introduced as an effective dynamic shunt compensator in transmission and distribution systems [2–16]. Based on solid-state converter topologies, the STATCOMs present fast response time, less space requirement, higher operational flexibility, and excellent dynamic characteristics under various operating conditions.

For medium voltage (MV) applications, multilevel topologies become attractive for high power STATCOMs using commercially available switching devices, such as insulated gate bipolar transistor (IGBT) and integrated gate commutated thyristor (IGCT) [14]. Since multilevel converter-based STATCOMs provide less harmonic generation and higher voltage capability, multilevel STATCOM configuration is a key for the direct connection to the power grid. The number of the STATCOM voltage levels should be maximized to obtain sinusoidal output waveforms and be minimized to make the STATCOM less complicated for reliable power stage and simple control purposes. For high power systems,

three-level diode-clamped multilevel converter (DCMC)-based STATCOMs have been extensively adopted in high voltage power systems.

To reduce harmonic injection into the power grid and realize the transformerless direct connection, five-level DCMC-based STATCOMs have been receiving more attention recently [15,16]. However, the primary obstacle of the five-level DCMC-based STATCOMs is control complexity to control 24 switching devices and achieve charge balance of four dc-link capacitors, for example, by using a modified space vector pulse width modulation (SVPWM) and a capacitor current prediction algorithm with or without additional hardware [15,16]. As far as the implementation of the SVPWM technique is concerned, it is computationally very difficult to realize. For example, there are 125 switching state vectors to operate the five-level DCMC-based STATCOM in [15].

A SVPWM-based switching strategy for a five-level DCMC-based STATCOM was presented without auxiliary power circuits for dc-link capacitor voltage balancing in [15]. The proposed SVPWM method used the redundant switching vectors to mitigate dc-link capacitor voltage drift. However, this SVPWM method had limits of dc-link capacitor voltage balancing, depending on its modulation index. For example, when AC-side current angle was below 10 degrees, the proposed SVPWM method could not provide dc-link voltage balancing for the operating points above 0.55 modulation index. During the transient period, the proposed STATCOM operating point also passed through the region in which dc-link capacitor voltage balancing was not guaranteed.

In [16], a SVPWM switching method for a DCMC-based STATCOM was proposed with a dc-link capacitor current prediction algorithm. First, the proposed SVPWM switching vectors were transferred into the 2-D elliptical plane ($\alpha'\beta'$ frame) instead of the traditional $\alpha\beta$ frame to simplify non-integer calculation. Similar to [15], the redundant switching vectors were used for dc-link capacitor voltage balancing with the help of the additional high-density FPGA-based hardware to accomplish the complex calculation of the proposed SVPWM algorithm. In simulation results, the proposed SVPWM algorithm showed better performance of dc-link capacitor voltage balancing compared to the previous SVPWM-based switching methods. However, the time delay generated by the optimal value calculation algorithm would make an effect in the total performance of dc-link voltage balancing. And it is really difficult to apply the proposed SVPWM algorithm to high-level DCMC-based STATCOMs.

In [17], a modified SPWM method was proposed in order to balance the two dc-link capacitor voltages for the three-level diode-clamped inverters. It is based on changing the boundary offset on the middle point of two carrier signals, which can control the neutral-point current to ensure balanced dc-link capacitor voltages. However, the boundary offset on the middle point restricts the compensation capability of the neutral-point potential when the modulation index is high and this modulation method cannot be directly applicable to the higher level DCMCs, for example, a five-level DCMC since there are more inner junctions between the dc-link capacitors. In addition, the main drawback in this approach is also the restricted stability in order to obtain a simple control strategy.

In [18], a new carrier-based SPWM method with voltage balancing capability was proposed for the five-level diode-clamped back-to-back converter. For the back-to-back configuration, the unbalance tendencies of both sides (a rectifier and an inverter) have a potential to compensate each other because of the symmetry. By controlling proper offset voltages on both rectifier and inverter sides, the average current flowing into the inner junction can be adjusted to be equal to that flowing out from it. Then, the voltage balancing of the inner junction can be achieved. However, this voltage balancing method can be only applied to the back-to-back configuration, not the single type five-level DCMCs. In addition, the switch angles cannot be directly controlled in the proposed SPWM control. Instead, the offset voltage of each inner junction should be calculated and added to the phase voltage reference, which is not the sinusoidal reference.

A closed-loop neutral-point voltage balancing method based on carrier-overlapped pulse width modulation (COPWM) is proposed for the five-level diode-clamped multilevel

inverters in [19]. The COPWM method is a new carrier-based PWM modulation method, which satisfies the volt-second balance principle and has the voltage balancing ability for neutral-point-clamped (diode-clamped) multilevel converters. All the switching signals are obtained by comparing one reference voltage with four carrier signals. However, the generation of the four carrier signals require complex calculation by a DSP chip. Most of all, the four dc-link capacitor voltage balancing is achieved by three steps: (1) voltage balancing between the two outer capacitors, (2) voltage balancing between the two inner capacitors, and (3) voltage balancing between the two inner and the two outer capacitors, which also require complicated calculation and control procedure by the DSP chip. In addition, the harmonic performance of the COPWM method is worse than the phase-disposition PWM methods with the same voltage levels and carrier frequency. Finally, the proposed COPWM method is only applicable when each dc-link capacitance is the same.

In [20], a modified inner-hexagon-vector-decomposition-based space-vector modulation (VDSVM-H1) method was introduced in order to obtain the capacitor voltage balancing with high modulation index and high-power factor by introducing six new vector sequences to each triangle and applying a new vector selection rule. However, the VDSVM-H1 control method has two drawbacks in practice. First, the power factor is very small when the converter works as an active power filter, which brings little challenge to the voltage balancing control. Second, since an error exists between the reference vector and the actual synthesized vector, the magnitude and phase errors increase with the increasing dwelling time of transitional vectors.

A new hybrid voltage balance method was proposed for the five-level DCMCs in [21], where additional flying-capacitor-based auxiliary circuits were used to balance the upper or lower two capacitors, along with a zero-sequence injection method to balance the midpoint voltage. Based on this hybrid approach, the voltage stresses of power devices can be equalized, and the current ripples of inductors can also be suppressed. However, the proposed hybrid voltage balance method requires the auxiliary circuits to balance the upper or lower two capacitors, which need two flying capacitors and inductors, and eight IGBTs with freewheeling diodes for each phase.

As mentioned above, when the voltage level of the DCMC-based STATCOMs increases, the real-time SVPWM balancing control of the dc-link capacitors becomes an enormous challenge. Since thousands of switching space vectors require real-time process, it is extremely time consuming and burden for real-time controller implementation.

The main motivation of this paper on the five-level DCMC-based STATCOMs focuses on developing a simple control method which provides automatic voltage balancing of the dc-link capacitors and dynamic voltage regulation for the power grid. The proposed control method can be easily extended to the high-level DCMC-based STATCOMs by increasing the number of the voltage compensators and the control core circuits and be applicable to other multilevel converter-based STATCOMs, for example, a cascaded multilevel converter (CMC)-based STATCOM.

In this paper, a new five-level DCMC-based STATCOM is proposed using a simple one-cycle control (OCC) [22–26] based on the level-shifted multilevel control, which presents a simple multilevel control approach with automatic dc-link voltage balancing. Compared to the conventional level-shifted control, the proposed level-shifted OCC of the five-level DCMC-based STATCOM has the variable amplitudes of four carrier signals instead of the fixed amplitudes. With variable amplitude control of the four carrier signals, the dc-link capacitor voltages automatically become balanced and equal to the reference voltage ($V_{DC}/4$) for the five-level DCMC-based STATCOM. Applying the proposed multilevel OCC method, voltage regulation at the point of common coupling (PCC) is achieved by dynamically changing the control reference for proper reactive power compensation. The most important merit of the proposed multilevel OCC method is to reduce a heavy computing burden. Especially, this merit is very effective in controlling high-level DCMC-based STATCOMs. In this paper, the voltage regulation equations of the proposed multilevel OCC for the five-level DCMC-based STATCOM are derived to describe its capability of

voltage regulation at the PCC. Simulation and experimental results are presented to verify the proposed five-level STATCOM operation and the multilevel OCC performance during steady-state and dynamic operation modes.

2. Principle of One-Cycle Control for STATCOMs

STATCOMs improve the power factor and the power quality by providing the compensation current for the power grid. To accomplish this goal, the grid voltages are sensed and synchronized in generating the compensation current of the STATCOMs.

Figure 1 shows a five-level DCMC-based STATCOM configuration. The MV grid is represented by a three-phase voltage source and a three-phase load with the proposed five-level STATCOM connected in the PCC. However, if needed, the STATCOM can also be connected through the step-up transformer to high voltage transmission systems. The proposed five-level STATCOM system is comprised of three main parts: a five-level DCMC, a set of coupling inductors or a step-up transformer, and a STATCOM controller. First, the five-level DCMC has four dc-link capacitors (C_1-C_4) to produce a five-level output phase voltage (V_{AN}). In each phase leg, there are four complementary main switches (S_{A1}-S_{A4} and $S_{A'1}$-$S_{A'4}$ for the phase-A leg, S_{B1}-S_{B4} and $S_{B'1}$-$S_{B'4}$, and etc.). The voltage stress of each main switch is limited to one dc-link capacitor voltage ($V_{DC}/4$) thanks to the clamping diodes. Second, the main purpose of the coupling inductors is to filter out the harmonic components of the injected reactive current, which are generated by the pulsating output voltage of the five-level DCMC. Third, the STATCOM controller performs reactive power compensation by controlling the gate signals of the main switches, based on the measured grid phase voltages, grid phase currents, and dc-link capacitor voltages.

The proposed control method of the five-level DCMC-based STATCOM is based on injecting the compensation current into the power grid using the OCC controller. To derive the multi-carrier level-shifted OCC control equation of the five-level DCMC-based STATCOM, the main principle of the OCC method for a two-level voltage source converter (VSC) is reviewed first. For the three-phase two-level VSC, the relationship between the duty ratios of the VSC switches and the grid phase voltages can be defined as follows [25]:

$$\begin{bmatrix} -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} \begin{bmatrix} d_{SA'} \\ d_{SB'} \\ d_{SC'} \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{1}$$

where $d_{SA'}$, $d_{SB'}$, $d_{SC'}$ are the duty ratios of the bottom switches ($S_{A'}$, $S_{B'}$, $S_{C'}$) in the two-level VSC and V_{DC} is the dc bus voltage, and V_A, V_B, V_C are the grid phase voltages.

One possible solution for (1), containing singular matrix and thus having no unique solution can be defined as follows:

$$\begin{bmatrix} d_{SA'} \\ d_{SB'} \\ d_{SC'} \end{bmatrix} = K_1 + \frac{K_2}{V_{DC}} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{2}$$

Assume $K_2 = -1$, then from $0 \leq d \leq 1$, K_1 can be defined as:

$$\frac{V_A}{V_{DC}} \leq K_1 \leq 1 + \frac{V_A}{V_{DC}} \tag{3}$$

where V_A/V_{DC} is a modulation index and for the three-phase VSC with sinusoidal PWM, its maximum value is equal to $1/\sqrt{3}$. Thus, based on the defined K_1 and K_2, (2) can be rewritten by:

$$\begin{bmatrix} d_{SA'} \\ d_{SB'} \\ d_{SC'} \end{bmatrix} = \frac{1}{\sqrt{3}} - \frac{1}{V_{DC}} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{4}$$

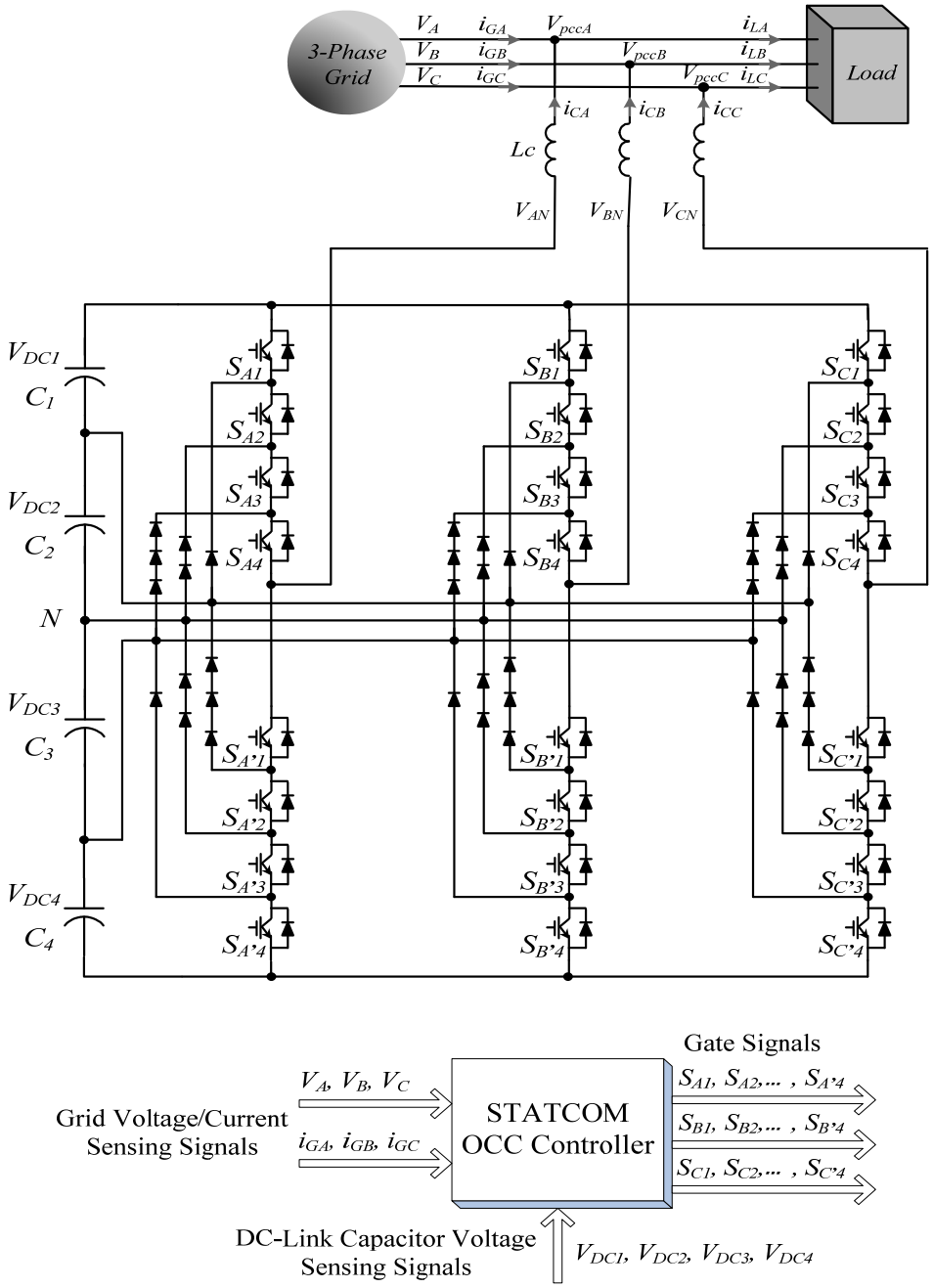


Figure 1. Five-level DCMC-based STATCOM with coupling inductors.

The control goal of the reactive compensation for the STATCOM is to realize the following relationship between the grid phase voltages and the grid phase currents to achieve power factor correction (PFC) operation for the power grid by the reactive currents of the STATCOM:

$$\begin{bmatrix} i_{GA}+i^*_{CA} \\ i_{GB}+i^*_{CB} \\ i_{GC}+i^*_{CC} \end{bmatrix} = \frac{1}{R_E}\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (5)$$

where R_E is the emulated resistance, V_A, V_B, V_C are the grid phase voltages and i_{GA}, i_{GB}, i_{GC} are the grid phase currents, and i^*_{CA}~i^*_{CC} are the STATCOM current references which can be defined as follows:

$$\begin{bmatrix} i^*_{CA} \\ i^*_{CB} \\ i^*_{CC} \end{bmatrix} = jG_R \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \left(K_P + \frac{K_I}{s}\right) \begin{bmatrix} \Delta V_{pccA} \\ \Delta V_{pccB} \\ \Delta V_{pccC} \end{bmatrix} \quad (6)$$

where G_R is the reference conductance related to the voltage fluctuation at the point of the STATCOM connection, K_P and K_I are the proportional and integral coefficients related to the grid impedances, and ΔV_{pccA}, ΔV_{pccB}, ΔV_{pccC} are the voltage variations at the PCC.

Combining (4) and (5) yields the control key equation of the three-phase two-level STATCOM, of which the reactive compensation strategy can be achieved by controlling the VSC switches in such a way that the duty ratios, the grid phase currents, and the compensation currents satisfy the following equation:

$$\begin{bmatrix} R_S \cdot i_{GA} + V_{ICAref} \\ R_S \cdot i_{GB} + V_{ICBref} \\ R_S \cdot i_{GC} + V_{ICCref} \end{bmatrix} = V_m \begin{bmatrix} 1 - \sqrt{3}d_{SA'} \\ 1 - \sqrt{3}d_{SB'} \\ 1 - \sqrt{3}d_{SC'} \end{bmatrix} \quad (7)$$

where $V_m = V_{DC}\, R_S / \sqrt{3} R_E$, R_S is the sensing resistance of the grid phase current and i_{GA}, i_{GB}, i_{GC} are the grid phase currents, and $V_{ICjref} = R_S \cdot i^*_{Cj}$ at $j = A, B, C$.

In (7), the emulated resistance (R_E) of the STATCOM system is adjusted by the duty ratios of the bottom switches in the two-level VSC during each switching cycle to keep the dc bus voltage (V_{DC}) at the constant level.

A similar approach is developed for the higher-level DCMC-based STATCOMs with the level-shifted carrier signals. For the five-level DCMC-based STATCOM, four level-shifted carrier signals (V_{car1}-V_{car4}) are arranged so that they fully occupy contiguous bands in the range of ($-V_{DC3} - V_{DC4}$) to ($V_{DC1} + V_{DC2}$). The three-phase sinusoidal control references are then compared with these carrier signals to determine the switched voltage level. The five-level STATCOM is switched to ($V_{DC1} + V_{DC2}$) when the control reference is greater than four carrier signals by switching the first upper switch (S_{A1}, S_{B1}, S_{C1}) and its complementary switch ($S_{A'1}$, $S_{B'1}$, $S_{C'1}$). Then the STATCOM is switched to $+V_{DC2}$ when the control reference is greater than three lower carrier signals (V_{car2}, V_{car3}, V_{car4}) but less than the upper carrier signal (V_{car1}) by switching the second upper switch (S_{A2}, S_{B2}, S_{C2}) and its complementary switch ($S_{A'2}$, $S_{B'2}$, $S_{C'2}$). The STATCOM is switched to zero (N) when the control reference is greater than two lower carrier signals (V_{car3}, V_{car4}) but less than two upper carrier signals (V_{car1}, V_{car2}) by switching the third upper switch (S_{A3}, S_{B3}, S_{C3}) and its complementary switch ($S_{A'3}$, $S_{B'3}$, $S_{C'3}$). Similarly, the STATCOM is switched to $-V_{DC3}$ when the control reference is greater than the lower carrier signal (V_{car4}) but less than three upper carrier signals (V_{car1}, V_{car2}, V_{car3}) by switching the fourth upper switch (S_{A4}, S_{B4}, S_{C4}) and its complementary switch ($S_{A'4}$, $S_{B'4}$, $S_{C'4}$). Finally, the STATCOM is switched to ($-V_{DC3} - V_{DC4}$) when the control reference is less than four carrier signals.

Based on the above five-level carrier-based modulation, the control key equation of the three-phase five-level STATCOM can be represented by the following equations:

$$\begin{aligned} \begin{bmatrix} R_S \cdot i_{GA} + V_{ICAref} \\ R_S \cdot i_{GB} + V_{ICBref} \\ R_S \cdot i_{GC} + V_{ICCref} \end{bmatrix} &= V_{m1} \begin{bmatrix} 1 - \sqrt{3}d_{SA'1} \\ 1 - \sqrt{3}d_{SB'1} \\ 1 - \sqrt{3}d_{SC'1} \end{bmatrix} \\ &= V_{m2} \begin{bmatrix} 1 - \sqrt{3}d_{SA'2} \\ 1 - \sqrt{3}d_{SB'2} \\ 1 - \sqrt{3}d_{SC'2} \end{bmatrix} \\ &= V_{m3} \begin{bmatrix} 1 - \sqrt{3}d_{SA'3} \\ 1 - \sqrt{3}d_{SB'3} \\ 1 - \sqrt{3}d_{SC'3} \end{bmatrix} \\ &= V_{m4} \begin{bmatrix} 1 - \sqrt{3}d_{SA'4} \\ 1 - \sqrt{3}d_{SB'4} \\ 1 - \sqrt{3}d_{SC'4} \end{bmatrix} \end{aligned} \quad (8)$$

where V_{m1}-V_{m4} are the carrier amplitudes of four level-shifted carrier signals, depending on each dc-link capacitor voltage (V_{DC1}-V_{DC4}), R_S is the sensing resistance of the grid phase current and i_{GA}, i_{GB}, i_{GC} are the grid phase currents, and $V_{ICjref} = R_S \cdot i^*_{Cj}$ at $j = A$, B, C.

For the three-phase five-level DCMC-based STATCOM, the OCC control equation can be expressed as follows:

$$\begin{bmatrix} R_S \cdot i_{GA} + V_{ICAref} \\ R_S \cdot i_{GB} + V_{ICBref} \\ R_S \cdot i_{GC} + V_{ICCref} \end{bmatrix} = V_{mj} \begin{bmatrix} 1 - \sqrt{3} d_{SA'j} \\ 1 - \sqrt{3} d_{SB'j} \\ 1 - \sqrt{3} d_{SC'j} \end{bmatrix} \quad (9)$$

where j = 1,2,3,4 and $V_{mj} = V_{DCj}\, R_S / \sqrt{3} R_E$, and $d_{SA'j}$, $d_{SB'j}$, $d_{SC'j}$ are the duty ratios of the bottom switches in the three-phase five-level DCMC-based STATCOM.

Figure 2 shows the proposed level-shifted OCC control of the five-level DCMC-based STATCOM, based on (9). The three sinusoidal control references are compared with four level-shifted carrier signals (V_{car1}-V_{car4}) to determine the output voltage levels for each phase: (V_{DC1} + V_{DC2}), +V_{DC2}, 0, −V_{DC3}, (−V_{DC3} − V_{DC4}). The eight main switches per phase are controlled as complementary pairs (S_{A1}, $S_{A'1}$, etc.). As shown in Figure 2, the first upper carrier signal V_{car1} has V_{m1} amplitude and determines the switching status of the first upper switch (S_{A1}, S_{B1}, S_{C1}) and its complementary switch ($S_{A'1}$, $S_{B'1}$, $S_{C'1}$). Similarly, the second upper carrier signal V_{car2} has V_{m2} amplitude and decides the switching status of the second upper switch (S_{A2}, S_{B2}, S_{C2}) and its complementary switch ($S_{A'2}$, $S_{B'2}$, $S_{C'2}$). For the other two carrier signals (V_{car3}, V_{car4}), the same control approach is applied to determine the switching condition of the related main switches.

For the sinusoidal control reference of Phase-A, the line period is divided into four operation regions, according to where the control reference signal lands, named as I, II, III, and IV.

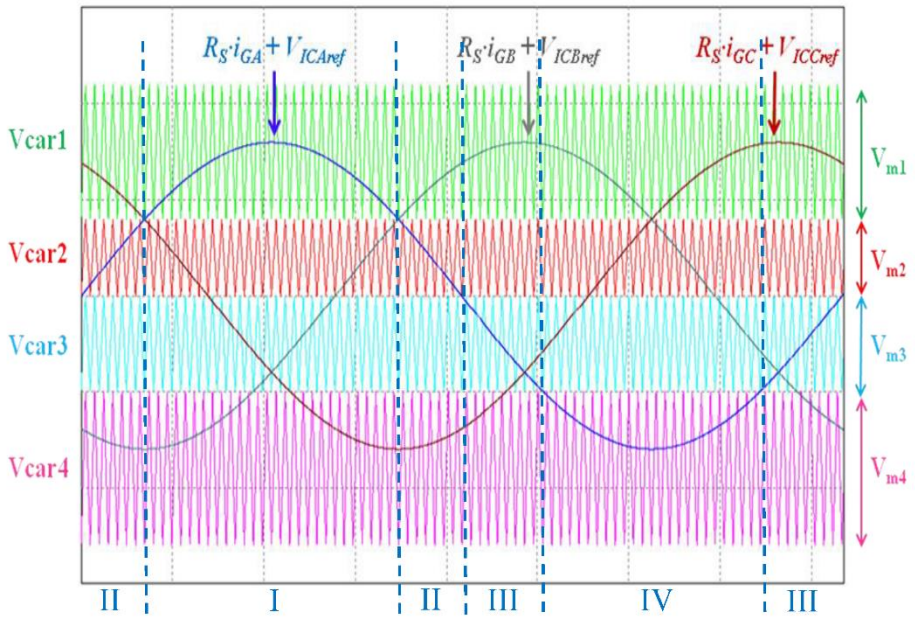


Figure 2. Proposed multi-carrier level-shifted OCC control with variable carrier-amplitude.

Table 1 shows the five-level STATCOM output voltages (V_{AN}) and their switching states of Phase A. In region I in Figure 2, the STATCOM output voltage is switched between V_{DC1} + V_{DC2} and V_{DC2} by the first upper switch S_{A1} and its complementary switch $S_{A'1}$. In addition, the other upper switches (S_{A2}-S_{A4}) are kept on in region I. Similarly, in region II, the second upper switch S_{A2} and its complementary switch $S_{A'2}$ are switched to provide the STATCOM output voltage between V_{DC2} and 0. In this region, the first upper switch S_{A1} is

turned off, and the other two upper switches (S_{A3}, S_{A4}) are always turned on to provide the neutral point connection (0 or N) in Figure 1. For region III and IV, the same switching approach is applied to produce the negative STATCOM output voltages. From Section 2, the control key equations of the five-level DCMC-based STATCOM for four operation regions of Phase A can be derived in Table 2.

Table 1. Switching states and STATCOM output voltages of phase A.

	S_{A1}	S_{A2}	S_{A3}	S_{A4}	$S_{A'1}$	$S_{A'2}$	$S_{A'3}$	$S_{A'4}$	V_{AN}	
									PWM-ON	**PWM-OFF**
I	PWM	ON	ON	ON	$\overline{\text{PWM}}$	OFF	OFF	OFF	$+V_{DC1} + V_{DC2}$	$+V_{DC2}$
II	OFF	PWM	ON	ON	ON	$\overline{\text{PWM}}$	OFF	OFF	$+V_{DC2}$	0
III	OFF	OFF	PWM	ON	ON	ON	$\overline{\text{PWM}}$	OFF	0	$-V_{DC3}$
IV	OFF	OFF	OFF	PWM	ON	ON	ON	$\overline{\text{PWM}}$	$-V_{DC3}$	$-V_{DC3} - V_{DC4}$

Table 2. Control key equations for four operation regions of phase A.

	Switching State I	**Switching State II**	**Switching State III**	**Switching State IV**
Control Key Equations	$R_S \cdot i_{GA} + V_{ICAref} = V_{m2} + V_{m1} \cdot d_{SA1}$	$R_S \cdot i_{GA} + V_{ICAref} = V_{m2} \cdot d_{SA2}$	$R_S \cdot i_{GA} + V_{ICAref} = -V_{m3} + V_{m3} \cdot d_{SA3}$	$R_S \cdot i_{GA} + V_{ICAref} = -(V_{m3} + V_{m4}) + V_{m4} \cdot d_{SA4}$
Region Selections	$V_{m2} \leqq R_S \cdot i_{GA} + V_{ICAref} \leqq (V_{m1} + V_{m2})$	$0 \leqq R_S \cdot i_{GA} + V_{ICAref} < V_{m2}$	$-V_{m3} \leqq R_S \cdot i_{GA} + V_{ICAref} < 0$	$-(V_{m3} + V_{m4}) \leqq R_S \cdot i_{GA} + V_{ICAref} < -V_{m3}$
	Region I	**Region II**	**Region III**	**Region IV**

3. OCC Controller for DCMC-Based STATCOMs

The proposed OCC controller for the five-level DCMC-based STATCOM is shown in Figure 3. The four-carrier level-shifted OCC controller is realized using a clock signal (CLK), four integrators, four comparators, four RS flip-flops, and four reset switches for PWM generation. The four-channel voltage compensators and the level-shifted carrier generators produce four carrier ramps and four level-shifted carrier signals. In detail, the four identical voltage compensators (G_{DC1}-G_{DC4}) determine four carrier amplitudes (V_{m1}-V_{m4}) depending on deviation of each dc-link capacitor voltage (V_{DC1}-V_{DC4}) from the reference voltage V^*_{DC} (=$V_{DC}/4$). To compensate the dc-link capacitor voltage variations, the equivalent STATCOM resistance (R_E) is adjusted by each carrier amplitude (V_{m1}-V_{m4}) in (9).

The transfer function of the four identical voltage compensators $G_{DCi}(s)$ can be obtained as follows [26]:

$$G_{DCi}(s) = \frac{\Delta V_{mi}}{\Delta V_{DCi}} = K_{mi} \cdot \frac{\left(1 + \frac{s}{\omega_{zmi}}\right)}{s \cdot \left(1 + \frac{s}{\omega_{pmi}}\right)} \tag{10}$$

where K_{mi} is the proportional coefficient, ω_{zmi} is the zero far below the zero crossover frequency, and ω_{pmi} is the pole located right at the zero crossover frequency.

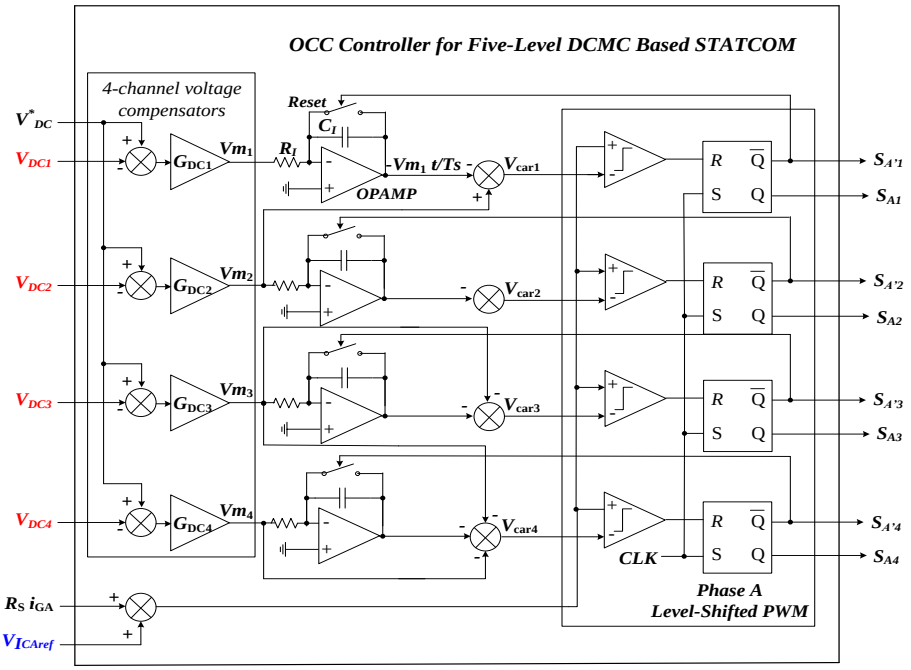


Figure 3. OCC control circuit of the five-level DCMC-based STATCOM for Phase A.

Using the four integrators with reset and three adders, the four level-shifted carrier signals (V_{car1}-V_{car4}) are generated with the different amplitudes and dc-level shifts. The proposed level-shifted carrier signals can be respectively represented as follows:

$$V_{car1}(t) = \frac{V_{m1}}{T_S} \cdot t + V_{m2} \tag{11}$$

$$V_{car2}(t) = \frac{V_{m2}}{T_S} \cdot t \tag{12}$$

$$V_{car3}(t) = \frac{V_{m3}}{T_S} \cdot t - V_{m3} \tag{13}$$

$$V_{car4}(t) = \frac{V_{m4}}{T_S} \cdot t - (V_{m3} + V_{m4}) \tag{14}$$

where $0 < t \leq T_S$, T_S is the period of the carrier signals, and V_{m1}-V_{m4} are the amplitudes of the four carrier signals.

The maximum amplitude of the four carrier signals can be decided by the supply voltage or the maximum differential input voltage of the comparators. Since the maximum input voltage of the (−) input terminal (V_{car1}) of the first upper comparator in Figure 3 is (V_{m1} + V_{m2}), one-quarter of the supply voltage can be selected for the maximum amplitude of the four carrier signals. For example, if the supply voltage of the comparators is ±15 V~±18 V, the maximum amplitude of the four carrier signals is 3.75 V~4.5 V. The minimum amplitude of the four carrier signals can be the minimum output voltage of the op-amps in the OCC controller or zero. When the amplitude of the carrier signal reaches its minimum value, the voltage control of the related dc-link capacitor by the carrier signal is somewhat limited during minimum value operation cycles but the total dc-link capacitor voltage balancing would be continuously handled by the other carrier signals and dc-link capacitors.

The resulting level-shifted carrier signals (V_{car1}-V_{car4}) with variable amplitudes and dc-level shifts are shown in Figure 2. When the four dc-link capacitor voltages (V_{DC1}-V_{DC4}) are out of balance due to any reason or there are dynamic load changes, the four-channel voltage compensators continuously adjust the amplitudes of the four carrier signals (V_{m1}-V_{m4})

to stabilize each dc-link capacitor voltage based on the reference voltage ($V_{DC}/4$). In addition, OCC double-edge modulation can be also used in the proposed OCC controller for the DCMC-based STATCOM to provide high-quality output voltage with reduced harmonics.

With the proposed variable amplitude control of the carrier signals, each dc-link capacitor voltage can be properly balanced and equal to the reference voltage even under different dc-link capacitances (C_1-C_4). The actual duty ratios of the main switches for the phase-A leg (S_{A1}-$S_{A'4}$) are achieved by comparing the control reference ($R_S \cdot i_{GA} + V_{ICAref}$) with the four level-shifted carrier signals in the level-shifted PWM block. When the amplitude of the carrier signals reaches its maximum value, the voltage control capability of the related dc-link capacitors is limited, including overmodulation condition.

The control system of the five-level DCMC-based STATCOM is shown in Figure 4. The proposed level-shifted OCC controller produces the control references for the current control loop and generates the gate signals for the five-level STATCOM. In addition, the voltage control loop generates the STATCOM current references for the reactive compensation which is implemented with proportional and integral (PI) control algorithm. For voltage regulation in the power system, the reactive power compensation is realized by controlling the injected or absorbed reactive current of the five-level STATCOM.

Assuming that there is a voltage sag ($+\Delta V_{pccA}$) in Phase A, the five-level STATCOM tries to regulate the grid voltage and make it come back to normal. From the multilevel OCC control Equation (9) of the five-level STATCOM, the following control equations can be derived to compensate the voltage sag and regulate the grid voltage within the standard.

In region I of Figure 2, since the STATCOM output voltage is only switched between $V_{DC1} + V_{DC2}$ and V_{DC2} by the first upper switch S_{A1} and the other upper switches (S_{A2}-S_{A4}) are kept on from Table 1, the voltage regulation is only controlled by the first upper switch S_{A1} in region I as follows:

$$\begin{aligned} R_S \cdot i_{GA} + \left(K_P + \tfrac{K_I}{s}\right)\left(V_{Aref} - V_A\right) &= R_S \cdot i_{GA} + \left(K_P + \tfrac{K_I}{s}\right)\left(+\Delta V_{pccA}\right) \\ &= V_{m1}\left(1 - \sqrt{3} d_{SA'1}\right) \end{aligned} \tag{15}$$

From above, the duty ratios of the first upper switch S_{A1} (d_{SA1}) and its complementary switch $S_{A'1}$ ($d_{SA'1}$) can be derived as follows:

$$d_{SA'1} = \frac{1}{\sqrt{3}} - \frac{1}{\sqrt{3} V_{m1}}\left[R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)\left(+\Delta V_{pccA}\right)\right] \tag{16}$$

$$d_{SA1} = 1 - d_{SA'1} = \left(1 - \frac{1}{\sqrt{3}}\right) + \frac{1}{\sqrt{3} V_{m1}}\left[R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)\left(+\Delta V_{pccA}\right)\right] \tag{17}$$

From (17), it is clear that the duty ratio of the first upper switch S_{A1} (d_{SA1}) increases by the voltage sag ($+\Delta V_{pccA}$) in Phase A and the STATCOM output voltage (V_{AN}) can be increased by the duty ratio (d_{SA1}) to inject the reactive power into the power grid for the voltage regulation.

In region II, since the second upper switch S_{A2} and its complementary switch $S_{A'2}$ are only switched to provide the STATCOM output voltage between V_{DC2} and 0 as shown in Table 1, the voltage regulation is achieved by the second upper switch S_{A2} in region II as follows:

$$\begin{aligned} R_S \cdot i_{GA} + \left(K_P + \tfrac{K_I}{s}\right)\left(V_{Aref} - V_A\right) &= R_S \cdot i_{GA} + \left(K_P + \tfrac{K_I}{s}\right)\left(+\Delta V_{pccA}\right) \\ &= V_{m2}\left(1 - \sqrt{3} d_{SA'2}\right) \end{aligned} \tag{18}$$

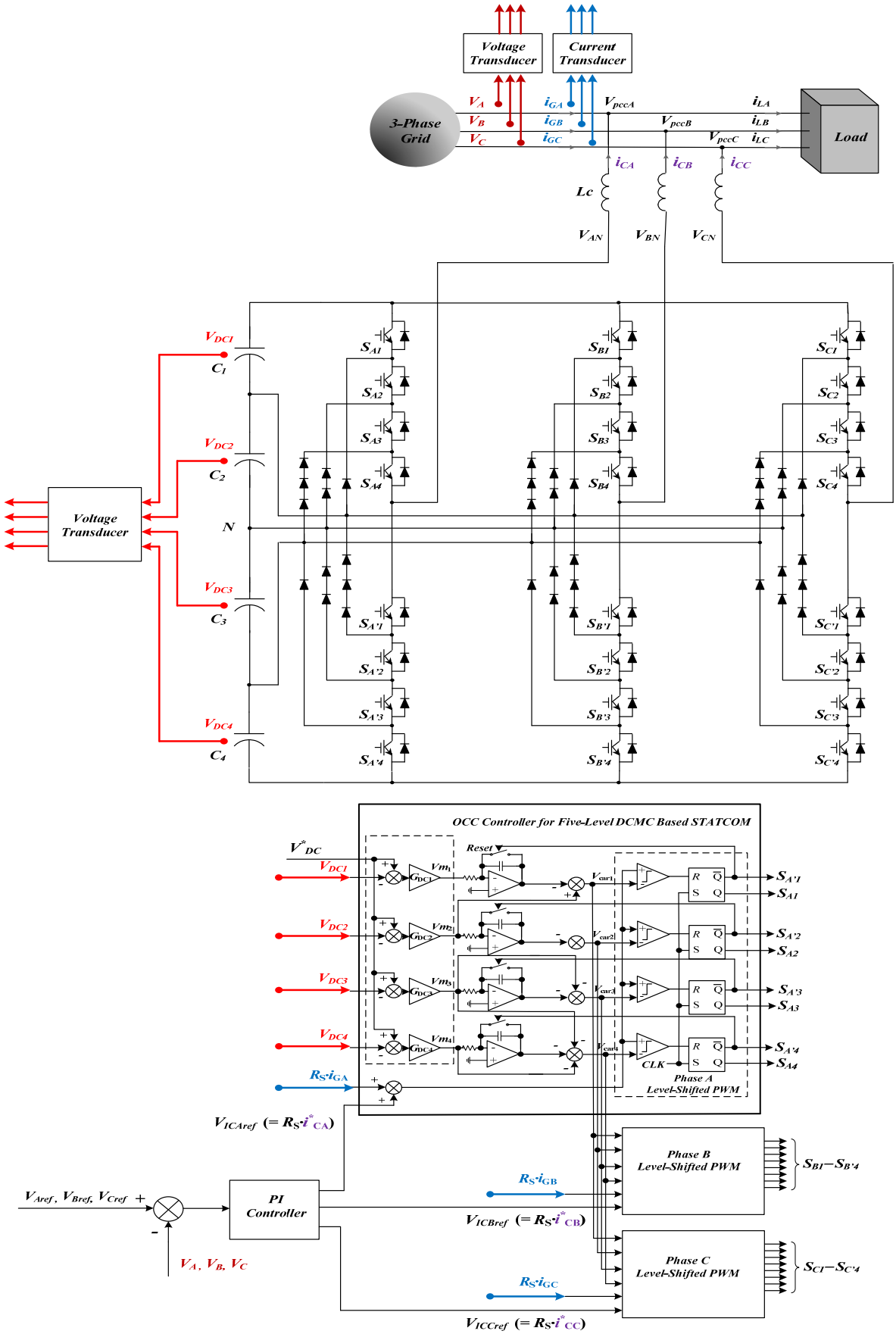


Figure 4. Control diagram of the five-level DCMC-based STATCOM.

Similarly, the duty ratios of the second upper switch S_{A2} (d_{SA2}) and its complementary switch $S_{A'2}$ ($d_{SA'2}$) can be expressed as follows:

$$d_{SA'2} = \frac{1}{\sqrt{3}} - \frac{1}{\sqrt{3}V_{m2}}\left[R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)(+\Delta V_{pccA})\right] \tag{19}$$

$$d_{SA2} = 1 - d_{SA'2} = \left(1 - \frac{1}{\sqrt{3}}\right) + \frac{1}{\sqrt{3}V_{m2}}\left[R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)(+\Delta V_{pccA})\right] \tag{20}$$

From (20), it is also clear that the duty ratio of the second upper switch S_{A2} (d_{SA2}) increases by the voltage sag ($+\Delta V_{pccA}$) in Phase A and the STATCOM output voltage (V_{AN}) can be also increased by the duty ratio (d_{SA2}) to inject the reactive power for the voltage regulation in region II.

In addition, the voltage regulation of the proposed STATCOM in region II can be also explained by Table 2. In region II, the control key equation of the STATCOM is given by:

$$R_S \cdot i_{GA} + V_{ICAref} = R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)(+\Delta V_{pccA}) = V_{m2} \cdot d_{SA2} \tag{21}$$

From above, the duty ratio of the second upper switch S_{A2} (d_{SA2}) can be expressed as follows:

$$d_{SA2} = \frac{1}{V_{m2}}\left[R_S \cdot i_{GA} + \left(K_P + \frac{K_I}{s}\right)(+\Delta V_{pccA})\right] \tag{22}$$

From (22), when there is the voltage sag ($+\Delta V_{pccA}$) in Phase A, the STATCOM output voltage (V_{AN}) can be increased by the duty ratio (d_{SA2}) to inject the reactive power into the power grid for the voltage regulation in region II.

For the diode-clamped multilevel converters, a major challenge is to keep all dc-link capacitor voltages balanced, which was achieved with an extra voltage-balancing circuitry or a specific voltage-balancing control previously. For example, a modified SPWM method was proposed in [17] in order to balance the two dc-link capacitor voltages for the three-level diode-clamped inverters. It is based on changing the boundary offset on the middle point of two carrier signals, which can control the neutral-point current to ensure balanced dc-link capacitor voltages. However, the main drawback in this approach is the restricted stability in order to obtain a simple control strategy.

Figure 5 shows the proposed four-carrier level-shifted OCC control algorithm of the proposed five-level STATCOM to maintain the dc-link capacitor voltage balance in region I and II.

For the detailed analysis of the dc-link capacitor voltage balance, the two dc-link capacitor currents (i_{C1}, i_{C2}) in region I can be described by the following expressions:

$$i_{C1} = C_1\frac{dV_{DC1}}{dt} = i_{CHA1} - i_{DIS1}$$

$$i_{C2} = C_2\frac{dV_{DC2}}{dt} = i_{C1} + i_{CHA2} - i_{DIS2} \tag{23}$$

Similarly, the two dc-link capacitor currents in region II can be expressed as:

$$i_{C1} = C_1\frac{dV_{DC1}}{dt} = -i_{DIS1}$$

$$i_{C2} = C_2\frac{dV_{DC2}}{dt} = i_{C1} + i_{CHA2} - i_{DIS2} \tag{24}$$

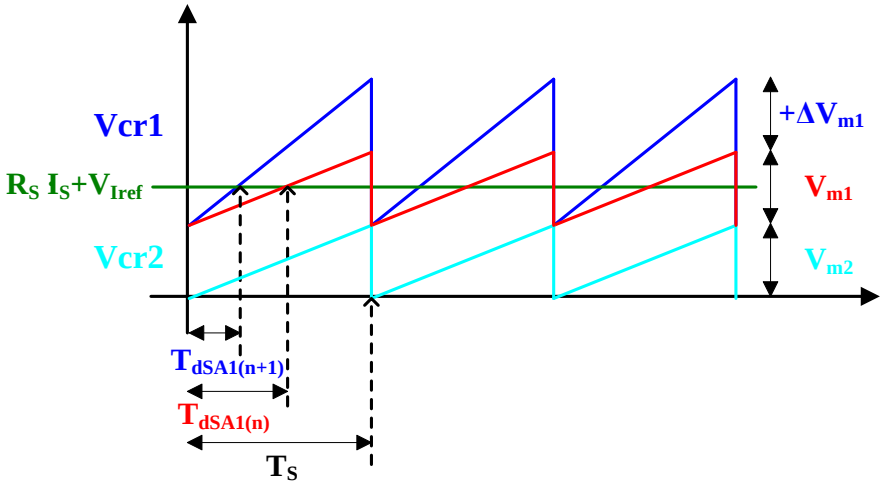
Assuming that the four dc-link capacitors (C_1-C_4) have the same capacitance, when a disturbance causes imbalance in the two upper dc-link capacitor voltages ($V_{DC1} > V^*_{DC} > V_{DC2}$), a state variable ΔV is defined as half the difference between the two upper dc-link capacitor voltages (V_{DC1}, V_{DC2}), which should converge to zero with the proposed OCC control. In

the unbalanced condition, each dc-link capacitor voltage can be defined as a function of the voltage difference ΔV by:

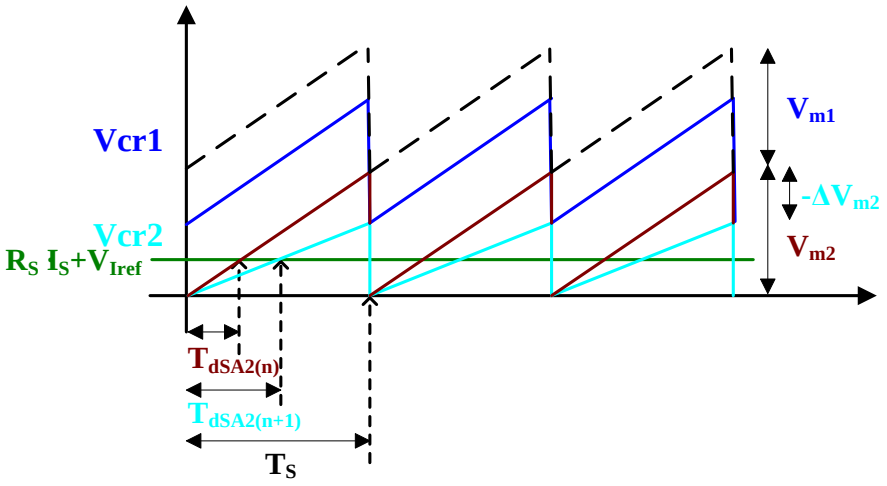
$$V_{DC1} = V_C + \Delta V$$
$$V_{DC2} = V_C - \Delta V \quad (25)$$

where

$$V_C = \frac{V_{DC1} + V_{DC2}}{2}$$
$$\Delta V = \frac{V_{DC1} - V_{DC2}}{2} \quad (26)$$



(**a**)



(**b**)

Figure 5. Proposed four-carrier level-shifted OCC PWM control of the proposed five-level STATCOM in region I and II. (**a**) *Vcr*1 carrier signal modulation when $V_{DC1} > V^*_{DC}$; (**b**) *Vcr*2 carrier signal modulation when $V_{DC2} < V^*_{DC}$.

In order to maintain the dc-link capacitor voltage balance, the proposed control of the five-level STATCOM in region I and II is shown in Figure 5. From Figure 5a, the duty ratios of the S_{A1} switch under an unbalanced dc-link condition can be described as follows:

$$d_{SA1(n)} = \frac{T_{dSA1(n)}}{T_S} = \frac{R_S \cdot i_{GA} + V_{ICAref} - V_{m2}}{V_{m1}}$$

$$d_{SA1(n+1)} = \frac{T_{dSA1(n+1)}}{T_S} = \frac{R_S \cdot i_{GA} + V_{ICAref} - (V_{m2} - \Delta V_{m2})}{V_{m1} + \Delta V_{m1}} \quad (27)$$

where $d_{SA1(n)}$ and $d_{SA1(n+1)}$ are the duty ratios of the S_{A1} switch at the $(n)_{\text{th}}$ and $(n+1)_{\text{th}}$ switching cycles, and

$$V_{m1} = \frac{V_{DC1} \cdot R_S}{\sqrt{3}R_E}$$

$$\Delta V_{m1} = \frac{R_S}{\sqrt{3}R_E} \cdot \Delta V_{DC1} = \frac{R_S}{\sqrt{3}R_E} \cdot \Delta V \quad (28)$$

From (27) and (28), the duty ratio variation of the S_{A1} switch (Δd_{SA1}) to compensate the unbalanced dc-link capacitor voltages can be obtained by:

$$\Delta d_{SA1} = d_{SA1(n+1)} - d_{SA1(n)} = \frac{-\Delta V_{DC1(n)}[R_E(i_{GA}+i^*_{CA})+V_{DC2(n)}]+\Delta V_{DC2(n)} \cdot V_{DC1(n)} - V_{DC1(n)}(V_{DC1(n)}+V_{DC2(n)})}{V_{DC1(n)}(V_{DC1(n)}+\Delta V_{DC1(n)})} \quad (29)$$

Assuming $V_{DC1(n)} >> \Delta V_{DC1(n)}$, the above equation can be simplified as:

$$\Delta d_{SA1} = -\frac{\Delta V_{DC1(n)}}{V^2_{DC1(n)}}[R_E(i_{GA} + i^*_{CA}) + V_{DC2(n)}] + \frac{\Delta V_{DC2(n)}}{V_{DC1(n)}} - \frac{(V_{DC1(n)} + V_{DC2(n)})}{V_{DC1(n)}} \quad (30)$$

From (23) and (30), it is possible to define the relationship between the duty ratio variation of the *Vcr1* carrier signal and the compensation for the dc-link capacitor voltage unbalance. The voltage variations of the two upper dc-link capacitors (C_1, C_2) in region I are given by:

$$\Delta V_{DC1(n+1)} = -\frac{T_S}{C_1 \cdot V^2_{DC1(n)}}[R_E(i_{GA} + i^*_{CA}) + V_{DC2(n)}](i_{GA} + i^*_{CA}) \cdot \Delta V_{DC1(n)} + \frac{T_S}{C_1 \cdot V_{DC1(n)}}(i_{GA} + i^*_{CA}) \cdot \Delta V_{DC2(n)}$$
$$-\frac{T_S}{C_1 \cdot V_{DC1(n)}}(V_{DC1(n)} + V_{DC2(n)})(i_{GA} + i^*_{CA}) - \frac{T_S}{C_1} \cdot \Delta I_{DIS1} = A_1 \cdot \Delta V_{DC1(n)} + A_2 \cdot \Delta V_{DC2(n)} + A_{C1} + A_{C2}$$

$$\Delta V_{DC2(n+1)} = \frac{T_S}{C_2}(-\Delta I_{DIS1} - \Delta I_{DIS2}) = B_{C1} + B_{C2} \quad (31)$$

When $V_{DC1} > V^*_{DC} > V_{DC2}$, Δd_{SA1} is negative and ΔI_{DIS1} is positive in region I. Therefore, the over-charged C_1 capacitor voltage (V_{DC1}) will decrease and the under-charged or over-discharged C_2 capacitor voltage (V_{DC2}) will increase to reduce the dc-link capacitor voltage deviation, depending on the difference between ΔI_{DIS1} and ΔI_{DIS2}. In this unbalanced condition, ΔV_{DC1} is decreasing during each switching cycle to reach the nominal dc-link capacitor voltage.

Since $\Delta V_{DC1(n)} - \Delta V_{DC1(n+1)} = (1 - A_1) \cdot \Delta V_{DC1(n)} - A_2 \cdot \Delta V_{DC2(n)} - A_{C1} - A_{C2} > 0$, the following compensation control is obtained:

$$\frac{\Delta V_{DC1(n+1)}}{\Delta V_{DC1(n)}} < 1 \quad (32)$$

In this unbalanced condition, ΔV_{DC1} is decreasing during each switching cycle to reach the nominal dc-link capacitor voltage. From Figure 5b, similarly, the duty ratios of the S_{A2} switch under an unbalanced dc-link condition can be described as follows:

$$d_{SA2(n)} = \frac{T_{dSA2(n)}}{T_S} = \frac{R_S \cdot i_{GA} + V_{ICAref}}{V_{m2}}$$
$$d_{SA2(n+1)} = \frac{T_{dSA2(n+1)}}{T_S} = \frac{R_S \cdot i_{GA} + V_{ICAref}}{V_{m2} - \Delta V_{m2}} \quad (33)$$

where $d_{SA2(n)}$ and $d_{SA2(n+1)}$ are the duty ratios of the S_{A2} switch at the $(n)_{\text{th}}$ and $(n+1)_{\text{th}}$ switching cycles, and

$$V_{m2} = \frac{V_{DC2} \cdot R_S}{\sqrt{3}R_E}$$
$$\Delta V_{m2} = \frac{R_S}{\sqrt{3}R_E} \cdot \Delta V_{DC2} = \frac{R_S}{\sqrt{3}R_E} \cdot \Delta V \quad (34)$$

From (33) and (34), the duty ratio variation of the S_{A2} switch (Δd_{SA2}) to adjust the unbalanced dc-link capacitor voltages can be obtained by:

$$\Delta d_{SA2} = d_{SA2(n+1)} - d_{SA2(n)} = \frac{\Delta V_{DC2(n)} \cdot R_E(i_{GA} + i^*_{CA})}{V_{DC2(n)}(V_{DC2(n)} - \Delta V_{DC2(n)})} \quad (35)$$

Assuming $V_{DC2(n)} >> \Delta V_{DC2(n)}$, the duty ratio variation of the S_{A2} switch can be simplified as:

$$\Delta d_{SA2} = d_{SA2(n+1)} - d_{SA2(n)} = \frac{\Delta V_{DC2(n)}}{V^2_{DC2(n)}} R_E(i_{GA} + i^*_{CA}) \quad (36)$$

From (24) and (36), the voltage variations of the two upper dc-link capacitors (C_1, C_2) in region II are given by:

$$\Delta V_{DC1(n+1)} = \frac{T_S}{C_1}(-\Delta I_{DIS1}) = A_{C2}$$

$$\Delta V_{DC2(n+1)} = \frac{T_S}{C_2 \cdot V^2_{DC2(n)}} R_E(i_{GA} + i^*_{CA})^2 \cdot \Delta V_{DC2(n)} - \frac{T_S}{C_2}(\Delta I_{DIS1} + \Delta I_{DIS2}) = B_2 \cdot \Delta V_{DC2(n)} + B_{C1} + B_{C2} \quad (37)$$

When $V_{DC1} > V^*_{DC} > V_{DC2}$, Δd_{SA2} is positive and ΔI_{DIS1} is also positive in region II, the over-charged C_1 capacitor voltage (V_{DC1}) will decrease and the under-charged C_2 capacitor voltage (V_{DC2}) will increase to eliminate the dc-link capacitor voltage deviation.

Finally, the voltage variations of the four dc-link capacitors (C_1-C_4) can be described as follows:

$$\begin{bmatrix} \Delta V_{DC1(n+1)} \\ \Delta V_{DC2(n+1)} \\ \Delta V_{DC3(n+1)} \\ \Delta V_{DC4(n+1)} \end{bmatrix} = \begin{bmatrix} -\frac{T_S}{C_1 \cdot V^2_{DC1(n)}}[R_E(i_{GA} + i^*_{CA}) + V_{DC2(n)}](i_{GA} + i^*_{CA}) & \frac{T_S}{C_1 \cdot V_{DC1(n)}}(i_{GA} + i^*_{CA}) & 0 & 0 \\ 0 & \frac{T_S}{C_2 \cdot V^2_{DC2(n)}} R_E(i_{GA} + i^*_{CA})^2 & 0 & 0 \\ 0 & 0 & \frac{T_S}{C_3 \cdot V^2_{DC3(n)}} R_E(i_{GA} + i^*_{CA})^2 & 0 \\ 0 & 0 & \frac{T_S}{C_4 \cdot V_{DC4(n)}}(i_{GA} + i^*_{CA}) & -\frac{T_S}{C_4 \cdot V^2_{DC4(n)}}[R_E(i_{GA} + i^*_{CA}) + V_{DC3(n)}](i_{GA} + i^*_{CA}) \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC2(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix}$$
$$+ \begin{bmatrix} -\frac{T_S}{C_1 \cdot V_{DC1(n)}}(V_{DC1(n)} + V_{DC2(n)})(i_{GA} + i^*_{CA}) - \frac{T_S}{C_1} \cdot \Delta I_{DIS1} \\ -\frac{T_S}{C_2} \cdot \Delta I_{DIS1} - \frac{T_S}{C_2} \cdot \Delta I_{DIS2} \\ -\frac{T_S}{C_3} \cdot \Delta I_{DIS3} - \frac{T_S}{C_3} \cdot \Delta I_{DIS4} \\ -\frac{T_S}{C_4 \cdot V_{DC4(n)}}(V_{DC3(n)} + V_{DC4(n)})(i_{GA} + i^*_{CA}) - \frac{T_S}{C_4} \cdot \Delta I_{DIS4} \end{bmatrix} = \begin{bmatrix} A_1 & A_2 & 0 & 0 \\ 0 & B_2 & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ 0 & 0 & D_3 & D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC2(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_{C1} + A_{C2} \\ B_{C1} + B_{C2} \\ C_{C1} + C_{C2} \\ D_{C1} + D_{C2} \end{bmatrix} = \begin{bmatrix} A_1 & A_2 & 0 & 0 \\ 0 & B_2 & 0 & 0 \\ 0 & 0 & C_3 & 0 \\ 0 & 0 & D_3 & D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC2(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_C \\ B_C \\ C_C \\ D_C \end{bmatrix} \quad (38)$$

Using (38), the voltage variation vector $\Delta V_{DC}(n)$ can be written by a 4×4 matrix A and the initial voltage variation vector $\Delta V_{DC}(0)$:

$$\Delta V_{DC}(n) = \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC2(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} = A \begin{bmatrix} \Delta V_{DC1(n-1)} \\ \Delta V_{DC2(n-1)} \\ \Delta V_{DC3(n-1)} \\ \Delta V_{DC4(n-1)} \end{bmatrix} + B = A^n \begin{bmatrix} \Delta V_{DC1(0)} \\ \Delta V_{DC2(0)} \\ \Delta V_{DC3(0)} \\ \Delta V_{DC4(0)} \end{bmatrix} + C = A^n \cdot \Delta V_{DC}(0) + C \quad (39)$$

where

$$A^n = \begin{bmatrix} A_1^n & \left(A_1^{n-1} + A_1^{n-2}B_2 + \cdots + A_1B_2^{n-2} + B_2^{n-1}\right)A_2 & 0 & 0 \\ 0 & B_2^n & 0 & 0 \\ 0 & 0 & C_3^n & 0 \\ 0 & 0 & \left(C_3^{n-1} + C_3^{n-2}D_4 + \cdots + C_3D_4^{n-2} + D_4^{n-1}\right)D_3 & D_4^n \end{bmatrix} \quad (40)$$

and $\boldsymbol{C} = \left[\boldsymbol{A}^n + \boldsymbol{A}^{n-1} \cdot \cdots \cdot + \boldsymbol{A} + \boldsymbol{I}\right] \cdot \boldsymbol{B}$

From (38)–(40), it is clear that the voltage variations of the four dc-link capacitors become zero in steady state, even though there are some voltage variations of the dc-link capacitors in the beginning or induced by some perturbation. Based on the proposed four-carrier level-shifted OCC control, dc-link capacitor voltage balance can be successfully achieved. It is also clear that the stabilizing time required to eliminate the dc-link voltage unbalance is proportional to the dc-link capacitance and inversely proportional to the amplitude of the input current. However, the proposed multilevel OCC controller may have limited control capability of the dc-link voltage balance during AC network failures since the low AC voltage over a long period prevents the proposed multilevel OCC controller from switching the first upper switches in region I to control the upper dc-link capacitor (C_1) voltage. During the low AC voltage condition, the proposed multi-carrier level-shifted OCC control loses its controllability of the dc-link voltage balance.

For region III and IV, the same control approach is applied to regulate the grid voltage from the voltage variation at the PCC, for example, the voltage sag (or swell). Finally, it is concluded that the voltage variation (sag or swell) can be automatically compensated by the proposed five-level STATCOM with the multilevel OCC controller for all operation regions.

4. Simulation and Experimental Results

4.1. Simulation Results

The proposed five-level DCMC-based STATCOM with the OCC controller for reactive power compensation has been verified by simulation using MATLAB/Simulink. The simulation circuit model presented in Figure 6 is composed of: a three-phase voltage source (V_A, V_B, V_C), two three-phase RL-loads (R_1L_1, R_2L_2), and the shunt-connected five-level DCMC-based STATCOM with coupling inductors (Lc). IGBTs are used for the main switches of the proposed STATCOM.

The parameters of the simulation circuit are as follows: V_A, V_B, V_C = 4.16 kV/$\sqrt{3}$ (rms), R_1 = 150 Ω, R_2 = 300 Ω, L_1 = 350 mH, and L_2 = 250 mH. The dc bus voltage (V_{DC}) is 8 kV and the reference voltage (V^*_{DC}) of each dc-link capacitor voltage (V_{DC1}-V_{DC4}) is 2 kV. The dc-link capacitors (C_1-C_4) have the different capacitances to emulate the voltage unbalance: C_1 = 1.3 mF, C_2 = 1.1 mF, C_3 = 0.8 mF, and C_4 = 0.9 mF. The grid line frequency is 60 Hz and the carrier frequency is 5 kHz. The grid impedance is considered as 0.001 Ω–0.5 mH. The main parameters of the simulation circuit model are listed in Table 3.

To simulate the dynamic behavior of the proposed STATCOM, at the time moment t_C = 0.25 s, the load change switches S_1 and S_2 are commutated to change the load from the R_1L_1 to the R_2L_2 load.

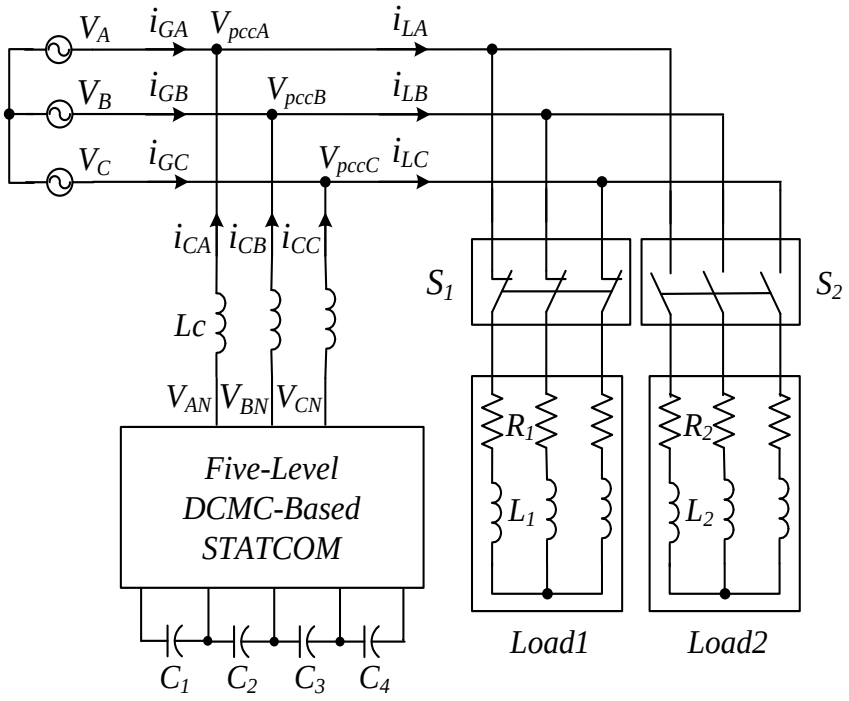


Figure 6. Simulation setup.

Table 3. Parameters of the simulation system.

Parameter	Value
Grid phase voltage (V_A, V_B, V_C)	2.4 kV
DC bus voltage (V_{DC})	8 kV
DC-link capacitor voltage (V_{DC1}-V_{DC4})	2 kV
Coupling inductor (L_C)	10 mH
DC-link capacitor (C_1)	1.3 mF
DC-link capacitor (C_2)	1.1 mF
DC-link capacitor (C_3)	0.8 mF
DC-link capacitor (C_4)	0.9 mF
Three-phase RL-load (R_1L_1)	150 Ω, 350 mH
Three-phase RL-load (R_2L_2)	300 Ω, 250 mH
Carrier frequency	5 kHz
Grid line frequency	60 Hz

Figure 7 shows the simulation waveforms of the STATCOM line-to-line output voltage (Figure 7a) and phase output voltage (Figure 7b). As can be seen, the phase output voltage has five output voltage levels and the voltage step is equal to the reference voltage 2 kV, as the line-to-line voltage has nine output voltage levels with the same voltage step.

Figure 8 shows the four voltage waveforms across the dc-link capacitors with the proposed OCC balancing technique. It is shown that when the load has a step transient, the four dc-link capacitor voltages of the proposed DCMC-based STATCOM are equally balanced in dynamic state even under unequal dc-link capacitances.

Figure 9 shows the four level-shifted carrier signals (V_{car1}-V_{car4}) with variable amplitudes and dc-level shifts determined by V_{m1}-V_{m4} values. Unlike the conventional approaches with multi-carrier level-shifted PWM control, the amplitudes of the four carrier signals (V_{m1}-V_{m4}) in the proposed level-shifted OCC controller vary in such a way to stabilize the dc-link capacitor voltages and provide reactive power compensation in accordance with (9). By comparing the control reference with the four carrier signals, the actual gate signals are produced by the RS flip-flops. With variable amplitude control of the four carrier signals, the dc-link capacitor voltages can become balanced and equal to the reference

voltage ($V_{DC}/4$) even under different dc-link capacitances (C_1-C_4). During dynamic load change, the amplitudes of the four carrier signals become larger first to stabilize the dc-link capacitor voltages since variations of the dc-link capacitor voltages are rapidly increased. Then the amplitudes of the four carrier signals are decreasing to provide smaller reactive power for the light RL-load (R_2L_2). As shown in Figure 9, the proposed level-shifted OCC controller rapidly regulates the five-level STATCOM operating conditions in response to the step change in the reactive loads. However, the minimum amplitude of the carrier signals impacts on the distortion level of the synthesized multilevel waveforms.

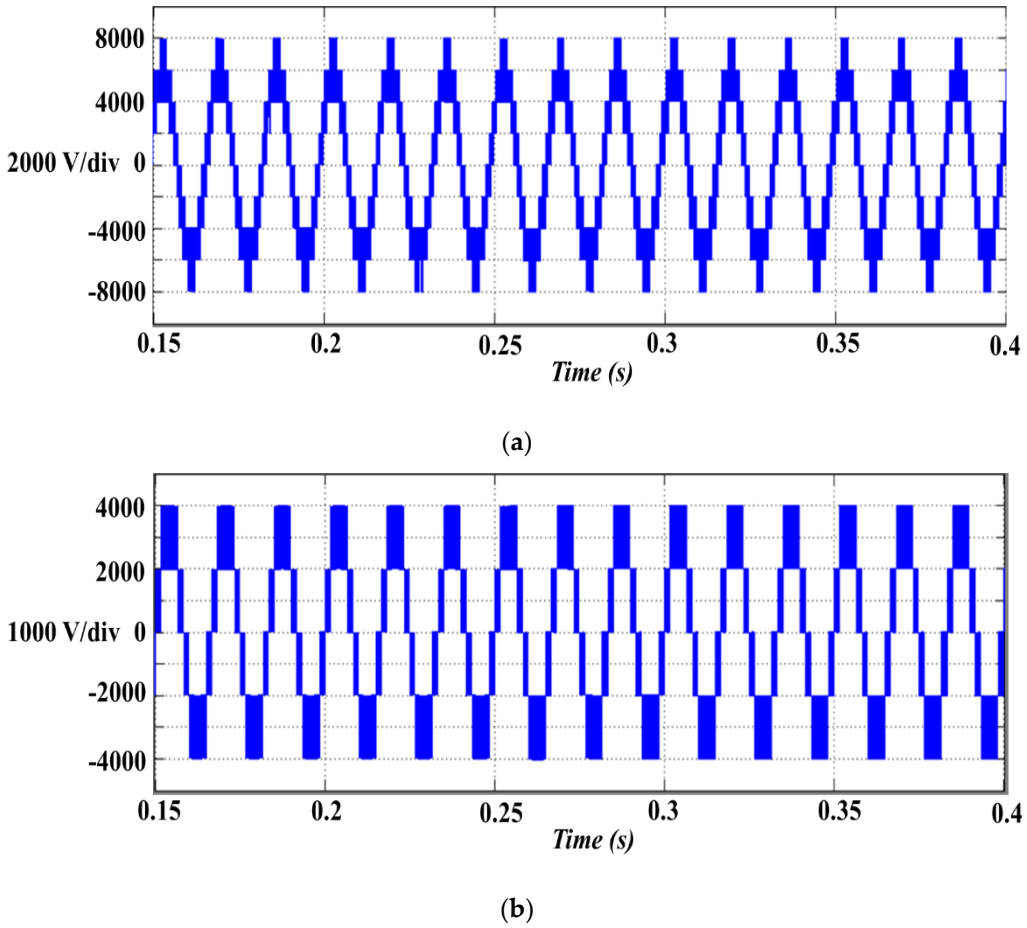


Figure 7. Simulation waveforms of the proposed five-level STATCOM. (**a**) Line-to-line output voltage (V_{AB}); (**b**) Phase output voltage (V_{AN}).

Figure 10 shows the simulation waveforms of the proposed five-level STATCOM with the multilevel OCC control. The grid phase voltage (V_A), the load current (i_{LA}), the STATCOM current (i_{CA}), the grid phase current (i_{GA}), and the two upper dc-link capacitor currents (i_{C1}, i_{C2}) are shown in Figure 10 when the load has a step transient. As shown in Figure 10e,f, the two dc-link capacitor currents (i_{C1}, i_{C2}) have the balanced and proper current direction, following the STATCOM current (i_{CA}). Since the first upper switch S_{A1} is turned off and the second upper switch S_{A2} is switched to provide the STATCOM output voltage between V_{DC2} and 0 in region II of Figure 2, the second upper dc-link capacitor current (i_{C2}) only has the continuous current flow to generate the STATCOM current (i_{CA}) in region II.

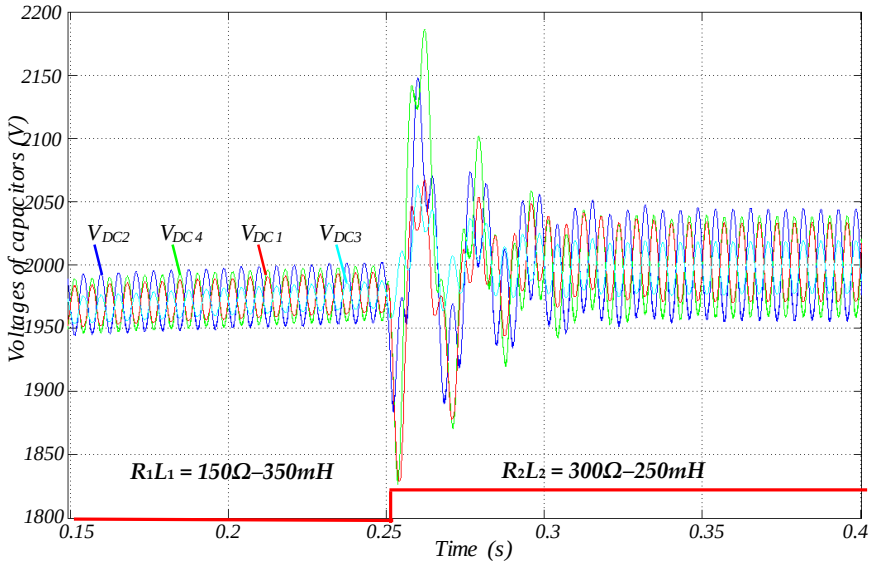


Figure 8. Simulation waveforms of the dc-link capacitor voltages (V_{DC1}-V_{DC4}).

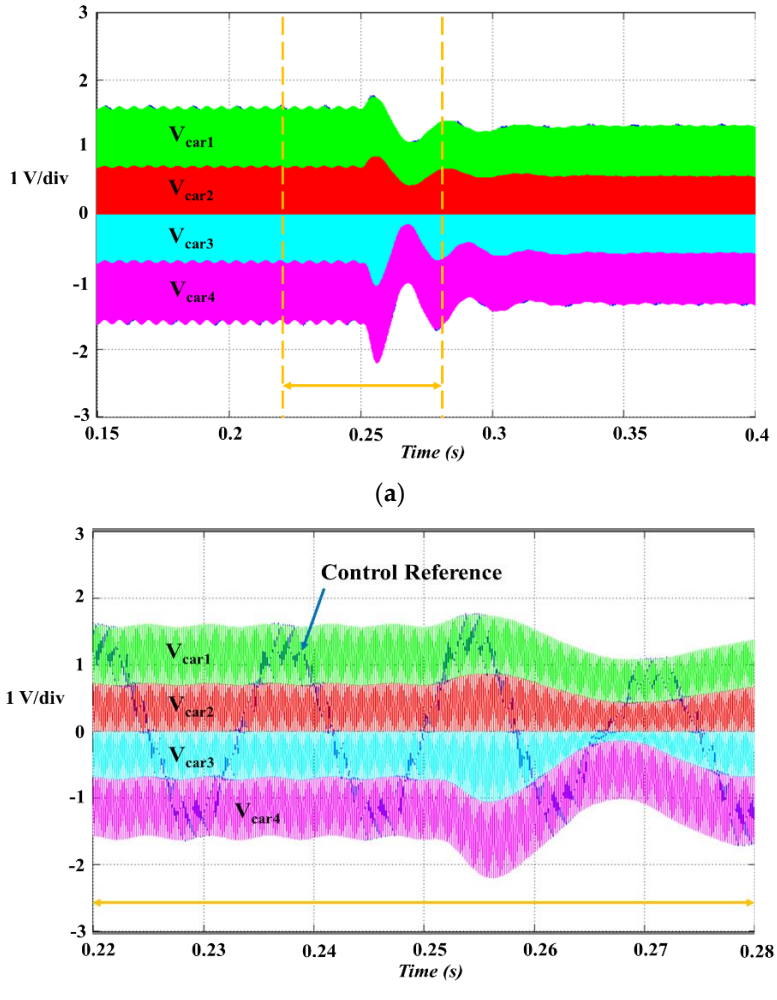


Figure 9. Simulation waveforms of the level-shifted OCC control. (**a**) Four carrier signals (V_{car1}-V_{car4}) and control reference for Phase A; (**b**) Zoomed carrier signals and control reference for Phase A.

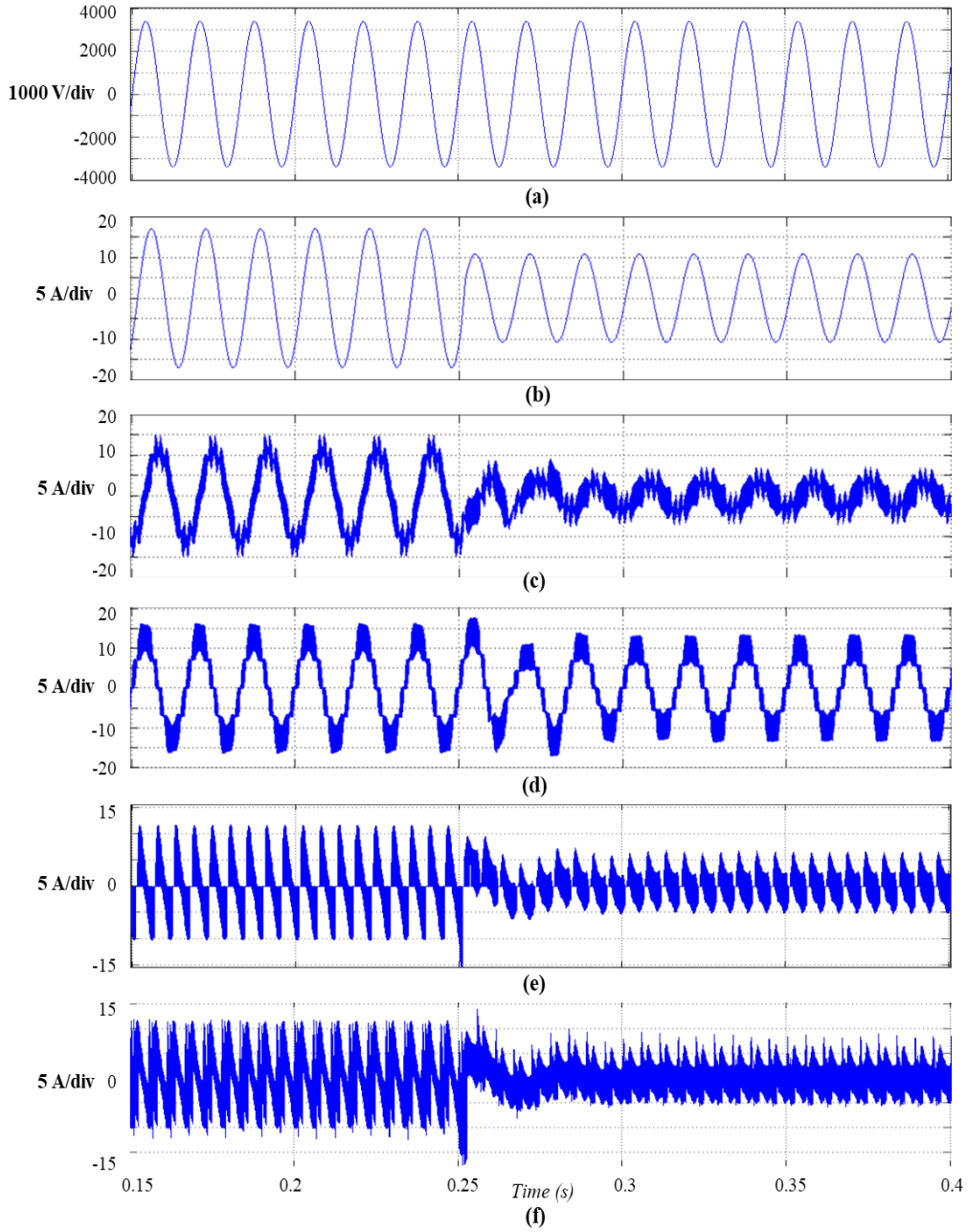


Figure 10. Simulation waveforms of the proposed five-level STATCOM with the multilevel OCC control. (**a**) Grid phase voltage (V_A); (**b**) Load current (i_{LA}); (**c**) STATCOM current (i_{CA}); (**d**) Grid phase current (i_{GA}); (**e**) First upper dc-link capacitor current (i_{C1}); (**f**) Second upper dc-link capacitor current (i_{C2}).

With reactive power compensation by the proposed multilevel OCC STATCOM, the grid phase current is in phase with the grid phase voltage and during dynamic load change, the dc-link capacitor voltages can become balanced with the stabilized dc-link capacitor currents (i_{C1}, i_{C2}) even under different dc-link capacitances (C_1-C_4).

Figure 11 shows the simulation waveforms of the proposed five-level STATCOM with a three-phase diode rectifier load to verify the effectiveness of the proposed multilevel OCC control method under nonlinear load conditions. In Figure 11, the same simulation model and parameters in Table 3 have been used except the three-phase diode rectifier, which is connected to the single-phase RL-load (R_1L_1). As shown in Figure 11, the four dc-link capacitor voltages (V_{DC1}-V_{DC4}) of the proposed DCMC-based STATCOM with unequal dc-link capacitances are stably balanced (2 kV) even under the diode rectifier

load condition, which produces severe harmonic voltage disturbance in the power grid system. When the proposed DCMC-based STATCOM is enabled and connected to the PCC, the highly distorted grid phase current (i_{GA}) with 27.1% total harmonic distortion (THD) becomes sinusoidal with 8.1% THD.

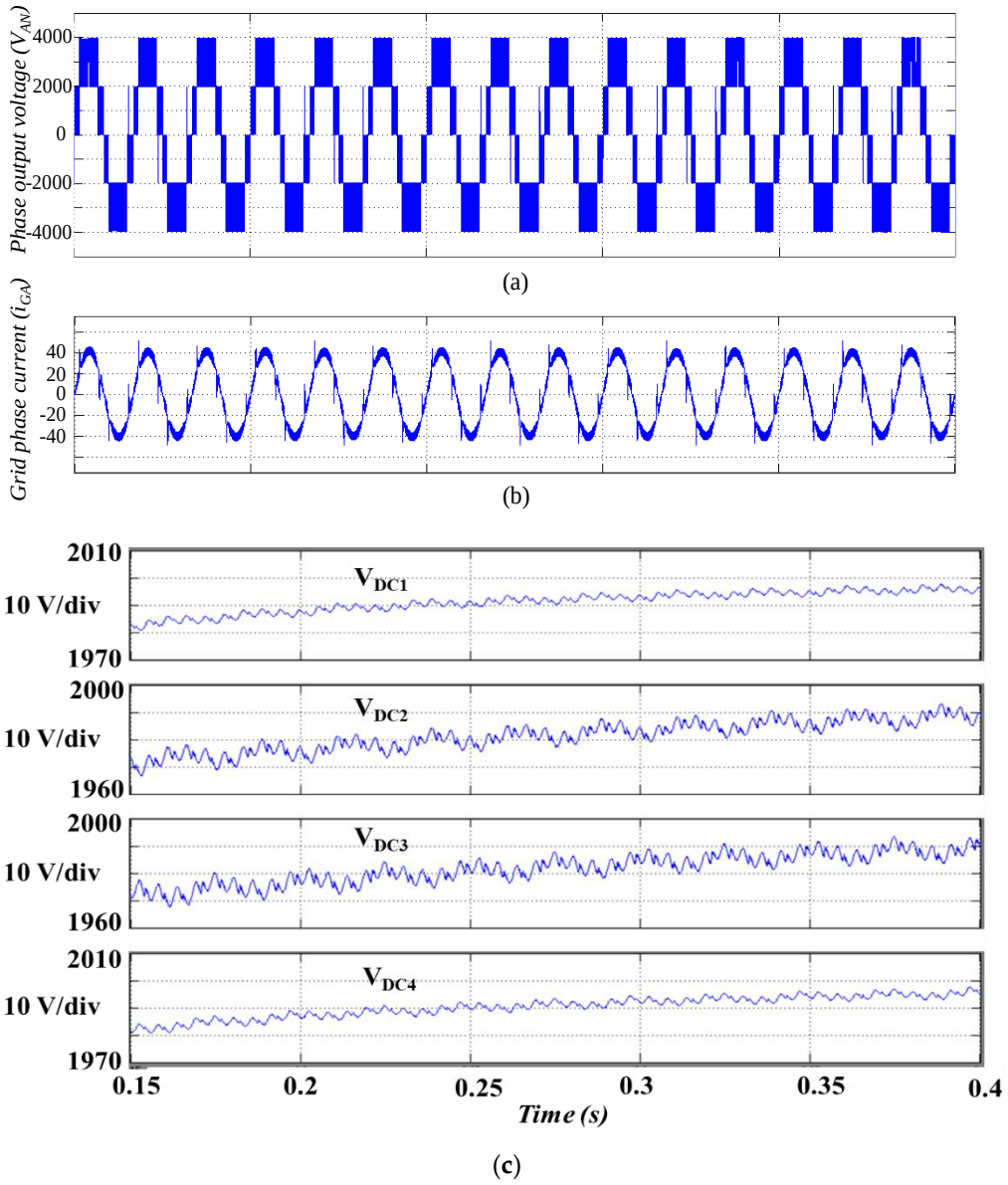


Figure 11. Simulation waveforms of the proposed five-level STATCOM with a three-phase diode rectifier load. (**a**) Phase output voltage (V_{AN}) for Phase A; (**b**) Grid phase current (i_{GA}) for Phase A; (**c**) DC-link capacitor voltages (V_{DC1}-V_{DC4}).

Figures 12 and 13 show the effectiveness of the proposed multilevel OCC control method on source-side voltage sag and swell conditions. The same simulation model and parameters in Figure 6 have been used except the voltage sag or swell condition of the grid phase voltage (V_A) from the time moment t = 0.40 s to t = 0.45 s (3 cycles). To emulate the voltage sag and swell conditions, 0.2 pu voltage decrease in Figure 12 and 0.2 pu voltage increase in Figure 13 have been considered. As shown in Figures 12 and 13, the four dc-link capacitor voltages (V_{DC1}-V_{DC4}) of the proposed DCMC-based STATCOM with unequal dc-link capacitances are stably balanced even under the voltage sag and swell conditions.

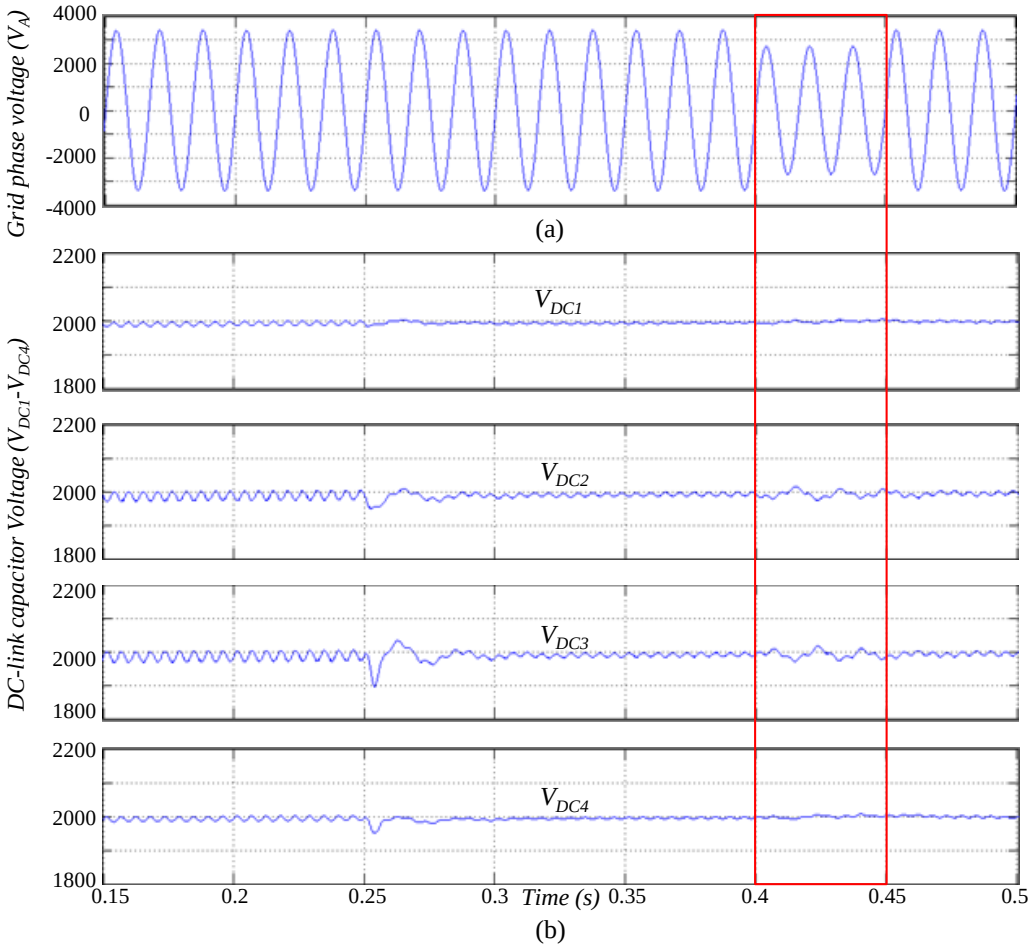


Figure 12. Simulation waveforms of the proposed five-level STATCOM under voltage sag condition. (**a**) Phase output voltage (V_{AN}) for Phase A; (**b**) DC-link capacitor voltages (V_{DC1}-V_{DC4}).

4.2. Experimental Results

A 2 kVA five-level DCMC-based STATCOM prototype was built in Figure 14 for performance verification. As the main switches, IGBTs (IRGP4072DPbF) with 2.5 A optocoupler gate drivers (VO3120) were used in the prototype. In addition, ultrafast diodes (MUR1520) were also applied to the STATCOM prototype as the clamping diodes. The three-phase grid phase voltage (V_A, V_B, V_C) is 120 V and adjustable by a three-phase variable transformer (T_V). The dc bus voltage (V_{DC}) is 400 V and each dc-link capacitor (C_1-C_4) is 2.72 mF. Three 2.8 mH coupling inductors (Lc) are used to connect the proposed STATCOM to the power grid. The grid line frequency is 60 Hz and the carrier frequency is 5 kHz, which are the same frequencies in simulation. The sensing resistance (R_S) of the grid phase current is 0.5 Ω. For dc-link voltage measurement, four isolation amplifiers (AD202KN) are used to sense each dc-link capacitor voltage (V_{DC1}-V_{DC4}) with 0.02 V/V gain. Based on discrete analog circuit, the proposed multilevel OCC controller is implemented. To realize a simple and flexible controller, field programmable analog arrays (FPAAs) can be used to implement the analog multilevel OCC controller. The main parameters of the experimental system are listed in Table 4.

In the test, a 1 kW 1800 rpm three-phase synchronous motor was used as an inductive load. Figure 15 shows the system configuration under the test.

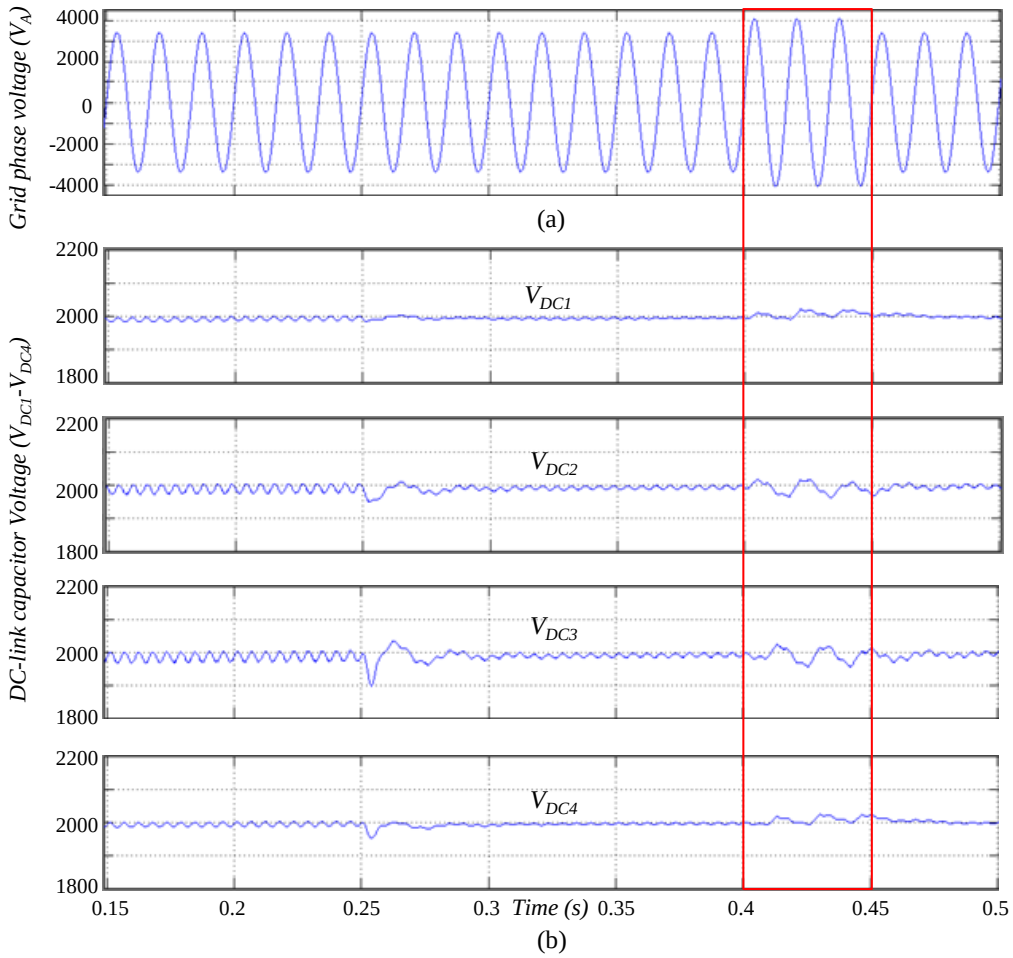


Figure 13. Simulation waveforms of the proposed five-level STATCOM under voltage swell condition. (**a**) Phase output voltage (V_{AN}) for Phase A; (**b**) DC-link capacitor voltages (V_{DC1}-V_{DC4}).

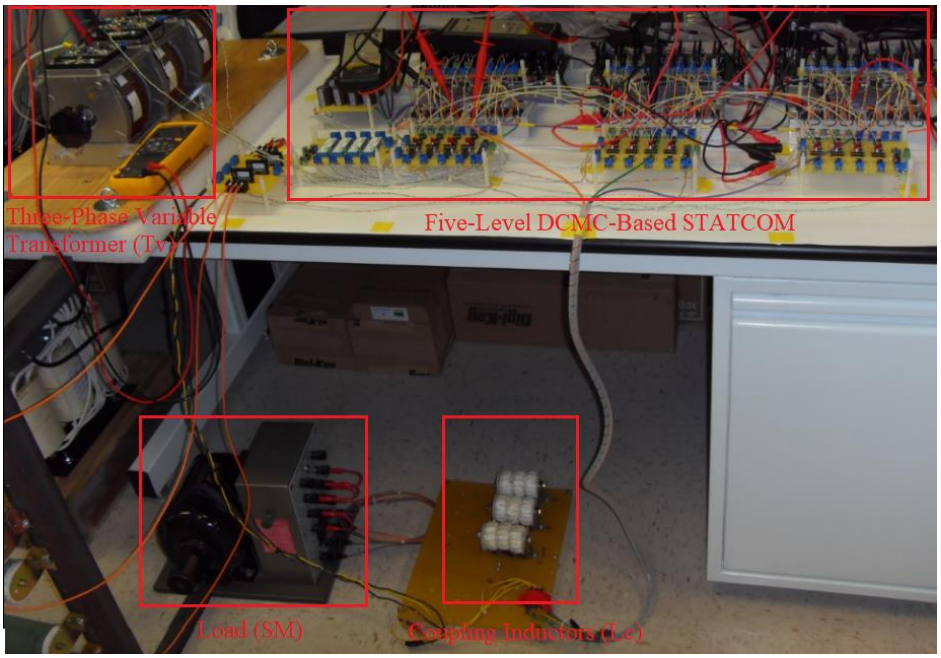


Figure 14. 2 kVA five-level DCMC-based STATCOM prototype.

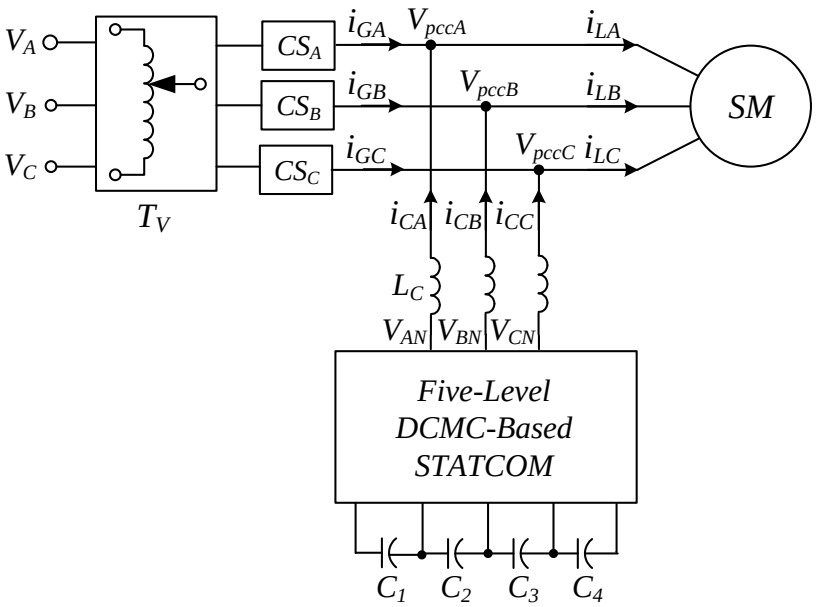


Figure 15. Experiment setup.

Table 4. Parameters of the experimental system.

Parameter	Value
Grid phase voltage (V_A, V_B, V_C)	120 V
DC bus voltage (V_{DC})	200~400 V
DC-link capacitor voltage (V_{DC1}-V_{DC4})	50~100 V
Coupling inductor (L_C)	2.8 mH
DC-link capacitor (C_1-C_4)	2.72 mF
Three-phase motor load (*SM*)	1 kW 1800 rpm
Carrier frequency	5 kHz
Grid line frequency	60 Hz

It consists of the three-phase variable transformer, the synchronous motor (*SM*), the five-level DCMC-based STATCOM with the proposed level-shifted OCC controller, and phase current sensors (CS_A-CS_C). The proposed STATCOM is connected to the point of the motor connection via the coupling inductors, as shown in Figure 15.

The line-to-line output voltage of the proposed five-level DCMC-based STATCOM is shown in Figure 16. As can be seen, the line-to-line voltage of the proposed STATCOM has nine output voltage levels with 50 V voltage step. In this test condition, the dc-link voltage is 200 V and equally shared by the four dc-link capacitors (C_1-C_4).

Figure 17 shows that the four dc-link capacitor voltages of the proposed five-level DCMC-based STATCOM can keep balanced in steady state. During operation, each capacitor voltage is automatically maintained by the voltage compensator without additional voltage-balancing hardware.

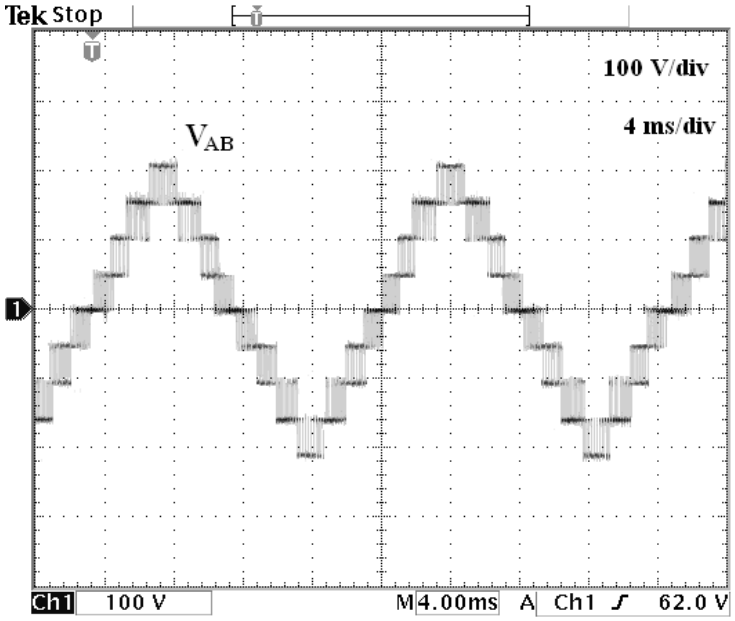


Figure 16. Line-to-line output voltage (V_{AB}) of the five-level DCMC-based STATCOM.

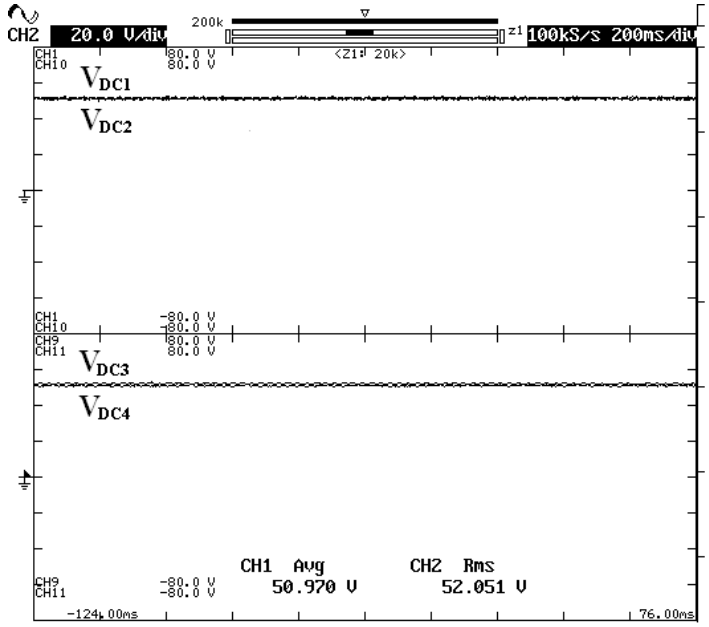
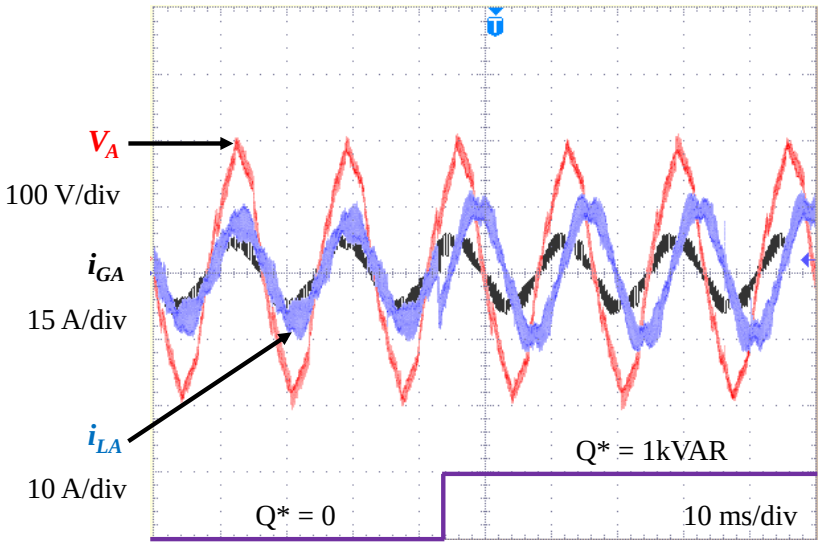
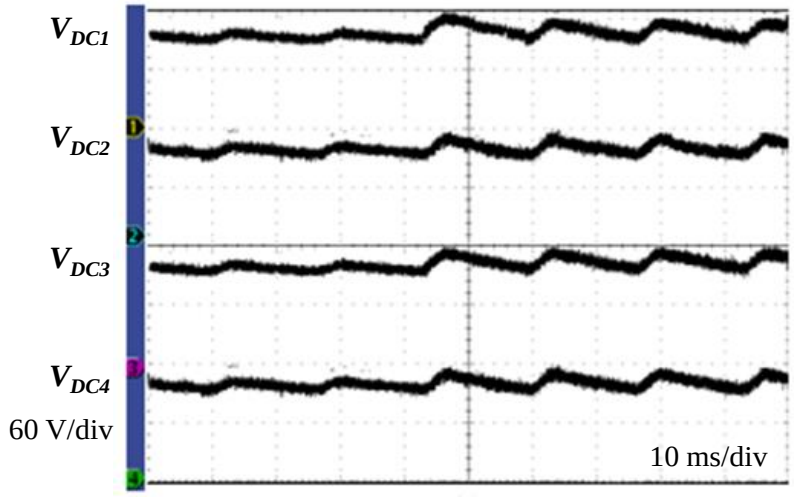


Figure 17. DC-link capacitor voltages (V_{DC1}-V_{DC4}) of the five-level DCMC-based STATCOM.

Figure 18 shows the experimental waveforms in the transient state when the load is changed from a resistive to inductive load. In this test condition, the three-phase grid phase voltage (V_A, V_B, V_C) is 120 V and the dc-link voltage is 380 V, which is equally shared by the four dc-link capacitors (C_1-C_4) at the beginning of the operation. Since the initial load is purely resistive (R_O), the load only consumes the active power, 1.8 kW and the proposed STATCOM delivers no reactive power. To evaluate the dynamic performance of the proposed STATCOM, the load change is made from R_O to $R_O + j\omega_o L_O$ load. In this case, the inductive load consumes 1 kVAR reactive power (Q*). For the proposed OCC controller, the overall control goal is that if the voltage at the PCC is within the standard, the STATCOM will work to improve the power factor for the power grid or if the voltage at the PCC is out of the standard limitation, the STATCOM will regulate the voltage at the PCC.



(**a**)



(**b**)

Figure 18. Experimental waveforms of the dynamic performance from resistive to inductive load. (**a**) Grid phase voltage (V_A), grid phase current (i_{GA}), and load current (i_{LA}) for Phase A; (**b**) DC-link capacitor voltages (V_{DC1}-V_{DC4}).

As shown in Figure 18, the proposed five-level STATCOM provides satisfactory operating performance, including unity power factor for the power grid and dc-link capacitor voltage (V_{DC1}-V_{DC4}) regulation in the steady and transient states. However, since some high harmonics are injected from the three-phase variable transformer (T_V), the experimental results in Figure 18a show the distorted voltage and current waveforms.

Figure 19 shows the experimental waveforms of the grid phase voltage (V_A), the load current (i_{LA}), and the grid phase current (i_{GA}). In Figure 19, the load current has some phase delay with the grid phase voltage since the synchronous motor consumes the reactive power, working as a RL load. With reactive power compensation by the proposed STATCOM, the grid phase current is in phase with the grid phase voltage and has smaller amplitude compared with the load current amplitude. Therefore, the proposed STATCOM can provide power factor improvement for the power grid.

The voltage variation is directly related to real and reactive power variations and is commonly classified as voltage sag, voltage swell, short interruption, and long duration

voltage variation. The voltage flicker happens when there are dynamic variations in the power system caused by dynamic loads or sources. The amplitude of voltage fluctuation depends on grid strength, network impedance, and phase angle or power factor of the dynamic loads. Huge non-linear industrial loads such as electrical arc furnaces, pumps, welding machines, and rolling mills are known as voltage flicker generators.

In this test, the three-phase synchronous motor is used to create the voltage fluctuation in the power system. When the output voltage of the three-phase variable transformer is under the input voltage rating of the synchronous motor, the stator winding is partially excited and creates a weak rotating magnetic field, which revolves at the designated motor speed. However, the rotor, due to its inertia, could not follow the revolving magnetic field since the intensity of the rotating magnetic field is not enough to overcome the rotor inertia and resistance to the rotation. During this operating condition, the synchronous motor is not fully synchronized and behaves in the form of a variable impedance load which can create the voltage flicker in the power system.

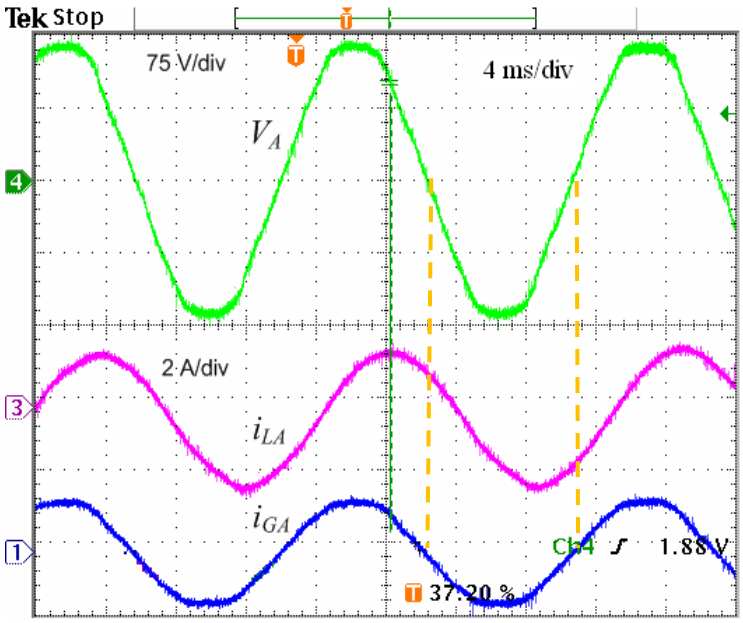


Figure 19. Grid phase voltage (V_A), load current (i_{LA}), and grid phase current (i_{GA}) for Phase A.

Figure 20 shows the experimental waveforms without and with the proposed five-level DCMC-based STATCOM, operating under dynamic load change. When the synchronous motor operates under the rated input voltage, the unstable rotation of the synchronous motor changes the load current by consuming different active and reactive currents. This operating condition can emulate the dynamic change of the inductive load.

As shown in Figure 20a, there is about 10% periodic voltage variation or voltage flicker at the PCC (V_{pccA}), when the STATCOM is not in operation. In Figure 20b,c, the five-level DCMC-based STATCOM dynamically provides the reactive compensation current (i_{CA}) to eliminate the voltage flicker and keep the constant voltage at the PCC.

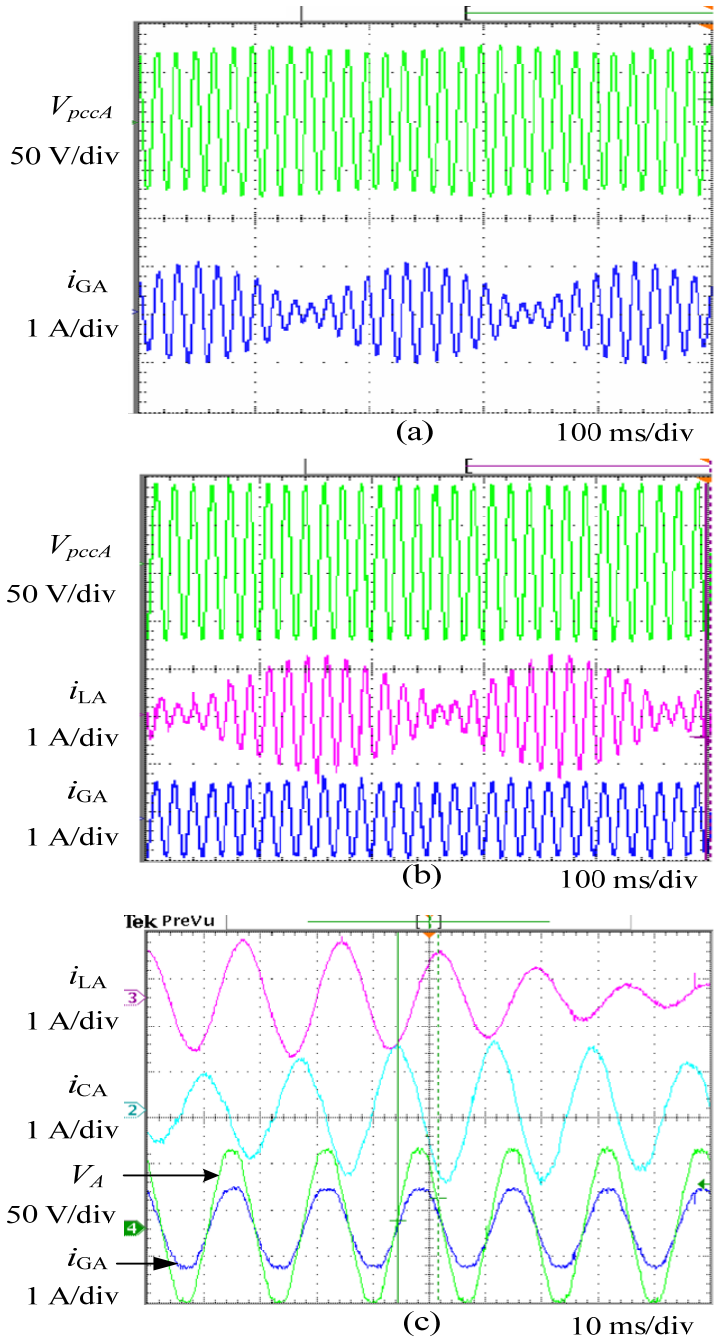


Figure 20. Experimental waveforms of the voltage flicker compensation. (**a**) Coupling-point phase voltage (V_{pccA}) and grid current (i_{GA}) without compensation; (**b**) Coupling-point phase voltage (V_{pccA}), load current (i_{LA}), and grid phase current (i_{GA}) with reactive power compensation; (**c**) Zoomed load current (i_{LA}), STATCOM current (i_{CA}), grid phase voltage (V_A), and grid phase current (i_{GA}) with reactive power compensation.

5. Conclusions

This paper presents the five-level DCMC-based STATCOM with the OCC controller for power quality improvement or grid voltage stabilization. Simulation and experiments have shown that the proposed five-level OCC DCMC-based STATCOM has excellent steady-state and dynamic performance for power factor improvement and is capable of stabilizing the unstable voltage or voltage flicker at the point of the STATCOM connection. The demonstrated features are very important to stabilize the grid voltage to allow increased penetration of renewable energy resources (e.g., wind).

The proposed OCC voltage-balancing technique of the dc-link capacitors is capable of keeping the dc-link capacitor voltages balanced even when the four dc-link capacitors have different capacitance or initial voltage condition. However, the proposed multilevel OCC controller may have limited control capability of the dc-link voltage balance under low AC voltage conditions. It is suitable for MV high power distribution system applications.

Author Contributions: Conceptualization, methodology, validation, formal analysis, and writing—original draft preparation, I.W.J.; writing—review and editing, and supervision, T.H.S. Both authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea. (No. 20192010106790).

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

OCC	One-cycle control
DCMC	Diode-clamped multilevel converter
CMC	Cascaded multilevel converter
VSC	Voltage source converter
STATCOM	Static VAR compensator
MV	Medium voltage
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
SVPWM	Space vector pulsewidth modulation
PCC	Point of common coupling
PFC	Power factor correction
FPAA	Field programmable analog array

References

1. Wind Power Becomes More Cost Effective with 340,000 Turbines Already Installed Worldwide by 2016. Available online: https://www.eqmagpro.com/wind-power-becomes-more-cost-effective-with-340000-turbines-already-installed-worldwide-by-2016 (accessed on 12 January 2018).
2. Fujii, K.; Schwarzer, U.; De Doncker, R.W. Comparison of Hard-Switched Multi-Level Inverter Topologies for STATCOM by Loss-Implemented Simulation and Cost Estimation. In Proceedings of the 2005 IEEE 36th Annual Power Electronics Specialists Conference (PESC), Recife, Brazil, 12–16 June 2005; pp. 340–346.
3. Akagi, H.; Fujita, H.; Yonetani, S.; Kondo, Y. A 6.6-kV Transformerless STATCOM Based on a Five-Level Diode-Clamped PWM Converter: System Design and Experimentation of a 200-V 10-kVA Laboratory Model. *IEEE Trans. Ind. Appl.* **2008**, *44*, 672–680. [CrossRef]
4. Chen, B.S.; Hsu, Y.Y. A Minimal Harmonic Controller for a STATCOM. *IEEE Trans. Ind. Electron.* **2008**, *55*, 655–664. [CrossRef]
5. Singh, B.; Murthy, S.S.; Gupta, S. STATCOM-Based Voltage Regulator for Self-Excited Induction Generator Feeding Nonlinear Loads. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1437–1452. [CrossRef]
6. Saeedifard, M.; Nikkhajoei, H.; Iravani, R. A Space Vector Modulated STATCOM Based on a Three-Level Neutral Point Clamped Converter. *IEEE Trans. Power Deliv.* **2007**, *22*, 1029–1039. [CrossRef]
7. Sternberger, R.; Jovcic, D. Theoretical Framework for Minimizing Converter Losses and Harmonics in a Multilevel STAT-COM. *IEEE Trans. Power Deliv.* **2008**, *23*, 2376–2384. [CrossRef]
8. Song, Q.; Liu, W. Control of a Cascade STATCOM With Star Configuration Under Unbalanced Conditions. *IEEE Trans. Power Electron.* **2009**, *24*, 45–58. [CrossRef]
9. Barrena, J.A.; Marroyo, L.; Vidal, M.Á.R.; Apraiz, J.R.T. Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM. *IEEE Trans. Ind. Electron.* **2008**, *55*, 21–29. [CrossRef]
10. Cheng, Y.; Qian, C.; Crow, M.L.; Pekarek, S.; Atcitty, S. A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM with Energy Storage. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1512–1521. [CrossRef]
11. Pirouz, H.M.; Bina, M.T. A Transformerless Medium-Voltage STATCOM Topology Based on Extended Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2011**, *26*, 1534–1545.

12. Singh, B.; Al-Haddad, K.; Saha, R.; Chandra, A. Static synchronous compensators (STATCOM): A review. *IET Power Electron.* **2009**, *2*, 297–324. [CrossRef]
13. Botao, M.; Congwei, L.; Yang, Z.; Fahai, L. New SVPWM Control Scheme for Three-Phase Diode Clamping Multilevel Inverter with Balanced DC Voltages. In Proceedings of the IEEE 2002 28th Annual Conference of the Industrial Electronics Society (IECON), Sevilla, Spain, 5–8 November 2002; pp. 903–907.
14. Abu-Rub, H.; Holtz, J.; Rodriguez, J.; Baoming, G. Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2581–2596. [CrossRef]
15. Saeedifard, M.; Iravani, R.; Pou, J. Control and DC-capacitor voltage balancing of a space vector-modulated five-level STATCOM. *IET Power Electron.* **2009**, *2*, 203–215. [CrossRef]
16. Shu, Z.; Ding, N.; Chen, J.; Zhu, H.; He, X. Multilevel SVPWM With DC-Link Capacitor Voltage Balancing Control for Diode-Clamped Multilevel Converter Based STATCOM. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1884–1896. [CrossRef]
17. Espinoza, J.E.; Espinoza, J.R.; Morán, L.A. A Systematic Controller-Design Approach for Neutral-Point-Clamped Three-Level Inverters. *IEEE Trans. Ind. Electron.* **2005**, *52*, 1589–1599. [CrossRef]
18. Pan, Z.; Peng, F.Z. A Sinusoidal PWM Method with Voltage Balancing Capability for Diode-Clamped Five-Level Converters. *IEEE Trans. Ind. Appl.* **2009**, *45*, 1028–1034. [CrossRef]
19. Wang, K.; Zheng, Z.; Xu, L.; Li, Y. Neutral-Point Voltage Balancing Method for Five-Level NPC Inverters Based on Carrier-Overlapped PWM. *IEEE Trans. Power Electron.* **2021**, *36*, 1428–1440. [CrossRef]
20. Zhao, Z.; Zhao, J.; Huang, C. An Improved Capacitor Voltage-Balancing Method for Five-Level Diode-Clamped Converters with High Modulation Index and High Power Factor. *IEEE Trans. Power Electron.* **2016**, *31*, 3189–3202. [CrossRef]
21. Cui, D.; Ge, Q. A Novel Hybrid Voltage Balance Method for Five-Level Diode-Clamped Converters. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6020–6031. [CrossRef]
22. Smedley, K.M.; Ćuk, S. One-Cycle Control of Switching Converters. In Proceedings of the 1991 IEEE 22nd Annual Power Electronics Specialists Conference (PESC), Boston, MA, USA, 24–27 June 1991; pp. 888–896.
23. Jin, T.; Li, L.; Smedley, K. A Universal Vector Controller for Three-phase PFC, APF, STATCOM, and Grid-Connected Inverter. In Proceedings of the 2004 Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 22–26 February 2004; pp. 594–600.
24. Slepchenkov, M.; Smedley, K. Flicker Mitigation and Load Balancing in Steel Plants Power Systems by OCC-Hexagram Con-verter Based STATCOM. In Proceedings of the 2009 IEEE Industry Applications Society Annual Meeting (IAS), Houston, TX, USA, 4–8 October 2009; pp. 1–8.
25. Qiao, C.; Jin, T.; Smedley, K.M. One-Cycle Control of Three-Phase Active Power Filter with Vector Operation. *IEEE Trans. Ind. Electron.* **2004**, *51*, 455–463. [CrossRef]
26. Qiao, C.; Smedley, K.M.; Maddaleno, F. A Single-Phase Active Power Filter with One-Cycle Control under Unipolar Operation. *IEEE Trans. Circuits Syst. I* **2004**, *51*, 1623–1630. [CrossRef]