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Partial O-state Clamping PWM Method for Three-Level NPC Inverter with a SiC Clamp Diode

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Abstract – This paper presents the reverse recovery characteristic according to the change of switching states when Si diode and SiC diode are used as clamp diode and proposes a method to minimize the switching loss containing the reverse recovery loss in the neutral-point-clamped inverter at low modulation index. The previous papers introduce many multiple circuits replacing Si diode with SiC diode to reduce the switching loss. In the neutral-point-clamped inverter, the switching loss can be also reduced by replacing device in the clamp diode. However, the switching loss in IGBT is large and the reduced switching loss cannot be still neglected. It is expected that the reverse recovery effect can be infrequent and the switching loss can be considerably reduced by the proposed method. Therefore, it is also possible to operate the inverter at the higher frequency with the better system efficiency and reduce the volume, weight and cost of filters and heatsink. The effectiveness of the proposed method is verified by numerical analysis and experiment results.

Keywords: Multi-level inverter, PWM method, SiC diode

1. Introduction

Because of a growing demand for higher efficiency, higher power density and higher temperature capability of the power converter, there has been a lot of effort in developing power semiconductor devices with Silicon Carbide (SiC) which has the better material properties, compared with them of Silicon [1-6]. SiC schottky diode is superior to Si diode in some characteristics, such as the high-breakdown voltage, the high temperature capability and almost zero reverse-recovery current [7-9] It is already verified that the SiC diode has extremely low reverse recovery current and low switching loss characteristics compared to those of the Si diode at the same forward current [10, 11]. Many multiple circuits replacing Si diode with SiC diode for more improved performance is introduced in the recent studies [12-18]. The behavior of SiC diode in the circuit-level is analyzed by a thorough characterization [19-21]. The neutral-point-clamped (NPC) inverter using SiC diode as the clamp diode has already come into the market. The reverse recovery loss and the switching loss can be partly reduced by replacing Si diode with SiC diode in the clamp diode of NPC inverter. However, the switching loss in IGBT is quite large and the reverse recovery loss caused by the anti-parallel diode of IGBT still remains in the system. The reverse recovery current causes unwanted EMI noise in the circuit and additional efficiency reduction in the system [22-24]. In the worst case, the reverse recovery current has the excessive peak value, this current leads to the destruction of the switching devices.

This paper presents a performance comparison of a 3-level NPC inverter using Si and SiC clamp diodes and proposes the pulse with modulation (PWM) method to minimize the rest of the switching loss containing the reverse recovery loss by maximizing the reverse recovery characteristics of the SiC diode. The performance is evaluated by the reverse recovery characteristics, system efficiency and total harmonic distortion (THD). For the operation of NPC inverter at the higher switching frequency, SiC diode and IGBT which has the low switching energy are selected to prevent a severe increase in the switching loss. Instead of having the low switching energy, the IGBT device has the high forward voltage drop because there is usually a trade-off. When the proposed method is applied, there is the disadvantage that the conduction loss increases in the system. However, a decrease of switching loss is larger than an increase of conduction loss and the total loss is reduced in the inverter system. Therefore, the disadvantage is also covered by the proposed method.

It is expected that the proposed method is valuable to the applications required the high switching frequency operation with high efficiency and useful in reducing the volume, weight and cost of filters and heatsink. The effectiveness of the proposed PWM method is verified by the numerical calculation based on the performance evaluation of each device and experiment results.

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2. A Comparison of the Reverse Recovery Characteristics in NPC Inverter

Fig. 1 shows a schematic diagram of a three-level NPC inverter. Each leg of the inverter consists of two clamped diodes, four IGBT and four anti-parallel diodes. The three-level inverter has three kinds of the switching states such as p, o and n in each leg. Table 1 shows the switching states and the output leg voltages of the three-level NPC inverter.

2.1 NPC Inverter with a Si clamp diode

In case of using Si diode as the clamp diode in NPC

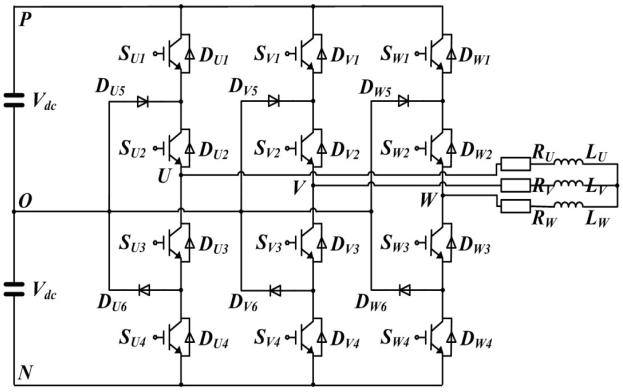
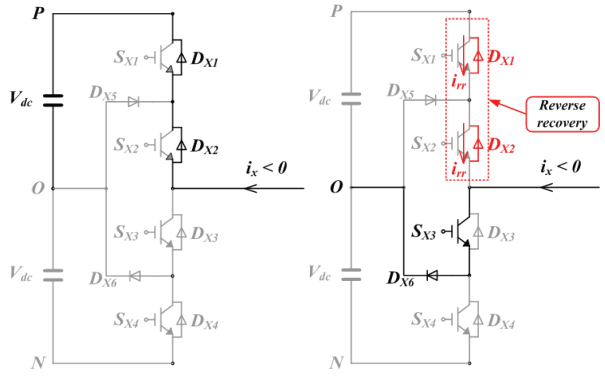
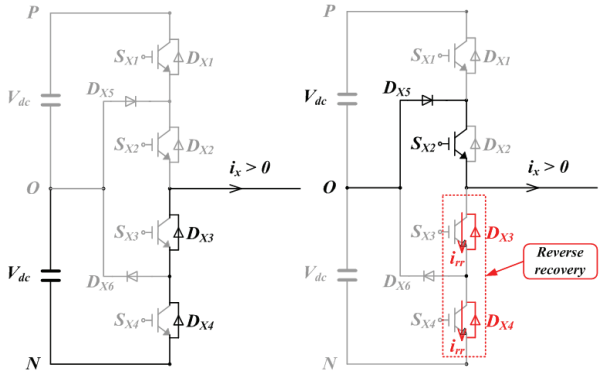


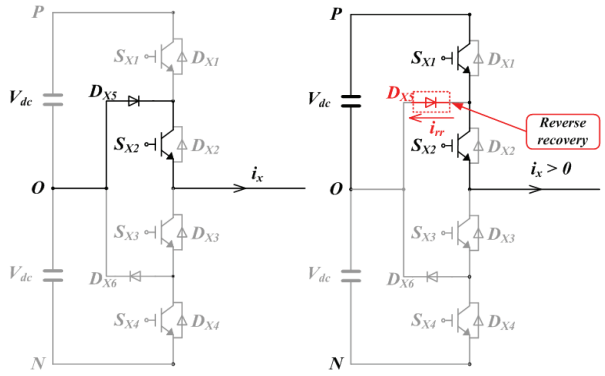
Fig. 1. The NPC 3-level inverter



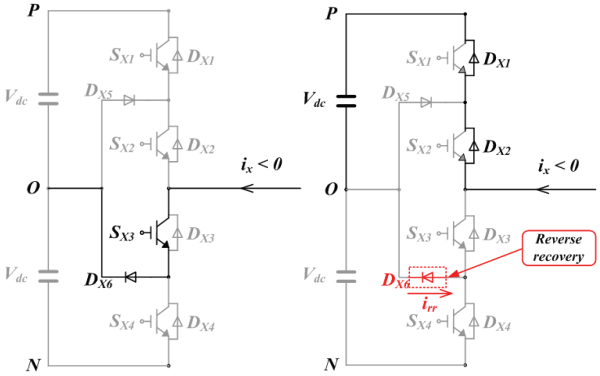
(a) switching state : P → O ($i_x > 0$)



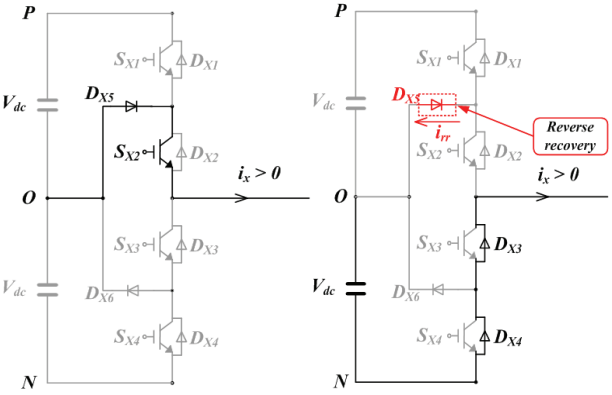
(b) switching state : N → O ($i_x > 0$)



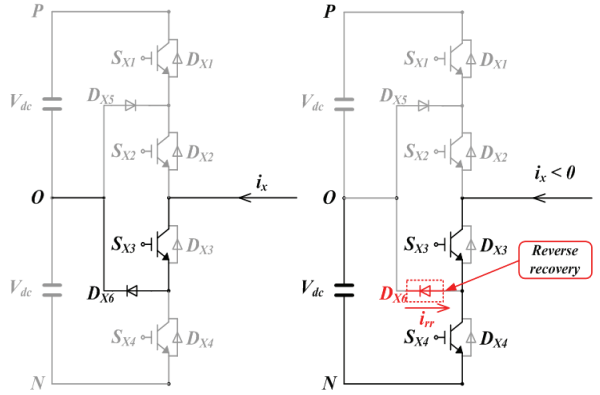
(c) switching state : O → P ($i_x > 0$)



(d) switching state : O → P ($i_x < 0$)



(e) switching state : O → N ($i_x > 0$)



(f) switching state : O → N ($i_x < 0$)

Fig. 2. The reverse recovery effects in NPC inverter with Si clamp diode

Table 1. Switching states of a three-level NPC inverter

Switching states	S1	S2	S3	S4	Output leg voltage
P	ON	ON	OFF	OFF	Vdc/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

inverter presented in Fig. 1, the reverse recovery effects occur whenever the switching states of NPC inverter change from a state, the clamp diode or the anti-parallel diode of IGBT is in the ON state, to the other states as presented in Fig. 2. The reverse recovery effects cause the reverse recovery loss and the extra conduction loss due to the reverse recovery current, i_{rr} in Fig. 2.

2.2 NPC inverter with a SiC clamp diode

In case of using SiC diode as the clamp diode in NPC inverter, there is no reverse recovery effect in the clamp diode due to the property of SiC diode. So the reverse recovery effects are quite reduced than the above case. The reverse recovery effects occur whenever the switching states of NPC inverter change from the P state or the N state, the anti-parallel diode of IGBT is in the ON state, to the O state. According to the direction of the load current, i_x in Fig. 2, it is decided whether the reverse recovery effects will occur or not. The only cases that the reverse recovery effects occur in NPC inverter using SiC diode are presented in Fig. 2 (a), (b).

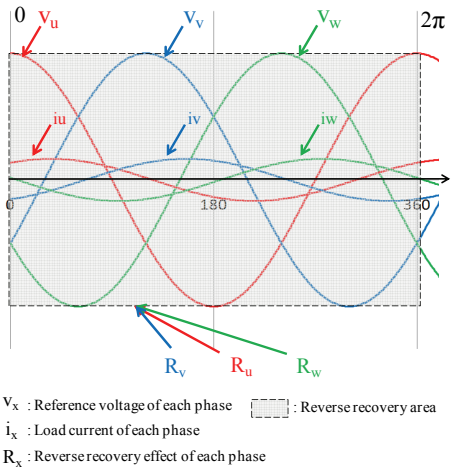
The remained reverse recovery effects only occur when the reference voltage and the load current have the opposite sign each other. When the phase angle between reference voltage and load current is θ, the power factor is $\cos\theta$. In other words, as the power factor is smaller, the area where the reverse recovery effects occur becomes wider.

3. The Proposed Method

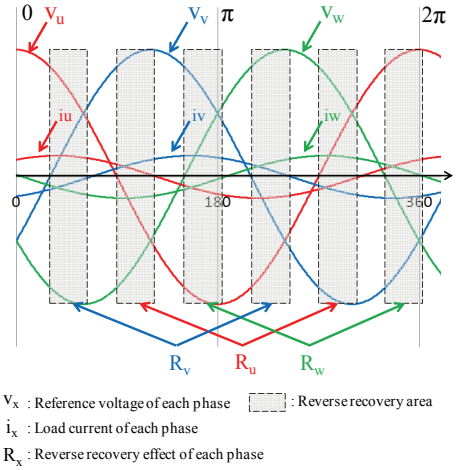
Fig. 3 shows the example comparing the Sinusoidal PWM(SPWM) method and the proposed method which adds the offset voltage to the reference voltages of each phase in the SPWM method when the power factor angle is about 36° (the power factor is about 0.8). There is a remarkable difference in the reverse recovery area.

In Fig. 3 (a), the reverse recovery effect always occurs during the whole period in the SPWM method with Si clamp diode.

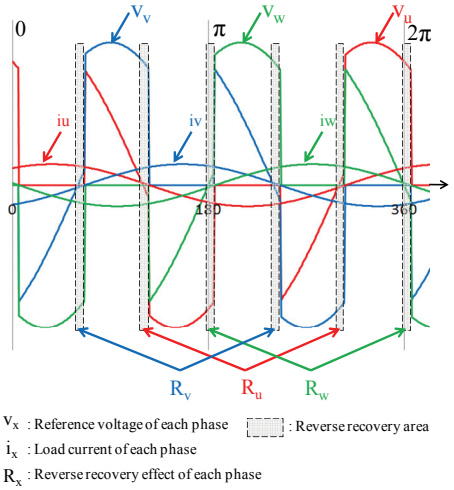
In Fig. 3 (b), when the switching states change from the O state to the P state or the N state, there is no reverse recovery effect due to the performance characteristics of the SiC diode. So, the single reverse recovery area is 36° in the SPWM method with SiC clamp diode. A section, in which the load current of a phase has the maximum amplitude, compared with the others, is arranged every 60° intervals in Fig. 3. The single reverse recovery area in the SPWM method with SiC clamp diode overlaps with



(a) SPWM with Si clamp diode



(b) SPWM with SiC clamp diode

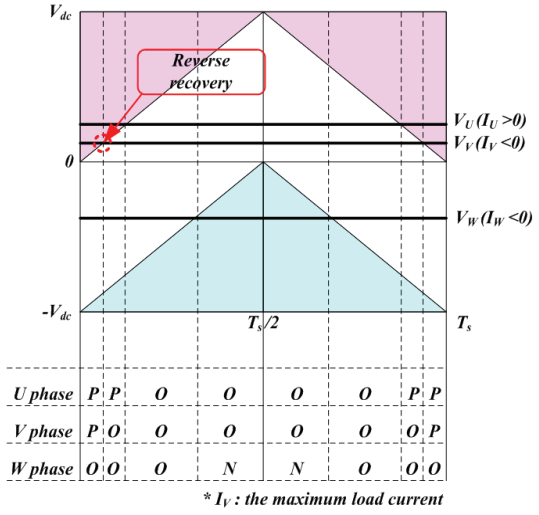


(c) Proposed method with SiC clamp diode

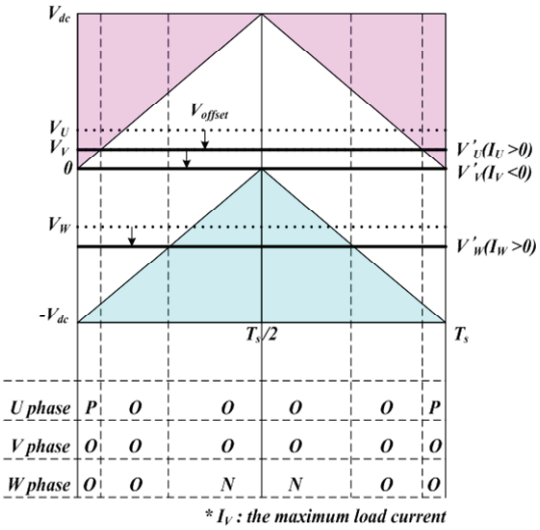
Fig. 3. The comparison in the reverse recovery area

this area.

In Fig. 3 (c), the single reverse recovery area is only 6° in the proposed method with SiC clamp diode and the load current is absolutely small in the reverse recovery



(a) SPWM with SiC clamp diode



(b) Proposed method with SiC clamp diode

Fig. 4. The reference voltages and switching states

Table 2. The offset voltage according to the condition

Offset voltage	Condition
$V_{offset} = -V_u$	$\max(\lvert i_u\rvert, \lvert i_v\rvert, \lvert i_w\rvert) = \lvert i_u\rvert$
$V_{offset} = -V_v$	$\max(\lvert i_u\rvert, \lvert i_v\rvert, \lvert i_w\rvert) = \lvert i_v\rvert$
$V_{offset} = -V_w$	$\max(\lvert i_u\rvert, \lvert i_v\rvert, \lvert i_w\rvert) = \lvert i_w\rvert$

area. So the remained reverse recovery losses are very small. If the power factor angle is smaller than $30°$, the proposed method makes the reverse recovery loss to zero during the whole period.

In the proposed method, an offset voltage is added to the reference voltages of each output leg voltages (V_u, V_v, V_w). Because the reverse recovery area and the peak current area overlap each other and both the switching loss containing the reverse recovery loss and the conduction loss are a function of the load current [5], the offset voltages added to the reference voltages are determined according to the magnitude of each load currents (I_u, I_v, I_w). Table 2 shows the offset voltage according to the condition. In Fig. 4, new output leg voltages $V_u^{'}$, $V_v^{'}$ and $V_w^{'}$ are given by:

$$\begin{aligned} V_u^{'} &= V_u + V_{offset} \\ V_v^{'} &= V_v + V_{offset} \\ V_w^{'} &= V_w + V_{offset} \end{aligned} \tag{1}$$

The modulation index is restricted to a low value under 0.5 because the magnitude of the reference voltage should be lower than the dc-link voltage. The reference voltage of the phase which has the maximum load current is clamped to the O rail in the section by adding the offset voltage. So, it is possible to reduce the reverse recovery loss and minimize the switching loss in IGBT by placing a phase, of which a load current has the maximum amplitude, on the O rail. Moreover, because there are no changes in the switching states when the phase is clamped to the O rail, the switching loss are perfectly eliminated.

4. Performance Evaluation

For the performance evaluation of the proposed method, the switching losses in the devices are compared when Si diode and SiC diode are used as clamp diode in NPC inverter. The experiment setup is shown in Fig. 5 and the setup information is shown in Table 3 and Table 4. To

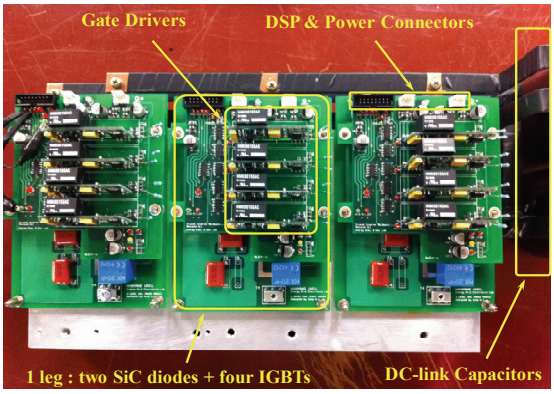


Fig. 5. NPC 3-level inverter experiment setup

Table 3. The experimental setup information

DC-link Voltage		200V
Output Current		3A
Power Factor		0.8
Modulation Index		0.3
RL Load	Resistor	10Ω
	Inductor	20mH, 0.5Ω
Switching Frequency		20kHz
Carrier Frequency		20kHz

calculate the switching loss, the switching energy losses of each device are measured by experiments.

Fig. 6 and Fig. 7 present the turn ON/OFF characteristic examples of each device measured by experiments. $E_{on/off}$ is approximately calculated by using the waveforms in Fig. 8 and (2)-(4).

$$E_{on/off}\left(I_F[k]\right) = \int_{t_{on/off}} v \cdot i \, dt \tag{2}$$

$$E_{on}[k] = m \cdot \left(I_F[k]\right)^{n} \tag{3}$$

$$E_{off}[k] = p \cdot \left(I_F[k]\right)^{q} \tag{4}$$

where $E_{on/off}$ is the switching ON/OFF energy loss, $t_{on/off}$ is the switching time, I_F is the peak value of the forward current and k denotes an integer that means the switching number. When the output frequency is 60Hz and the switching frequency is 25kHz, k has the boundary between 0 and 416 ($\cong 25k/60$).

The calculated switching energy is presented in Fig. 8. The constant values m, n, p and q are obtained by using the trend line function of Excel. The constant values of clamp diode, m, n, p, and q in (3) and (4), are 0.00000458, 0.1566274225, 0.00000572 and 0.0330124878, respectively. The constant values of IGBT are 0.00001094, 0.3571856833, 0.00023134 and 0.7988970686, respectively. The constant values of anti-parallel diode are 0.00000626, 0.6550135871 and 0.00000754, respectively.

In each sampling time, the number of switch changing the switching state is two. In other words, ON and OFF operation in the single leg occur one in each sampling time. After calculating each $E_{on/off}$ by using the obtained m, n, p and q, the switching loss in each sampling time is calculated by (5). Finally, p_{total} is calculated by (6) with considering the area occurring the switching of each device during a period.

$$p[k] = \frac{1}{T}\left(E_{on}[k] + E_{off}[k]\right) \tag{5}$$

$$p_{total} = \sum\nolimits^{*} p[k] \tag{6}$$

Table 4. The switch device information

-	Devices		
Parameter	IGBT	Si Diode	SiC Diode
Manufacturer	Microsemi Power Products Group	ST Microelectronics	Cree
Part No.	APT15GT120	STTH1512PI	C2D10120
Type	NPT	Ultrafast recovery	SiC Schottky
Breakdown Voltage	1200V	1200V	1200V
Rated Current	36A	15A	17A
Forward Voltage	3.6V@15V, 15A	2.1V@15A	1.8V@10A
Max. Junction Temperature	-	175 ˚C	175 ˚C

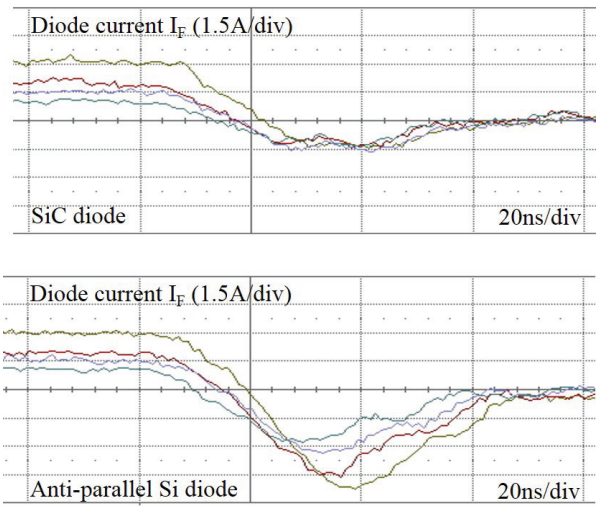


Fig. 6. The reverse recovery characteristic of SiC diode and anti-parallel Si diode of IGBT

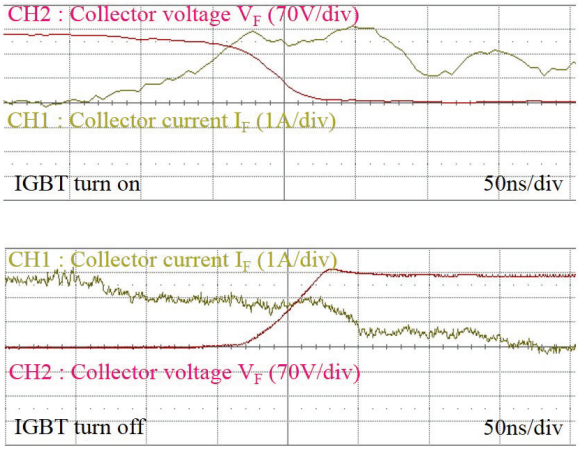


Fig. 7. The IGBT turn ON/OFF characteristic

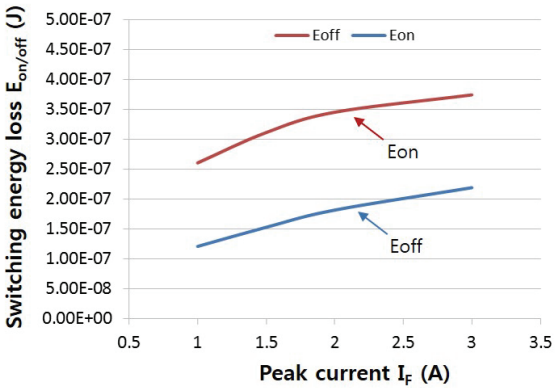


Fig. 8. The switching energy loss of IGBT

Table 5. The switching loss in a clamp diode

Condition	Switching loss
SPWM Method, Clamp diode : Si diode	0.2054W
SPWM Method, Clamp diode : SiC diode	0.1343W
Proposed Method, Clamp diode : SiC diode	0.0876W

where T is the switching period, $p[k]$ is the average value of an instantaneous switching loss in a device and p_{total} is the total average value of the switching loss in a device during one period. In (6), the star(*) means only k in the area occurring the switching of each device during a period.

The calculated switching loss in the clamp diode on each condition is shown in Table 5. When Si diode is replaced by SiC diode under the SPWM method, the decreasing rate of the switching loss in the clamp diode is about 35%. In the proposed method, when Si diode is replaced by SiC diode, the decreasing rate of the switching loss in the clamp diode is about 57%.

The calculated switching loss in each switch by each condition is shown in Table 6, Table 7 and Table 8. Because the switching loss in IGBT is greatly large, the effectiveness is small when Si diode is only replaced by SiC diode. However, the effectiveness is obvious in proposed method.

The calculated total switching loss is shown in Table 9. When using proposed method, the total switching loss reduction is about 7W, equivalently 31% of a total switching loss under general SPWM with Si clamping diode.

Both the inverters using SiC clamp diode and using Si clamp diode were tested with a resistive-inductive load and experimental setup with the same procedure and the same conditions. For the load test, the output leads of the inverter are connected to a three-phase resistor and inductor in series. The DC-link voltage was 200 V and modulation index was varied from 0 to 1. The switching frequency is 20 kHz.

For each value of modulation index, input / output power, the dc-link voltage, dc-link current, output current, output voltage, efficiency and THD of output current were measured by power analyzer PPA5530 from Newtons 4th Ltd. Fig. 9 compares the inverter system efficiency measured in inverter using proposed method and that of conventional

Table 6. The switching loss in each switch (SPWM method and Si clamped diode)

Switch devices	Switching loss
$S_{X1} + S_{X2} + S_{X3} + S_{X4}$	9.9088W
$D_{X1} + D_{X2} + D_{X3} + D_{X4}$	0.1266W
$D_{X5} + D_{X6}$	0.4106W
Total switching loss	10.4460W

Table 7. The switching loss in each switch (SPWM method and SiC clamped diode)

Switch devices	Switching loss
$S_{X1} + S_{X2} + S_{X3} + S_{X4}$	9.9088W
$D_{X1} + D_{X2} + D_{X3} + D_{X4}$	0.1266W
$D_{X5} + D_{X6}$	0.2686W
Total switching loss	10.3040W

Table 8. The switching loss in each switch (Proposed method and SiC clamped diode)

Switch devices	Switching loss
$S_{X1} + S_{X2} + S_{X3} + S_{X4}$	3.0647W
$D_{X1} + D_{X2} + D_{X3} + D_{X4}$	0.0100W
$D_{X5} + D_{X6}$	0.1750W
Total switching loss	3.2524W

Table 9. The total switching loss

Condition	Switching loss
SPWM Method, Clamp diode : Si diode	10.44W
SPWM Method, Clamp diode : SiC diode	10.30W
Proposed Method, Clamp diode : SiC diode	3.25W

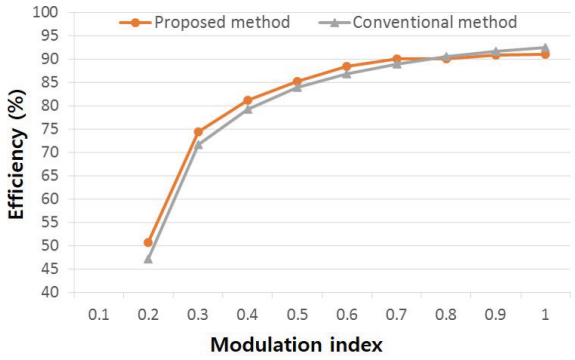


Fig. 9. Inverter system efficiency curves for various modulation index.

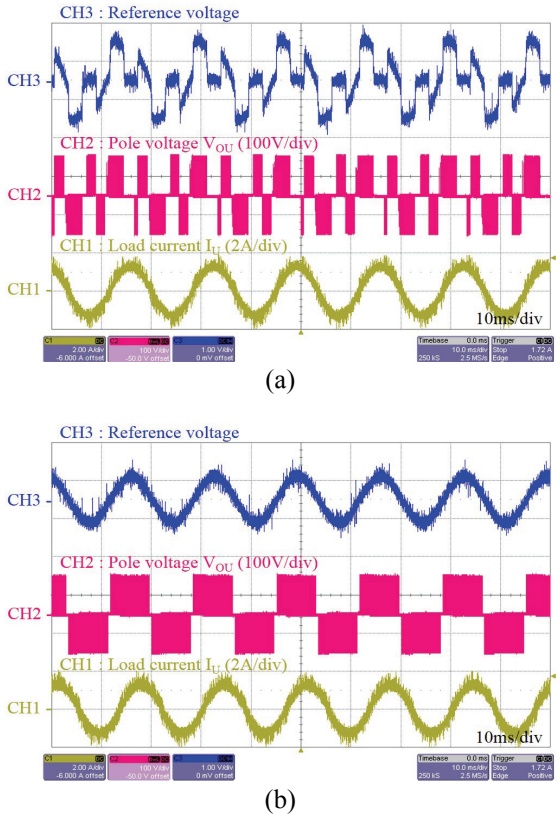
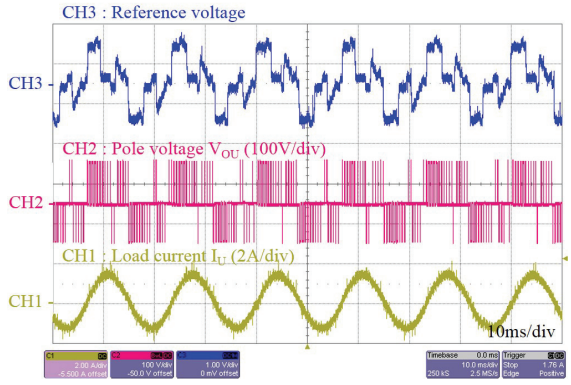


Fig. 10. Inverter reference voltage, pole voltage and load current during RL load test for two different methods: (a) Proposed method; (b) Conventional method; V_{dc} = 200V, $i_{u,\ peak\text{-}to\text{-}peak}$ = 3A and f_{sw} = 20kHz.

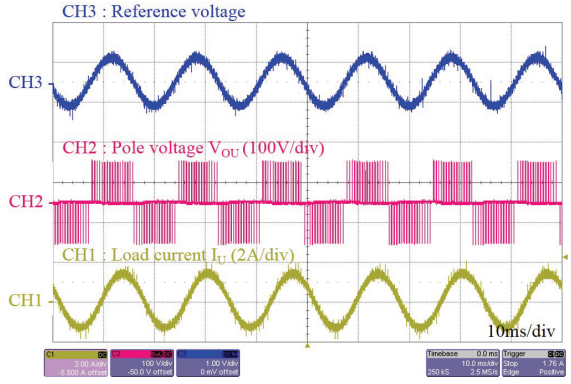
method at each modulation index. On average, 2.05 % loss reduction in inverter system using the proposed method is observed during the modulation index is varied from 0.2 to 0.7. After the modulation index is 0.8, the efficiency of inverter system using the conventional method is 0.87% higher on average because the correct offset voltage in Table 2 cannot be added to the reference voltages due to a restriction of the modulation index. The more a modulation index increases, when the output current has a maximum value, the more a section where the correct offset voltage is applied becomes narrow and the efficiency decreases.

The inverter operation waveforms, efficiency and THD for two different methods with different switching frequency are shown in Fig. 10, Fig. 11 and Table 10.

There is a slight difference 0.2% between the efficiency on both methods at 2kHz switching frequency. In the case of 20kHz switching frequency, the gap widened up to 2.8%. Although the output current THD of proposed method is worse than that of conventional method due to a nonsinusoidal reference voltage, the value is allowable at high switching frequency.



(a)



(b)

Fig. 11. Inverter reference voltage, pole voltage and load current during RL load test for two different methods. (a) Proposed method, (b) Conventional method; V_{dc} = 200V, $i_{u,\ peak\text{-}to\text{-}peak}$ = 3A and f_{sw} = 2kHz.

Table 10. Efficiency and the output current THD of the inverter system using proposed method and conventional method with different switching frequency condition

PWM		Proposed method	Conventional method
Modulation index	Switching frequency	Efficiency / THD	Efficiency / THD
0.3	2 kHz	Eff : 82.82 % THD : 1.122 %	Eff : 83.06 % THD : 0.444 %
0.3	20 kHz	Eff : 74.46 % THD : 0.659 %	Eff : 71.66 % THD : 0.366 %

It is verified through the experiment that the proposed method is more effective on high switching frequency and low modulation index condition.

5. Conclusion

In this paper, a partial O-state clamping PWM method for three-level NPC inverter using SiC diode as clamp diode. On three-level NPC inverter system replacing Si clamp diode with SiC clamp diode, the occurrence of the reverse recovery effects are compared according to the change of switching state. Because the occurrence frequency is significantly reduced by adding offset voltage to the reference voltage, the reverse recovery loss is reduced by proposed method. The switching loss is simultaneously reduced by clamping the reference voltage of one phase to the O rail in the section where the phase has the maximum load current. The switching energy loss of IGBT and the reverse recovery characteristics of each diode are measured by the repeated experiment and the switching losses of each device are compared in three cases. In comparison with conventional method, it is possible to reduce most of the switching loss in IGBT and the reverse recovery loss or eliminate the reverse recovery loss perfectly by using the proposed method. The validity of proposed method is verified by numerical analysis and the experiment results. Consequently, the proposed method is effective for operating three-level NPC inverter at the higher switching frequency with the improved efficiency.

References

[1] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC and Si for power devices," *IEEE Trans. Electron. Devices*, vol. 40, no. 3, pp. 645-655, Mar. 1993.

[2] R. Singh, J. A. Cooper, M. R. Melloch, T. P. Chow and J. W. Palmour, "SiC power schottky and PiN diodes," *IEEE Trans. Electron. Devices*, vol. 49, no. 4, pp. 665-672, Apr. 2002.

[3] B. Ozpineci, L. M. Tolbert, S. K. Islam and F. Z. Peng, "Testing, characterization and modeling of SiC

diodes for transportation applications," *in IEEE 2002 Power Electronics Specialists Conference*, 2002.
[4] J. L. Hudgins, G. S. Simin, E. Santi and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron*, vol.18, no. 3, pp. 907-914, May. 2003.
[5] B. Ozpineci and L. M. Tolbert, "Characterization of SiC schottky diodes at different temperatures," *IEEE Power Electronics Letters*, vol. 1, no. 2, pp. 54-57, June. 2003.
[6] S. Kyungmin, M. Kamaga, Y. Tanaka and H. Ohashi, "Optimum combination of SiC-diodes and Si-switching devices in high power application," *in IEEE 2006 Power Electronics Specialists Conference*, 2006.
[7] M.E. Levinshteina, P.A. Ivanova, M.S. Boltovetsb, V. A. Krivutsab, J. W. Palmourc, M. K. Dasc and Brett A. Hullc, "High-temperature(up to 773K) operation of 6kV 4H-SiC junction diodes," *Solid-State Electronics*, vol. 49, no. 7, pp. 1228-1232, July. 2005.
[8] M. Holza, G. Hultschb, T. Scherga and R. Ruppa, "Reliablility considerations for recent Infineon SiC diode releases," *Microelectronics Reliability*, vol.47, no.9, pp.1741-1745, Sep. 2007.
[9] A. Agarwal, "600V, 1-40A, Schottky diodes in SiC and their applications," [Online] Available : http://www.cree.com/products/pdf/PWRTechnicalPaper1.pdf
[10] R. Singh and M. Pecht, "Commercial impact of silicon carbide," *IEEE Ind. Electron. Mag.*, vol. 2, no. 3, pp. 19-31, Sep. 2008.
[11] Q. Zhang, R. Callanan, M. K. Das, S. H. Ryu, A. K. Agarwal and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp.2889-2896, Dec. 2010.
[12] G. Spiazzi, S. Buso, M. Citron, M. Corradin and R. Pierobon, "Performance evaluation of a schottky SiC power diode in a boost PFC application," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1249-1253, Nov. 2003.
[13] A. Elasser, M. H. Kheraluwala, M. Ghezzo, R. L. Steigerwald, N. A. Evers, J. Kretchmer and T. P. Chow, "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 915-921, Jul. 2003.
[14] M.M. Hernando, A. Fernandez, J. Garcia, D.G. Lamar and M. Rascon, "Comparing Si and SiC diode performance in commercial AC-to-DC rectifiers with power factor correction," *IEEE Trans. Ind. Electron.*, vol.53, no.2, pp.705-707, Apr. 2006.
[15] B. Ozpineci, M. Chinthavali, A. Kashyap, L. M. Tolbert and A. Mantooth, "A 55 kW three-phase inverter with Si IGBTs and SiC schottky diodes," *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 278-285, Jan. 2009.
[16] M. Chinthavali, H. Zhang, L. M. Tolbert and B. Ozpineci, "Update on SiC-based inverter technology," *in IEEE 2009 Power Electronic Conference*, 2009.
[17] J. Sabate, J. M. Rivas, P. Szczesny and L. Stevanovic, "A high-bandwidth high-power inverter," *in IEEE 2009 Power Electronics and Applications Conference*, 2009.
[18] K. Takao, Y. Tanaka, S. Kyungmin, K. Wada, T. Shinohe, T. Kanai and H. Ohashi, "3-Level power converter with high-voltage SiC-PiN diode and hardgate-driving of IEGT for future high-voltage power conversion systems," *in IEEE 2010 Applied Power Electronics Conference and Exposition*, 2010.
[19] C. Ho, F. Canales, A. Coccia and M. Laitinen, "A circuit-level analytical study on switching behaviors of SiC diode at basic cell for power converters," *in Proceedings of IEEE Ind. Appl. Soc. Annu. Meet.*, Oct. 2008.
[20] C. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. A. Serpa and A. Coccia, "Practical design and implementation procedure of an interleaved boost converter using SiC diodes for PV applications," *IEEE Trans. Power. Electron.*, vol. 27, no. 1, pp. 2835-2845, Jun. 2012.
[21] C. Ho, H. Breuninger, S. Pettersson, G. Escobar and F. Canales, "A comparative performance study of an interleaved boost converter using commercial Si and SiC diodes for PV applications," *IEEE Trans. Power. Electron.*, vol. 28, no. 1, pp. 289-299, Jan. 2013.
[22] Y. Wang, Q. Zhang, J. Ying and C. Sun, "Prediction of PiN diode reverse recovery," *in IEEE 2004 Power Electronics Specialists Conference*, 2004.
[23] G. Busatto, C. Abbate, L. Fratelli, F. Iannuzzo, G. Giannini and B. Cascone, "EMI analysis in high power converters for traction application," *in IEEE 2005 European Conference Power Electronics and Applications*, 2005.
[24] Yong-Ming Yang, He-Meng Peng and Quan-Di Wang, "Common Model EMI Prediction in Motor Drive System for Electric Vehicle Application," *Journal of Electrical Engineering & Technology*, vol. 10, no. 1, pp. 205-215, Jan. 2015.

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