A Q-Modulation Technique for Efficient Inductive Power Transmission

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***Abstract*—A fully integrated power management ASIC for efficient inductive power transmission has been presented capable of automatic load transformation using a method, called Q-modulation. Q-modulation is an adaptive scheme that offers load matching against a wide range of loading (R_L) and coupling distance (d_{23}) variations in inductive links to maintain high power transfer efficiency (PTE). It is suitable for inductive powering implantable microelectronic devices (IMDs), recharging mobile electronics, and electric vehicles. In Q-modulation, the zero-crossings of the induced current in the receiver (Rx) LC-tank are detected and a low-loss switch chops the Rx LC-tank for part of the power carrier cycle to form a high-Q LC-tank and store the maximum energy, which is then transferred to R_L by opening the switch. By adjusting the duty cycle (D), the loaded-Q of the Rx LC-tank can be dynamically modulated to compensate for variations in R_L. A Q-modulation power management (QMPM) prototype chip was fabricated in a 0.35 μm standard CMOS process, occupying 4.8 mm^2. In a 1.45 W wireless power transfer setup, using a class-E power amplifier (PA) operating at 2 MHz, the QMPM successfully increased the inductive link PTE and the overall power efficiency by 98.5% and 120.7% at $d_{23} = 8$ cm, respectively, by compensating for 150 Ω variation in R_L at $D = 45\%$.**

***Index Terms*—Battery charging, electric vehicles, implantable microelectronic devices, inductive links, power management, Q-modulation, wireless power transmission.**

I. Introduction

NEAR-FIELD wireless power transmission (WPT) has a wide variety of applications, such as implantable microelectronic devices (IMDs) that substitute sensory or motor modalities lost to an injury or a disease, or collect information from the nervous system and send outside of the body for further processing. Among popular examples of this group of IMDs are the cochlear implants, visual prostheses, and invasive brain–computer interfaces (iBCI) [1]–[8]. The use of WPT is expected to see an explosive growth over the next decade as engineers try to cut the last cord for recharging the batteries of mobile electronics, small home appliances, and electric vehicles [9]–[15].

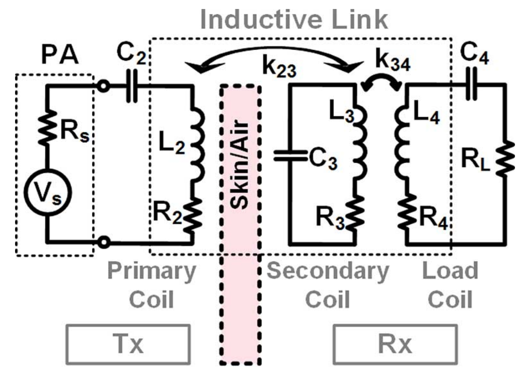

Fig. 1. Lumped circuit model of the 3-coil inductive link, in which k_{34} is used to transform R_L to the optimal loading for the loosely coupled $L_2 - L_3$ link to achieve the highest PTE.

The mutual coupling (k_{23}) between a pair of coupled coils (e.g., $L_2 - L_3$ in Fig. 1) is inversely proportional to the distance (d_{23}) between the coils when they are in parallel planes and perfectly aligned [16]. A key requirement in all of the aforementioned applications is to deliver sufficient power to the load with high power transfer efficiency (PTE) in worse case conditions when d_{23} is relatively large or the coils are misaligned, otherwise PTE is high at small d_{23} when the coils are aligned. The PTE of an inductive link is defined as the ratio of the delivered power to the AC load (R_L in Fig. 1) to the AC power at the input of the inductive link (PA output power in Fig. 1). High PTE is required to reduce tissue exposure to the RF magnetic field in IMDs, heat dissipation within the coils, size of the external energy source, and potential interference with nearby electronics, which is highly regulated [17]–[19].

The PTE of conventional 2-coil inductive links is also dependent on the loading of the receiver (Rx) coil, which represents the AC equivalent of the power conversion circuitry and the DC load in the rest of this paper [20]. The magnetic resonance-based power transmission in the form of 3- and 4-coil inductive links has been proposed to maximize the PTE for any given loading, R_L, by adding an additional coil, L_4, on the Rx side, as shown in Fig. 1, which depicts the circuit model of the 3-coil inductive link [21]–[25]. Compared to their 2-coil counterpart, the 3- and 4-coil links add a new degree of freedom (k_{34}) to transform any given R_L to the optimal matched load, which is required to achieve high PTE in the loosely coupled $L_2 - L_3$ link. However,

Manuscript received April 25, 2015; revised June 03, 2015; accepted June 30, 2015. Date of publication July 28, 2015; date of current version November 24, 2015. This paper was approved by Guest Editor Makoto Takamiya. This work was supported in part by the National Institutes of Health, grant 1R21EB018561, and the National Science Foundation under awards IIP-1439426, ECCS-1407880, and ECCS-1408318.

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Digital Object Identifier 10.1109/JSSC.2015.2453201

these links need an additional coil in the Rx, which adds to the size and cost of the system. More importantly in the above applications, R_L can change significantly during the operation while the optimal k_{34}, which depends on the geometries of L_3 and L_4 and their relative distance (d_{34}), can only be adjusted during the design and fabrication phase. Thus, 3- and 4-coil links cannot dynamically compensate for R_L variations during the system operation to maintain high PTE.

Alternatively, several groups have suggested to use off-chip matching circuits to transform R_L [26]–[28]. In [26] and [27], L-match networks with one inductor and one capacitor have been employed to match R_L to the optimal load. In [28], different types of matching networks, such as π, T, and L have been proposed for inductive links, and the L-match has been chosen due to its higher power efficiency. While R_L can be transformed by a simple L-match network, in practice, a network of capacitors and inductors is needed to dynamically tune a wide range of R_L during the operation. These are often off-chip due to the low-frequency operation of the inductive links (<20 MHz), which again adds to the size, cost, and power loss in the Rx.

In recent years, several groups including ours have proposed passive and active rectifiers to convert the AC voltage of the inductive link to DC with high power conversion efficiency (PCE) [29]–[33]. The PCE of a rectifier is defined as the ratio of the delivered power to the DC load at the output of the rectifier to the incoming AC power at the input of the rectifier. Power management integrated circuits (PMICs) have been presented to improve the PCE by employing threshold-voltage (V_{th}) cancelation or offset-controlled high-speed comparators [34], [35]. Recently, reconfigurable voltage rectifier/doubler (1X/2X) PMICs have been added to this collection to extend the range of inductive power transmission [36], [37]. While these methods can increase the PCE of the PMIC, none of them are equipped with automatic load transformation capability to dynamically optimize the PTE in the presence of R_L variations. There have also been some early studies to transform R_L by a DC-DC converter or controlling the phase shift of an active rectifier [38], [39]. However, these systems are not equipped with automatic load transformation circuitry to dynamically optimize the PTE in the presence of R_L variations during the system operation.

This was the motivation behind the Q-modulation technique, shown in Fig. 2(a), to enable adaptive and efficient WPT when R_L varies during operation [40]. The proposed Q-modulation technique utilizes two resonant coils for WPT. A novel aspect of the Q-modulation is the utilization of an on-chip switch across the Rx LC-tank to transform a wide range of R_L to the optimal load by changing the duty cycle, D. In this paper, we present the circuit theory behind the Q-modulation along with the design and measurement results of a fully integrated proof-of-concept Q-modulation power management (QMPM) ASIC. The Q-modulation theory is discussed in Section II followed by detailed description of the QMPM circuit in Section III. The QMPM ASIC characterization and measurement results are presented in Section IV, followed by the concluding remarks in Section V.

II. Q-Modulation Theory and Operation

In the proposed Q-modulation inductive link, shown in Fig. 2(a), the current in the series Rx L_3C_3-tank (I_3) is sampled, and a switch (SC) shorts it for the duration of T_{on} at the zero-crossings of I_3 once in every half-cycle of the power carrier $(T_p = 1/f_p)$. As shown in the switching diagram of Fig. 2(b), by closing SC during Φ_1 and shorting R_L as a result, the high-Q L_3C_3-tank stores the maximum energy (proportional to I_3) that is transferrable from the transmitter (Tx). During Φ_2, SC is opened and the L_3C_3-tank delivers its stored energy to R_L. Therefore, the amount of the transferred energy to R_L can be controlled by the SC duty cycle, $D = 2T_{\mathrm{on}}/T_p$.

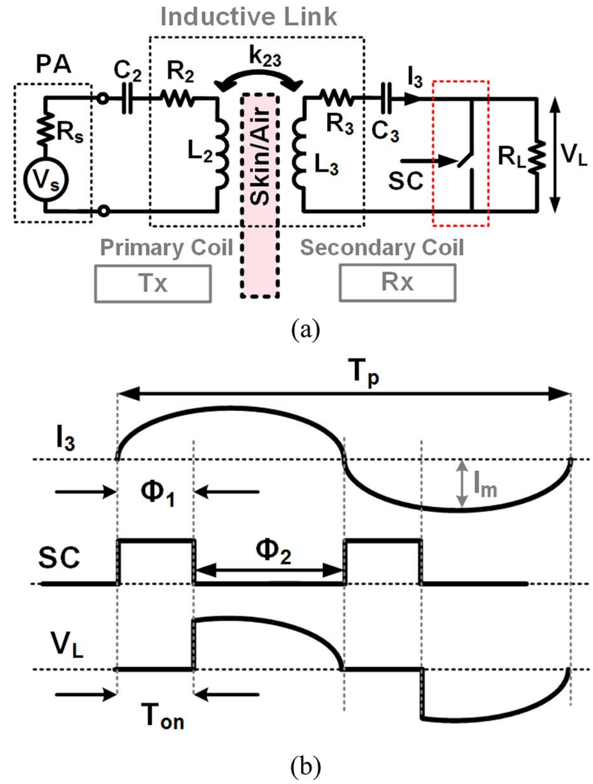


Fig. 2. (a) The circuit model of the proposed Q-modulation inductive link that chops the Rx L_3C_3-tank (shorts R_L) during Φ_1 by closing the SC switch to store maximum energy in the high-Q L_3C_3-tank, and then deliver that energy to R_L during Φ_2 when SC is open. (b) Switching waveforms to control Q_{3L} by changing the duty cycle of the SC signal, $D = 2T_{\mathrm{on}}/T_p$.

The equivalent loaded quality factor (Q) of the switched L_3C_3-tank in Fig. 2(a) can be found by calculating the ratio of the energy stored in the L_3C_3-tank to the average Rx power dissipation in the steady state:

$$Q_{3L,eq} = \omega_p \frac{0.5 L_3 |I_m|^2}{P_{Rsw} + P_{R3} + P_{RL}} \tag{1}$$

where I_m is the peak current in L_3, and P_{Rsw}, P_{R3}, and P_{RL} are the average power dissipations in the switch on resistance (R_{sw}), R_3, and R_L, respectively. $Q_{3L,eq}$ should be called the average loaded-Q of the L_3C_3-tank, as the tank is chopped periodically over time twice in every T_p. Since L_3 is always carrying a sinusoidal current (I_3) regardless of D, P_{R3} can be written as

$$P_{R3} = 0.5 R_3 |I_m|^2. \tag{2}$$

However, as shown in Fig. 2(b), I_3 flows in R_{sw} and R_L only for the durations of $2T_{\mathrm{on}}$ and $T_p - 2T_{\mathrm{on}}$ in every T_p, respectively. Therefore, P_{Rsw} and P_{RL} can be calculated by averaging the instantaneous power dissipations in R_{sw} and R_L within one carrier cycle:

$$\begin{aligned} P_{Rsw} &= R_{sw}|I_m|^2 \frac{\omega_p}{2\pi}\left[T_{\rm on} - \frac{1}{2\omega_p}\sin(2\omega_p T_{\rm on})\right] \\ &= 0.5 R_{sw}|I_m|^2 \left[D - \frac{1}{2\pi}\sin(2\pi D)\right] \\ P_{RL} &= R_L|I_m|^2 \frac{\omega_p}{2\pi}\left[\frac{\pi}{\omega_p} - T_{\rm on} + \frac{1}{2\omega_p}\sin(2\omega_p T_{\rm on})\right] \\ &= 0.5 R_L|I_m|^2 \left[1 - D + \frac{1}{2\pi}\sin(2\pi D)\right] \end{aligned} \tag{3}$$

where $\omega_p = 2\pi/T_p$. By substituting (2) and (3) in (1), the $Q_{3L,eq}$ can be written as

$$\begin{aligned} &Q_{3L,eq} \\ &= \frac{\omega_p L_3}{R_3 + R_{sw}\left[D - \frac{1}{2\pi}\sin(2\pi D)\right] + R_L\left[1 - D + \frac{1}{2\pi}\sin(2\pi D)\right]} \\ &= \frac{\omega_p L_3}{R_{3,eq} + R_{L,eq}} \end{aligned} \tag{4}$$

where $Q_3 = \omega_p L_3/R_3$ is the unloaded-Q of L_3, and $R_{3,eq}$ and $R_{L,eq}$ are the overall loss in the L_3C_3-tank with Q-modulation and transformed R_L, respectively. It can be seen from (4) that for $D = 0$ or 1, where only R_L or R_{sw} is connected to the L_3C_3-tank, $Q_{3L,eq} = \omega_p L_3/(R_3 + R_L)$ or $\omega_p L_3/(R_3 + R_{sw})$, respectively [25].

It can be concluded based on (4) that Q-modulation transforms R_L to

$$R_{L,eq} = R_L\left[1 - D + \frac{1}{2\pi}\sin(2\pi D)\right] \tag{5}$$

which can be adjusted by D. Fig. 3 shows that in (5) there is a monotonic relationship between $R_{L,eq}$ and D. The effect of R_{sw} in lowering the PTE has also been included in R_3 as

$$R_{3,eq} = R_3 + R_{sw}\left[D - \frac{1}{2\pi}\sin(2\pi D)\right]. \tag{6}$$

Therefore, the PTE derivation of the conventional 2-coil inductive link can be used to calculate the PTE of the Q-modulated inductive link in Fig. 2(a) by substituting $Q_{3L,eq}$ and $R_{L,eq}$ from (4) and (5) with the Q_{3L} and R_L of the 2-coil link [25]

$$\eta_{QM} = \frac{k_{23}^2 Q_2 Q_{3L,eq}}{1 + k_{23}^2 Q_2 Q_{3L,eq}} \cdot \frac{Q_{3L,eq}}{Q_{L,eq}} \tag{7}$$

where k_{23} is the mutual coupling between L_2 and L_3, $Q_2 = \omega_p L_2/R_2$, R_2 is the parasitic resistance of L_2, and $Q_{3L,eq}$ can be found form (4) for a given D [20]. $Q_{L,eq}$ in (7), which is often defined as the load-Q, can be written as

$$\begin{aligned} Q_{L,eq} &= \frac{\omega_p L_3}{R_{L,eq}} = \frac{\omega_p L_3}{R_L\left[1 - D + \frac{1}{2\pi}\sin(2\pi D)\right]} \\ &= \frac{Q_L}{\left[1 - D + \frac{1}{2\pi}\sin(2\pi D)\right]} \end{aligned} \tag{8}$$

where $Q_L = \omega_p L_3/R_L$ in the series L_3C_3-tank and $R_{L,eq}$ is the transformed load based on (5) for a given D [25]. Based on our prior work in [25], to achieve the maximum PTE for any given R_L:

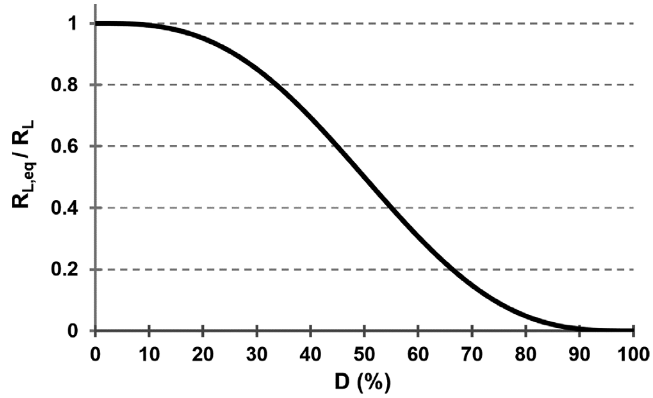


Fig. 3. The $R_{L,eq}/R_L$ vs. D based on (5) to show that there is a specific D for any given $R_{L,eq}$.

$$Q_{L,eq} = \frac{Q_3}{\left(1 + k_{23}^2 Q_2 Q_3\right)^{1/2}} = \frac{R_L Q_L}{R_3\left(1 + k_{23}^2 Q_2 Q_3\right)^{1/2}}. \tag{9}$$

Therefore, using (8) and (9) the optimal D for any given R_L and (L_2, L_3) coil geometries can be found from

$$1 - D + \frac{1}{2\pi}\sin(2\pi D) = \frac{R_3(1 + k_{23}^2 Q_2 Q_3)^{1/2}}{R_L}. \tag{10}$$

D is a dynamically adjustable degree of freedom in Q-modulated links that is not present in 3-coil inductive links during operation because the fixed d_{34} and geometries of L_3 and L_4 determine k_{34}. As a design example, the calculated PTE of the 3-coil link in Fig. 1, which has been optimized for $R_L = 10\ \Omega$, has been compared with that of the Q-modulated link in Fig. 2(a), assuming $R_{sw} = 0.5\ \Omega$. As shown in Fig. 4(a), the PTE of the 3-coil link is only maximum at the designated $R_L = 10\ \Omega$, where k_{34} is designed to be optimal, while the Q-modulated link can achieve high PTE for a wide range of R_L from 1 Ω to 100 Ω by adjusting D from 0 to 90%. For $R_L < 5\ \Omega$ the PTE of the Q-modulated link also drops due to the significant increase in the power loss of the L_3C_3-tank ($R_3 = 2\ \Omega$) compared to the load power, $\sim R_3/(R_3 + R_L)$. For $R_L > 5\ \Omega$, the power loss in the L_3C_3-tank is negligible. Fig. 4(b) shows the effect of R_{sw} on the calculated PTE of the Q-modulation link. The PTE reduces as R_{sw} increases, because the loss in the Q-modulation switch increases. Since the link has initially been optimized for $R_L = 10\,\Omega$, as R_L increases, D should also increase to improve the $Q_{3L,eq}$ in (4). Therefore, more power is dissipated in the switch and consequently the PTE drops. As a design guideline, the size of the switch should be chosen such that $R_{sw} < 0.1 R_3$ to achieve high PTE, at the cost of more chip area.

III. Q-Modulation Power Management Architecture

Fig. 5 shows the block diagram of a prototype QMPM ASIC, which was designed to operate at $f_p = 2$ MHz and demonstrate the functionality of the proposed Q-modulation technique. We chose f_p of 2 MHz in this proof-of-concept prototype to show the advantages of Q-modulation in improving PTE in the presence of R_L variations. However, standard f_p of 6.78 MHz or

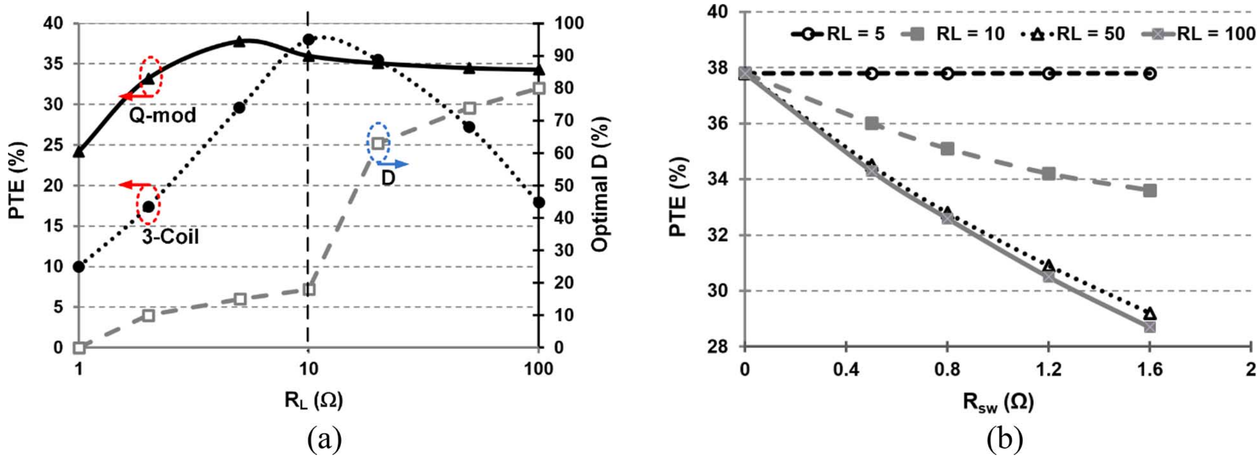


Fig. 4. (a) Comparing the calculated PTE vs. R_L for the 3-coil link in Fig. 1, which is optimized to match with $R_L = 10\ \Omega$ by setting k_{34}, and the Q-modulated link in Fig. 2(a) with $R_{sw} = 0.5\ \Omega$, which achieves higher PTE for all R_L values by adjusting D. (b) The calculated PTE of the Q-modulation link vs. R_{sw} for different R_L values at the optimal D. $Q_2 = 250$, $Q_{3,4} = 157$, $R_{3,4} = 2\ \Omega$, $k_{23} = 0.01$, and $k_{34} = 0.08$.

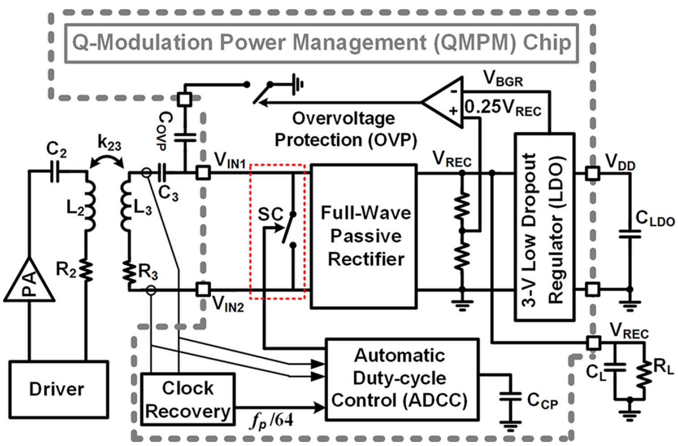


Fig. 5. Block diagram of the adaptive QMPM ASIC, which includes a full-wave passive rectifier, LDO, over-voltage protection, and ADCC circuitry to dynamically transform R_L during the operation.

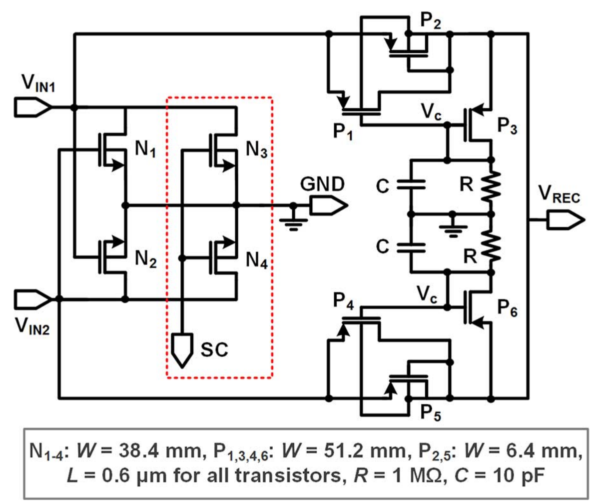


Fig. 6. Schematic diagram of the full-wave passive rectifier with V_{th}-cancellation scheme [34]. For Q-modulation, N_3 and N_4 transistors play the role of SC in Fig. 5 and short the Rx $\mathrm{L}_3\mathrm{C}_3$-tank.

13.56 MHz in the ISM band can be chosen in future implementations of the QMPM ASIC. This QMPM ASIC includes a full-wave passive rectifier, a 3 V low-dropout regulator (LDO), an automatic duty-cycle control (ADCC) to dynamically perform load transformation, and an over-voltage protection (OVP) circuitry. A class-E power amplifier (PA) with maximum output power of 8 W drives the Tx coil, L_2, at f_p. The AC signal across the Rx $\mathrm{L}_3\mathrm{C}_3$-tank is rectified and regulated to generate V_{REC} and $V_{DD} = 3$ V, respectively. The ADCC block controls SC during WPT operation and ensures that D for Q-modulation is set at its optimal value to maximize V_{REC} for any given R_L. For over-voltage protection, a hysteresis comparator detunes the $\mathrm{L}_3\mathrm{C}_3$-tank by adding a $C_{ovp} = 100$ nF when $V_{REC} > 4.8$ V.

Fig. 6 shows the schematic diagram of the full-wave passive rectifier, consisting of NMOS transistors $(\mathrm{N}_{1,2})$ for full-wave rectification and PMOS pass transistors $(\mathrm{P}_{1,2})$ equipped with V_{th}-cancellation circuit to reduce their dropout voltage and improve the PCE [34]. In this scheme, initially V_{REC} reaches $V_{IN1} - V_{\mathrm{th(P2)}}$ through P_2, leading to $V_C = V_{REC} - V_{\mathrm{th}(P3)} = V_{IN1} - 2V_{\mathrm{th(P2,3)}}$. Since $V_{SG(P1)} = V_{IN1} - V_C = 2V_{\mathrm{th(P2,3)}} > V_{\mathrm{th}(P1)}$, P_1 is pushed into triode, and V_{REC} is charged up until V_C becomes $V_{IN1} - V_{\mathrm{th(P1)}}$. Therefore, V_{REC} finally reaches $V_{IN1} - V_{\mathrm{th(P1)}} + V_{\mathrm{th(P3)}}$, which means that P_{1-3} play the role of a diode with a small effective voltage drop of $V_{\mathrm{th(P1)}} - V_{\mathrm{th(P3)}}$. This significant reduction in V_{th}, which also applies to P_{4-6}, improves the PCE. The size of $\mathrm{N}_{1,2}$ and $\mathrm{P}_{1,4}$ transistors (W) are chosen large enough ($W_{N1,2} = 38.3$ mm and $W_{P1,4} = 51.2$ mm) to minimize losses in the rectifier. For Q-modulation, the $\mathrm{L}_3\mathrm{C}_3$-tank ($V_{IN1,2}$ in Fig. 6) is shorted by $\mathrm{N}_{3,4}$ transistors, which are chosen large enough ($W_{3,4} = 38.4$ mm) to reduce the switch loss (R_{sw}) to 0.1 Ω, and improve the PTE, particularly when D is large [see Fig. 4(b)].

Fig. 7 shows the detailed schematic diagram of the ADCC block. By default, D is either gradually increased or decreased by controlling the reference voltage (V_{CP}) of the comparators of a mono-stable pulse generator that generates the SC signal. At the same time, the carrier envelope across the $\mathrm{L}_3\mathrm{C}_3$-tank (V_{ENV}) is continuously sampled and compared with its old value to detect whether V_{ENV} is increasing or decreasing due to

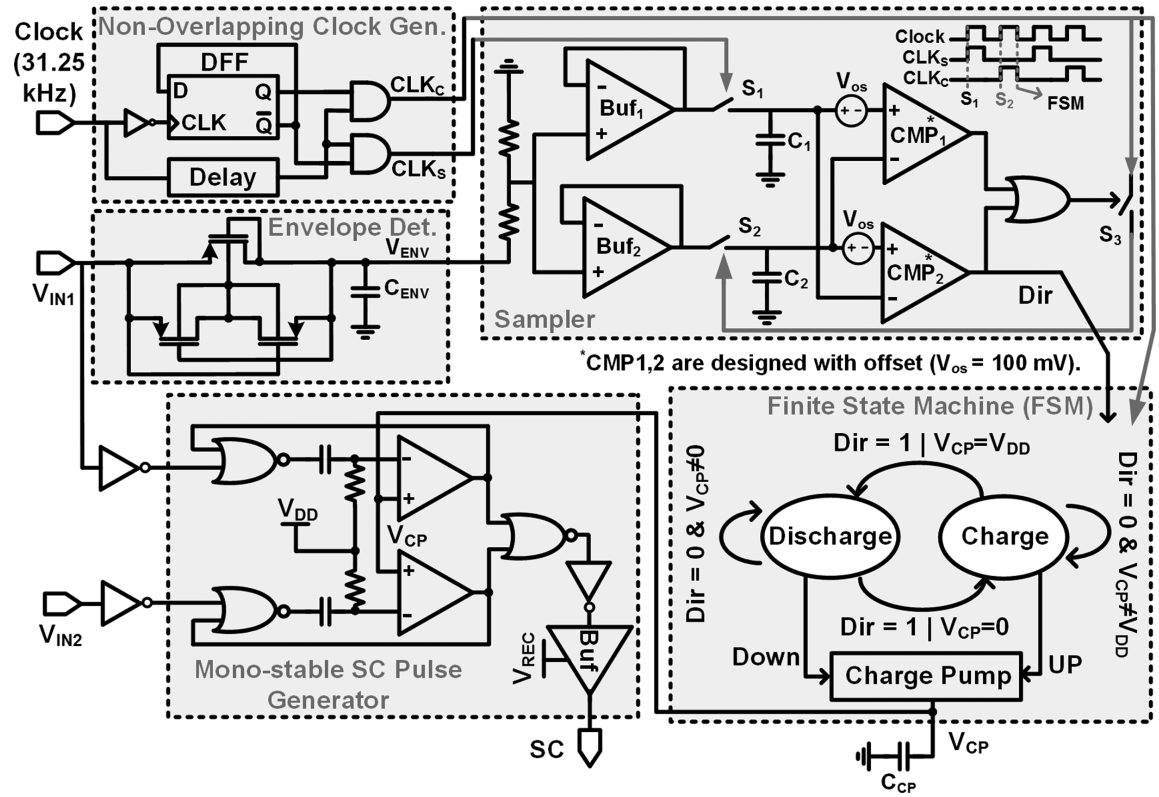


Fig. 7. Schematic diagram of the ADCC block in the QMPM ASIC for dynamic adjustment of D to achieve the highest PTE, corresponding to the highest V_{ENV}, for any given R_L.

the current status of D variation (i.e., increasing or decreasing). Based on this information, a finite state machine (FSM) controls a charge pump with the adjustable output voltage of $V_{\rm CP}$ to provide the optimal variations in D for increasing V_{ENV}. Upon startup, the FSM forces the charge pump to either charge or discharge its output capacitor, $C_{\rm CP} = 6$ pF, with 7 nA, and change D until V_{ENV} is reduced by 100 mV. Then, the charge/discharge state changes, resulting in V_{ENV} to increase till V_{ENV} reaches to its maximum by reaching the optimal R_L transformation condition. Then V_{ENV} reduces again by 100 mV when D deviates from the optimal condition. This up and down cycle ensures that V_{ENV} remains close to its peak value, maintaining the optimal load condition for achieving high PTE despite loading and coupling variations.

In the ADCC, V_{ENV} is first generated by a passive rectifier that operates as a fast-tracking envelope detector due to its small output capacitance ($C_{ENV} = 5$ pF), divided by 1.4, and then buffered before being sampled. A clock recovery block generates two non-overlapping clocks, $\rm CLK_C$ and $\rm CLK_S$, from a 31.25 kHz ($= f_p/64$). The first sampler, S_1, always samples V_{ENV} at the rising edge of $\rm CLK_S$, while S_2 only samples V_{ENV} at the rising edge of $\rm CLK_C$ when V_{ENV} increases or reduces by 100 mV. Thus, C_2 always holds the old value of V_{ENV}, which will be within a 100 mV difference from the current value of V_{ENV} sampled by S_1, and is updated to the current value of V_{ENV} only when V_{ENV} increases or reduces by 100 mV. This happens because $\rm CMP_{1,2}$, which are identical comparators with 100 mV offset, close S_3 and connect $\rm CLK_C$ to S_2 when the difference between sampled C_1 and C_2 voltages is $\pm$100 mV. In summary, these circuits continuously track V_{ENV} and detect a 100 mV decrease in V_{ENV} at the output of $\mathrm{CMP}_2(Dir)$. A high *Dir* signal warns FSM that the current state of D variations are not optimal. Thus, FSM changes the charge or discharge state of the charge pump to control D. Two inverters connected to the $\rm L_3C_3$-tank terminals (V_{IN1}, V_{IN2}) detect the zero-crossings of the V_{IN1} and V_{IN2} voltages, which are in sync with I_3. Therefore, the SC signal includes two pulses with variable pulse width $(T_{\rm on})$, determined by the comparators and $V_{\rm CP}$, starting at the zero-crossings of V_{IN1} and V_{IN2}.

IV. Measurement Results

The QMPM prototype ASIC, which specifications have been listed in Table I, was fabricated in a 0.35 μm 2P4M standard CMOS process, occupying 4.8 mm^2 of chip area, as shown in Fig. 8. Fig. 9 shows the QMPM experimental setup. The chip was wire bonded in a QFN package, mounted on a 2-layer FR4 printed circuit board (PCB). The geometries of Tx (L_2) and Rx (L_3) wire-wound coils (WWCs) in Fig. 9 were optimized to wirelessly transfer 400 mW to $R_L = 50\ \Omega$ from a nominal distance of $d_{23} = 8$ cm at $f_p = 2$ MHz [41]. The inductive link specifications are summarized in Table II. A class-E PA was designed to drive L_2 with adjustable output power of 100 mW to 8 W by controlling its supply $(\rm PA\_V_{DD})$ from 0.8 V to 10 V. For $R_L = 50\ \Omega$, the class-E PA was optimized to achieve a high efficiency of 92.8% at 2 MHz by zero-voltage switching of the $\rm M_1$ transistor (IRFR110) in Fig. 9 [42].

Fig. 10(a) shows the full-wave passive rectifier measured input and output voltage waveforms (V_{IN1} and V_{IN2} in Fig. 6)

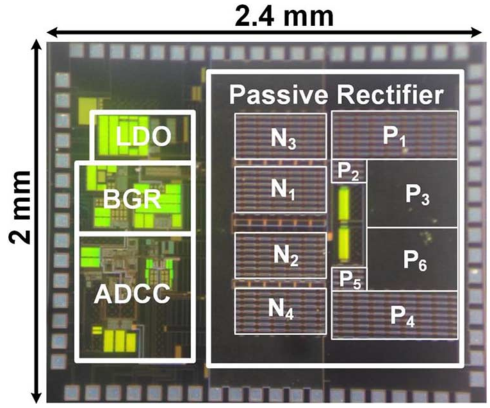


Fig. 8. QMPM chip microphotograph, occupying 4.8 mm² in TSMC 0.35 μm process.

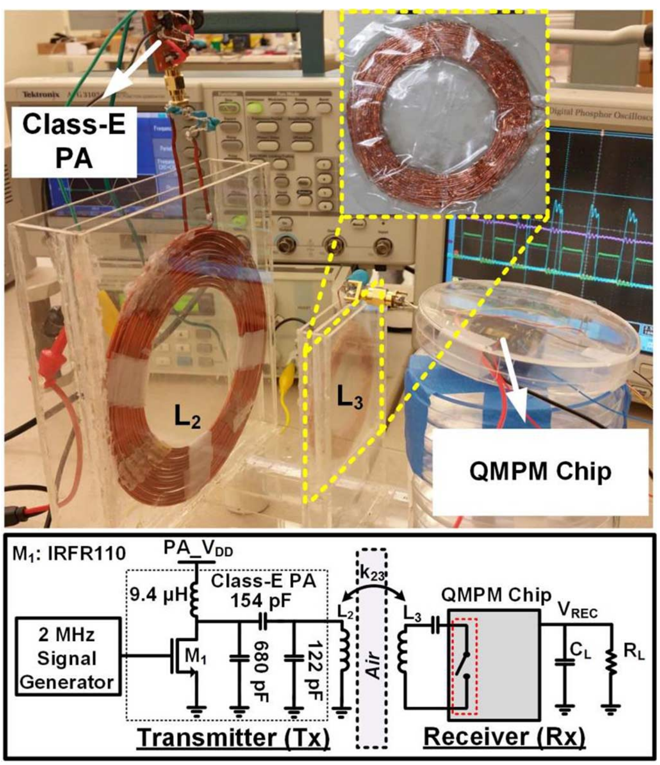


Fig. 9. The QMPM measurement setup showing Tx (L_2) and Rx (L_3) wire-wound coils (WWCs). A class-E PA was used to drive L_2 at 2 MHz with high efficiency, while L_2 was followed by the QMPM ASIC and $R_L = 100\,\Omega \| C_L = 4\,\mu$F loading.

without Q-modulation $(D = 0)$ when loaded by $C_L = 4\ \mu$F and $R_L = 100\ \Omega$, as well as the LDO output ($V_{DD} = 3$ V). Fig. 10(b) shows the rectifier measured PCE and output power (P_{out}) vs. R_L at 2 MHz for different V_{REC} values, which were set in our measurements by manually adjusting PA_V$_{\text{DD}}$. As R_L increases, the voltage drop across rectifier pass transistors, $P_{1,4}$ in Fig. 6, reduces, decreasing the rectifier power loss and increasing its PCE. At higher V_{REC} values, the PCE is slightly increased because the rectifier voltage drop is relatively smaller compared to V_{REC}. It can be seen from Fig. 10(b) that for a wide range of R_L and V_{REC}, the rectifier PCE is >70%. The maximum output power $(P_{\text{out,max}})$ of 1.45 W ($R_L = 15\ \Omega$ and $V_{REC} = 4.7$ V) was achieved with the PCE of 76%, while the

TABLE I
QMPM ASIC SPECIFICATIONS

Technology (TSMC)	0.35-µm 2P4M CMOS
Power Management supply voltage, V_{DD}	3 V
Nominal rectifier voltage, V_{REC}	4.5 V
Power carrier frequency, f_p	2 MHz
Duty cycle, D	10% - 70%
ADCC operating frequency	31.25 kHz
Static power consumption	300 µW
Maximum delivered power, $P_{out,max}$	1.45 W
Rectifier filtering capacitor, C_L	4 µF
Rectifier power conversion efficiency	76%
Die area	4.8 mm²

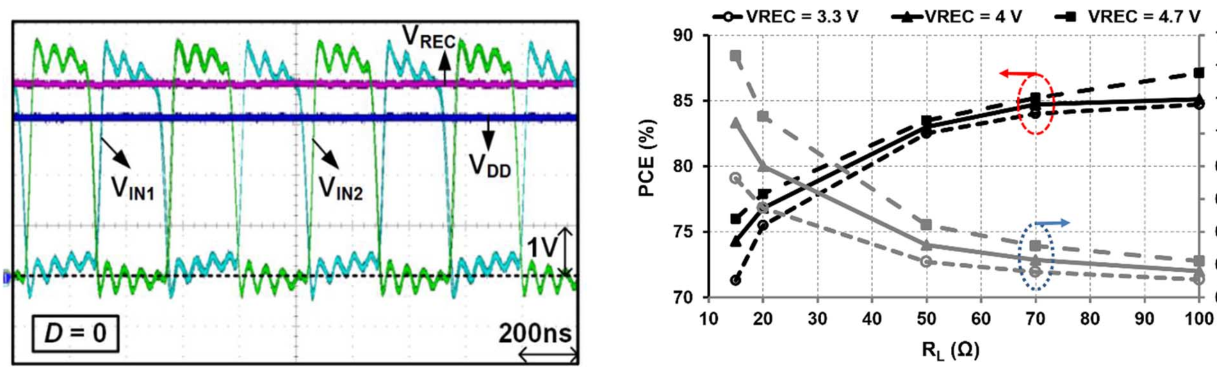
highest PCE was 87.1% at $V_{REC} = 4.7$ V with $R_L = 100\ \Omega$, corresponding to $P_{\text{out}} = 220$ mW.

Fig. 11 shows measured input and output waveforms of the rectifier at $d_{23} = 8$ cm, as well as the SC signal, generated by the ADCC block to perform dynamic Q-modulation. Fig. 11(a) shows the transient waveforms when R_L changed from 100 Ω to 200 Ω, resulting in an increase in V_{REC} from 3.6 V to 4.5 V. Figs. 11(b) and (c) show the steady-state waveforms witt $R_L = 100\ \Omega$ and 200 Ω, respectively. It can be seen that the ADCC block has automatically increased D from 24% to 45% to increase $Q_{3L,eq}$ in (4) by disconnecting $R_L = 200\ \Omega$ from the L_3C_3-tank for a longer period. Increasing $Q_{3L,eq}$ increases the reflected resistance at the output of the class-E PA and consequently reduces the inductive link input power [25]. The measured inductive link PTEs without and with the Q-modulation for $R_L = 200\ \Omega$ were 20.4% and 40.5%, respectively, which correspond to 98% improvement in the PTE, thanks to Q-modulation.

The measured waveforms in Fig. 11 also demonstrate the functionality and stability of the ADCC block. The reason for the larger ripple on V_{REC} in Fig. 11 (with Q-modulation) compared to Fig. 10(a) (without Q-modulation) is that the ADCC block chops the L_3C_3-tank twice in every carrier cycle. This high-frequency switching of large $N_{3,4}$ transistors by a buffer, which has been supplied by V_{REC}, as shown in Fig. 7, results in large instantaneous currents form V_{REC}, leading to more ripples. The increased ripple does not affect the system performance as long as the LDO output capacitor (C_{LDO} in Fig. 5) can filter the ripple. The power supply rejection ratio (PSRR) of the LDO can be further improved to oppose V_{REC} ripples [43].

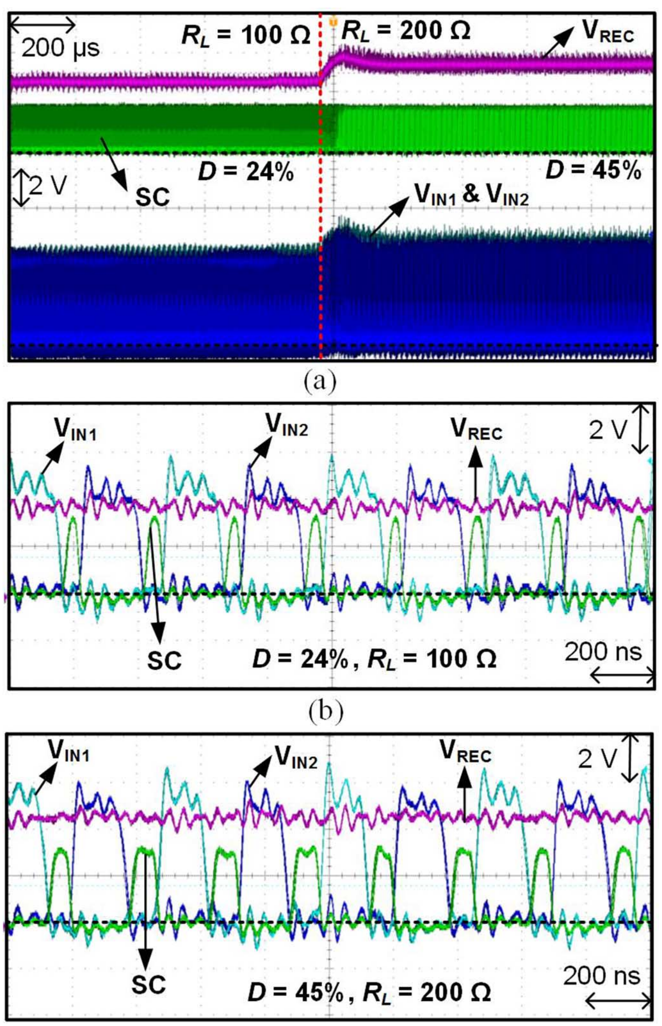
In order to evaluate the functionality of the ADCC block and measure its accuracy in finding the optimal D, the inductive link PTE and the overall system power efficiency ($\eta_{ov} = \eta_{\text{PA}} \times \eta_{\text{Link}} \times \eta_{REC}$), including the PA, inductive link, and rectifier efficiencies were measured vs. R_L and d_{23} in three different conditions: 1) without Q-modulation by keeping the SC switch in Fig. 5 open, 2) with Q-modulation by externally controlling the SC and manually adjusting D to maximize the PTE, using a square wave synchronized with the power carrier, and 3) with Q-modulation by dynamically controlling the SC, using the on-chip ADCC block.

Fig. 12(a) and (b) shows the measured inductive link PTE, η_{ov}, and the corresponding optimal D vs. different R_L values at $d_{23} = 8$ cm and $V_{REC} = 4.5$ V for the inductive link that has



(a) (b)

Fig. 10. (a) Measured input and output waveforms of the passive rectifier without Q-modulation ($D = 0$) at 2 MHz when loaded by $C_L = 4\ \mu$F and $R_L = 100\ \Omega$. The regulator output, $V_{DD} = 3$ V, has also been shown. (b) PCE of the rectifier vs. R_L for different V_{REC} values.



(c)

Fig. 11. Measured input and output waveforms of the rectifier with dynamic Q-modulation, provided by the ADCC block, generating the SC signal. (a) Transient waveforms when R_L changes from 100 Ω to 200 Ω, (b) steady state waveforms for $R_L = 100\ \Omega$, and (c) $R_L = 200\ \Omega$. The ADCC block has automatically increased D from 24% to 45% to improve the PTE by 98% compared to the same setup without Q-modulation ($d_{23} = 8$ cm).

been optimized for $R_L = 50\ \Omega$ (see specifications in Table II). By comparing the power efficiency and optimal D values for the external control and the ADCC, it can be seen that the ADCC has successfully found the optimal D for most R_L values with a maximum error of 21% in D at $R_L = 200\ \Omega$. Overall, Q-modulation has improved the PTE and η_{ov} by 98.5% (from 20.4% to 40.5%) and 120.7% (from 14.5% to 32%), respectively, by setting $D = 45\%$ at $R_L = 200\ \Omega$. It is interesting to note that at $R_L = 50\ \Omega$, the link has achieved the same efficiency with and without Q-modulation because the inductive link was originally optimized for this R_L value. A PTE drop of 20% can be seen at $R_L = 50\ \Omega$ with the ADCC operation, because the minimum D in the current QMPM ASIC was 10%, which is higher than the optimal value for this loading condition (for $R_L = 50\ \Omega$ the optimal D is zero). Nevertheless, the amount of efficiency improvement for $R_L > 50\ \Omega$ is significant using the dynamic Q-modulation with the ADCC block, which was not possible with other methods in the literature.

The higher η_{ov} compared to the inductive link PTE, 120.7% vs. 98.5%, shows that the Q-modulation technique has also helped in increasing the PA efficiency by ~12%. This is because with Q-modulation, the PA loading remains almost constant despite R_L variations. According to (4), when $Q_{3L,eq}$ is modulated by D, a relatively constant $Q_{3L,eq}$ is seen through the Tx coil, L_2, leading to a fixed reflected load at the PA output [25]. This is particularly important when class-E PAs are used to drive the inductive link because they are very sensitive to load variations [42].

Fig. 13(a) and (b) shows the measurement results of the inductive link PTE, η_{ov}, and the corresponding optimal D vs. d_{23} at $R_L = 100\ \Omega$ and $V_{REC} = 4.5$ V. Since k_{23} is inversely proportional to d_{23}, when d_{23} is increased, the ADCC block automatically increases D to compensate for the drop in k_{23} according to (9) and (10), and improve the power efficiency. It can be seen from the D values of the external manual control and the ADCC that this block has successfully found the optimal D for maximum power efficiency when $d_{23} \leq 8$ cm. However, for $d_{23} \geq 9$ cm the optimal D is higher in the ADCC compared to that of the external D control, resulting in less efficiency improvement. We suspect that this can be the result of larger ripples on V_{REC}, as well as the electromagnetic interference, which have affected the operation of the ADCC block in the current implementation, when the Tx coil is driven at a higher power level to deliver power across larger distances.

TABLE II
BENCHMARKING OF RECENT INDUCTIVELY POWERED POWER MANAGEMENT ASICs

Publication		2013 [9]	2011 [35]	2012 [36]	2013 [37]	**This Work**
CMOS Technology (μm)		0.35	0.5	0.5	0.35	**0.35**
f_p (MHz)		6.78	13.56	13.56	13.56	**2**
*V_{REC} (V)		5	3.1	3.1	4	**4.5**
$P_{out,max}$ (W)		6	20	0.037	0.032	**1.45**
*PCE (%)		86	80.2	77	84	**76**
L_2/L_3	Diameter, D_o (cm)	-	16.8 / 3	16.8 / 3	- / 1.8	**14 / 6.5**
	Wire width, w (mm)		-	-	-	**1.5 / 0.5**
	# of turns, n		2 / -	2 / -	-	**16 / 16**
	Quality factor, Q		-	-	-	**42.2 / 41.2**
	Inductance, L (μH)		0.88 / 0.41	0.88 / 0.41	-	**40 / 20**
Coils distance, d_{23} (cm)		< 1+	4	7	-	**8**
Coils coupling factor, k_{23}		-	-	-	-	**0.05**
*Overall efficiency (%)		55	-	-	-	**27**
Rectifier (1X)/Doubler (2X)		1X	1X	1X/2X	1X/2X	**1X**
Active/Passive		Passive	Active	Active	Active	**Passive**
Load matching		**No**	**No**	**No**	**No**	**Yes**

* For the maximum output power ($P_{out,max}$)
+From the measurement setup

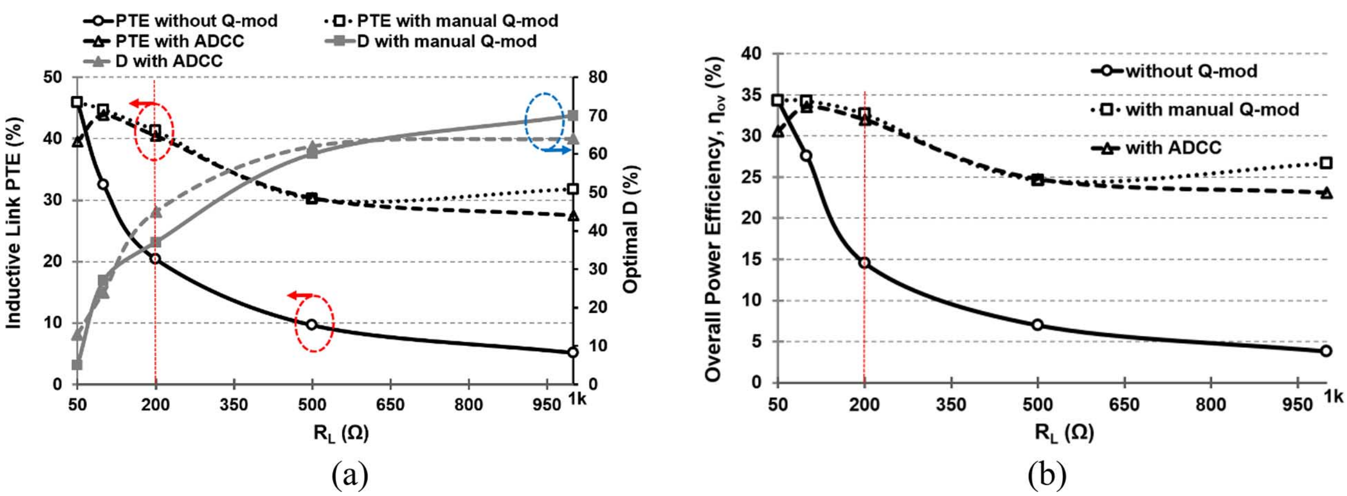


Fig. 12. Measured (a) inductive link PTE, and (b) overall system power efficiency (η_{ov}) vs. R_L with and without Q-modulation at $d_{23} = 8$ cm and $f_p = 2$ MHz. At $R_L = 200\ \Omega$, Q-modulation has improved the PTE of the inductive link and the overall efficiency for 98.5% and 120.7%, respectively.

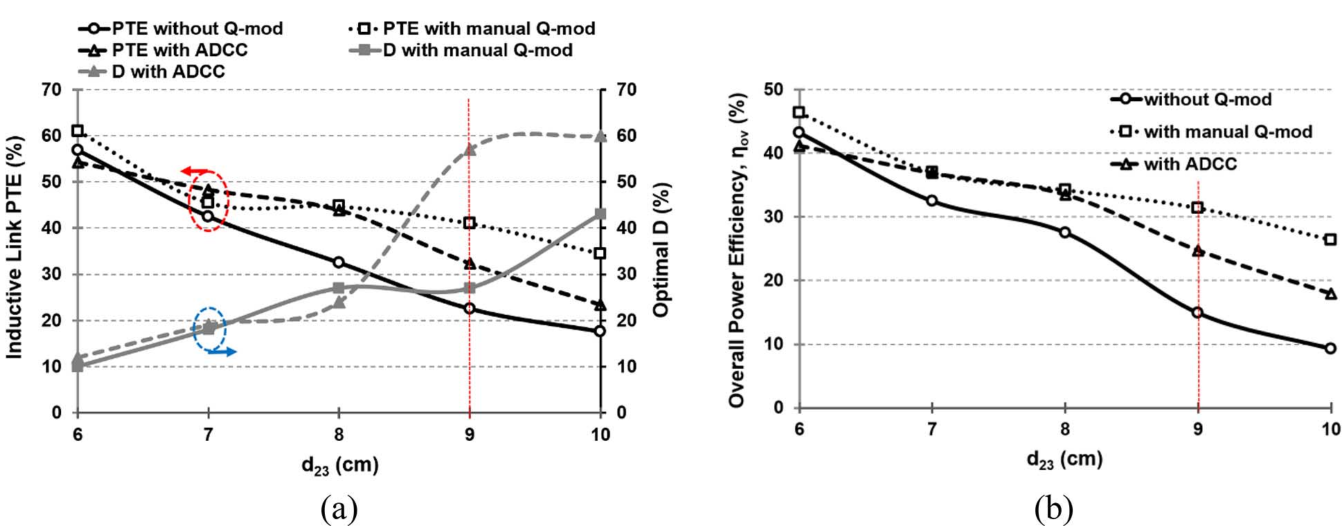


Fig. 13. Measured (a) inductive link PTE, and (b) overall system power efficiency (η_{ov}) vs. d_{23} with and without Q-modulation for $R_L = 100\ \Omega$ and $f_p = 2$ MHz. At $d_{23} = 9$ cm, Q-modulation has improved the PTE of the inductive link and the overall efficiency for 43.5% and 65.7%, respectively.

Nonetheless, Q-modulation with ADCC has improved the inductive link PTE and η_{ov} by 43.5% (from 22.5% to 32.3%) and 65.7% (from 14.9% to 24.7%) at $d_{23} = 9$ cm, respectively, by setting D at 57%.

Table II benchmarks the QMPM ASIC against recent inductive power management solutions in the literature. To best of our knowledge, QMPM offers the first integrated power management mechanism with dynamic load transformation, which is suitable for inductively-powered systems with variable loading and coupling distance. Using our proof-of-concept Q-modulation prototype, a DC power of 1.45 W was delivered across a 2 MHz inductive link with 8 cm coil separation at an overall power efficiency of 27%. Integrating the Q-modulation technique with active rectifiers and reconfigurable rectifiers/doublers promises considerable improvement in the next generation of highly efficient power management ASICs for a variety of WPT applications.

V. Conclusion

We have presented the theory, first ASIC implementation, and measurement results of the Q-modulation technique in inductive power transmission. The Q-modulation power management (QMPM) has enabled us to achieve dynamic load transformation during circuit operation, using an on-chip switch across the Rx LC-tank of the inductive link. It turns out that periodically chopping the received power carrier at every half cycle improves the PTE by increasing the loaded-Q of the LC-tank. The prototype QMPM ASIC includes an automatic duty-cycle control (ADCC) block that dynamically adjusts the switching waveform to maximize the rectifier output voltage. Our next goal is to improve the QMPM ASIC performance by adding the Q-modulation technique to active and reconfigurable rectifiers and migrating to smaller feature size processes with high-voltage option to further increase the overall system power efficiency, output voltage, and operating carrier frequency (e.g., 13.56 MHz).

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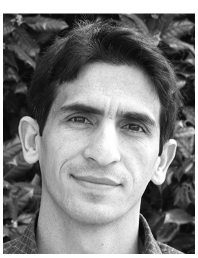

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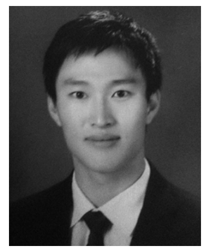

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