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# Solution-processed n-type fullerene field-effect transistors prepared using CVD-grown graphene electrodes: improving performance with thermal annealing†

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Solution-processed organic field effect transistors (OFETs), which are amenable to facile large-area processing methods, have generated significant interest as key elements for use in all-organic electronic applications aimed at realizing low-cost, lightweight, and flexible devices. The low performance levels of n-type solution-processed bottom-contact OFETs unfortunately continue to pose a barrier to their commercialization. In this study, we introduced a combination of CVD-grown graphene source/drain (S/D) electrodes and fullerene (C<sub>60</sub>) in a solution-processable n-type semiconductor toward the fabrication of n-type bottom-contact OFETs. The C<sub>60</sub> coating in the channel region was achieved by modifying the surface of the oxide gate dielectric layer with a phenyl group-terminated self-assembled monolayer (SAM). The graphene and phenyl group in the SAMs induced  $\pi$ - $\pi$  interactions with C<sub>60</sub>, which facilitated the formation of a C<sub>60</sub> coating. We also investigated the effects of thermal annealing on the reorganization properties and field-effect performances of the overlaying solution-processed C<sub>60</sub> semiconductors. We found that thermal annealing of the C<sub>60</sub> layer on the graphene surface improved the crystallinity of the face-centered cubic (fcc) phase structure, which improved the OFET performance and yielded mobilities of 0.055 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. This approach enables the realization of solution-processed C<sub>60</sub>-based FETs using CVD-grown graphene S/D electrodes *via* inexpensive and solution-process techniques.

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## 1. Introduction

Organic field-effect transistors (OFETs), which are compatible with low-temperature and solution processing methods, have received significant attention as key elements for realizing commercially viable all-organic electronics, including cheap, light, flexible, and large-area electronic products.<sup>1–3</sup> These advantages may be accessed primarily by depositing the organic semiconductors onto substrates using various solution processes including novel techniques (spin-coating, layer-by-layer, or Langmuir–Blodgett techniques).<sup>4–7</sup>

Numerous studies have attempted to rationally design solution-processable organic semiconductors composed of small molecules and polymers, such as triethylgermyl ethynyl-substituted anthradithiophene (diF-TEG ADT) or 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT), in an effort to achieve a high oxidation stability and good electrical performance.<sup>8,9</sup> Pentacene, fullerene (C<sub>60</sub>), and their derivatives have been extensively studied in small molecule semiconductors.<sup>10–12</sup> Among these, C<sub>60</sub> and its derivatives have been most attractive because of their good solubility in a variety of organic solvents.<sup>13,14</sup> However, the studies on the solution-processable C<sub>60</sub>-based FETs reported to date have focused only on the effects of surface modifications on the insulating layer and solvent dependence of the formation of a stable C<sub>60</sub> thin film, and the electron transfer properties.<sup>15–17</sup> As the field progresses, understanding the characteristics of electrode/semiconductor interfaces has become important because the crystallinity of the semiconductor deposited on electrodes may depend on the surface properties of the electrodes in a bottom-contact configuration. Source/drain (S/D) electrodes are typically patterned prior to the deposition of an organic semiconductor layer.<sup>18–20</sup> This configuration avoids damaging the organic semiconductor films during certain patterning processes.<sup>21</sup>

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† Electronic supplementary information (ESI) available: Optical microscopy images of the aggregated C<sub>60</sub> on aluminum electrodes, 2D-GIXD patterns of the C<sub>60</sub> films deposited onto graphene and thermally annealed at three different T<sub>A</sub> values (50, 90, or 130 °C), and width-normalized total resistance (R<sub>total</sub>W) values obtained from the C<sub>60</sub> FETs annealed at three different T<sub>A</sub> values as a function of the gate voltages are provided. See DOI: 10.1039/c4cp05787b

The development of appropriate S/D electrode materials is, therefore, vital. Metal S/D electrodes (e.g. gold, aluminum, and calcium) are typically used in OFETs, even though these electrodes have hydrophilic surfaces that can hinder uniform C<sub>60</sub> film formation via solution processing.<sup>22,23</sup>

CVD-grown graphene films have recently been considered as potential alternative S/D electrodes for use in OFETs due to their thinness, high electrical conductivity, and good oxidation/thermal stabilities.<sup>24–26</sup> The two-dimensionally flat sp<sup>2</sup> carbon network of a graphene film can interact with the molecules of a carbon-based organic semiconductor including C<sub>60</sub>.<sup>26–28</sup> This organic/organic interface between graphene and an organic semiconductor could reduce the contact resistance compared to the metal/organic semiconductor interface having high contact resistance due to the formation of an unfavorable interface dipole layer.<sup>20,29,30</sup> To enlarge the benefits of graphene S/D electrodes, it is necessary to investigate the growth behavior of C<sub>60</sub> molecules on graphene, and the ways to improve the crystalline morphology of C<sub>60</sub> on the graphene, with a goal to enhance device performance.

Here, we prepared the C<sub>60</sub> thin films deposited on graphene S/D electrodes using solution processing techniques toward the fabrication of bottom-contact OFETs for the first time. Moreover, we studied the effects of thermal annealing on the crystallinities, morphologies, and OFET performances of C<sub>60</sub> thin films on graphene. Uniform C<sub>60</sub> thin films may be obtained by treating the surfaces of the oxide dielectric layers with self-assembled monolayers (SAMs) that include terminal phenyl groups.<sup>31</sup> Higher annealing temperatures physicochemically reorganized the C<sub>60</sub> molecules and yielded their thin films on the graphene electrodes with better crystallinities and *fcc* structures.

The resulting OFETs exhibited high performances with an average mobility of 0.055 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> using the graphene S/D electrodes. This study enables the realization of C<sub>60</sub> bottom-contact FETs using CVD-grown graphene S/D electrodes via inexpensive and solution-process techniques.

## 2. Experimental section

The graphene was synthesized on a 25 μm thick copper foil using CVD methods at low pressures. The graphene layers were then transferred onto a pre-cleaned SiO<sub>2</sub>/Si substrate, as described previously.<sup>22,32</sup> The CVD-grown graphene was monolayer films with some existing bilayer island from the scanning electron microscopy image and Raman spectra, as shown in Fig. S1 in the ESI.†<sup>33,34</sup> The SiO<sub>2</sub>/Si substrate was cleaned by piranha treatment, followed by multiple DI water rinses and then further cleaned by exposure to UV-ozone (UVO) for 20 min. After thermal annealing above 350 °C for 1 h to obtain the cleaned graphene surface, the graphene was patterned by using standard photolithography. The device fabrication steps are briefly summarized in Fig. 1. A negative-type photoresist (PR) was spin-coated onto the graphene films and then exposed to UV light through a photo-mask. The PR was then washed away using a developer and DI water. All parts of the graphene films other than the part used as a S/D or contact electrode were not covered by the PR and were etched with the O<sub>2</sub> plasma. The phenyl group-terminated SAM treatment was accomplished by applying phenyltrimethoxysilane (PTS) (C<sub>6</sub>H<sub>5</sub>Si(OCH<sub>3</sub>)<sub>3</sub>, 97%, Aldrich Co.) to the 300 nm thick SiO<sub>2</sub>/Si substrates. The substrates were exposed to UVO for 10 min and then to PTS vapor at 140 °C for 40 min. The substrates were

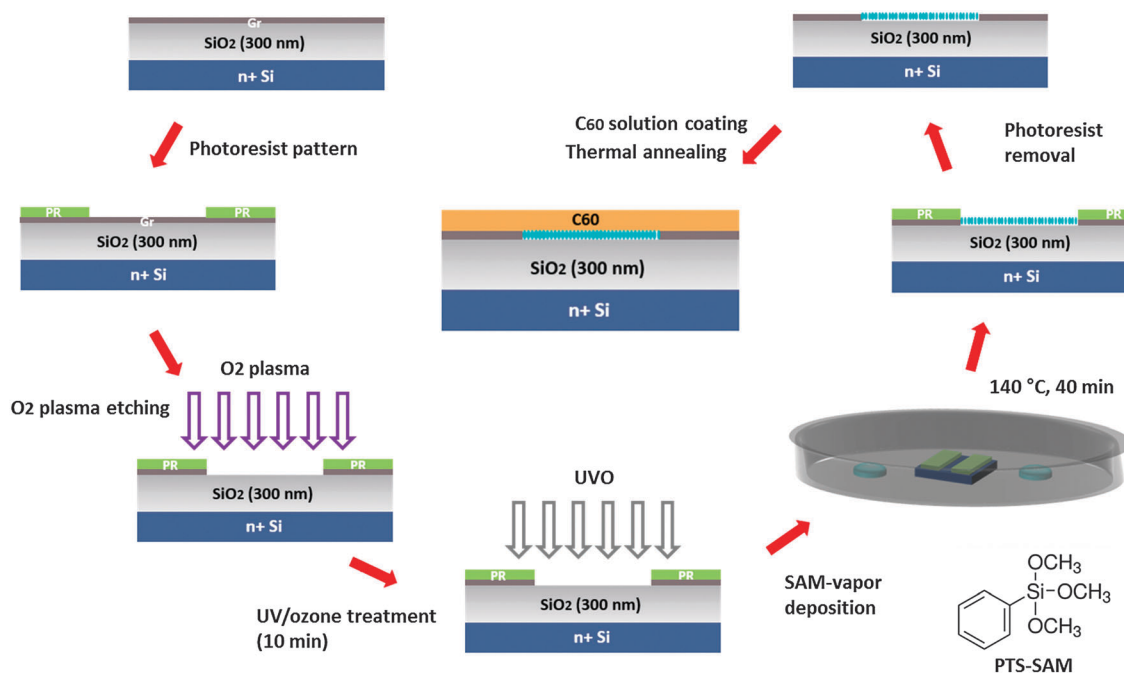


Fig. 1 Schematic illustration of the experimental procedure and sample structure used in this study. The lower right inset shows the chemical structures of phenyltrimethoxysilane (PTS).

then baked at 120 °C for 20 min. After the PR had been removed in a warm acetone solution (Fig. S2 shows the optical microscopy image of patterned graphene electrodes without contact pad, ESI†), a 0.6% C<sub>60</sub> solution in dichlorobenzene was spin-coated to cover the substrates with graphene S/D electrodes. The C<sub>60</sub> thin film coatings were thermally annealed at 50, 90, or 130 °C for 1 h and then were slowly cooled to room temperature in a vacuum chamber. The channel width (*W*) of the OFETs was 1000 μm, and the channel lengths (*L*) were 20, 50, 100, or 150 μm. The C<sub>60</sub> was spin-coated onto the substrates in a N<sub>2</sub>-rich glove box, and the other fabrication steps were performed in ambient air (RH: 40% ± 10%).

All electrical measurements were performed using a Keithley 4200 SCS in a N<sub>2</sub>-rich glove box. The morphologies of the C<sub>60</sub> films were investigated using atomic force microscopy (AFM, Multimode AFM, Digital Instruments), and their  $\theta$ -2 $\theta$  mode out-of-plane X-ray diffraction (XRD) patterns and two-dimensional grazing incidence wide-angle XRD (2D-GIXD) patterns were collected using a synchrotron X-ray beam source at the 5A and 3C beamline of the Pohang Accelerator Laboratory (PAL). The work functions of the graphene electrodes and the energy level alignment of the C<sub>60</sub>/graphene structures were investigated using ultraviolet photoelectron spectroscopy (UPS, beam diameter: 5 mm). The top-surface regions of the C<sub>60</sub> layers were cleaned using an Ar gas cluster ion beam sputtering process prior to the UPS measurements in order to remove air contamination and any oxidized C<sub>60</sub> layers. The optical band gap of C<sub>60</sub> was studied using reflective electron energy loss spectroscopy (REELS, using an electron gun and a photodetector manufactured by PSP Vacuum Technology Ltd.). The water contact angles were measured using SEO300A.

### 3. Results and discussion

The water contact angles ( $\theta_{\text{water}}$ ) on the UVO-exposed and PTS-modified SiO<sub>2</sub>/Si substrates (prepared using the vapor deposition method) were measured to confirm whether the substrates were effectively modified with PTS by the vapor deposition method. Fig. 2a shows the optical images captured while the water droplets were seeded onto the UVO- and PTS-modified SiO<sub>2</sub>/Si substrates. The values of  $\theta_{\text{water}}$  on the UVO-treated SiO<sub>2</sub>/Si substrates were less than 1°, whereas those obtained from the PTS-modified SiO<sub>2</sub>/Si substrates were found to be  $\sim 54 \pm 2^\circ$ , which are smaller than the values reported for the PTS-modified SiO<sub>2</sub>/Si substrates prepared using the solution dipping method.<sup>35,36</sup> In addition, the contact angle of dichlorobenzene on PTS SAM modified substrates had the value of  $\sim 11 \pm 2^\circ$  (Fig. S3, ESI†), in good agreement with the reported values.<sup>37</sup> These results suggested that the SiO<sub>2</sub>/Si substrate surfaces were effectively modified with the PTS-SAM.

The wettability of C<sub>60</sub> at the electrode and channel regions was examined by spin-casting 25 nm thick C<sub>60</sub> films onto the substrates bearing graphene S/D electrodes. The channel areas were modified with the PTS-SAM or were left unmodified. C<sub>60</sub> was only deposited onto the graphene electrodes in the

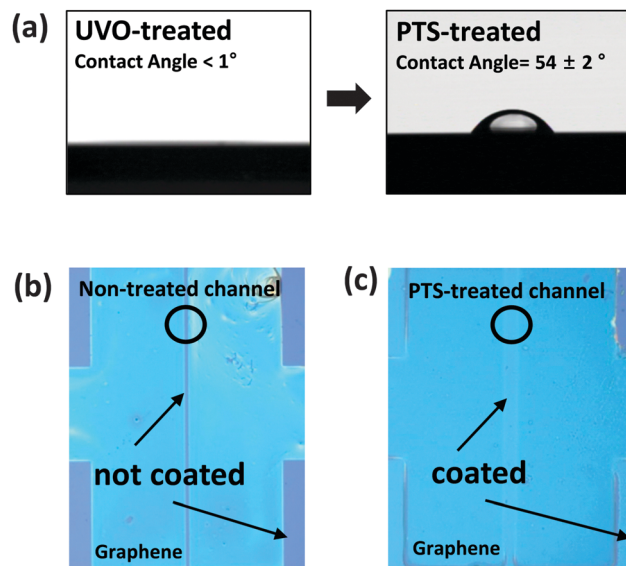


Fig. 2 (a) Optical images of the seeding water droplet on the UVO- and PTS-treated SiO<sub>2</sub>/Si substrates. Optical microscopy images of the C<sub>60</sub> thin film coatings deposited onto the patterned graphene electrodes, with an untreated channel (b), or with a PTS-treated channel (c).

substrate prepared without the PTS modification, and the C<sub>60</sub> layer was fully dewetted from the SiO<sub>2</sub> (Fig. 2b). By contrast, the PTS modification allowed C<sub>60</sub> to form a wetted film on the channel, leading to the successful deposition of C<sub>60</sub> films onto both the graphene and channel regions (Fig. 2c). These results may have been facilitated by  $\pi$ - $\pi$  interactions between the C<sub>60</sub> molecules and the two-dimensional carbon sheet formed by a honeycomb lattice of graphene and phenyl groups in the PTS-SAM.<sup>16,31</sup> In this way, it was possible to fabricate bottom-contact C<sub>60</sub> FETs using spin-coating techniques if the graphene and PTS-SAM were organized as an S/D electrode and a channel modifying layer, respectively. On the other hand, the metal electrodes prepared with aluminum could not be used in solution-processed C<sub>60</sub> FETs with a bottom-contact geometry because C<sub>60</sub> molecules were aggregated on the metal electrodes during the spin-coating process, as shown in Fig. S4 (ESI†).

High OFET performances require highly crystalline semiconductor thin films that favor effective charge transport and enhanced mobility.<sup>38</sup> Previous studies have used thermal treatment with heating around 100 °C to enhance the crystallinity of C<sub>60</sub> in a polymer gate dielectric, resulting in improved OFET performances.<sup>15</sup> In the present work, C<sub>60</sub> thin films deposited onto graphene were annealed at a variety of temperatures. AFM, XRD, 2D-GIXD, and UPS analyses were performed to examine the effects of thermal annealing on the crystalline morphology and electronic structure of the C<sub>60</sub> film on graphene, as well as to establish the optimal conditions (such as annealing temperature (*T<sub>A</sub>*)) for achieving a high OFET performance.

Fig. 3a–c show the AFM topography images and height profiles of C<sub>60</sub> thin films prepared on graphene S/D electrodes after thermal annealing at three different *T<sub>A</sub>* values of 50, 90, or 130 °C, respectively. The C<sub>60</sub> molecules in the films deposited on graphene formed a military topology of small ellipsoidal balls.

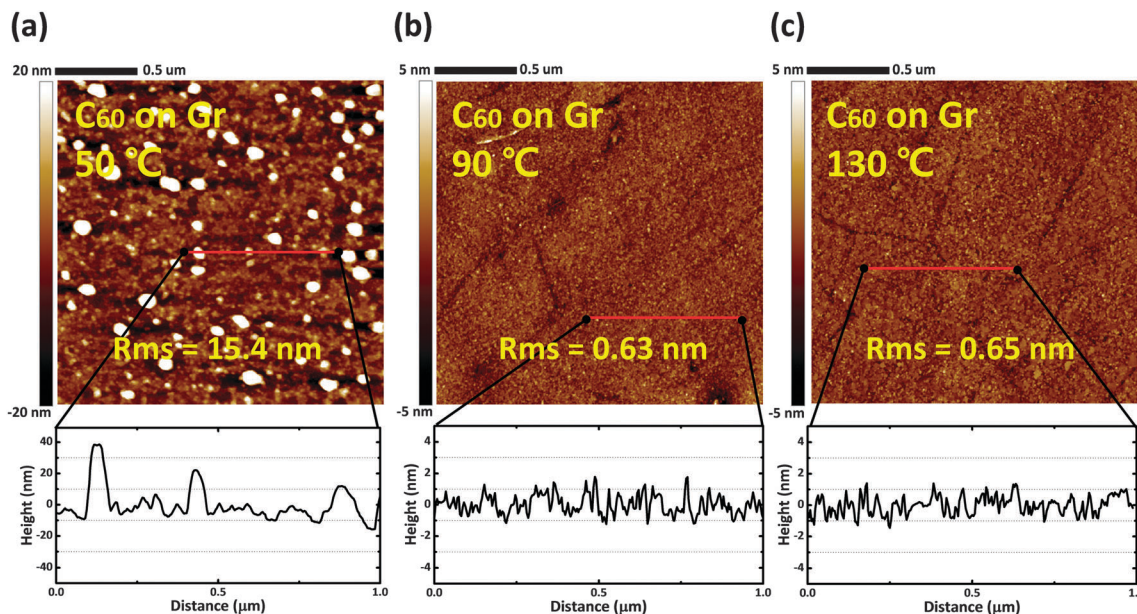


Fig. 3 AFM topography images of thermally annealed  $C_{60}$  films deposited onto a graphene electrode at (a) 50 °C, (b) 90 °C, or (c) 130 °C. The bottom graphs display the corresponding AFM cross-sectional height profiles of the  $C_{60}$  films.

Some of the  $C_{60}$  molecular bunches formed aggregates on the graphene electrode in the films that were thermally annealed at 50 °C, whereas the self-organized  $C_{60}$  molecules were present in the films deposited on graphene after thermal annealing at 90 or 130 °C. The rms roughness ( $R_{\text{ms}}$ ) of the  $C_{60}$  films annealed at 50 °C was much higher than the value obtained after annealing at 90 or 130 °C. The cross-sectional height profiles also revealed that the  $C_{60}$  layer formed a flat and smooth film on graphene after thermal annealing at 90 or 130 °C, whereas some  $C_{60}$  molecules were aggregated to form 20–40 nm thick bunches on graphene after thermal annealing at 50 °C.

In addition to the morphological studies conducted using AFM analysis, we also investigated the X-ray diffraction patterns to analyze the crystalline structure of the  $C_{60}$ /graphene bilayer. Fig. 4a shows the  $\theta$ - $2\theta$  mode out-of-plane XRD patterns obtained from the thermally annealed  $C_{60}$  films deposited onto graphene at various  $T_A$  values. As shown in the XRD patterns, the out-of-plane XRD peak intensity obtained from the  $C_{60}$  film annealed at 130 °C was much higher than the corresponding peaks in films annealed at 50 °C or 90 °C, suggesting better crystallinity along the out-of-plane direction as a result of thermal annealing at high  $T_A$ . The intense peak at  $q_z = 0.75 \text{ \AA}^{-1}$  and the small peak at  $q_z = 1.52 \text{ \AA}^{-1}$  in the out-of-plane XRD patterns obtained from a  $C_{60}$  thin film corresponded to the (111) and (311) reflections, respectively. Previous studies revealed that the  $C_{60}$  crystals formed a face-centered cubic (*fcc*) phase structure.<sup>15,17,39</sup>

The relationship between the crystallinity and  $T_A$  was further explored and an in-depth analysis of the crystalline structure of the  $C_{60}$  thin films prepared on graphene was conducted by collecting 2D-GIXD measurements. Fig. S5a–c (ESI†) show the 2D-GIXD patterns obtained from a  $C_{60}$  layer annealed at various  $T_A$ . The 2D-GIXD patterns obtained from the  $C_{60}$  film annealed

at 130 °C displayed reflection spots with apparent intensities that were higher than those obtained from other patterns, strongly suggesting that the  $C_{60}$  molecules formed more extensive crystal structures as  $T_A$  increased, in good agreement with the XRD analysis.

The hypothesis described above, that the  $C_{60}$  crystals formed an *fcc* phase structure, was tested by indexing the 2D-GIXD patterns collected from  $C_{60}$  films deposited onto graphene and thermally annealed at 130 °C. The measured patterns were compared with  $C_{60}$  *fcc* reference patterns reported in previous studies, as shown in Fig. 4b.<sup>40–42</sup> The lower spectrum shown in Fig. 4b reveals the integrated GIXD intensity in the in-plane direction. All structural information collected from the XRD and 2D-GIXD profiles indicated that the crystalline growth in the  $C_{60}$  films formed an *fcc* phase structure on graphene. Some peaks were absent, and even the 2D-GIXD profile peaks observed in Fig. 4b had lower intensities than the corresponding peaks obtained from reference *fcc*  $C_{60}$  structures. Because film formation *via* solution processing may be disrupted by the presence of solvent molecules, solution-deposited  $C_{60}$  molecules formed random crystalline domains more frequently than did  $C_{60}$  molecules deposited through vacuum evaporation processes.

The electron injection barrier at the  $C_{60}$ /graphene interface was examined by collecting UPS spectra and performing REELS analyses of the  $C_{60}$ /graphene structures annealed at different  $T_A$ . Fig. 5a–c show the UPS spectra (secondary cut-off and valence band region) and REELS spectra of  $C_{60}$ /graphene films annealed at different  $T_A$ . The graphene layers examined here were thermally treated at 350 °C for 1 h to remove the polymer residue that remained after the transfer process. In general, thermal treatment of transferred graphene induced charge transfer between graphene and  $\text{SiO}_2$ , which resulted in p-type

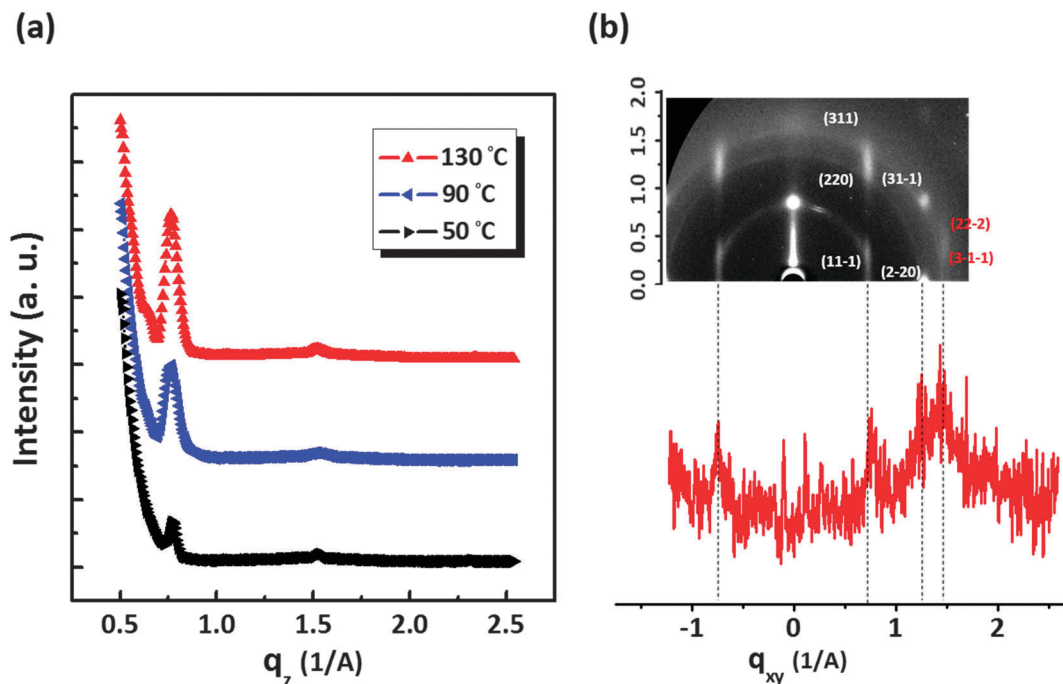


Fig. 4 (a)  $\theta$ - $2\theta$  mode out-of-plane XRD profiles of thermally annealed  $C_{60}$  films deposited onto graphene electrodes at different  $T_A$  ( $\lambda = 1.07$  Å). (b) 2D-GIXD patterns of the  $C_{60}$  films deposited onto graphene and thermally annealed at 130 °C, indexed according to the  $C_{60}$  fcc phase structure. The bottom graph displays the corresponding in-plane profiles extracted from the 2D-GIXD pattern obtained from a  $C_{60}$  film.

graphene doping.<sup>26</sup> Therefore, the work functions of the thermally annealed graphene films were found to be 4.81 eV evaluated from the UPS data (Fig. 5a). The vacuum level shift and electron injection barrier ( $\Phi_{E,B}$ ) between  $C_{60}$  and graphene were calculated using the UPS and REELS spectra.  $\Phi_{E,B}$  was calculated from the difference between the lowest unoccupied molecular orbital (LUMO) level of  $C_{60}$  and the Fermi energy level ( $E_f$ ) of graphene. This value also corresponded to the difference between the band gap ( $E_g$ ) and the hole injection barrier ( $\Phi_{H,B} = E_{HOMO} - E_f$ , where HOMO refers to the highest occupied molecular orbital). The band gap of the  $C_{60}$  film deposited onto each sample was measured directly from the electron energy level difference between the zero-energy loss position and the onset of the minimum energy loss peak in the REELS spectra.<sup>43,44</sup> Although the band gap of an organic semiconductor measured using REELS data is generally lower than the corresponding transport band gap due to the exciton binding energy difference,<sup>43,44</sup> the band gap obtained using the REELS technique, which is relatively insensitive to the substrate-induced charge carrier concentration, was used to characterize the electron injection barrier at the  $C_{60}$ /graphene interface. Despite the crystallinity differences among the  $C_{60}$  films annealed at different  $T_A$  values, the UPS and REELS spectra, which queried the electronic structures of both the occupied and unoccupied states, gave nearly identical energy distributions. Highly crystalline organic semiconductor films can reduce the exciton binding energy by the scale at mere tens meV due to the weak intermolecular van der Waals interactions.<sup>45</sup> For these reasons, the  $C_{60}$  films prepared at different  $T_A$  have no distinction in the band gap energies.

The UPS and REELS spectra of the annealed  $C_{60}$  film coatings on graphene were used to generate the schematic diagrams of the energy bands at the  $C_{60}$ /graphene interfaces, as shown in Fig. 5d-f. As  $T_A$  increased from 50 °C to 130 °C, the vacuum level shift increased from 0.16 eV to 0.23 eV, whereas  $\Phi_{E,B}$  decreased slightly from 0.26 eV to 0.19 eV. The changes in the vacuum level shift and  $\Phi_{E,B}$  with  $T_A$  were attributed to the crystalline morphologies of the  $C_{60}$  films deposited on graphene and annealed at different  $T_A$  values.<sup>46</sup> These results demonstrated that carrier injection could be facilitated in OFETs by reducing the electron injection barrier from graphene to  $C_{60}$  after thermal annealing at high  $T_A$ .

The CVD-grown graphene films were used as S/D electrodes and the  $SiO_2$  surface was modified with a PTS-SAM to enable the fabrication of solution-processed  $C_{60}$  FETs prepared using a bottom-contact geometry, as shown in Fig. 6a. The device characteristics, determined by measuring the electrical properties of the OFETs, were examined in three different  $C_{60}$  FETs prepared under various  $T_A$  values to investigate the effects of thermal annealing of the spin-coated  $C_{60}$  films. Fig. 6b and c show, respectively, the transfer and output characteristics of the OFETs. The field-effect mobility ( $\mu$ ) in the saturation regime (drain voltage,  $V_D = 80$  V) was calculated from the slope of the square root drain current ( $I_D^{1/2}$ ) versus the gate voltage ( $V_G$ ) using the following equation:

$$I_D = \frac{\mu C_i W}{2L} (V_G - V_{th})^2 \quad (1)$$

where  $C_i$  is the capacitance per unit area of the gate dielectric ( $\approx 10$  nF cm<sup>-2</sup>) and  $V_{th}$  is the threshold voltage. The electrical

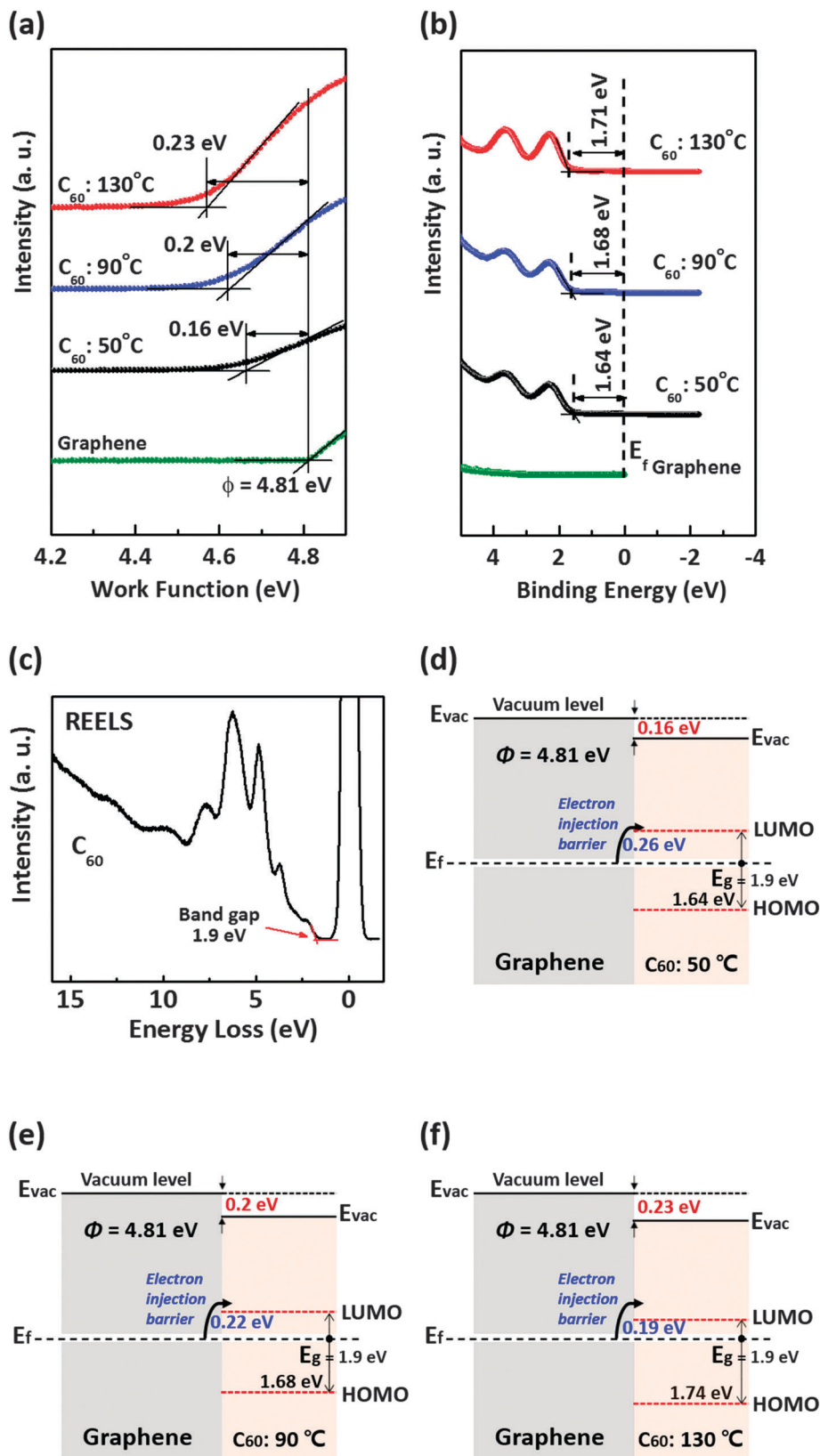


Fig. 5 Comparative UPS spectra showing the secondary cutoff region (a) and valence regions (b) of  $C_{60}$ /graphene films annealed at different  $T_A$  (50, 90, or 130 °C). (c) REELS spectrum of a  $C_{60}$ /graphene film. Schematic energy diagram of the  $C_{60}$ /graphene film interface after annealing at (d) 50 °C, (e) 90 °C, or (f) 130 °C, including the work function of the graphene films, the HOMO and the LUMO levels, the electron injection barriers, and the vacuum level shift. The electron injection barriers between graphene and the thermally annealed  $C_{60}$  films were calculated from the UPS and REELS spectra.

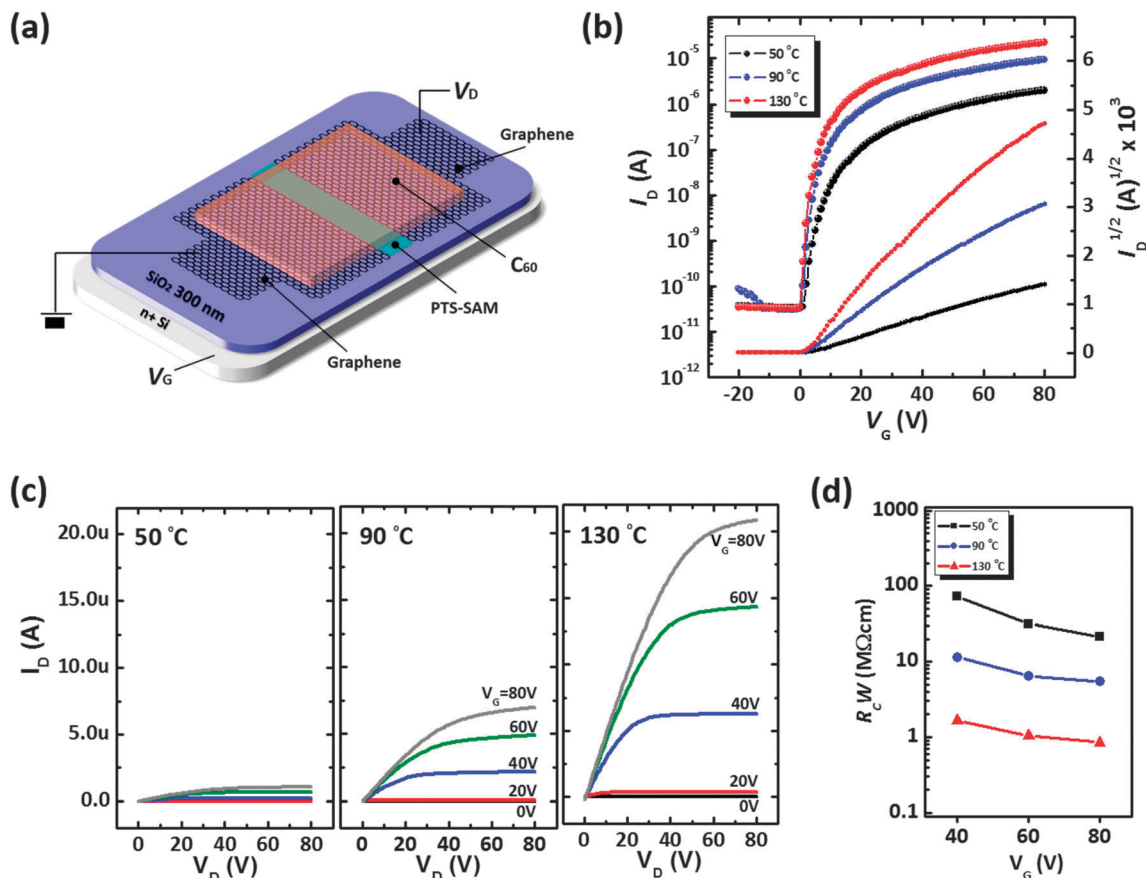


Fig. 6 (a) Schematic illustration of a bottom-contact  $C_{60}$  FET prepared using graphene S/D electrodes in this study. (b) Transfer characteristics in the saturation regime ( $V_D = 80$  V), and (c) output characteristics of three types of  $C_{60}$  FETs prepared using graphene S/D electrodes and thermally annealed at various  $T_A$  values (50, 90, or 130 °C). The channel lengths ( $L$ ) and widths ( $W$ ) of the OFETs were 100 and 1000  $\mu\text{m}$ , respectively. (d) The  $R_cW$  values for three types of  $C_{60}$  FETs prepared using graphene S/D electrodes, as a function of the  $V_G$  values.

Table 1 Electrical characteristics of the  $C_{60}$  FETs prepared using graphene S/D electrodes and thermally annealed at various  $T_A$  values (50, 90, and 130 °C)

$T_A$ [°C]	$\mu$ [ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ]	$V_{\text{th}}$ [V]	$I_{\text{on/off}}$	SS [ $\text{V dec}^{-1}$ ]
50	$0.002 \pm 0.001$	2.93	$\sim 10^4$	-3.45
90	$0.027 \pm 0.002$	3.20	$\sim 10^5$	-3.88
130	$0.055 \pm 0.004$	2.39	$\sim 10^6$	-3.28

characteristics of the OFETs are summarized in Table 1. As  $T_A$  increased, the resulting  $C_{60}$  FETs showed higher mobilities and on-state currents, demonstrating that high  $C_{60}$  crystallinity improved the OFET performance. The  $C_{60}$  FET devices that were thermally annealed at 130 °C exhibited the highest electrical performances, with an average  $\mu$  of  $0.055 \pm 0.004 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  and an on/off ratio of  $10^6$ .

The origin of these field-effect mobility variations was investigated by calculating the contact resistance of each device using the transfer-line method.<sup>21,47</sup> The total width-normalized resistances ( $R_{\text{total}}W$ ) were determined from the inverse slope of the  $I$ - $V$  curve for each device ( $W = 1000 \mu\text{m}$  and  $L = 20, 50, 100, 150 \mu\text{m}$ ) in the linear regime at each gate voltage (Fig. S6, ESI†).

The  $R_{\text{total}}W$  value could be expressed as

$$R_{\text{total}}W = R_cW + \frac{L}{\mu C_i (V_G - V_{\text{th}})} \quad (2)$$

where  $R_cW$ ,  $\mu$ , and  $V_{\text{th}}$  are the width-normalized contact resistance, intrinsic field-effect mobility, and threshold voltage, respectively. Therefore,  $R_cW$  could be approximated based on the y-intercept of the linear extrapolation of the plots of  $R_{\text{total}}W$  versus channel length ( $L$ ). Fig. 6d plots the width-normalized contact resistances ( $R_cW$ ) of these OFETs under various gate voltages. It should be noted that the  $C_{60}$  FET devices thermally annealed at 130 °C showed the smallest contact resistances between the electrode and the active layer. These results demonstrated that highly crystalline  $C_{60}$  films formed on the graphene S/D electrodes and a small charge injection barrier in  $C_{60}$ /graphene led to a small  $R_cW$ , which enhanced the OFET performance. Because thermal annealing also increased the crystallinity of  $C_{60}$  in the channel area,<sup>15</sup> the channel resistance may also be reduced by thermal annealing. Therefore, we believed that reductions in both the contact and channel resistances contributed to the high OFET performances in  $C_{60}$ -based FETs.

## 4. Conclusions

In conclusion, we realized solution-processable C<sub>60</sub>-based bottom-contact OFETs for the first time by using CVD-grown graphene as the S/D electrodes. C<sub>60</sub> was effectively spin-coated onto graphene, which formed stabilizing  $\pi$ - $\pi$  interactions, whereas the film was not spin-coated onto the metal electrodes. In the channel region, the phenyl group of the SAM formed  $\pi$ - $\pi$  interactions with the C<sub>60</sub> molecules, which further stabilized the C<sub>60</sub> coating and enabled OFET preparation. We found that the thermally annealed C<sub>60</sub> films on graphene displayed surprisingly good crystallinities and low electron injection barriers between the graphene and C<sub>60</sub>, leading to effective charge injection and transport. The resulting devices exhibited field effect mobility values up to 0.055 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> with high on/off ratios exceeding 10<sup>6</sup>. These results constitute significant progress toward the realization of all-organic integrated devices based on CVD-grown graphene electrodes prepared using inexpensive and simple fabrication techniques.

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