

Circuit Model Analysis for Traces that Cross a DGS

Kibum Jung¹ · Jongkyung Lee¹ · Yeon-Choon Chung² · Jae-Hoon Choi³

Abstract

This paper presents a novel modeling technique for traces that cross a defected ground structure. A simple and accurate equivalent circuit model provides clear insight into the coupling mechanism between a microstrip line and a slot or split. The circuit models consist of a transformer as the coupling mechanism and LC resonators as the ground with a slot or split structure. Resistors, capacitors, and inductors are added to the model to increase accuracy and equivalence at high frequency. Simulated and measured S -parameters are presented for defected ground structures. The accuracy and validity of the proposed equivalent circuit model is verified by evaluation of the S -parameter characteristics of the defected ground structures and comparison with measured results.

Key words: Circuit Model, Defected Ground Structure (DGS).

I. Introduction

Recently, interest in defected ground structures has grown among EMC engineers. A common practice is to introduce slots or splits in the power/ground planes in high-speed/below 1 GHz printed circuit boards (PCBs) designed for automotive uses. In mixed signal circuits, a slot/split in the power/ground plane can isolate a sensitive analog circuit from a noisy digital circuit. Slots/splits in the power/ground planes are also employed in PCBs with multiple power supplies, in order to provide DC isolation among different supplies and suppression noise filters for common-mode [1]. However, power/ground partitioning generates undesired electromagnetic effects such as signal integrity (SI) degradation, electromagnetic interference (EMI), and generalized cross-talk [2]. Stitching or AC-shorting the slot with capacitors under or near the traces improves the cross-talk immunity and SI/EMI problems [3].

In this paper we propose a simple and accurate equivalent circuit model that provides clear insight into the coupling mechanism between the microstrip line and the slot or split in the ground plane. This model provides a physical understanding of the problem of the defected ground structures (DGS), and hence it provides new insights into the operation of the DGS.

II. Circuit Model for Traces That Cross a Defected Ground Structure

The proposed defected ground structures are shown in Fig. 1. The structure under consideration is a microstrip line on the top surface of a dielectric substrate that has a slot or a split on a ground plane.

Table 1 shows the geometrical parameters. The microstrip line has a width of 2.85 mm to ensure that the characteristic impedance of the structure is approximately 50 [Ω] at 1 GHz.

In these models, the microstrip line and ground plane are made of copper and the permittivity of the dielectric substrate is 4.8. The microstrip line was driven at one end and terminated with a 50 [Ω].

When current is flowing through the microstrip line

Table 1. Parameters for the geometry under consideration.

Parameter	Value	Description
W_m	2.58 mm	Trace width
W_s	1.5 mm	Slot/split width
L_s	26 mm	Slot/split length
h	1.6 mm	PCB height
ϵ_r	4.8	Relative permittivity

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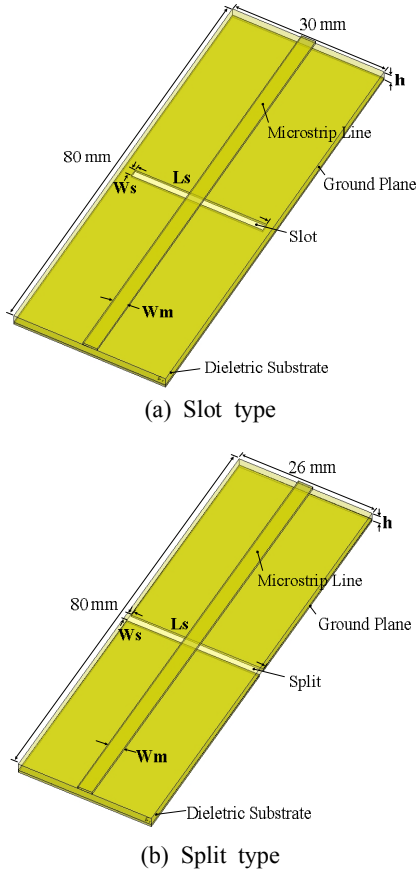


Fig. 1. The proposed defected ground structures.

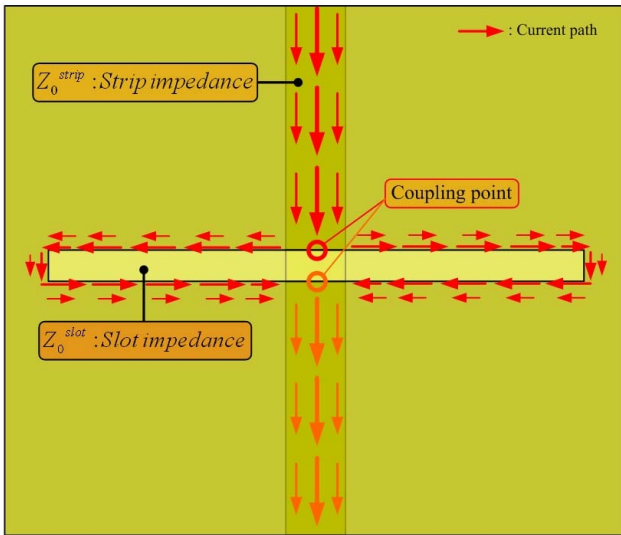


Fig. 2. Current paths on defected ground structure.

signal trace, across the defected ground, the current is generated along the periphery of the slot due to the coupling between the microstrip line and the DGS, as shown in Fig. 2.

2-1 Equivalent Circuit Model for a DGS

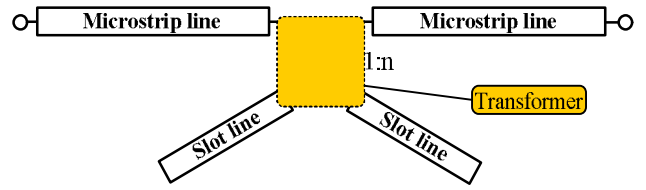


Fig. 3. Equivalent circuit model for coupling mechanism.

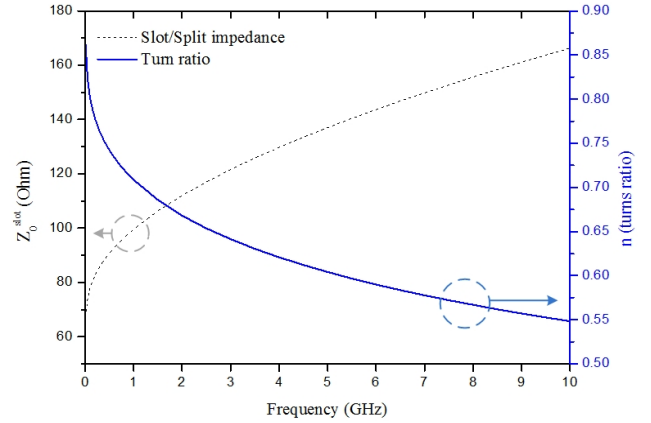


Fig. 4. Determination of the turn ratio, n , for the transformer.

The coupling between the trace and the DGS is due to magnetic field coupling. We can therefore represent this coupling using a mutual inductance. The defected ground structure and the trace can also be considered as a slot line and a microstrip line, respectively. Thus, coupling between the trace and DGS can be modeled by an ideal transformer with a turn ratio given by [1].

$$n = \sqrt{\frac{Z_{in}}{Z_L}} \cong \sqrt{\frac{Z_0^{strip}}{Z_0^{DGS}}} \quad (1)$$

where Z_{in} is the input impedance and Z_L is the load impedance. An equivalent circuit model for the geometry in Fig. 1 is illustrated in Fig. 3.

The slot line impedance varies with frequency extremes due to n computed by (1) as shown in Fig. 4. However, the variation (from DC to 10 GHz) of the turn ratio was not critical and taking the value of n in the middle of its variation range logically yields the most accurate results [4].

Among the various parameters that decide the resonance frequency, the length of the slot plays the most important role. The relationship between the slot length L_s and the resonance frequency f_{res} is given by

$$L_{eq} = L_s + 2\Delta \quad (2)$$

$$f_{res} = \frac{c}{\sqrt{\epsilon_r} \cdot L_{eq}} \quad (3)$$

where Δ is the end reactance ratio of a shorted slot, ϵ_r is the relative permittivity of the dielectric substrate, f_{res} is the resonance frequency, and L_{eq} is the electrical resonant length [5]. Generally, the electrical resonant length is longer than the real resonant length due to the inductive effect arising from the end of a slot when the slot trace is cut vertically. It increases with the increase in slot width and h/λ ratio. The equivalent length of the short end (Δ) may be up to $0.1\lambda_{slot}$ [6] [7].

However, in the case of a split, no end reactance occurs, so the electrical resonant length L_{eq} is the same as the physical length of the split. For this reason, the split type has a higher resonance frequency than the slot type.

A microstrip line coupled to the slot type DGS can be considered effectively as a short-circuited $\lambda/4$ line and it acts as a parallel LC resonance circuit near the resonance frequency, as shown in Fig. 5. The simulation results of Fig. 5 are shown in Fig. 6. The resonance frequency is observed around 4.3 GHz.

The capacitance of the equivalent circuit is given by

$$C_{slot2} = \frac{\pi}{4(2\pi f_{res})Z_0^{slot}} \quad (4)$$

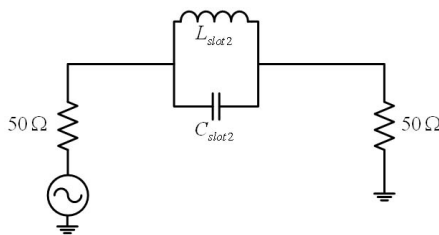


Fig. 5. Basic equivalent circuit model for a slot type DGS.

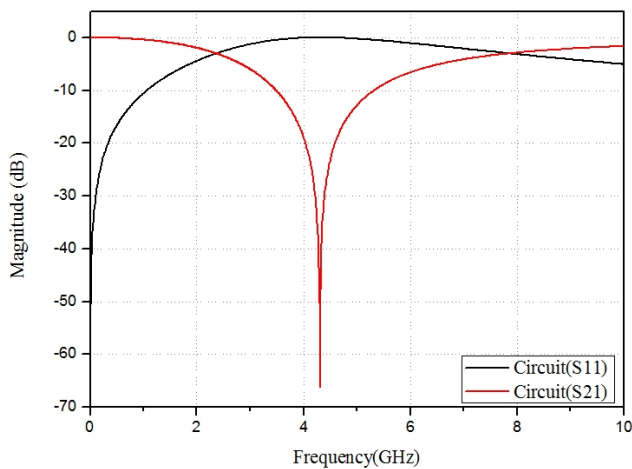


Fig. 6. S-parameter of the basic equivalent circuit model for a slot type DGS.

The simplest model of the slot type DGS shown in Fig. 5 can be extracted from the physical structure. However, for a more accurate and reliable model, losses at high frequencies have to be considered. Fig. 7 shows the equivalent circuit model of a slot type DGS structure and the dominant path in an equivalent circuit model. Before the resonance frequency, path 1 in the proposed model in Fig. 7 predominates because the inductive characteristic of the slotted ground plane is dominant. However, after the resonance frequency, path 2 in the proposed model in Fig. 7 predominates because the capacitive characteristic of the slot type DGS is dominant. R_{slot2} , which represents the ac resistance of a slot type DGS, can be obtained simply from equation (5) [8].

$$R_{slot2} = \frac{Z_0^{slot}}{\alpha(L_{eq}/2)} \quad (5)$$

where α is the attenuation constant. Inductor L_{slot1} affects the performance at high frequencies because it acts as a series LC resonance circuit. The simulation results of Fig. 7 are shown in Fig. 8.

Table 2 lists the extracted slot type DGS model parameter values.

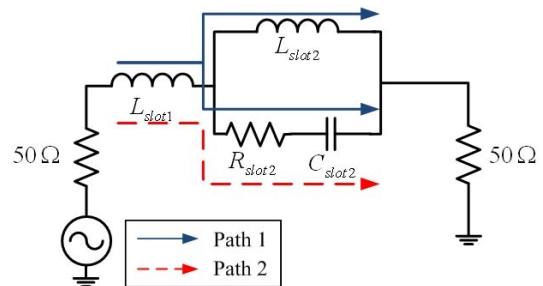


Fig. 7. Equivalent circuit model for a slot type DGS.

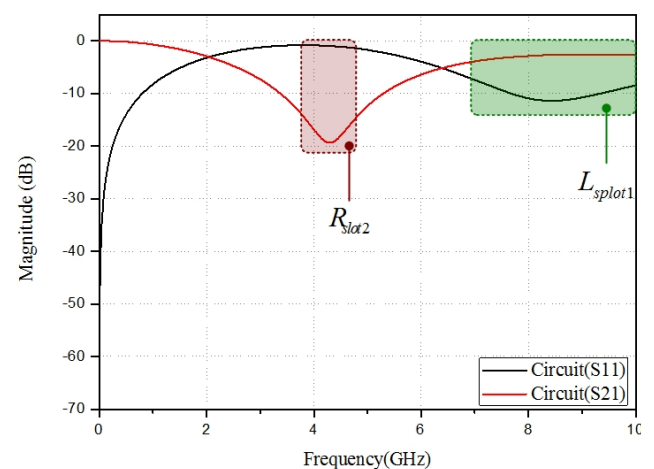


Fig. 8. S-parameter of equivalent circuit model for a slot type DGS.

Table 2. Extracted slot type DGS model parameters.

Parameter	L_{slot1}	L_{slot2}	R_{slot2}	C_{slot2}	n
Value	1.7 nH	4.12 nH	28 Ω	0.29 pF	0.68

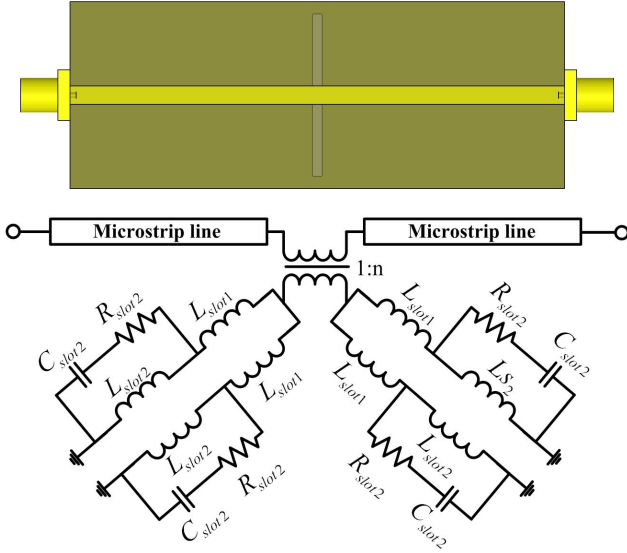


Fig. 9. The proposed equivalent circuit model for a slot type DGS.

Finally, an equivalent circuit model that represents the all current flow for a slot type DGS is proposed in Fig. 9.

2-2 Equivalent Circuit Model for a Split Type DGS

A microstrip line coupled to the split type DGS can be considered effectively as an open-circuited line and it acts as a series LC resonance circuit near the resonance frequency, as shown in Fig. 10. The simulation results of Fig. 10 are shown in Fig. 11. The resonance frequency is observed around 5.2 GHz.

The capacitance and inductance of the equivalent circuit are given by [8].

$$C_{split2} = \frac{4}{(2\pi f_{res})Z_0^{slot}\pi} \quad (6)$$

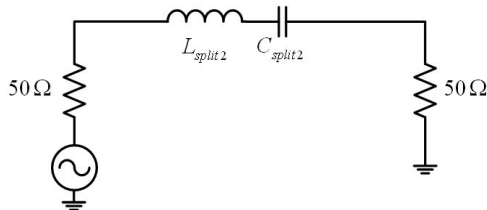


Fig. 10. Basic equivalent circuit model for a split type DGS.

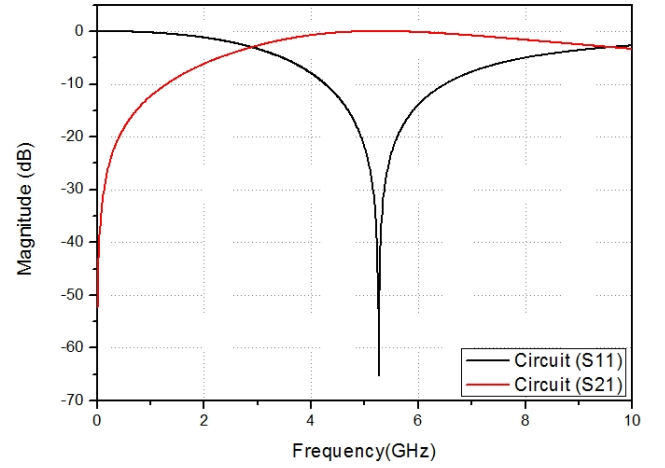


Fig. 11. S-parameters of a basic equivalent circuit model for a split type DGS.

$$L_{split2} = \frac{1}{(2\pi f_{res})^2 C_{split2}} \quad (7)$$

A more accurate and closer to equivalent model is generated by adding R_{split1} , R_{split2} , and C_{split1} , as shown in Fig. 12. Before the resonance frequency, path 1 in the proposed model in Fig. 12 is dominant because the inductive characteristic of split type DGS is dominant. However, after the resonance frequency, path 2 becomes dominant because the capacitive characteristic of the split ground plane is dominant. Therefore, resistance R_{split2} representing the ac resistance of type DGS can be obtained simply from equation (8) [8].

$$R_{split2} = \frac{Z_0^{slot}}{\alpha(L_{eq}/2)} \quad (8)$$

Where α is a attenuation constant. R_{split1} and C_{split1} have to be modified with the capacitive part of the plot because those parameters predominantly represent a capacitive characteristic of the split type DGS model. Therefore, loss from the magnitude of the impedance at the high frequency band is represented as R_{split1} .

The C_{split1} loss arises from blocking the return path in the low frequency band and it represents a parallel LC resonance circuit in the high frequency band. The simulation results of Fig. 12 are shown in Fig. 13. Table 3 lists the extracted split type DGS model parameter values.

Table 3. Extracted split type DGS model parameters.

Parameter	L_{split2}	C_{split1}	C_{split2}	R_{split1}	R_{split2}	n
Value	2.3nH	0.2pF	0.3pF	7.5 Ω	28 Ω	0.68

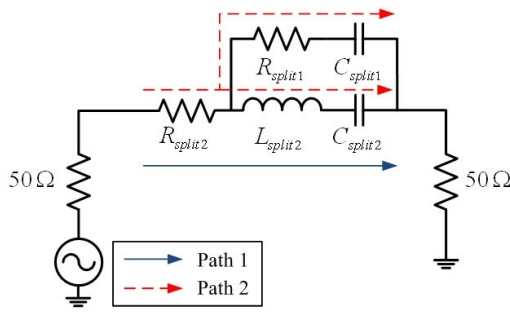


Fig. 12. Equivalent circuit model for a split type DGS.

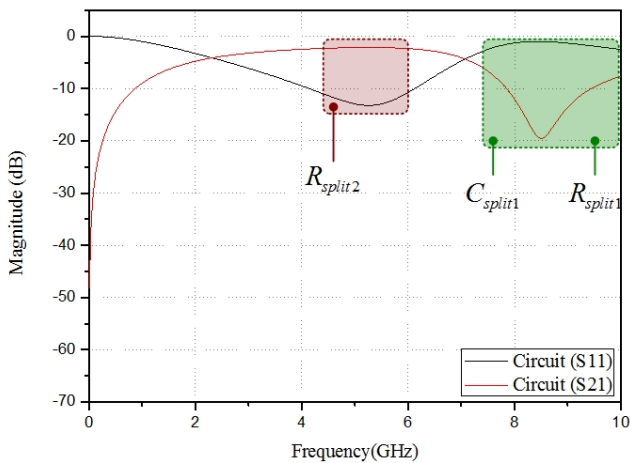


Fig. 13. S-parameter of an equivalent circuit model for a split type DGS.

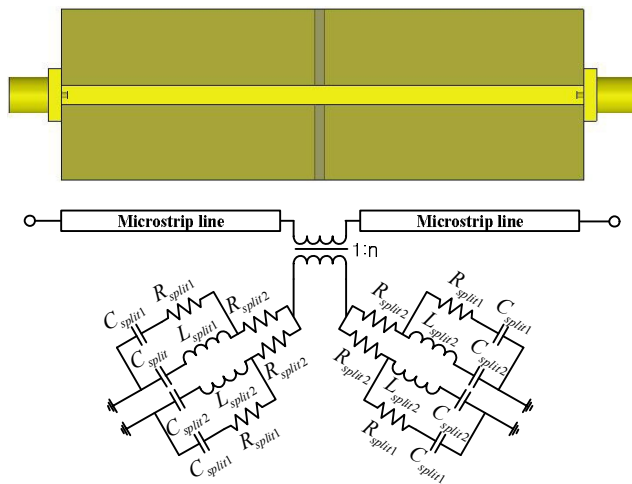


Fig. 14. The proposed equivalent circuit model for a split type DGS.

The proposed equivalent circuit model for a split type DGS, as shown in Fig. 14.

III. Results

The accuracy and the validity of the proposed model

is verified by comparing the S-parameter characteristics of the equivalent circuits shown in Figs. 9 and 14 with those measured for the actual structures shown in Fig. 1. The S-parameters for the proposed circuit model are calculated using the Designer [9] and those for the structure shown in Fig. 1 are simulated by HFSS [10].

Fig. 15(a), showing the return loss, is path 2 dominant in Fig. 7 because the capacitive characteristic of the slot type DGS is dominant. However, Fig. 15(b), showing the insertion loss, is path 1 dominant in Fig. 7 because the inductive characteristic of the slot type DGS is dominant. In contrast, Fig. 16, showing the return loss, is path 1 dominant in Fig. 12 because the inductive characteristic of the split type DGS is dominant. However, Fig. 16, showing the insertion loss, is path 2 dominant in Fig. 12 and becomes dominant because the capacitive characteristic of the split type DGS is dominant.

Return loss and insertion loss characteristics of a slot type DGS and split type DGS are shown in Fig. 15 and

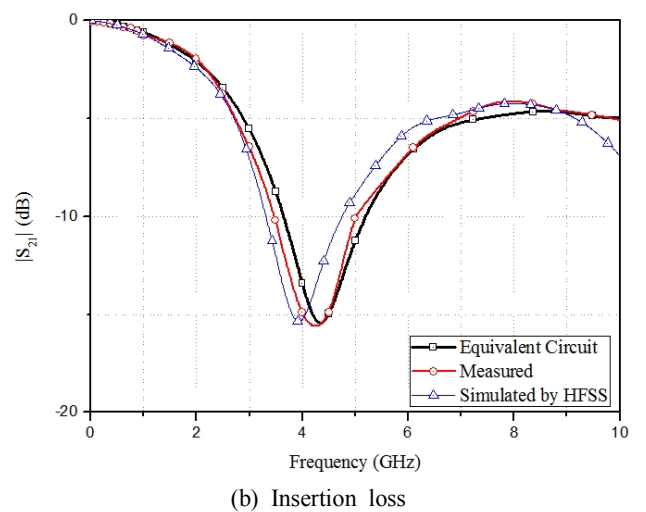
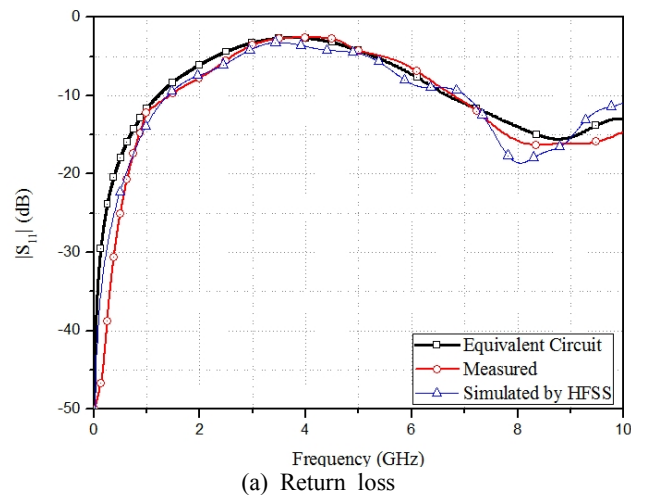


Fig. 15. Comparison of S-parameters for a slot type DGS.

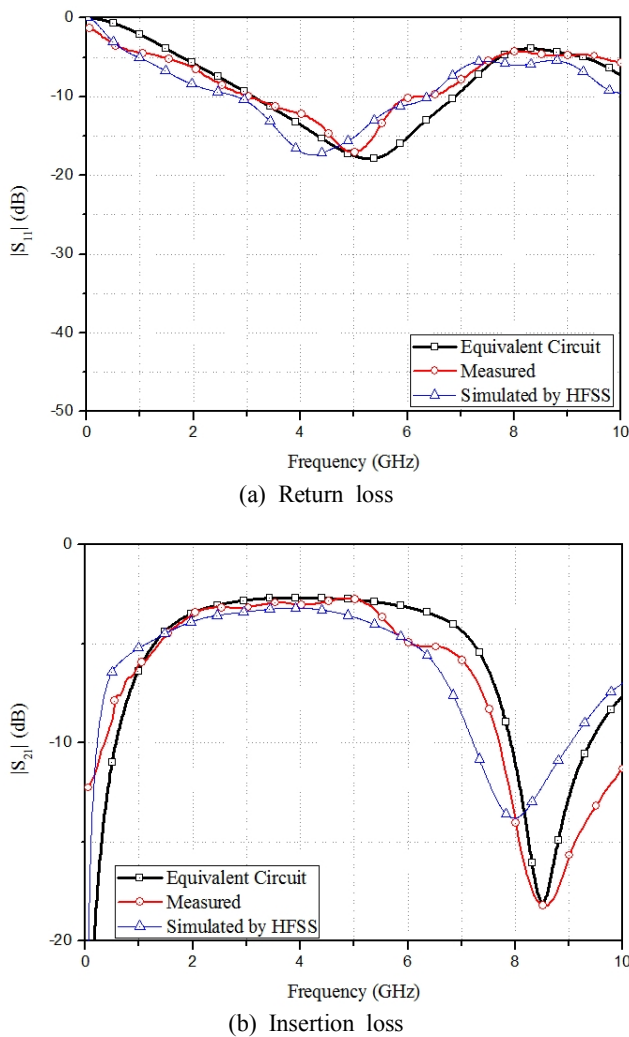


Fig. 16. Comparison of S -parameters for a split type DGS.

16, respectively. Good agreement exists between the equivalent circuit model and measurement.

IV. Conclusions

This paper proposes accurate circuit models to analyze structures with traces that cross a defected ground plane. It provides clear insight into the coupling mechanism between the microstrip line and the DGS. The circuit models consist of a transformer for a coupling mechanism and LC resonators for the DGS. A more accurate and closer equivalent model at high frequency is created by adding, resistors, capacitors, and inductors.

The calculated S -parameters using the equivalent circuit model are in excellent agreement with those of measurement over a wide frequency band. Good agreement could be achieved because the proposed model considered the frequency dependent characteristics of a defected ground structure with lumped components. This model can be easily embedded into a circuit and can be used for simulation of noisy circuits. Therefore, this model can be very useful for the analysis of various defected ground plane structures.

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