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A novel sensing algorithm for Spin-Transfer-Torque magnetic RAM (STT-MRAM) by utilizing dynamic reference

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Abstract: A novel sensing algorithm for non-volatile Spin-Transfer Torque Magneto-resistive Random Access Memory (STT-MRAM) is presented. The dynamic reference sense amplifier (DRSA) improves sensing margin to achieve high reliability and sensitivity by increasing the difference of input voltages of sense amplifier. A dynamic reference sensing algorithm is proposed as a solution for the read margin loss due to variation in magnetic tunneling junction (MTJ) parameters of the STT-MRAM. The proposed sensing method was designed in standard 0.18 um process parameters, and simulation results indicate simultaneously increased the read margin compared with the conventional sensing method.

Keywords: Spin-Transfer-Torque magneto resistive RAM (STT-MRAM), sense amplifier, dynamic reference, read margin

Classification: Integrated circuits

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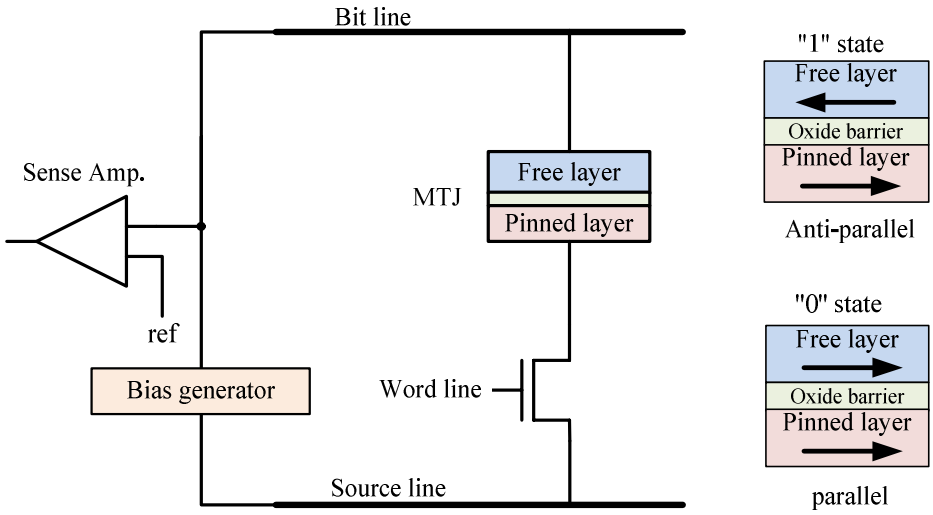
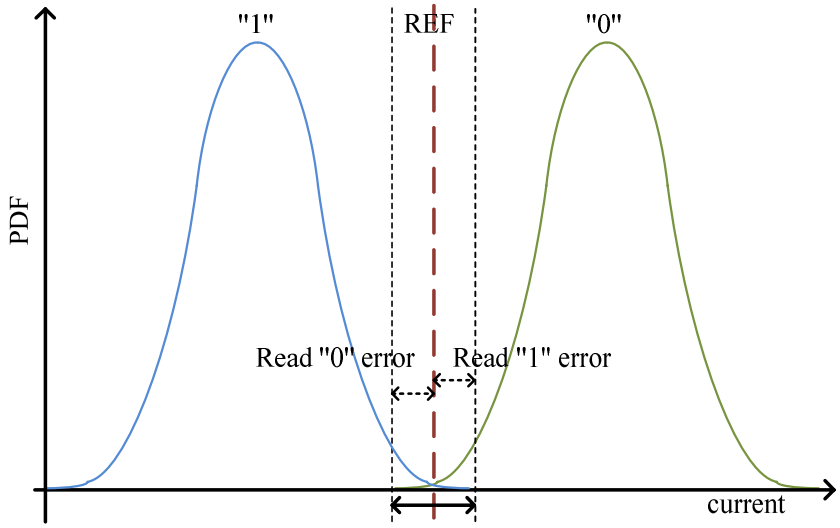
1 Introduction

Spin-Transfer-Torque Magneto Resistive Random Access Memory (STT-MRAM) has emerged as a promising candidate for embedded, high-density, and scalable nonvolatile memory technology [1, 2]. A STT-MRAM cell consists of word line (WL) transistor connected in series with magnetic tunneling junction (MTJ) between a bit-line (BL) and source-line (SL). MTJ is made of thin tunneling dielectric film (called oxide barrier, usually, MgO) and two ferromagnetic layers. Magnetization in one ferromagnetic layers is fixed (called pinned layer), and the other one is variable as storage information (called free layer).



(a)



(b)

Fig. 1. (a) STT-MRAM structure (b) Relation between non-uniform distribution of cell data and read failure

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According to the direction of magnetization of free layer with respect to pinned layer, MTJ becomes a high resistance state (R_{AP}, the corresponding state is antiparallel or "1") or a low resistance state (R_P, the corresponding state is parallel or "0"). The writing operation of the cell involves passing a high switching current (I_{SW} or critical current I_C) to switch MTJ from low- to high-resistance state and vice versa. During write "1", the Bit-line (BL) is at higher voltage ($V_{BL} = V_{DD}$) than the source-line (SL, $V_{SL} = 0$), and the current flows from the BL to the SL. During write "0", $V_{SL} = V_{DD}$ and $V_{BL} = 0$, and the current flows from the SL to the BL. The conventional read operation for STT-MRAM impresses a small voltage across the cell (V_{BL} is positive and $V_{SL} = 0$). The current flowing through the cell depends on the MTJ resistance. This current is sensed directly or by perceiving the voltage drop at the pre-charged BLs to read the cell data [3].

One of the quality indicators for MTJ is tunneling magneto-resistance (TMR) ratio. TMR ratio of MTJ defined as $(R_{AP} - R_P)/R_P$ and MTJ with high TMR ratio is desirable because of its large noise margin ($\Delta R = R_{AP} - R_P$). The variation in transistor and MTJ parameters results in statistical variations in the MTJ switching current and cell read current. Due to variation, the cell read current can be larger than the MTJ switching current, then read disturb failure occurs. To reduce read disturb failure, the cell read current needs to be sufficiently smaller than switching current. Hence, the read margin requires that the read current needs to be scaled along with the write current [3].

In this paper, we propose a novel sensing method that improves read margin to reduce read failure for STT-MRAM. This scheme operates with constant cell read current and uses the modified reference voltage.

2 Problems of the conventional sensing method for STT-MRAM

The sense amplifier of memory circuits distinguishes the cell information by a comparison based on a cell value and a reference voltage or current. A sensing margin is the signal difference to determine the correct logic information. The sensing margin should be insensitive to various noises (PVT, offset noise, coupling noise, etc.) from MOSFET and MTJ characteristics that affect the sense amplifier. A variety of techniques to improve the sensing margin was examined for the existing memory such as offset cancellation, etc. [4]. Figure 1-(b) shows sensing margin loss due to non-uniform distribution of high and low resistance in the resistive memory devices. Due to current distributions, a read disturb failures can occur nearby reference value (voltage or current).

Typically, the STT-MRAM has $1 \sim 200\%$ TMR ratio. A sensing method using constant reference has a small sensing margin as decreasing difference of the cell information and the reference value. A very precise sense amplifier is required in order to avoid malfunction. A sensing method that impresses a small voltage is shown in Figure 1-(a). This method does not guarantee

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that a read current lower than the critical current due to device variance. Moreover, due to using a current sense amplifier, more area and complexity are required than voltage sense amplifier. As it uses cell current directly, the output of the sense amplifier has a potential to affect a cell data.

3 Proposed sensing method for STT-MRAM

In this section, we propose a new sensing method suitable for STT-MRAM to solve as mentioned above problems. Instead of impressing a small voltage from BL to SL, we use the constant read current flows from BL to SL. This current guarantees the read current under the critical current, and it prevents

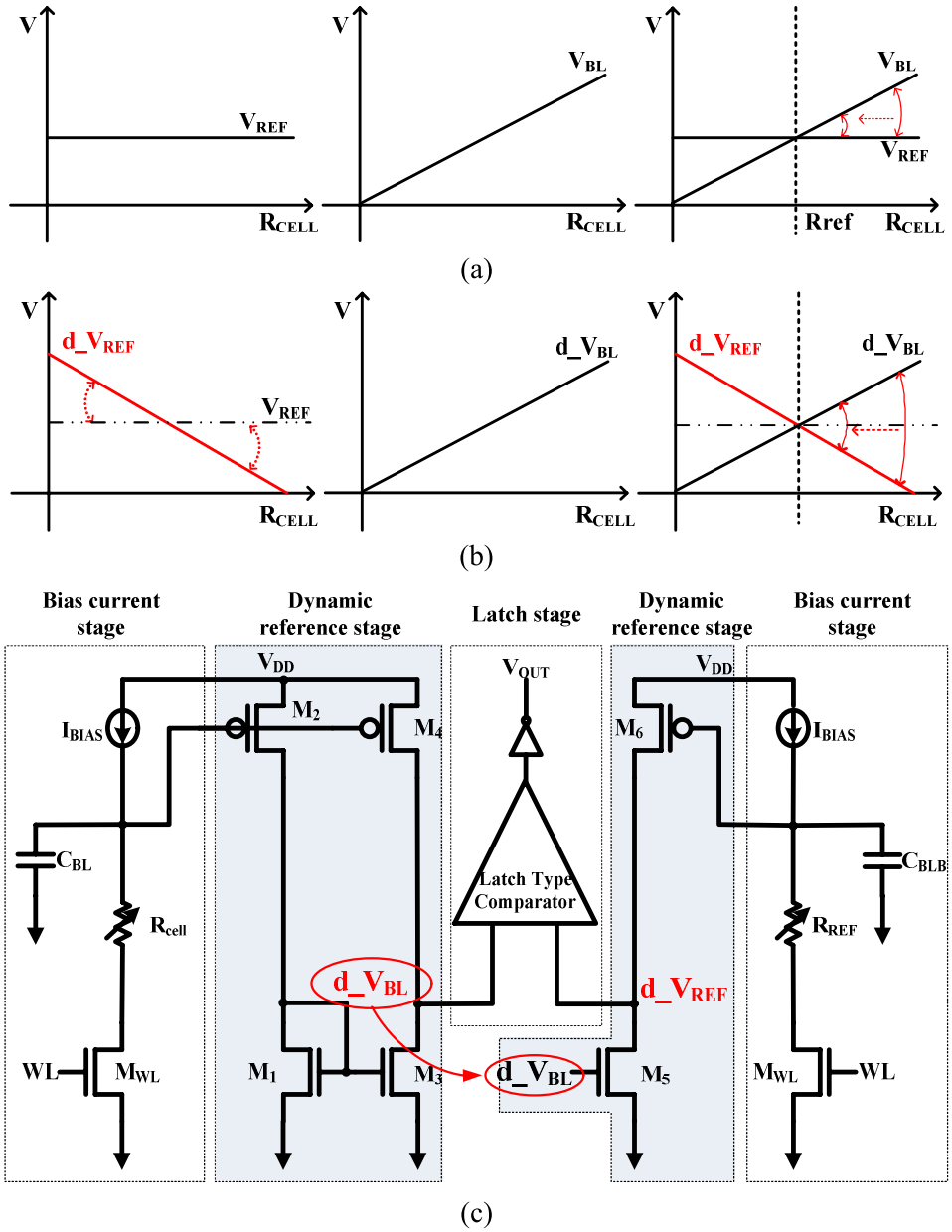

Fig. 2. R-V characteristics of (a) conventional static reference sensing method (b) proposed dynamic reference sensing method (c) dynamic reference sense amplifier scheme

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unnecessary write operation.

To improve read margin, we propose dynamic reference mechanism. The dynamic reference sense amplifier (DRSA) increases the difference between cell information and reference voltage. The voltage of the dynamic reference varies inversely with the cell information. Figure 2 shows R-V characteristics of conventional and proposed sensing method. In Figure 2-(a), a reference voltage remains constant regardless of a cell state, and the sense amplifier perceives data according to the cell state. The difference between the reference value and sensing data becomes significantly smaller where the sensing data is closer to the reference (R_{REF}) and the read disturb failure possibility increases. Figure 2-(b) shows the proposed dynamic reference. The d_V_{REF} varies depending on the cell value inversely. The dynamic reference is decreased when the cell value (resistance) increases. Therefore, the sense amplifier can achieve a larger sensing margin than the conventional reference, especially when the difference is delicate.

We designed the latch type sense amplifier to implement the dynamic reference for STT-MRAM. As shown in Figure 2-(c), the sense amplifier can be divided into three blocks. The first block is the bias current stage to control a current to flow into the cell. The second is the dynamic reference stage to ensure a sensing margin, which has separated inputs of sense amplifier and bit-line to protect the cell. The last block, latch stage, converts the cell information to the digital signal amplifying the difference between the cell and reference voltage. The reason to separate bit-line voltage and input of latch comparator is to protect the cell information from externals, as well as to manage the bit-line voltage. The d_V_{BL} generated by bit-line voltage is biased to the gate node of M5 in the reference stage for the feedback operation. The d_V_{REF}, the output of a common source amplifier formed M5 and M6 is biased to the reference voltage of the latch comparator. For example, if R_{cell} is large, bit-line voltage will be increased but the d_V_{BL} decreases. Then, the drain voltage of the M5-M6 common source amplifier will increase. Therefore a larger sensing margin can be achieved by increasing ΔV_{in} with the increase of d_V_{REF} due to decreasing d_V_{BL} in the input of the latch comparator.

4 Simulation result

The proposed DRSA was designed using a 0.18 μm process and simulation performed using HSPICE tool. The cell is modeled as a STT-MRAM where the read current, the bit-line capacitance and output capacitance are 2 μA, 1 pF and 100 fF, respectively. The resistances of the magnetic tunnel junction are 5 kΩ (parallel state) and 10 kΩ (antiparallel state). TMR ratio is 100%. In this case, the reference cell resistance is 7.5 kΩ. As shown in Figure 3-(a), the x-axis shows a resistance difference between the resistive memory cell and reference cell as ΔR. The y-axis shows the difference in input voltage of the sense amplifier as the sensing margin ΔV_{in}. From simulation results, the sensing margin of a conventional static reference method has a small

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variation according to the cell resistance difference. Otherwise, the proposed dynamic reference method improves the sensing margin by about 7 times at 5 kΩ cell resistance in Figure 3-(a). The simulation result of the proposed DRSA and the conventional SRSA with $\Delta R = 1\,k\Omega$ and $2\,k\Omega$ is shown in Figure 3-(b). Depending on these results, the dynamic reference can dramatically improve the sensing margin and thus can be implemented with high speed and reliability.

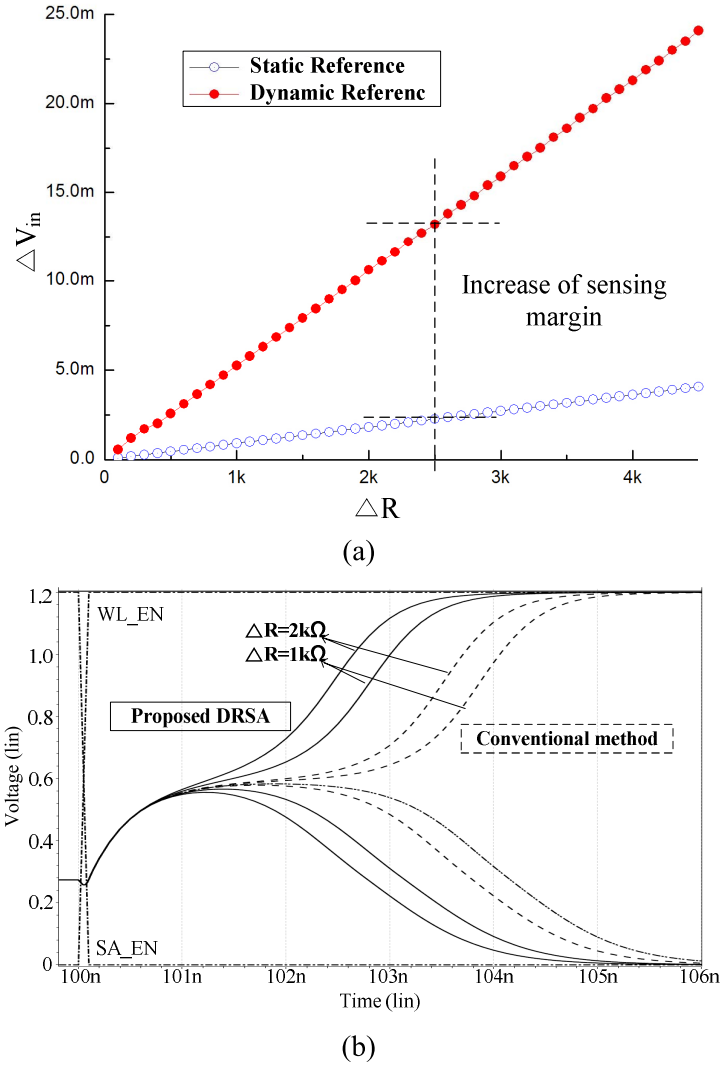

Fig. 3. (a) comparison of sensing margin between conventional and proposed sensing method (b) simulation result of the response time to compare the proposed DRSA and conventional method with ΔR of 1 kΩ and 2 kΩ, respectively

5 Conclusion

We have proposed a new concept of sense amplifier to improve the sensing margin for STT MRAM with a small magneto-resistance ratio. This method adopts a dynamic reference sense scheme with a bit-line feedback to the ref-

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erence cell, depending on the voltage level of the reading cell. Therefore, the sensing margin is significantly increased. From this work, it is expected that this scheme will be one of the solutions to increase sensing margin for several memories with a low sensing margin, such as DRAM, ReRAM, PcRAM, etc.

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