Kim et al. *NPG Asia Materials* (2020) 12:77
https://doi.org/10.1038/s41427-020-00261-0

NPG Asia Materials

ARTICLE Open Access

Enhanced analog synaptic behavior of SiN_x/a-Si bilayer memristors through Ge implantation

Keonhee Kim[1,2], Soojin Park[1,3], Su Man Hu[1,2], Jonghan Song[4], Weoncheol Lim[4], Yeonjoo Jeong[1], Jaewook Kim[1], Suyoun Lee[1], Joon Young Kwak[1], Jongkil Park[1], Jong Keuk Park[1], Byeong-Kwon Ju[2], Doo Seok Jeong[3] and Inho Kim[1]

Abstract

Conductive bridging random access memory (CBRAM) has been considered to be a promising emerging device for artificial synapses in neuromorphic computing systems. Good analog synaptic behaviors, such as linear and symmetric synapse updates, are desirable to provide high learning accuracy. Although numerous efforts have been made to develop analog CBRAM for years, the stochastic and abrupt formation of conductive filaments hinders its adoption. In this study, we propose a novel approach to enhance the synaptic behavior of a SiN_x/a-Si bilayer memristor through Ge implantation. The SiN_x and a-Si layers serve as switching and internal current limiting layers, respectively. Ge implantation induces structural defects in the bulk and surface regions of the a-Si layer, enabling spatially uniform Ag migration and nanocluster formation in the upper SiN_x layer and increasing the conductance of the a-Si layer. As a result, the analog synaptic behavior of the SiN_x/a-Si bilayer memristor, such as the nonlinearity, on/off ratio, and retention time, is remarkably improved. An artificial neural network simulation shows that the neuromorphic system with the implanted SiN_x/a-Si memristor provides a 91.3% learning accuracy mainly due to the improved linearity.

Introduction

As computing paradigms are shifting from a central processing unit-centric system to a data-centric system, a new computing architecture is demanded to overcome the performance limitations in the present von Neumann architecture[1–5]. Bioinspired neuromorphic computing is one of the alternatives to von Neumann computing. Emerging devices for artificial neurons and synapses as basic building blocks in neuromorphic systems have been extensively studied because many of them have high potential in terms of power consumption, scalability, and computation speed in comparison with complementary metal–oxide–semiconductor (CMOS)-based neurons and synapses[4,6–9]. The ideal analog behavior of artificial synapses is one of the key factors for high learning accuracy of neuromorphic systems based on artificial neural network algorithms. Linear and symmetric synapse conductance updates under identical spikes as well as a large on/off ratio are required to implement ideal analog synaptic devices[10].

Recently, several different approaches, such as flash memory, phase change memory (PCM), ferroelectric field effect transistors (FeFETs), and resistive random access memory (ReRAM), have been investigated to realize ideal analog synaptic devices. Multibit flash memory is one of the promising candidates, but the scaling issue due to its large footprint is a concern. Additionally, the programming speed and endurance of NAND flash memory cannot yet meet the requirements of neuromorphic applications[10]. In many studies, PCM has been demonstrated to act as analog synapses due to its high speed and good scalability, but the inherently high nonlinearity of the synapse weight update, especially in depression, poses a challenge to the implementation of ideal analog

Correspondence: Inho Kim (inhok@kist.re.kr)
[1]Center for Neuromorphic Engineering, Korea Institute of Science and Technology, Seoul 02792, South Korea
[2]School of Electrical Engineering, Korea University, Seoul 02841, South Korea
Full list of author information is available at the end of the article
These authors contributed equally: Keonhee Kim, Soojin Park

behavior[11]. An FeFET is another promising solution to achieve high linearity of the synapse weight update because the device conductance is modulated through a gate electrode that does not interfere with a current-conducting channel[12,13]. However, the implementation of FeFETs using conventional perovskite-type oxide materials finds difficulty in securing CMOS process compatibility[14,15].

ReRAM, where conductive filaments constitute conductive metal ions or oxygen vacancies in the resistive switching layer, provides excellent performance in terms of scalability, low switching current, endurance, and retention. Furthermore, the simple fabrication process and CMOS back-end of line compatibility make it a promising candidate for artificial synapses in neuromorphic systems, as reported in the literature[16]. Among various types of ReRAM devices, conductive bridging random access memory (CBRAM) has been suggested for artificial synapses because it has high potential, such as a large on/off ratio, a long retention time, and high speed[16]. However, the abrupt conductance changes due to the bridging and rupture of a nanoscale conductive filament cause highly nonlinear and asymmetrical conductance responses. This makes it difficult for CBRAM to be applied as ideal analog synapses in a neuromorphic system.

Various approaches have been proposed to suppress the abrupt nature of the filamentary switching of CBRAM devices: (i) multiple weak filament implementation, (ii) internal current limiting, and (iii) filament modulation. For implementation of multiple weak filaments, nanoscale metal particles are incorporated into a switching layer by cosputtering of metal and dielectric materials so that spatially uniform conduction can be formed between active metal-rich and active metal-poor regions through conductive multifilaments[5]. Annealing an active metal on a switching layer can be another approach to produce multiple weak filaments. The metal ions diffuse into the switching layer by annealing, achieving stochastic multiple conduction channels[17]. As multiple conductive ion transport channels are preformed in the switching layer in the case of multiple weak filaments, this approach suppresses abrupt strong filament formation and provides more reliable and gradual switching[4]. In the internal current limiting case, ReRAM includes a resistive layer as an internal current limiter in series with a switching layer[18]. The internal current limiter helps suppress the abrupt increase in the device current through the switching layer during the set transition via a so-called voltage divider effect[4,19]. In the filament modulation method, the diameter of the conductive filament is gradually adjusted in the set mode by additional voltage pulses. By controlling the conductive filament size successively, the device shows a gradual conductance change[20].

In this study, we demonstrate a novel approach to enhance the analog behavior of a (Ag top electrode (TE))/SiN_x/a-Si/(p^{++} Si bottom electrode)-based CBRAM device through Ge implantation. Depending on the voltage regime, the CBRAM device exhibits binary or analog switching behavior. Ge forms an ideal solid solution blended with Si. Therefore, the Ge implanted into the a-Si layer does not form any second phase materials. Furthermore, Ge has a higher atomic weight than Si, so it generates more defects by implantation. These are the main reasons why we chose Ge as the implantation ion.

The process of implantation in resistive switching devices has been introduced for various purposes. Some metal oxides, such as CuO_x and HfO_x, were synthesized at low temperature by implanting oxygen[21,22]. Metal or gas ions, such as oxygen, nitrogen, Au, Zr, and Ti, were also implanted in an effort to improve the resistive memory parameters, including the retention time, device yield, variations and forming voltage[23–25]. Unlike previous research, in this study, we introduced the implantation process to adjust the conductance of a current limiting layer and metal cluster morphology. If a sufficiently high voltage greater than the forming voltage is applied, the device becomes electrically formed and exhibits abrupt binary switching. By contrast, when a low voltage below the forming voltage is applied, the device shows a typical analog memristor behavior. In this case, the a-Si layer serves as an internal current limiter to suppress the abrupt strong filament formation, and the SiN_x top layer serves as a switching layer. The SiN_x/a-Si bilayer device shows analog behavior, but the nonlinearity of the conductance update, on/off ratio, and retention time are not desirable. In an effort to enhance the analog behavior of the CBRAM device, we introduced Ge implantation into the a-Si underlayer to modify the conductance and surface structure of the a-Si layer. Because of Ge implantation, the analog behavior in terms of the linearity, on-off ratio, and retention time was remarkably enhanced. We discuss the origin of the enhanced analog behavior through implantation. Last, we also perform an MNIST recognition simulation in memristor-based neural networks with consideration of the synapse nonlinearity. The implanted CBRAM device provided a learning accuracy of 91.3% due to its enhanced linearity of the synapse weight update, whereas the unimplanted device exhibited only a 62.8% accuracy.

Experimental

Implantation process

Ge implantation was conducted using a 400-kV ion implanter located at the Korea Institute of Science & Technology (KIST). The implanter consists of a high voltage generation part, a source withdrawing part, an ion acceleration part, an ion beam line, and an ion chamber. Amorphous Si thin films on crystalline Si wafers were irradiated by Ge ion beams accelerated with a 70-kV

voltage at a fluence of 1×10^{16} atoms/cm^2 at room temperature. The ion flux was measured by a Faraday cup and adjusted to be under 50 nA/cm^2·s.

Device fabrication process

The memristor synapse was designed to have a via-hole-type structure consisting of (Ag TE)/SiN_x/a-Si/(p^{++}-Si bottom electrode). Amorphous Si of a 78-nm thickness was deposited by low-pressure chemical vapor deposition (LPCVD) (SHF-150L) on Si wafers. In an LPCVD deposition process, SiH_4 gas was supplied at a 60-sccm flow rate, and the process pressure and temperature were set to 150 mTorr and 550 °C, respectively. Ge ions were then implanted in the amorphous Si layer. A SiN_x thin film of 100 nm thickness was deposited on the a-Si layer as an insulating layer by plasma-enhanced chemical vapor deposition (PECVD). The SiN_x film was selectively etched in a 1:6 BOE solution with a photoresist mask having circular hole arrays patterned by photolithography. By this process, the via-hole structure on the a-Si layer was prepared. After removing the photoresist, another SiN_x thin film of a 9–20-nm thickness as a switching layer was deposited by PECVD. Last, a Ag TE of a 300-nm thickness was prepared by a lift-off process. The Ag electrode was deposited by a thermal evaporator.

Current–voltage characteristics, pulse test, and retention test

Electrical characterization was performed with a source measure unit (Keithley 236) connected to a probe station. The direct current–voltage (I–V) characteristic curves of the devices were obtained under repetitive voltage sweeps of $0 \rightarrow +5$ V and $0 \rightarrow -5$ V. The scan speed was set to 0.098 V/s by adjusting the measurement delay time. The compliance current was set at 10 mA for all DC sweep measurements. The memristor devices were also operated under repetitive voltage pulse signals to observe potentiation/depression. For the implanted devices, the amplitudes of the potentiation/depression pulses were 7 V/−3 V with a 10-ms pulse width, and the readout pulse was 1 V with a 10-ms pulse width; for the unimplanted devices, the amplitude of the readout pulse was 2 V with the same pulse width. To determine the synapse retention time, the conductance of the synaptic device was measured as a function of elapsed time after 500 voltage pulses with a 100-ms width and various voltages (5, 6, 7 V). Endurance of potentiation/depression was tested at a 7 V/−4 V write voltage and a 1 V read voltage for 500 cycles.

Cross-sectional TEM (XTEM), scanning transmission electron microscopy (STEM), and energy dispersive X-ray spectroscopy (EDX)

TEM samples were prepared by using a focused ion beam (FIB) technique (Hitachi-NX5000). Through the FIB process, the device samples were thinned to have adequate width for TEM observation. The FEI equipment (TitanTM 80–300) was used for both conventional TEM and STEM observations. These analyses were carried out to visualize the cross-sectional area of the memristor devices. Through TEM and STEM, the structures of the devices and Ag nanoclusters embedded in active layers were observed. Moreover, the distribution of the Ge atoms implanted in the a-Si layer was characterized using EDX.

TRIM simulations

Full-cascade Monte Carlo simulations of Ge implantation were performed via a TRIM software package (SRIM 2003 ver.13). The spatial distributions of Ge atoms and vacancy defects along the depth were calculated by TRIM simulations. For the simulations, the stack of a-Si (78 nm)/c-Si wafer (semi-infinite) was used, and the densities of the LPCVD a-Si and Si wafer layer were set to be 2.285 and 2.329 g/cm^3, respectively[26]. The acceleration voltage was fixed at 70 kV, and the input values for the displacement energy and lattice binding energy were 12 and 2 eV, respectively. The vacancy concentration along the depth was determined from the number of vacancies created per implanted ion (ν_i) in the TRIM simulation by the following equation.

$$\text{Vancancy concentration} = \nu_i \left(\frac{\text{vacancies}}{\text{ions}}\right) \times \text{fluence}\left(\frac{\text{ions}}{\text{cm}^2}\right) \times \frac{1}{\rho\left(\frac{\text{atoms}}{\text{cm}^3}\right)} \times 0.01,$$

where fluence is the number of implanted ions per unit area and ρ is the atomic density of the substrate. ν_i is calculated by subtracting replacement collisions from target displacements in the simulation. The factor of 0.01 is used to account for the self-annealing effect. Approximately 99% of the implantation damage is instantly recovered during implantation at room temperature, resulting in only 1% damage[27,28].

MNIST pattern recognition simulation

An MNIST pattern recognition simulation was performed based on a memristor-based neural network with consideration of the synapse update model, which was experimentally determined in potentiation and depression under repetitive identical pulses. The artificial neural network algorithm model chosen for the simulation was a multilayer perceptron (MLP) with three neuron layers: an input layer with 784 neurons, a hidden layer with 128 neurons, and 10 output neurons for different labels. Information from the inputs flows into the next neuron layer via the fully connected synapses with different

weight strengths, and the collected data in the neurons are again transmitted to the next layer after performing nonlinear encoding, e.g., the rectified linear unit function. In the output stage, a softmax function produces the normalized probability distribution of each output value. For the training, batch-type learning was performed using 60,000 MNIST training datasets (batch size 400) and repeated 100 times (100 epochs). The cost of the neural network was calculated utilizing a cross-entropy equation, and the synapse weight was updated based on a gradient descent method. To put experimental synaptic device characteristics into the simulation, the nonlinearity in the analog conductance change with a limited number of states was considered.

Results and discussion

Current–voltage characteristics of SiN_x/a-Si bilayer devices and influences of implantation

The measurement configuration and fabrication process flow of the SiN_x/a-Si bilayer memristor sandwiched by a Ag electrode and a heavily doped p^{++} Si wafer are illustrated in Fig. 1a, b, respectively. Ge ions with a dose of $1.0 \times 10^{16}\ cm^{-2}$ were implanted into a-Si thin films before the deposition of SiN_x. For a comparative study, a device of the same device structure but without implantation was fabricated. When a high voltage sufficient for forming was applied, both devices exhibit a typical binary switching behavior regardless of implantation (Fig. S1). The implanted device shows a slightly higher forming voltage (13.2 V) than the device with no implantation (11.5 V), but the set and reset voltages of both devices lie in the similar range of 3.0–3.5 V in absolute value. They all show abrupt switching behavior, indicating that the formation of a strong conductive filament is the main mechanism for switching. In contrast, when the voltage was swept in a low voltage regime from 0 to +5 V and from 0 to −5 V repetitively, a gradual change in the device current depending on the sweep direction was observed, as shown in Fig. 2a. Hysteresis in a voltage–current sweep curve pinched at the origin is a fingerprint of a memristor device. The implanted device shows two orders of magnitude higher current values than the unimplanted device, and the current–voltage curve is relatively symmetrical, whereas the unimplanted device shows hysteresis only in the positive bias region. The same voltage sweep testing was performed for the devices without a SiN_x thin film, and the results are shown in Fig. 2b. The unimplanted device exhibits an asymmetric Schottky contact diode curve, where the carrier injection barrier heights under forward and reverse biases are different[29]. In this case, the contact barrier height under forward bias appears to be lower than that under reverse bias. A more detailed discussion is presented in supplementary information (Fig. S2).

The current–voltage curve of the implanted device was substantially influenced by the Ge implantation, as shown in Fig. 2a. The current level was increased by approximately two orders of magnitude, similar to the cases with the SiN_x thin film. Furthermore, the current–voltage curve became more symmetrical. High-energy particles implanted into materials induce structural defects in bulk materials, such as low-dimensional defects of vacancies and voids, which serve as deep trap states, resulting in increased conductance through trap-assisted tunneling[30]. After Ge implantation into the a-Si thin film, a XTEM image was taken and is presented in Fig. 2c. The XTEM image shows that the top surface region of the crystalline Si wafer amorphized due to the incident high energy Ge ions. The Si wafer from the original a-Si/c-Si interface to a depth of 32 nm transformed into the amorphous phase with the implantation. The Ge ion depth profile was

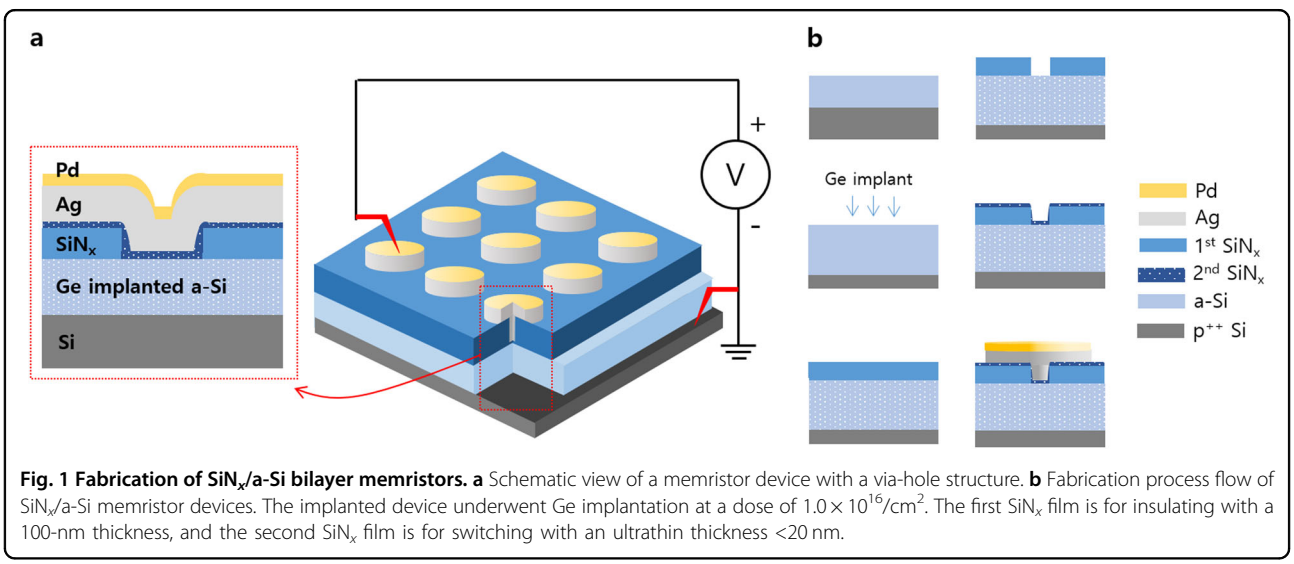

Fig. 1 Fabrication of SiN_x/a-Si bilayer memristors. a Schematic view of a memristor device with a via-hole structure. **b** Fabrication process flow of SiN_x/a-Si memristor devices. The implanted device underwent Ge implantation at a dose of $1.0 \times 10^{16}/cm^2$. The first SiN_x film is for insulating with a 100-nm thickness, and the second SiN_x film is for switching with an ultrathin thickness <20 nm.

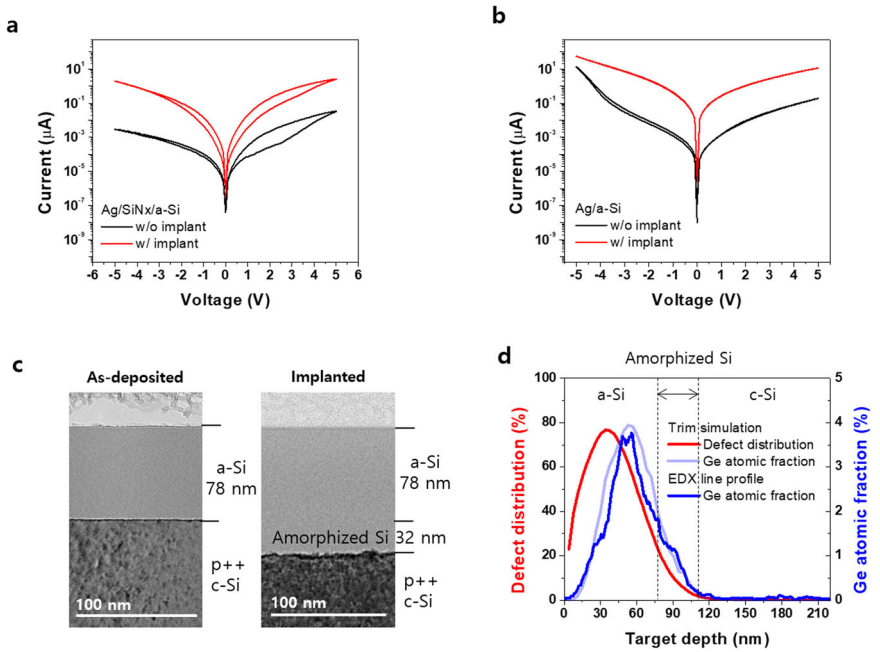

Fig. 2 Modulation of electrical conductances by ion implantation. Characteristic current–voltage curves of **a** an SiN_x/a-Si bilayer memristor device and **b** an a-Si single layer device with and without implantation. The voltage was swept repetitively following the sequence $0 \rightarrow +5 \rightarrow 0 \rightarrow -5 \rightarrow 0$. **c** XTEM image of an implanted a-Si on a p^{++} crystalline Si wafer. **d** Ge and defect (vacancy) distributions simulated by TRIM, and Ge atomic fraction determined by EDX.

simulated using a software package (TRIM) and compared with the EDS result taken in the TEM instrument. Both results are in good agreement, as shown in Fig. 2d. The vacancy concentration along the depth was simulated using TRIM and is also presented. The peak of the vacancy concentration lies in a shallower region than that of the Ge atoms. Note that the vacancy concentration even near the surface of the Si wafer (23% at the 3.8 nm depth) is substantial, whereas the Ge concentration (0.05% at the 3.5 nm depth) is negligible in the same region.

The analog synapse behavior of the bilayer memristor devices was investigated by applying consecutive triangular voltage pulses in the positive and negative bias regions, as shown in Fig. 3a, b. The unimplanted device shows gradual conductance changes only in the positive bias region, whereas the implanted device exhibits gradual conductance changes in both the positive and negative bias regions. The conductance (current) level of the implanted device is much greater than that of the unimplanted device, as expected from the current–voltage sweep curves in Fig. 2. The gradual conductance update behavior with increasing number of pulses is more clearly observed in the voltage–current–time graph (V–I–t) presented in Fig. 3c, d. The gradual conductance changes with repetitive voltage sweeps are a typical behavior of analog synaptic devices emulating a biological synapse. The conductance increase and decrease with repetitive voltage pulses can be viewed as potentiation and depression in a biological synapse[17].

Gradual conductance changes with repetitive voltage pulses are very rarely reported in CBRAM devices with a strong conductive filament. The formation and rupture of a strong filament during device operation result in abrupt conductance changes in general[11]. In this regard, the gradual conductance changes of the bilayer devices are very interesting results. Many research efforts have been made to fabricate analog CBRAM memristors. The formation of weak multifilaments and suppression of a strong filament are key directions for analog memristor devices. Blending of metal and dielectric materials by codeposition or high-temperature annealing is one way to induce multifilament formation, as reported in the literature[5,17]. Suppression of abrupt current increases during the reset-to-set transition is another approach. This can be realized by setting a compliance current; the amount of the compliance current determines the resistance in the set state, i.e., the size of the conductive filaments. Therefore, multiple resistance levels can be obtained by varying the compliance current values. The compliance current can also be implemented by internally including a resistive layer of a suitable resistance[4,19]. In this case, the resistance of the self-compliance layer should lie between the set and reset resistances for

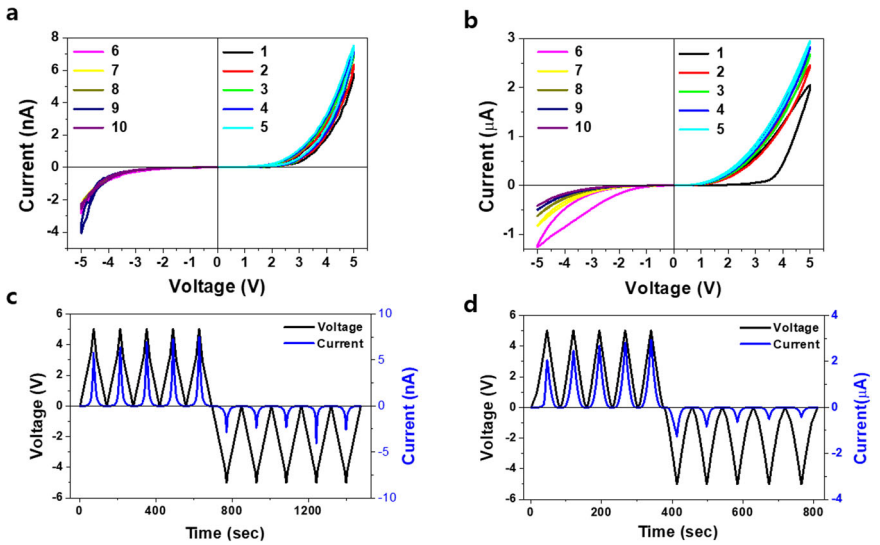

Fig. 3 Analog memristor behaviors. Memristor currents under five consecutive DC voltage sweeps of a SiN_x/a-Si memristor device **a** without implantation and **b** with implantation. Voltage and current curves of **a**, **b** in temporal space for **c** the unimplanted and **d** implanted devices (*V*–*I*–*t* curves).

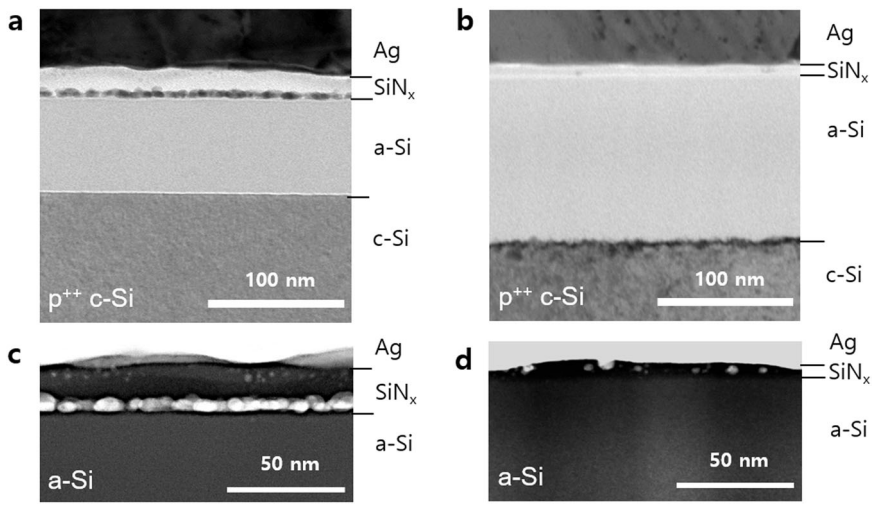

Fig. 4 Ag nanocluster distributions in the switching layers. XTEM images of **a** unimplanted and **b** implanted devices. The SiN_x switching layers with Ag nanoclusters are denoted by dashed rectangles. STEM images of the Ag nanoclusters within the SiN_x layer for the **c** unimplanted and **d** implanted devices. The brighter particles with strong contrast in the SiN_x layer are the Ag nanoclusters.

effective suppression of the abrupt current increase upon the set transition. To investigate the origin of the SiN_x/a-Si bilayer device behavior, a TEM study was conducted.

Ag nanocluster formation and device size dependence

XTEM images of the unimplanted and implanted devices after potentiation were taken and are shown in Fig. 4a, b. The potentiation for both devices was performed by applying 500 repetitive pulses of a 7.0-V amplitude and a 100-ms width. Ag nanoclusters were observed to be distributed within the thin layer of SiN_x in both cases, but the sizes and distributions of the Ag nanoclusters are very different. No Ag nanoclusters are observed in the a-Si underlayer. In the unimplanted device, the Ag nanoclusters are dominantly located at the SiN_x/a-Si interface with smaller nanoclusters within the SiN_x thin film. By contrast, in the implanted device, preferred sites for the Ag nanoclusters are not observed, and the Ag nanoclusters are randomly distributed within the SiN_x film. The STEM images at higher magnification more clearly reveal the existence of Ag clusters, as shown in Fig. 4c, d. Repetitive voltage pulses induce the

migration of Ag nanoclusters in the SiN_x thin layer. It is well known that Ag migration is more facilitated in dielectric materials such as SiN_x and SiO_x than in a-Si due to the differences in diffusivity[31,32]. For this reason, no Ag nanoclusters in the a-Si underlayer are observed, and the a-Si underlayer serves as a diffusion barrier for Ag in both devices. At the same time, the underlayer a-Si layer works as an internal resistor to suppress abrupt current changes caused by set switching.

The TEM results reveal that the current flow is not dominated by one strong filament but is formed by the randomly distributed Ag nanoclusters in the SiN_x layer. The conductance changes with repetitive pulses and the retention time are considered to be correlated with the Ag nanocluster morphologies. The size of the Ag nanoclusters densely distributed at the SiN_x/a-Si interface is 5.91 nm (±1.37 nm) on average. The preferred formation of Ag nanoparticles at the interface of a dielectric and Si has been reported in the literature and is considered to be related to the stress induced during thin film deposition of PECVD SiN_x on crystalline Si[31,32]. The preferred Ag formation at the interface seems to deplete Ag in the center zone of the SiNx film along the depth. Near the Ag TE region, small Ag nanoclusters with an average size of 2.02 nm (±0.62 nm) are observed. By contrast, the Ag nanoclusters in the case of the implanted device with potentiation are uniformly distributed within the SiN_x film, and the size is 2.84 nm (±1.96 nm) on average, which is greater than that in the case of the unimplanted device. Elemental analysis of the nanoclusters in the SiN_x film was performed using high-resolution TEM to confirm whether the nanoclusters were Ag, as given in supplementary information (Fig. S3). The nucleation and growth behavior of the Ag nanoclusters might be affected by implantation-induced defects on the surface of the a-Si layer. The increased defect density at the top interface region of the a-Si layer is likely to affect the Ag cluster formation at the SiN_x/a-Si interface. The TEM results show that the preferred Ag formation at the SiN_x/a-Si interface is greatly suppressed with Ge implantation. It can be deduced that the increased vacancies at the surface of the implanted a-Si region, as calculated by the TRIM simulation, relax the stress with the aid of vacancies induced by implantation, resulting in suppression of the preferred Ag nanocluster formation at the interface. The chemical effect of the implanted Ge element seems to be negligible since the Ge implanted in the top surface region of the a-Si layer is <0.1%, and Ag clusters are only observed in the SiN_x layer. Further study is needed to clarify this.

Detailed analysis of the current–voltage curves shown in Fig. 2a provides further information about conductive filament formation. The slopes of the current–voltage curves of the unimplanted and implanted devices in the log–log plot were extracted and are shown in supplementary information (Fig. S4 and Table S1). Both devices show gradually increasing slopes as the applied voltage increases. Abrupt changes in the slope were observed at a certain voltage, where it is considered that Ag ions are injected and nanoclusters are formed. Above the threshold voltage, the current increases very fast, so the slope is also high in both devices. The average threshold voltages are 2.9 and 3.2 V, respectively. The threshold voltage is related to the kinds of active metals and dielectric materials. The slopes of the on-state devices for both cases do not exhibit ohmic behavior because the slopes are in the range of 1–3. This supports that the devices do not have a strong conductive filament but have multiple weak filaments.

We also prepared an unimplanted device of a 5.5-nm thickness similar to the implanted device for fair comparison. The unimplanted device with a thinner SiN_x switching layer did not show a memresistive switching behavior; no repeatable hysteresis in DC current–voltage curves was observed, as shown below. In XTEM analysis, silver nanoclusters in the switching layer, even after a potentiation process, were not observed. It seems that the thinner switching layer (SiN_x) leads to increased leakage, resulting in reduced silver migration and suppressed cluster formation. The XTEM image and DC current–voltage characteristics are presented in supplementary information (Fig. S5).

The random and uniform distribution of the Ag nanoclusters may lead to interface-type behavior, which can be confirmed by analyzing devices with various cell areas. The circular via-hole size was varied from 5 to 20 μm, and the current–voltage characteristics of the implanted devices are presented in Fig. 5a. The current flow in filamentary memristor devices is dominated by a strong filament on the nanoscale; thus the device resistance is insensitive to the cell size[33]. Unlike strong filamentary-type devices, the implanted devices exhibit a clear dependency on the size of the via-hole. If the device is completely an interface-type device, then the resistance (R) and the cell diameter (d) obey the relationship $R \sim 1/d^2$ [34,35]. Figure 5b shows that the slope of the device resistance and via-hole size curve on the log–log scale takes values in the range of 2–3, supporting that the implanted devices work similarly to the interface-type device in terms of the device size dependency due to the multiple weak filaments.

Analog synapse behavior of the unimplanted and implanted devices

To implement neural network computing hardware with a high learning accuracy, a low nonlinearity of synaptic weights with repetitive input pulses and a large on/off synapse conductance ratio are required[36]. Synaptic

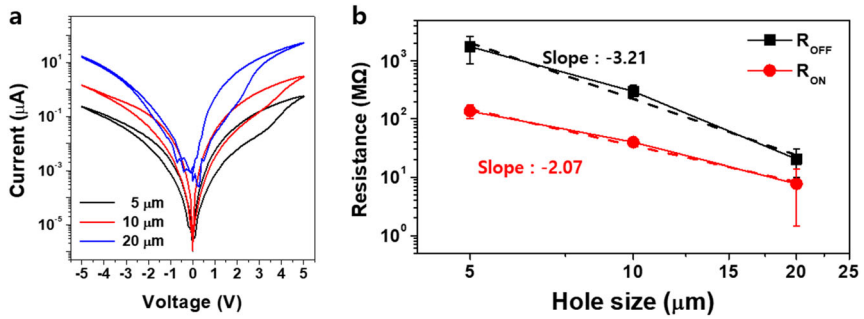

Fig. 5 Device size dependency. a Characteristic current–voltage curves of the implanted devices with varying via-hole size. **b** *R* vs. via-hole size of the implanted devices. The resistance (*R*) values were determined at a bias of 1.0 V.

potentiation and depression curves for both devices are presented in Fig. 6a, b. As seen in the figure, for the nonlinearity parameter in potentiation, both devices have similar values. However, the synapse conductance of the unimplanted devices in depression drops more abruptly with repetitive pulses than that of the implanted devices. The nonlinearity values of the unimplanted and implanted devices in potentiation and depression were extracted using the following equations[37].

$$G_{\mathrm{P}} = B\left[1 - e^{-\nu_{\mathrm{P}}P}\right] + G_{\mathrm{min}},$$

$$G_{\mathrm{D}} = G_{\mathrm{max}} - B\left[1 - e^{-\nu_{\mathrm{D}}(P-P_{\mathrm{max}})}\right],$$

$$B = \frac{G_{\mathrm{max}} - G_{\mathrm{min}}}{1 - e^{\nu}P_{\mathrm{max}}},$$

where G_{P} and G_{D} are the conductances for potentiation and depression, respectively. G_{max} and G_{min} are the maximum and minimum conductances extracted from the experimental results. P and P_{max} are the number of pulses and the maximum pulse number in each mode, respectively. ν_{P} and ν_{D} are the nonlinearities of the memristor conductance update in potentiation and depression, respectively, and are determined by fitting the above equations to the experimental results.

The extracted nonlinearities of the conductance update and the conductance on/off ratios of the unimplanted and implanted devices with varying number of pulses and voltage amplitude are provided in Table 1. The on/off ratio of the implanted device is much greater than that of the unimplanted device for the overall pulse numbers. The abrupt decreases in the device conductance in depression are considered to be related to the volatility of the memristor devices. This will be more discussed later in this section. The lower on/off ratios of the unimplanted device are attributed to a more resistive a-Si underlayer compared with the implanted device. The resistive unimplanted a-Si layer, which serves as an internal current limiter, limits current flow, resulting in limited Ag migration into the SiN_x layer with multiple voltage pulses. In contrast, the conductance of the implanted a-Si layer increases by nearly two orders of magnitude, as shown in Fig. 2b; thus the current flow increases at a given voltage compared with the unimplanted device. The increased current leads to enhanced Ag migration, resulting in increased Ag clusters in the SiN_x thin film and in turn a higher on/off ratio. The internal current limiter, the a-Si layer, plays an important role in the realization of the analog behavior. To investigate the role of the a-Si underlayer in the switching behavior, we fabricated memristor devices consisting of Ag/SiN_x/p^{++} Si with no a-Si layer, and the current–voltage characteristics are presented in Fig. S6. If we remove the a-Si layer in the memristor device, then the current during the set transition increases abruptly, and strong filamentary memristor behavior is observed. The size of the conductive filaments can be adjusted by setting a compliance current, but the gradual switching behavior was hardly observed. The threshold switching behavior was observed when the compliance current was set to be $<10^{-6}$ A. The compliance current approach only limits the current during device operation when the current reaches the set value. In contrast, when an internal current limiting layer is inserted, an abrupt current increase can be suppressed by the voltage divider concept. Furthermore, the on/off ratio can be adjusted by varying the resistance of the internal current limiting layer by changing the thickness, implantation dose, etc. To evaluate the endurance of the implanted device, 500 cycle tests of repetitive potentiation and depression were conducted, and the results are presented in Fig. 6c. The potentiation and depression curves after every 20 cycles are shown. Although slight changes in the on/off ratio are observed, the changes in the potentiation/depression nonlinearity can be neglected. Cycle-to-cycle and device-to-device variations are also important factors for synaptic operations. We extracted these parameters for the unimplanted and implanted devices and compared them in supplementary

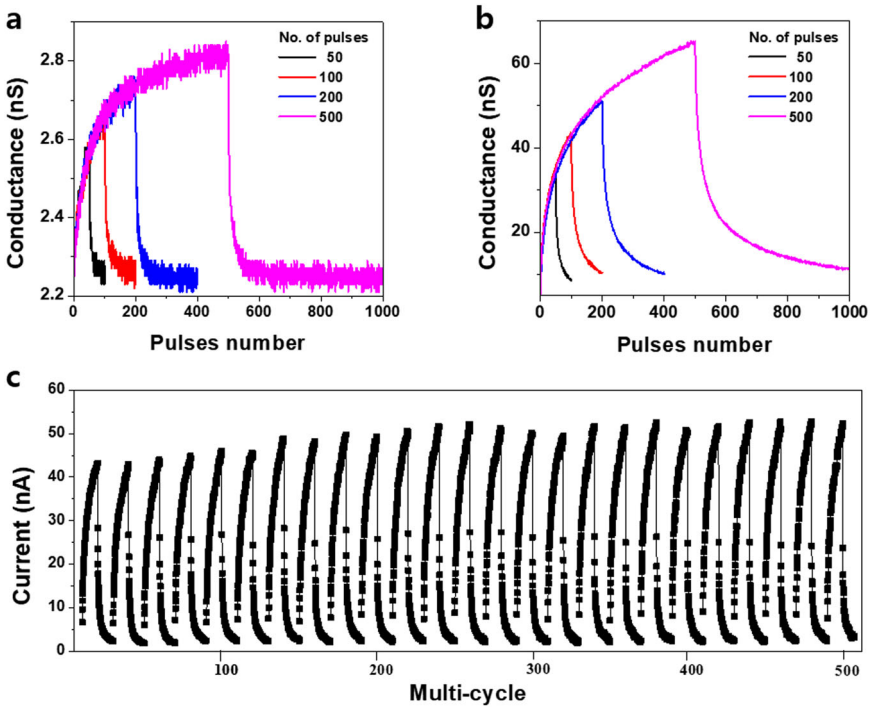

Fig. 6 Synpatic potentiation and depression. a Conductance updates of the unimplanted device with varying number of pulses (50, 100, 200, 500). The write voltages in potentiation and depression were 7.0 and −3.0 V, respectively. The read voltage was 2.0 V in both modes. **b** Conductance updates of the implanted device with the same numbers of pulses. The write and read voltages were 7.0 and −3.0 V. The read voltage was 1.0 V in both modes. **c** Repetitive potentiation and depression curves with 100 repetitive pulses in each mode. The write voltages were 7.0 and −4.0 V in potentiation and depression, respectively. The read voltage was 1.0 V in both modes. The potentiation and depression curves of every tenth cycle are presented. In all cases, the pulse width was set to 10 ms.

Table 1 Nonlinearity factors and on/off ratios of the unimplanted and implanted devices.

Number of pulses	Unimplanted device			Implanted device		
	Nonlinearity factor		On/off ratio	Nonlinearity factor		On/off ratio
	Potentiation	Depression		Potentiation	Depression	
50	4.32	−10.94	1.07	2.61	−7.08	8.80
100	4.08	−14.99	1.08	2.82	−5.78	9.77
200	6.12	−21.87	1.11	2.83	−6.85	12.87
500	12.43	−28.86	1.14	3.10	−6.27	13.50

information (Fig. S7 and Table S2). The results show that the implantation greatly reduced the device variations.

Retention time of the unimplanted and implanted devices

A long retention time is essential for implementation of long-term memory. We estimated the memory retention time of the unimplanted and implanted devices after potentiation. Five hundred pulses with varying voltage amplitude (5.0, 6.0, 7.0 V) and a 100-ms duration were applied to the implanted devices, and the conductance decay was measured as a function of time (Fig. 7). The retention time parameter was extracted by fitting the conductance decay curves to the following equation[38].

$$\frac{G_0 - G_t}{G_0} = A_1 \exp\left(-\frac{t}{\tau_{\text{short}}}\right) + A_2 \exp\left(-\frac{t}{\tau_{\text{long}}}\right) + M_0,$$

where G_0 and G_t are the conductances at the initial time and at a certain time t, respectively. τ_{short} and τ_{long} are short- and long-term retention time constants, which are

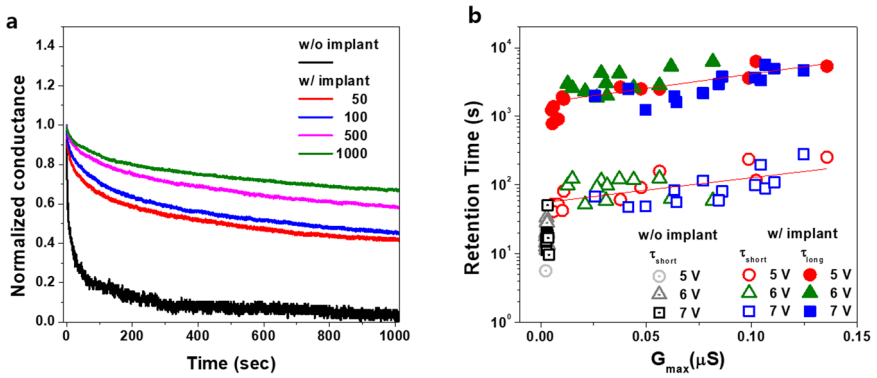

Fig. 7 Long term memory retention time. a Selected conductance decay curves after repetitive voltage (7.0 V) pulses with a 100-ms width for the unimplanted and implanted devices. The applied number of pulses was 500 for the unimplanted device and was 50, 100, 500, and 1000 for the implanted device. **b** Retention time constants extracted from the conductance decay curves for the unimplanted and implanted devices with varying voltage amplitude (5.0, 6.0, 7.0 V) and number of pulses. The voltage pulse width was set to 100 ms.

extracted from the experimental results. A_1, A_2, and M_0 are parameters for fitting the experimental data to the above equation. M_0 represents the memory retention in the long term.

In the case of the implanted devices, two kinds of characteristic time constants of short term (τ_{short}) and long term (τ_{long}) were determined using the above forgetting function. For the unimplanted devices, only the short-term time constant was extracted because of its high volatility. Selected decay curves of the unimplanted and implanted devices are presented in Fig. 7a. The long-term time constants of the implanted devices are in the range of 10^3–10^4 s, and the short-term time constants are approximately one order of magnitude shorter. A linear correlation between the retention time and the maximum conductance for the implanted devices is observed in a semilog plot, as denoted by the line in Fig. 7b. Only the short-term time constant is presented for the unimplanted device, and no clear dependence of the conductance on the retention time was observed in this case. The maximum conductance values of the implanted devices were increased by increasing the number of pulses and the voltage amplitude. The memory decay mechanism in a CBRAM based on dielectric materials is known to be caused by the surface diffusion of metal elements[39]. The repetitive voltage pulses (potentiation) induce the formation of Ag nanoclusters in the SiN_x thin film. The maximum conductance values after potentiation depend on the morphology of the Ag nanoclusters, such as the size and distribution. A greater voltage amplitude and more pulses lead to greater conductance values, as presented in Fig. 7b. The lifetime of nanoscale conductive filaments in CBRAM devices follows Herring's scaling law[40], where the filament lifetime (τ) increases as a function of the filament size (d_0): $\tau \sim {d_0}^4$ [39]. The decay of the conductance is considered to arise from the surface diffusion of Ag caused by the Gibbs–Thomson effect[41–45]. As confirmed by the TEM images in Fig. 4, Ag nanoclusters are formed and randomly distributed in the SiN_x thin film after potentiation, and the electronic current flows via the closely connected nanoclusters. When the voltage pulses are removed, the size of the Ag nanoclusters is reduced by surface diffusion, and as a result, the conductance decreases. The initial abrupt decay of the conductance in the retention time measurement might be attributed to the fragmentation or dissolution of small-size nanoclusters into a-Si, and the subsequent gradual decay is due to that of the larger-size nanoclusters. This would be a cause of the abrupt decay in the depression curves of the unimplanted devices. Additionally, as the maximum conductance increases, the size of the nanoclusters increases accordingly, resulting in increased retention time. Both of the time constants (τ_{short}, τ_{long}) increase with increasing maximum conductance.

Schematics of the operation mechanisms of the Ag/SiN_x/(unimplanted, implanted) a-Si device below the forming voltage are illustrated in Fig. 8a–d. The a-Si underlayer works as an internal current limiter and is denoted as a resistor. The resistance of the unimplanted a-Si is approximately two orders of magnitude higher than that of the implanted a-Si. The two figures at the top present the Ag morphologies immediately after potentiation, and the two figures at the bottom show them after a time comparable to the short-term time constant (τ_{short}). The size of the Ag nanoclusters in the unimplanted device in the initial stage is smaller than that in the implanted device. After a certain time τ_{short}, the small-size Ag nanoclusters are dissolved into smaller ones in both cases, resulting in an abrupt conductance decrease in both devices. The Ag nanoclusters in the center zone of the unimplanted device are depleted by the preferred

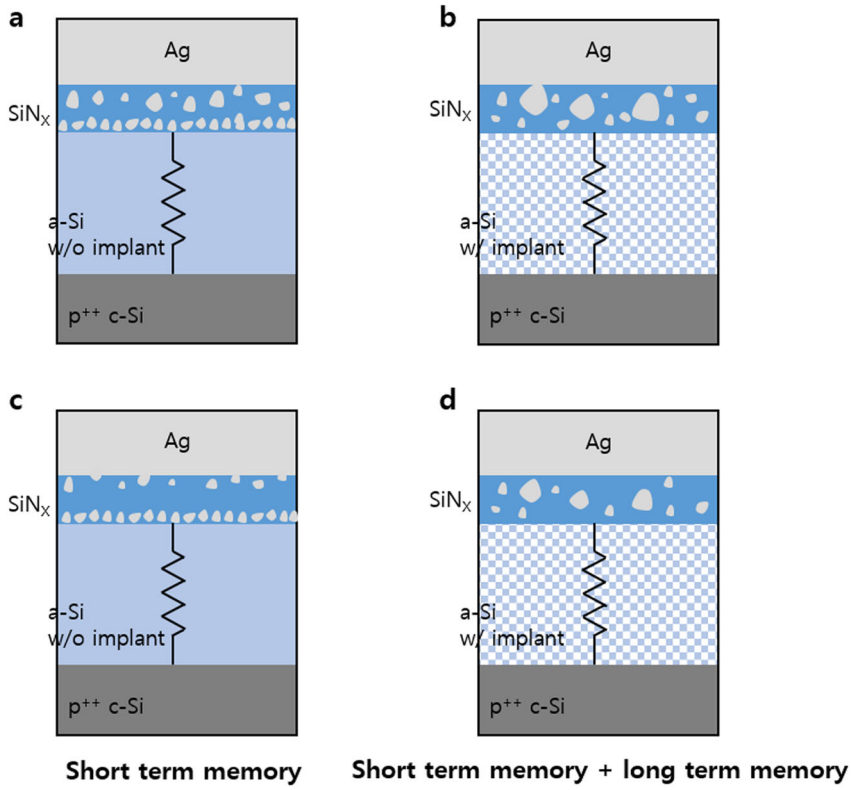

Fig. 8 Proposed operation mechanism. Schematics of Ag nanoclusters in the SiN_x layer immediately after potentiation with multiple voltage pulses of the **a** unimplanted devices and **b** implanted devices. Schematics of Ag nanoclusters at a time comparable to the short time constant (τ_{short}) after voltage pulses are removed for the **c** unimplanted and **d** implanted devices.

formation of Ag nanoclusters at the interface, and the loss of the long-term memory is attributed to this phenomenon. In contrast, the implanted device has large-size Ag nanoclusters in the layer, maintaining long-term memory. The unimplanted device has only a short lifetime and behaves like a short-term memory, whereas the implanted device has both long and short lifetimes and exhibits both short- and long-term memory behavior. When a voltage greater than the forming voltage is applied, a strong filament is formed across the SiN_x/a-Si bilayer; thus a binary switching behavior is exhibited, as presented in Fig. S1.

Artificial neural network simulation

We performed an artificial neural network simulation for supervised learning in MNIST classification with consideration of nonlinear synaptic weight updates with repetitive pulses, as shown in Table 1. For the simulation, we adopted an MLP algorithm with one hidden layer, 28×28 input neurons, and 10 output neurons. The nonlinearities of the unimplanted and implanted devices with varying number of pulses were considered in the simulation. The detailed hyperparameters used in the simulations are described in the "Methods" section. When a memristor-based neural network is trained, the synapse weights need to be changed gradually and linearly with consecutive identical voltage pulses in potentiation or depression[46,47]. Otherwise, the precise synapse weight update for error minimization in training can hardly be achieved. In this regard, in general, a multilevel synapse with a high linearity for the artificial neural network is desirable for high accuracy pattern recognition[48]. As shown in Table 1, the implanted devices in comparison with the unimplanted devices have lower nonlinearity values in both modes (potentiation and depression) and higher on/off ratios, which are required for multilevel operations. As a result, the implanted synaptic devices provide a higher pattern recognition accuracy. The MLP neural network structure used for the simulation is illustrated in Fig. 9a. The learning accuracies of the neural networks based on the implanted devices improve with increasing number of conductance states, as shown in Fig. 9b. The degraded learning accuracy of the unimplanted devices with >200 conductance states is attributed to the deteriorated linearity. In contrast, the nonlinearity values of the implanted devices relatively do not change in both the potentiation and depression modes. After 100 epochs of training, the unimplanted device only provides a 62.8% learning accuracy with 100 conductance levels,

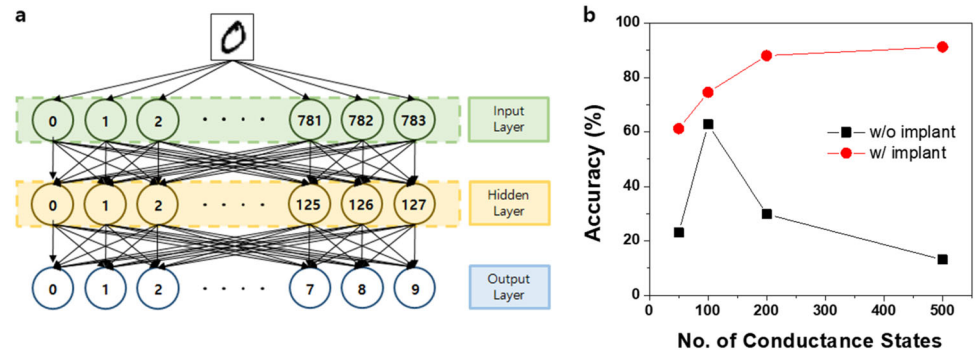

Fig. 9 MNIST recognition accuracy of the memristive neural network. a Schematic illustration of the MLP neural network for an MNIST pattern recognition test. **b** Learning accuracy of the neuromorphic system with the analog memristors after 100 epochs of training. The nonlinear synapse updates in Table 1 are considered in the simulation. The number of conductance states for the analog memristors is varied from 50 to 100, 200, and 500.

whereas the implanted device presents a 91.3% accuracy at 500 conductance levels. The achieved learning accuracy is very comparable to the state-of-the-art results in the literature[36,46,49].

Conclusions

In this study, we demonstrate that the analog memristor behavior required for neuromorphic computing hardware can be remarkably improved by Ge ion implantation. The memristor devices consisting of a SiN_x/a-Si bilayer with a Ag active electrode exhibit poor analog behavior below the forming voltage: high nonlinearity of synapse weight updates, a low on/off ratio, and volatility (low retention time). Ge ion implantation into the a-Si underlayer substantially modifies the devices by inducing structural defects and increasing the conductance of the a-Si layer. This promotes spatially uniform Ag cluster formation in the switching layer of SiN_x, and as a result, the linearity of the synapse weight updates, the on/off ratio, and the retention time are greatly improved. The Ag cluster formation was observed to be randomly distributed in the SiN_x layer, as confirmed by TEM. The implanted SiN_x/a-Si bilayer devices are of the interface type, where a uniform current flows through nearly the entire cell area. The synapse weight update model with identical consecutive voltage pulses was implemented in an artificial neural network simulation for supervised learning in MNIST classification. The implanted device provides an improved learning accuracy of 91.3% with 500 conductance states compared with the unimplanted device, which shows only 62.8%.

Acknowledgements
This work was supported by the Korea Institute of Science and Technology (Grant No. 2E30610, 2E30761), the Korea Institute of Energy Technology Evaluation and Planning (Grant No. 20163010012450), and the National Research Foundation of Korea (NRF) (NRF-2019M3F3A1A02072175).

Author details
[1]Center for Neuromorphic Engineering, Korea Institute of Science and Technology, Seoul 02792, South Korea. [2]School of Electrical Engineering, Korea University, Seoul 02841, South Korea. [3]Division of Materials Science and Engineering, Hanyang University, Seoul 04763, South Korea. [4]Center for Advanced Analysis, Korea Institute of Science and Technology, Seoul 02792, South Korea

Conflict of interest
The authors declare that they have no conflict of interest.

Supplementary information is available for this paper at https://doi.org/10.1038/s41427-020-00261-0.

Received: 24 June 2020 Revised: 19 October 2020 Accepted: 28 October 2020.
Published online: 11 December 2020

References

1. Mead, C. Neuromorphic electronic systems. *IEEE* **78**, 8 (1990).
2. Indiveri, G. & Liu, S.-C. Memory and information processing in neuromorphic systems. *Proc. IEEE* **103**, 1379–1397 (2015).
3. Ionescu, A. M. Energy efficient computing and sensing in the Zettabyte era: from silicon to the cloud. *IEDM Tech. Dig.* https://doi.org/10.1109/IEDM.2017.8268307 (2017).
4. Lim, S., Kwak, M. & Hwang, H. Improved synaptic behavior of CBRAM using internal voltage divider for neuromorphic systems. *IEEE Trans. Electron Devices* **65**, 3976–3981 (2018).
5. Jo, S. H. et al. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10**, 1297–1301 (2010).
6. Burr, G. W. et al. Neuromorphic computing using non-volatile memory. *Adv. Phys. X* **2**, 89–124 (2016).
7. Suri, M. *Advances in Neuromorphic Hardware Exploiting Emerging Nanoscale Devices* (Springer, 2017).
8. Park, S. et al. RRAM-based synapse for neuromorphic system with pattern recognition function. *IEDM Tech.* https://doi.org/10.1109/IEDM.2012.6479016 (2012).
9. Woo, J. et al. Improved synaptic behavior under identical pulses using AlOx/HfO_2 bilayer RRAM array for neuromorphic systems. *IEEE Electron Device Lett.* **37**, 994–997 (2016).
10. Chen, W., Tappertzhofen, S., Barnaby, H. J. & Kozicki, M. N. SiO_2 based conductive bridging random access memory. *J. Electroceram.* **39**, 109–131 (2017).

11. Wan, Q., Sharbati, M. T., Erickson, J. R., Du, Y. & Xiong, F. Emerging artificial synaptic devices for neuromorphic computing. *Adv. Mater. Technol.* https://doi.org/10.1002/admt.201900037 (2019).
12. Min, D.-H., Ryu, T.-H., Yoon, S.-J., Moon, S.-E. & Yoon, S.-M. Improvements in the synaptic operations of ferroelectric field-effect transistors using $Hf_{0.5}Zr_{0.5}O_2$ thin films controlled by oxygen partial pressures during the sputtering deposition process. *J. Mater. Chem. C* **8**, 7120–7131 (2020).
13. Kim, M.-K. & Lee, J.-S. Ferroelectric analog synaptic transistors. *Nano Lett.* **19**, 2044–2050 (2019).
14. Tokumitsu, E. Electrical properties of metal-ferroelectric-insulator-semiconductor (MFIS)- and metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-FETs using ferroelectric $SrBi_2Ta_2O_9$ film and $SrTa_2O_6$ SiON buffer layer. *Jpn. J. Appl. Phys.* **39**, 6 (2000).
15. Ambriz-Vargas, F. et al. Tunneling electroresistance effect in a $Pt/Hf_{0.5}Zr_{0.5}O_2/Pt$ structure. *Appl. Phys. Lett.* https://doi.org/10.1063/1.4977028 (2017).
16. Subhechha, S. Kinetic defect distribution approach for modeling the transient, endurance and retention of a-VMCO RRAM. *IEEE Int. Reliability Phys. Symp.* https://doi.org/10.1109/IRPS.2017.7936322 (2017).
17. Chen, W. et al. A CMOS-compatible electronic synapse device based on $Cu/SiO_2/W$ programmable metallization cells. *Nanotechnology* **27**, 255202 (2016).
18. Kim, M.-K. & Lee, J.-S. Design of electrodeposited bilayer structures for reliable resistive switching with self-compliance. *ACS Appl. Mater. Interfaces* **8**, 32918–32924 (2016).
19. Ilyas, N. et al. Analog switching and artificial synaptic behavior of Ag/SiO_x:Ag/TiO_x/p(++)-Si memristor device. *Nanoscale Res. Lett.* **15**, 30 (2020).
20. Mahalanabis, D. et al. Incremental resistance programming of programmable metallization cells for use as electronic synapses. *Solid State Electron.* **100**, 39–44 (2014).
21. Bishop, S. M., Rice, Z. P., Briggs, B. D., Bakhru, H. & Cady, N. C. Synthesis of resistive memory oxides by ion implantation. *MRS Proc.* https://doi.org/10.1557/opl.2012.934 (2012).
22. Nandi, S. K. et al. Room temperature synthesis of HfO_2/HfO_x heterostructures by ion-implantation. *Nanotechnology* **29**, 425601 (2018).
23. Liu, Q. et al. Resistance switching of Au-implanted-ZrO2 film for nonvolatile memory application. *J. Appl. Phys.* https://doi.org/10.1063/1.3033561 (2008).
24. Liu, Q. et al. Resistive switching memory effect of ZrO[sub$_2$] films with Zr[sup$^+$] implanted. *Appl. Phys. Lett.* https://doi.org/10.1063/1.2832660 (2008).
25. Gao, L., Hoskins, B., Zaynetdinov, M., Kochergin, V. & Strukov, D. The effect of Ti and O ion implantation on the resistive switching in $Pt/TiO_{2-x}/Pt$ devices. *Appl. Phys. A* **120**, 1599–1603 (2015).
26. Custer, J. S. et al. Density of amorphous Si. *Appl. Phys. Lett.* **64**, 437–439 (1994).
27. Ziegler, J. F. High energy ion implantation. *Nucl. Instrum. Methods Phys. Res. Sect. B Beam Interact. Mater. At.* **6**, 270–282 (1985).
28. Kinchin, G. H. & Pease, R. S. The displacement of atoms in solids by radiation. *Rep. Prog. Phys.* https://doi.org/10.1088/0034-4885/18/1/301 (1955).
29. Di Bartolomeo, A. et al. Asymmetric Schottky contacts in bilayer MoS_2 field effect transistors. *Adv. Funct. Mater.* **28**, 1800657 (2018).
30. Zhao, J., Rebohle, L., Gebel, T., von Borany, J. & Skorupa, W. Bulk-limited conduction of Ge-implanted thermally grown SiO_2 layers. *Solid State Electron.* https://doi.org/10.1016/S0038-1101(01)00322-7 (2002).
31. Ishikawa, J. et al. Formation of almost delta-layered nanoparticles in SiO2 thin film on Si substrate by metal negative-ion implantation. *Nucl. Instrum. Methods Phys. Res. Sect. B Beam Interact. Mater. At.* **237**, 422–427 (2005).
32. Pugliara, A. *Elaboration of Thin Nanocomposite Layers based on Ag Nanopartiles Embedded in Silica for Controlled Biocide Properties*. PhD thesis, Univ. Toulouse 3 Paul Sabatier (2016).
33. Yuan, F. et al. Real-time observation of the electrode-size-dependent evolution dynamics of the conducting filaments in a SiO_2 layer. *ACS Nano* **11**, 4097–4104 (2017).
34. Qu, B. et al. Synaptic plasticity and learning behavior in transparent tungsten oxide-based memristors. *Mater. Des.* **129**, 173–179 (2017).
35. Younis, A., Chu, D. & Li, S. Evidence of filamentary switching in oxide-based memory devices via weak programming and retention failure analysis. *Sci. Rep.* **5**, 13599 (2015).
36. Yu, S. Neuro-inspired computing with emerging nonvolatile memorys. *Proc. IEEE* **106**, 260–285 (2018).
37. Agarwal, S. Resistive memory device requirements for a neural algorithm accelerator. *Int. Jt. Conf. Neural Networks.* https://doi.org/10.1109/IJCNN.2016.7727298 (2016).
38. Wang, Z. Q. et al. Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor. *Adv. Funct. Mater.* **22**, 2759–2765 (2012).
39. Wang, W. et al. Surface diffusion-limited lifetime of silver and copper nanofilaments in resistive switching devices. *Nat. Commun.* **10**, 81 (2019).
40. Herring, C. Effect of change of scale on sintering phenomena. *J. Appl. Phys.* **21**, 301–303 (1950).
41. Mullins, W. W. Theory of thermal grooving. *J. Appl. Phys.* **28**, 333–339 (1957).
42. Wang, Z. et al. Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **16**, 101–108 (2017).
43. Yi, W. et al. Quantized conductance coincides with state instability and excess noise in tantalum oxide memristors. *Nat. Commun.* **7**, 11142 (2016).
44. Shukla, N., Ghosh, R. K., Grisafe, B. & Datta, S. Fundamental mechanism behind volatile and non-volatile switching in metallic conducting bridge ram. In *2017 IEEE International Electron Devices Meeting (IEDM)* 4.3.1–4.3.4 (IEEE, 2017).
45. Thomson, W. L. X. On the equilibrium of vapour at a curved surface of liquid. *Lond. Edinb. Dublin Philos. Mag. J. Sci.* **42**, 448–452 (2009).
46. Shi, Y. et al. Neuroinspired unsupervised learning and pruning with subquantum CBRAM arrays. *Nat. Commun.* **9**, 5312 (2018).
47. Kuzum, D., Jeyasingh, R. G., Lee, B. & Wong, H. S. Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing. *Nano Lett.* **12**, 2179–2186 (2012).
48. Suñé, J. *Memristors for Neuromorphic Circuits and Artificial Intelligence Applications* (MDPI, 2020).
49. Choi, S. et al. SiGe epitaxial memory for neuromorphic computing with reproducible high performance based on engineered dislocations. *Nat. Mater.* **17**, 335–340 (2018).