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A Discharge-Path-Based Sensing Circuit With OTS Snapback Current Protection for Phase Change Memories

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ABSTRACT A discharge-path-based sensing circuit is proposed to reduce the damage caused by an ovonic threshold switch (OTS) snapback current to a phase-change memory (PCM). OTS devices are used as access devices (selectors) in most PCM systems to increase the sensitivity and resolve the leakage current problem that occurs during sensing of the PCM cell. Snapback current, which occurs during an OTS phase change by using the OTS device, causes damage to the PCM device and deteriorates the read performance; thus, this study proposes a discharge path circuit as a new sensing method to reduce the damage inflicted on the PCM. In addition, a gate-coupled PMOS (GCPMOS) and a current mirror using a feed-forward technique are designed to reduce the peak value of the energy applied to the PCM. The discharge path circuit, GCPMOS, and the current mirror are designed in a 180-nm CMOS process and occupy an area of 0.19-mm². The measurement results after fabrication show that, compared to the conventional sense amplifier based scheme, the discharge path circuit reduces the amount of energy applied to the PCM by 21.8%, and the discharge path circuit with the GCPMOS reduces the total energy consumption by 27.7%. Furthermore, the discharge path circuit with a feed-forward current mirror reduces the initial peak level of the PCM current by 10.1% and the total energy consumption by 34.6%. The proposed sensing circuit is the first snapback protection circuit reported to the public domain.

INDEX TERMS Discharge, phase-change memories, sensors, snapback currents.

I. INTRODUCTION

Phase-change memory (PCM) is gaining interest as one of the next-generation memories along with resistive random-access memory (RRAM) and spin-transfer-torque magnetoresistive random access memory (STT-MRAM) [1]–[10]. PCM is a nonvolatile memory with low latency, which is mainly used to resolve the bottleneck between dynamic random-access memory (DRAM) and NAND flash memory [1]–[10]. A PCM distinguishes the on and off states of data based on the difference between the resistances of the

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amorphous and crystalline states [11], [12]. The first PCM was developed in the 1970s [13] but had not been used for a long time owing to its complicated structure in the amorphous state of a phase change material (PM) and large power consumption during melting and crystallization.

Researches on PCM became active after the line-type (L-type) PCM was released by Ovonic-Intel in 2002 [14]. The conventional L-type PCM heats the PM by flowing current through a bipolar junction transistor (BJT). However, the L-type PCM has a higher variation in V_{threset} due to its thermal disturbance (TDB) [15].

The C-type 3-D structure [16]–[18] was proposed to mitigate the TDB effect, where cells are stacked between two

crossing metal lines. In the C-type PCM, ovonic threshold switch (OTS) or mixed ion-electron conductor (MIEC) are used as access devices. The C-type PCM was developed to the X-Point PCM in recent years [19], [20]. However, the X-Point PCM suffers from snap currents in its OTS devices, which are used for implementing access devices [21]. During the read operation, the current flow through the OTS current abruptly increases due to the snapback phenomenon, which adversely affects the reading performance of the OTS-PRAM and inflicts damages on the memory element (PM). Therefore, this study examines the read disturbance and reliability issues in the presence of the OTS snapback current and proposes various techniques including discharge path circuit, gate-coupled PMOS (GCPMOS), and feed-forward current mirror to address the issues.

The remainder of this paper is organized as follows. Section II describes the structure of the X-point PCM and potential reliability issues. Section III presents the architecture and working principles of the discharge path circuit to enhance the robustness of the OTS-PRAM. The architecture and procedure of the GCPMOS and feed-forward current mirror are introduced in Sections IV and V. Measurement results and discussions for each circuit are provided in Section VI to validate the performance of the proposed circuits, and conclusions are drawn in Section VII.

II. SELECTOR OF PHASE-CHANGE MEMORY

Memory cell selection is inevitable during the reading and writing process in an arrayed memory structure [22]. Selector devices are required for the cell-selection processes to perform the read or write operations to the target cell without disturbing other cells.

An ideal memory cell selector has high on-state conductivity (for easy access) and an infinite off-state resistance (to achieve insensitivity to control signals when not selected). The selectors are required to occupy small areas as well to achieve high cell density. While large-sized MOSFETs were initially used for the selector devices [23], due to their poor area efficiency, p-n diodes with selective epitaxial growth were developed to replace the MOSFET selectors [24]. The diodes occupied small areas compared to MOSFETs and achieved low R_{on} and high R_{off} characteristics. However, the area efficiency improvement is limited as contact structures are required for the diode selectors and diode devices suffer from inconsistent $V_{threset}$ due to the TDB.

To overcome such drawbacks of previous selector devices, stackable C-type PCMs have been developed with various OTS-based selector devices [16]–[18]. In this section, we examine various aspects of the OTS device, including its basic operations, the readout method of the OTS-PRAM, and the OTS snapback current problem.

A. OVONIC THRESHOLD SWITCH

OTS-PRAM cell consists of an OTS and a PM (see Fig. 1(a)). The OTS device is a phase change element of which resistance varies depending on its crystalline (on-state) and

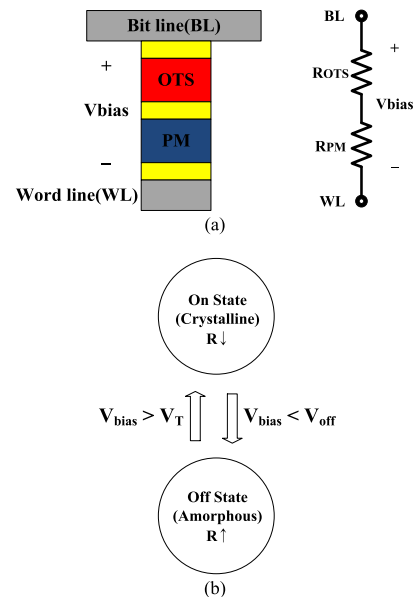


FIGURE 1. (a) Structure and equivalent circuit diagram for a cell stack of X-point PCM and (b) OTS states.

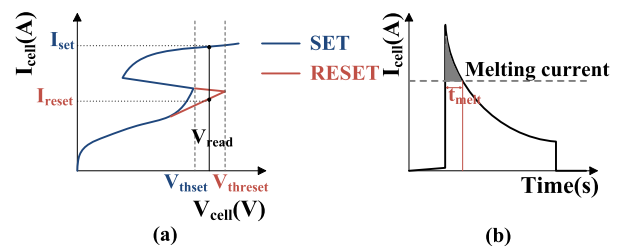


FIGURE 2. (a) I-V curve of OTS-PRAM cell and (b) current graph of PM cell.

amorphous (off-state) states [25]. The state (and resistance) of an OTS device is changed by applying bias voltages and heating the device. Fig. 1(b) shows the phase change process of the OTS device. When V_{bias} in the OTS becomes higher than V_T , which is the on-threshold voltage, the OTS is crystallized and enters the on-state in which the resistance decreases. When V_{bias} becomes lower than V_{off} , which is the off-threshold voltage, the OTS melts and enters the off-state in which the resistance is increased (Fig.1(b)).

By stacking the OTS device with the PM device (which is used for the actual memory element), the OTS-PRAM structure distinguishes between the set and reset states based on the resistance of the PM device. Fig. 2(a) shows the I-V curve of the OTS-PRAM cell in which the OTS and PM are combined. If the read bias voltage (V_{read}) is between the threshold voltage (V_{thset}) in the set state and the threshold voltage ($V_{threset}$) in the reset state, the cell current is determined by the PM state (I_{set} for the set state and I_{reset} for the reset state). By measuring the current flow, the on and off states of the selected cell can be distinguished. It should be noted that the ratio of the set-state current and the reset-state

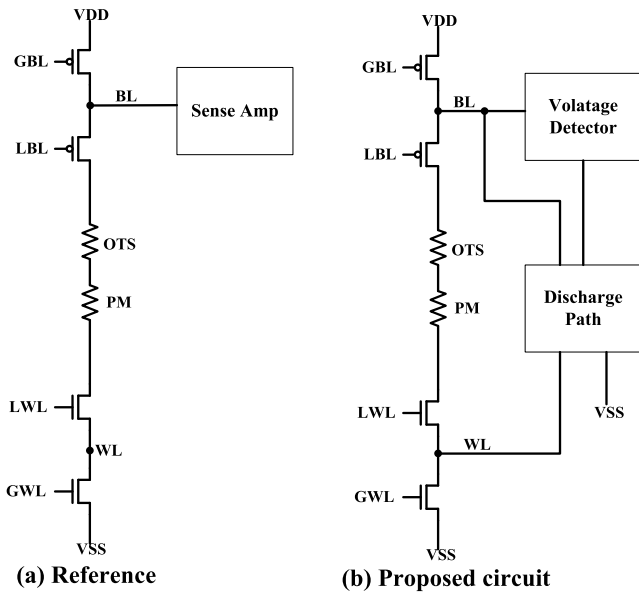


FIGURE 3. Topology of (a) conventional pre-charge scheme and (b) pre-charge scheme with discharge path circuit.

current should be sufficiently large (> 10) to guarantee robust operations across variation in the threshold voltage.

However, as mentioned earlier, the OTS snapback current is generated owing to the snapback phenomenon during the readout operation when the cell is in the set state. The snapback current can damage the PM cell and degrade the reliability characteristics, which are examined further in the next subsection.

B. READ DISTURB WITH OTS SNAPBACK CURRENT

As mentioned in the previous session, the resistance of the OTS device is determined by the bias voltage applied to the device. The resistance decreases significantly when V_{bias} exceeds V_T . Therefore, as shown in Fig. 2(a), when V_{bias} exceeds V_{thset} while the cell is in the set state, the resistance of the OTS abruptly decreases. This causes a drastically increased current flow through the cell, which is referred to as an OTS snapback current [21], [26]–[29].

If the snapback current is greater than the current needed to melt the PM (I_{melt}), the PM undergoes amorphization. If I_{cell} in Fig. 2(b) is greater than I_{melt} , the PM enters the amorphous state and distorts the stored data. In addition to the disturbance, the continuing injection of snap current can severely damage the cell and reduce its lifetime.

Therefore, new circuit techniques are required to reduce the damage inflicted by the OTS snapback current on the cell. In this study, we introduce the discharge path circuit to reduce the overall OTS snapback current. The discharge path is also combined with additional assistance techniques such as GCPMOS and current mirror to reduce the peak snapback current (I_{MAX}).

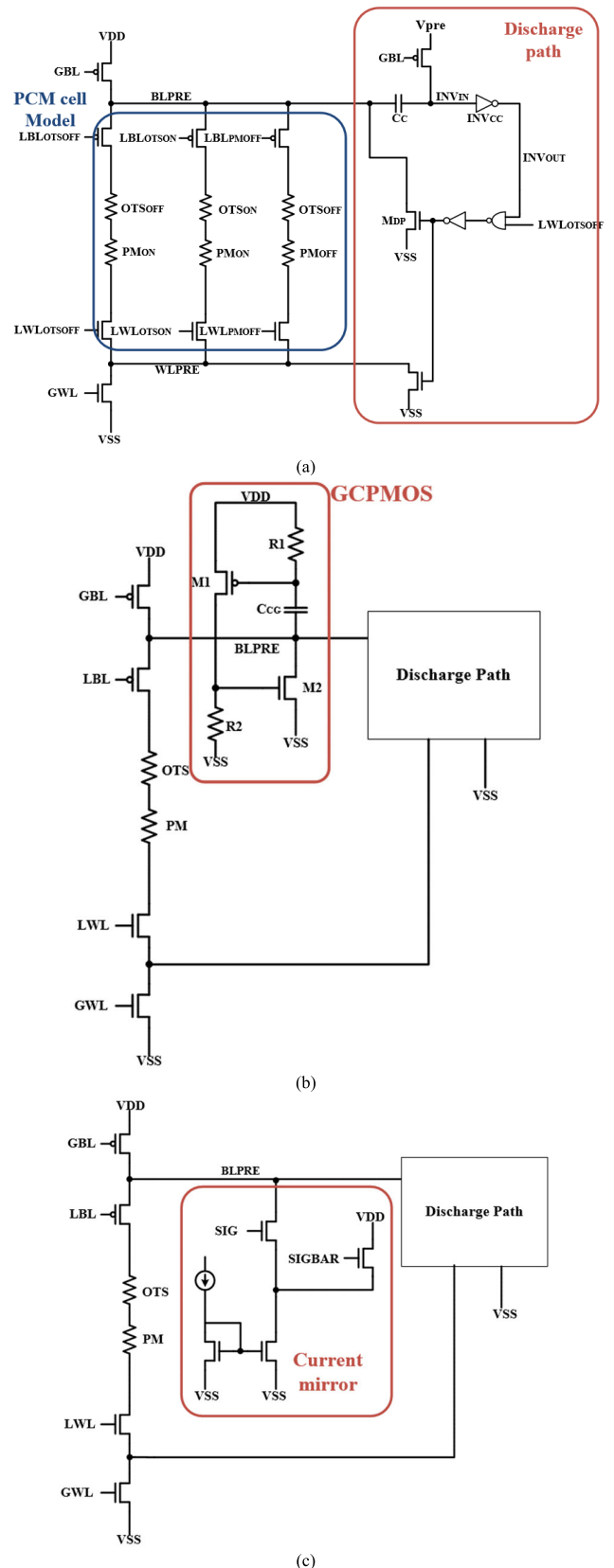


FIGURE 4. Architecture of the PCM modeling with (a) the discharge path circuit, (b) GCPMOS, and (c) feed-forward current mirror.

III. CIRCUITS FOR PCM PROTECTION

Fig. 3 (a) shows the typical structure of a PCM unit cell with its access transistors and readout circuitry. Global bit-line/wordline signals (GBL and GWL) are enabled when the sub-array that the unit cell belongs to is selected, and the unit cell is accessed through the local enable signals (LBL and LWL), to read-out the stored value by triggering the sense amplifier. If the snapback current is generated, the current directly flows through the cell in the conventional structure. Therefore, we propose the discharge path circuit (Fig. 3(b)) to reduce the total energy flowing in the cell by discharging the current through a separate path after sensing. The behavior of the discharge path is explained and analyzed in detail in the following paragraph, with a proper modeling circuit to emulate the current profile of the PCM structure in various modes of operation.

A. ARCHITECTURE OF THE DISCHARGE PATH CIRCUIT

Fig. 4(a) shows the detailed structure of the discharge path circuit and PCM cell modeling circuit. In this structure, for read operations, the transistors at the GBL and GWL select the desired cell array group and pre-charge the BLPRE node before actual sensing process occurs. The local section signals (LBLs and LWLs) turn on the access to the target cell. In order to emulate the behavior of the PCM cell in a conventional CMOS process, we introduced the PCM cell modeling circuit (blue box in Fig. 4(a)). The PCM cell model consists of R_{OTS} and R_{PM} , corresponding to the equivalent resistance of the OTS and PM devices, respectively. Various LBL/LWL switches (LBL_{OTSON} , LBL_{OTSOFF} , LBL_{PMOFF} , LWL_{OTSON} , LWL_{OTSOFF} , and LWL_{PMOFF}) are implemented to model the behavior of the PCM cell in different regions. For example, when the PM is in the set state, LBL_{OTSOFF} , LWL_{OTSOFF} , and LBL_{OTSON} , LWL_{OTSON} are turned on in order during the reading process; thus, the net resistance increase first and decreases as the OTS state shifts from off-state (R_{OTSOFF}) to on-state (R_{OTSON}). We also attached the 50fF loading capacitance to the modeling circuit to capture the array loading effect. When the PM was in the reset state, LBL_{PMOFF} and LWL_{PMOFF} are enable to turn on the high-resistance path corresponding to the reset state.

The discharge path circuit utilizes capacitive coupling to sense the abrupt voltage transient associated with the snapback operation. When the PM is in reset state, the charge of the BLPRE is hardly discharged due to the high resistance of PCM cell; therefore, the pre-charged voltage V_{BLPRE} remains consistent and the capacitive-coupled inverter output (V_{INVOUT}) is not flipped. On the other hand, when the PM is in the set state, V_{BLPRE} drops significantly due to the low resistance of the PCM cell. This voltage transient triggers the following inverter through the coupling capacitor (C_C) and flips the value of the following inverter output, turning on the discharge path to enable the side-current path to VSS and protect the PCM cell. It should be noted that the discharge path is activated based on the state of the PCM cell, the

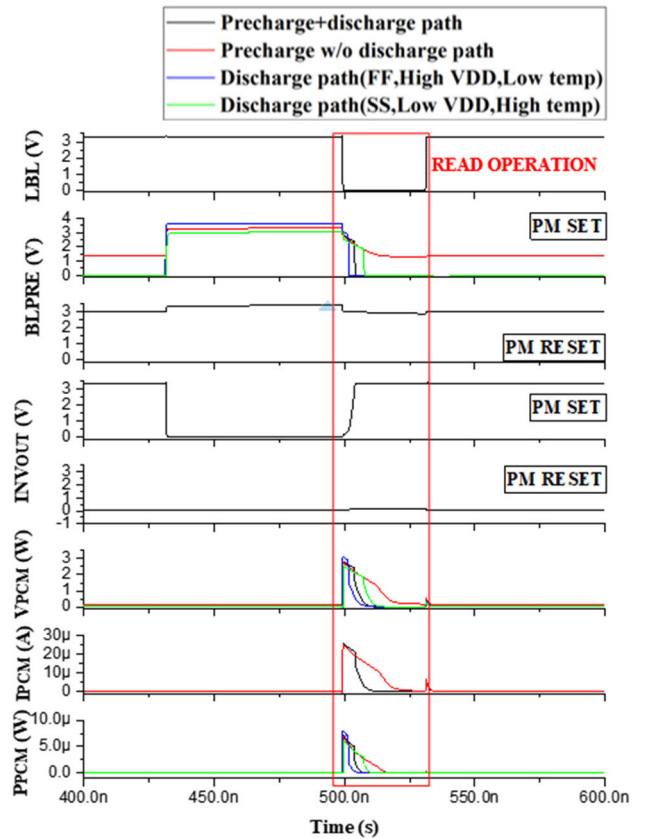


FIGURE 5. The waveform of the pre-charge scheme with discharge path circuit and without discharge path circuit.

proposed discharge path circuit can be used for readout sensing purposes as well as overcurrent protection. This removes the need for additional sense amplifiers for the readout operation.

B. DESIGN CONSIDERATIONS

The discharging speed of the proposed discharge-path circuit is affected by the parasitic loading capacitance at BLPRE. The discharge timing adjusted by the value of V_{pre} ; the precharge voltage at the coupling capacitor output. The size of the coupling capacitor (C_c) has to be large enough to provide sufficient voltage to trigger the sensing inverter.

Fig. 5 shows the simulation results of the PCM cell during the read operation. It is shown that the voltage of BLPRE node is reduced when the PM is in the set state, while V_{BLPRE} is maintained when the PM is in the reset state. If the discharge-path circuit is not used, the charge stored at BLPRE is discharged solely by the PCM cell, which increases the readout time and stresses the PCM device. However, as shown in the figure, when the discharge path is used, the pre-charged V_{BLPRE} is pulled down promptly by the discharging transistor. The robust operation of the proposed discharge-path circuit is verified across corners as indicated in Fig. 5.

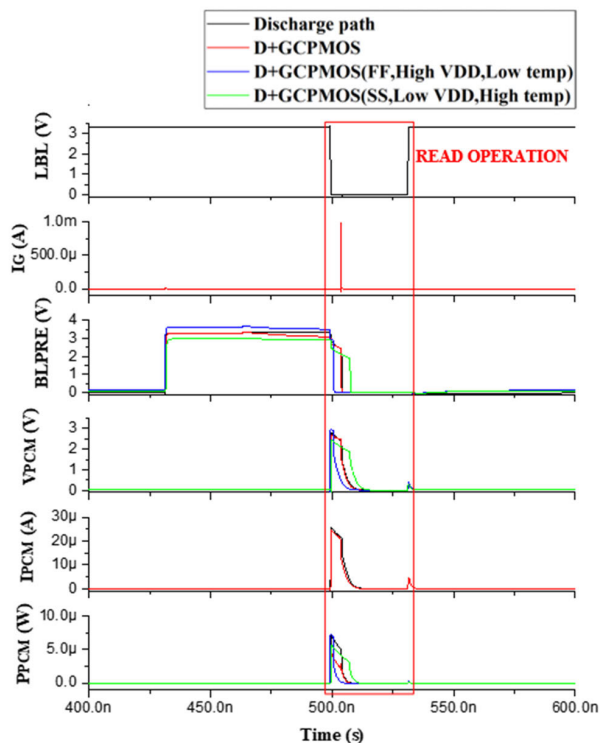


FIGURE 6. The waveform of the pre-charge scheme with discharge path circuit and GCPMOS when PM state is set.

IV. GCPMOS

While the discharge path circuit helps to protect the PM cell by removing the residual charge promptly, the PM cell is still susceptible to the initial current stress before the feedback-based discharge path is turned on. The impact of the initial stress could be significant as the value of the PCM current (I_{PCM}) gets higher when the cell is just turned on (Fig. 5). Therefore, we introduce two additional techniques, GCPMOS, and feed-forward current mirror, to reduce the initial current level.

The GCPMOS is a circuit generally used to reduce the electrostatic discharge (ESD) damage [30], [31] in pad cells. Fig. 4(b) shows the architecture of the PCM cells with the discharge path and GCPMOS. When the voltage of the BLPRE node drops, the gate voltage of transistor M1 decreases due to the capacitor coupling (C_{GC}) between BLPRE and the gate of M1, inducing the drain-source current in M1. The value of the C_{GC} is chosen such that the coupling is strong enough to turn on M1. Then the voltage coupling turns on the secondary device M2 by raising its gate voltage. The load resistance R_2 should be therefore sized such that the voltage drop across R_2 ($=I_2R_2$) should be large enough to completely turn on M2. R_1 determines the time constant associated with the GCPMOS operation, which should be long enough to reduce the initial current significantly.

The advantage of the GCPMOS technique is its faster operating speed, compared with the basic discharge path circuit in Section III. While the discharge path circuit requires the signal flow through the feedback path composed of logic

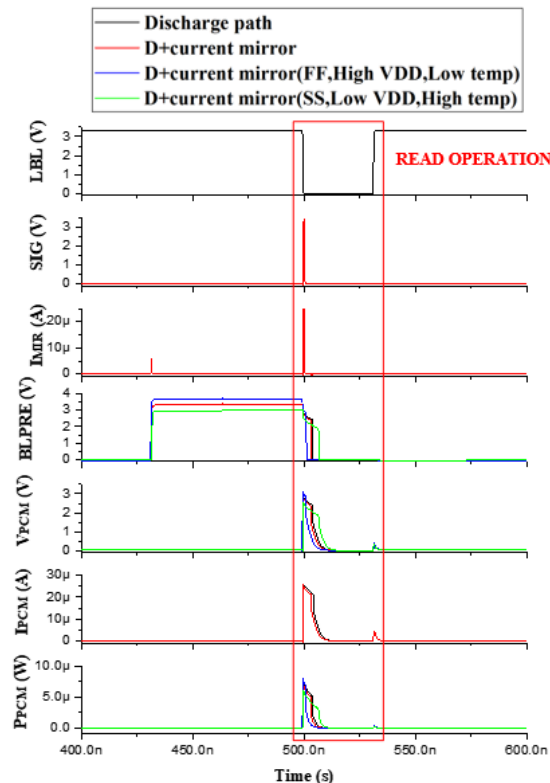


FIGURE 7. The waveform of the pre-charge scheme with discharge path circuit and feed-forward current mirror when PM state is set.

gates to turn on the discharge transistor, the feedback path in the GCPMOS contains only two transistors and passive devices, which take a much shorter time to discharge the current. Therefore, the initial level of the OTS snapback current can be reduced by using the GCPMOS network, as shown in Fig. 6. The P_{PCM} plot in Fig. 6 shows the simulated power dissipation in the PCM device for various structures. It reveals that the GCPMOS technique effectively decrease both the peak and overall power consumption in the PCM cell, which implies a reduced stress level.

V. FEED-FORWARD CURRENT MIRROR

Another method of reducing the initial current stress is the use of feed-forward current mirror. Fig. 4(c) shows the structure of the PCM cell with the discharge path circuit and feed-forward current mirror attached. In the feed-forward current mirror, a switch device is inserted to adjust the time at which the side discharging path is activated before the OTS becomes on-state. The amount of the current flow in the current mirror and its operation time are chosen not to interfere with the original sensing and discharge operation in the main discharge path while still providing a strong initial discharge current flow to reduce the OTS snapback current.

The main difference of the proposed feed-forward current mirror from the discharge-path circuit is its fast operating speed; the discharge path circuit relies on the feedback operation through the sensing chain, and thus, takes a longer time to respond to the initial sharp transient very quickly.

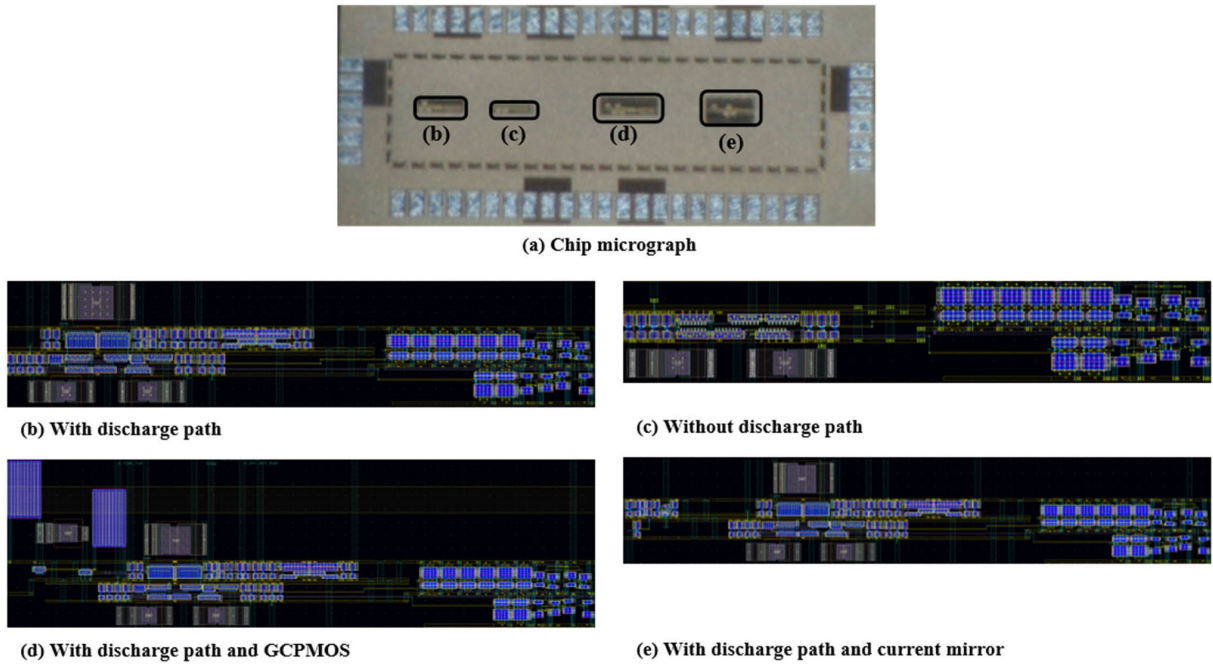


FIGURE 8. (a) Chip micrograph and (b)-(e) layout diagrams of the discharge path circuit, current mirror and GCPMOS.

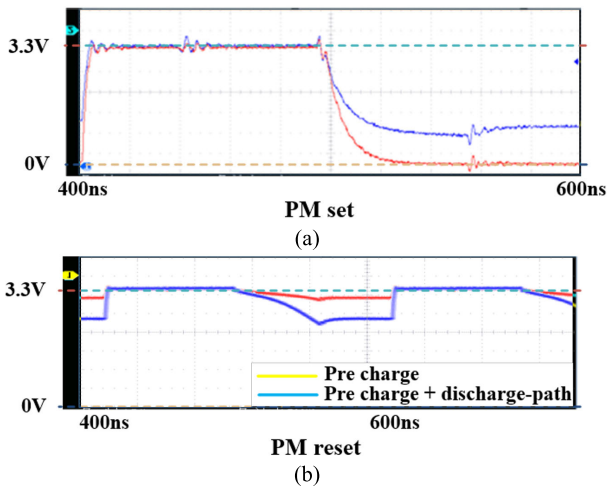


FIGURE 9. Measured voltage transients of PCM cell output (V_{BLPRE}) when (a) PM is in the set state ($R_{PMSET} = 100\text{-k}\Omega$), and (b) PM is in the reset state ($R_{PMRESET} = 3\text{-M}\Omega$) without (blue) and with (red) the discharge path circuit.

To overcome the speed limitation, in the feed-forward current mirror, a switch signal (SIG) turns on the current mirror before the snapback current occurs, as shown in Fig. 7, reducing the initial level of the OTS snapback current. Therefore, as shown in the P_{PCM} graph in Fig. 7, the initial peak power dissipation in the PCM cell is reduced by the use of the feed-forward current mirror.

VI. MEASUREMENT RESULTS

The discharge path circuit including the feedforward current mirror and GCPMOS is verified in a 180-nm CMOS process.

A chip micrograph is shown in Fig. 8. The active area of the proposed circuit is 0.19 mm^2 , excluding pads, test circuits, and decoupling capacitors. The PCM sensing circuit reads NRZ data at 1MHz frequency. The size of the PMOS transistors is $8/0.3\mu\text{m}$, and the size of the NMOS transistors is $8/0.35\mu\text{m}$ in the PCM modeling circuit. A $3\text{-M}\Omega$ poly resistor is used to model an OTS device in the off state and a $100\text{-k}\Omega$ poly resistor is used for the OTS in the on state. A 100-fF and a 50-fF capacitor are used to model parasitic loading capacitances at the BLPRE and WLPRE nodes, respectively. In the discharge-path circuit, an $8/0.35\mu\text{m}$ sized PMOS transistor is used for the pre-charging device to V_{PRE} ($=2.2\text{ V}$), and the size of the NMOS transistor for discharging is $40/0.35\mu\text{m}$. A 200-fF capacitor is used to implement the coupling capacitor C_c . In the GCPMOS, an additional 76-fF capacitor is used for the coupling to the GCPMOS path.

Fig. 9 shows the measured BLPRE signals when the discharge path is turned off (yellow) and one (cyan). The PM device in the set state is modeled by a $100\text{-k}\Omega$ resistor (R_{PMSET}), while the off-state device is modeled by a $3\text{-M}\Omega$ resistor ($R_{PMRESET}$). As shown in Fig. 9(a), when the PM is in the set state, the discharge path circuit is triggered, pulling down the voltage at BLPRE to 0 V, while it takes a much long time to discharge the node with only the PCM cell is connected to BLPRE. As the discharge-path is activated by the capacitive-coupled inverter, the sensing function of the discharge path is inspected.

Fig. 10 shows the measurement results comparing the voltage, current, power dissipation, and total amount of energy in various test cases (no additional circuit is used except the conventional pre-charge scheme, the discharge-path circuit

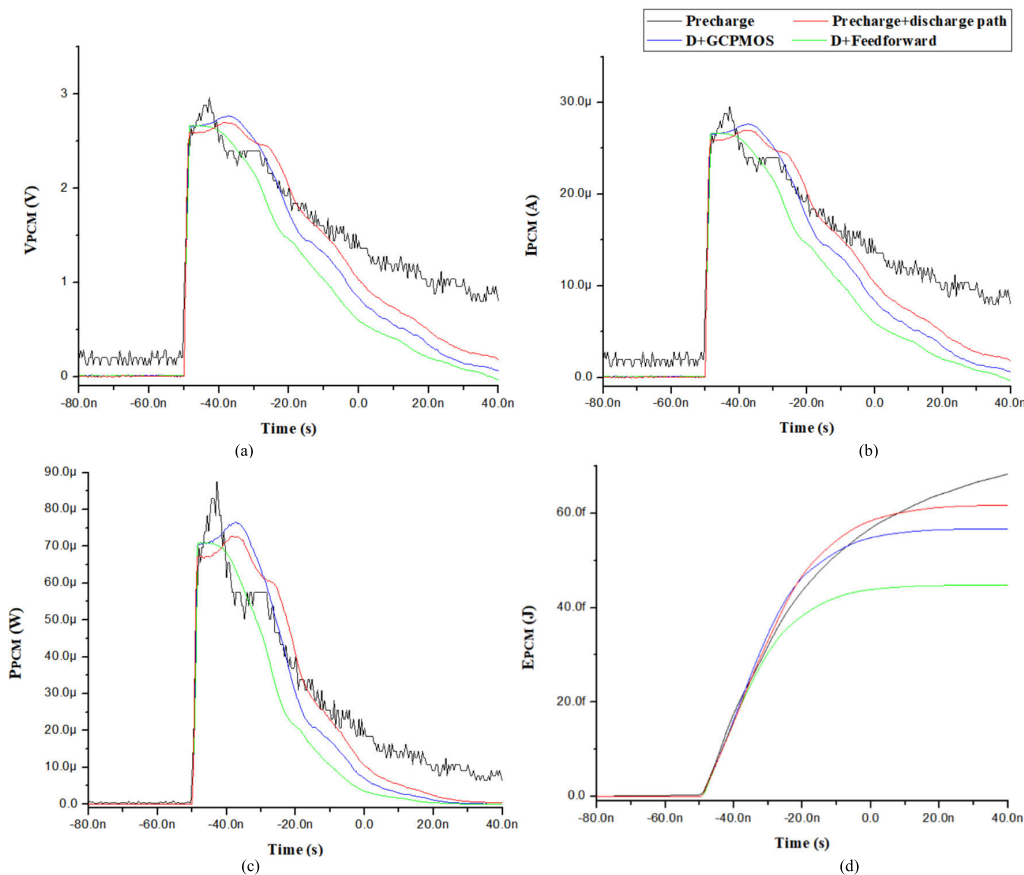


FIGURE 10. Measured (a) voltage of PCM cell (V_{PCM}), (b) current of PCM cell (I_{PCM}), (c) power of PCM cell (P_{PCM}), and (d) Energy of PCM cell (E_{PCM}), when the discharge-path circuit is not used (black), the discharge-path circuit is used (red), the GCPMOS circuit is used with the discharge-path circuit (blue), and the feed-forward current mirror is used with the discharge-path circuit (green).

TABLE 1. Performance summary.

	Conventional Pre-charge Scheme	Current Mirror with Comparator [32]	2-stage Full Cross-Coupled Latch [33]	Current Mirror with Comparator [34]	Single Stage Full Cross-Coupled Latch [35]	2-stage, Half Latch [36]	Discharge Path Circuit	Discharge Path with GCPMOS	Discharge Path with Current Mirror
Process [nm]	180	350	40	130	180	110	180	180	180
Area [mm^2]	0.00003	-	-	0.00003	-	-	0.03	0.05	0.043
Number of Transistors	10	13 and 2 stage Differential Amp in comparator	16 and trimming NMOS switches	12 and 2 stage Differential Amp in comparator	8 in first stage	16	18	20	22
Supply Voltage[V]	3.3	1.8	1.1	1.2	1.8	1.2	3.3	3.3	3.3
Peak Current [A]	29.6u						26.9u	27.6u	26.6u
Peak Power [W]	87.5 u	-	-	-	-	-	72.6 u	76.6 u	71.1 u
E_{PCM} [J]	68.3 f	-	-	-	-	-	61.7 f	56.7 f	44.7 f
Snapback protection	X	X	X	X	X	X	O	O	O

is used, the GCPMOS is used in combination with the discharge-path circuit, and the feed-forward current mirror is used with the discharge-path circuit). The voltage, current,

and power consumption of the PCM structure with the discharge path circuit (red color) decreased faster than the baseline case (black color), while the total energy consumption is

also decreased by 9.7% (−6.6 fJ). As the total energy applied to the PCM cell decreases, the damage inflicted on the PCM cell during read operations is also reduced.

When the GCPMOS technique is applied in addition to the discharge-path scheme, the circuit exhibited a faster-discharging speed on the PCM cell, lowering the energy consumption of the PCM cell by 17% (−11.6 fJ) compared with the baseline case. In the feed-forward current mirror case, the energy consumption is observed to be reduced by 34.6% (−23.6 fJ).

Table 1 shows the performance summary of this work and comparisons with prior works. Compared with the conventional pre-charge scheme, our discharge-path achieved a lower peak current (26.9 μ A) and E_{PCM} (61.7fJ, 90.3% of the conventional pre-charge scheme). The discharge path circuit with GCPMOS consumes 27.6A peak current and 56.7fJ cell energy (83% of the conventional pre-charge scheme). The discharge path circuit with feed-forward current mirror consumes 26.6 μ A peak current (90% of the conventional pre-charge scheme) and 44.7fJ cell energy (65.4% of the conventional pre-charge scheme). The proposed sensing schemes achieve the superior snapback current protection mechanism and comparable performances with the state-of-the-art works.

VII. CONCLUSION

The proposed discharge-path-based sensing scheme reduces the damage to the PCM cell while implementing the sensing function without using additional sense amplifiers. The PRAM structure with a discharge path circuit and feed-forward current mirror are applied has more than 45% reduced energy consumption than the conventional pre-charge scheme. When the GCPMOS technique is applied, the design achieves more than 28% reduced energy consumption than the conventional pre-charge scheme.

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