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ABSTRACT

In this Letter, we report a demonstration of p-channel tin monoxide (SnO) thin-film transistors (TFTs) with high field-effect mobility (μ_{FE}) exceeding 10 cm^2/Vs and hysteresis-free like behavior. We demonstrate that maintaining metallic states before encapsulation is a key process to enhance μ_{FE} in p-type SnO thin-films. Sustaining this meta-stability involves the following two processes during fabrication: (1) postdeposition annealing (PDA) in two steps and (2) encapsulation in the middle of each PDA. This simple process not only suppresses creation of oxidized states such as adverse Sn^{4+} but also facilitates the lateral growth of crystals with improved crystallinity by interfacial energy stabilization. The resultant SnO TFT reveals a record-high μ_{FE} up to 15.8 cm^2/Vs with a negligible hysteresis of 0.1 V. This study suggests a practical route to grant high μ_{FE} to p-channel SnO TFTs without any dopant or complex postdeposition treatment.

Oxide semiconductors are one of the strongest candidates for upper-layer devices in monolithic three-dimensional integration, a cutting edge complementary metal oxide semiconductor (CMOS) technology, because they possess outstanding advantages such as a moderate field-effect mobility (μ_{FE}), an extremely low off-current, a great uniformity, and low temperature processibility.[1–10] These fascinating characteristics mainly originate from their conduction band (*CB*) edge composed of effective intercalation of isotropic, spherical metal cation *ns* ($n \geq 4$) orbitals, which allow a great electron conduction path and a low effective mass (m_e^*) even in an amorphous structure. Moreover, facile processibility using CMOS-compatible methods such as physical/chemical vapor deposition, including magnetron sputtering and atomic layer deposition (ALD), makes them more attractive. However, the valence band (*VB*) edge generally originates from overlap of anisotropic oxygen *2p* orbitals with a small ionic radius in oxide semiconductors, which significantly localizes hole conduction path and results in large hole effective mass (m_h^*).[11] Furthermore, free holes are difficult to generate in the oxide semiconductor family due to high formation energies of cation vacancies.[11] To make matters worse, many of the created holes are easily compensated by native hole killers like oxygen vacancies (V_O), complicating the p-type conduction in most of the oxide semiconductors.

Tin monoxide (SnO) is one of the few oxide semiconductors that can exclusively reveal p-type behavior. It has intensively been studied owing to its advantages such as higher μ_{FE} and lower fabrication temperature than copper-based p-type oxide semiconductors.[11–16] Nevertheless, μ_{FE} stays at the level of ≤ 5 cm^2/Vs, which emphasizes a necessity to improve μ_{FE} in SnO thin-film transistors (TFTs). Furthermore, the large hysteresis frequently observed in p-channel SnO TFTs must be removed because it reduces the noise margin and increases delay variations in their potential CMOS logic applications. Here, this study reports a fabrication method of p-channel SnO TFTs with μ_{FE} exceeding 10 cm^2/Vs and negligible hysteresis of 0.1 V. Intermediate encapsulation helps accelerate lateral growth of crystals with improved crystallinity as well as prevents formation of oxidized states. As a result of this improved crystallization, the corresponding TFTs show device performances, including an unprecedentedly high μ_{FE} of 14.6 ± 1.5 cm^2/Vs and a negligible hysteresis of 0.1 ± 0.1 V with an $I_{ON/OFF}$ of $(3.4 \pm 0.9) \times 10^3$.

A 12-nm-thick hafnium-zirconium oxide (HZO) thin-film was deposited using tetrakis(ethyl-methyl-amino) hafnium and tetrakis(ethyl-methyl-amino) zirconium as the Hf and Zr sources, respectively, in the plasma-enhanced atomic layer deposition (PEALD) process at 200 °C under 1 Torr. A 4-nm-thick aluminum oxide (Al_2O_3) thin-film was deposited on top of the HZO thin-film using tri-methyl-aluminum as the Al source at 150 °C under 1 Torr. Oxygen plasma was used for oxidation in these PEALD processes. Then, postdeposition annealing (PDA) was conducted at 500 °C in ambient air.

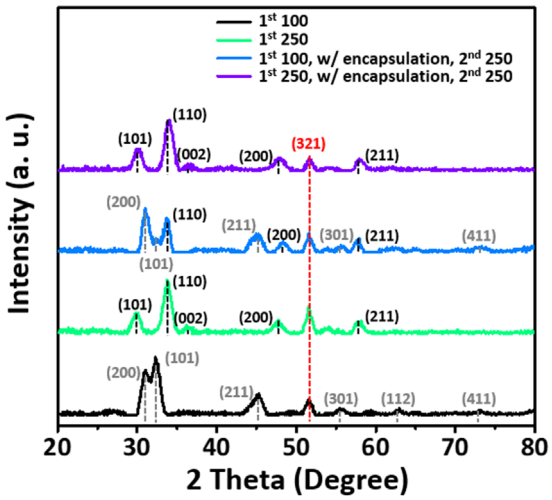

FIG. 1. XRD patterns of SnO thin-films with different postdeposition conditions. Gray, black, and red dashed lines represent tetragonal Sn, tetragonal SnO, and cubic Si references, respectively.

The 20-nm-thick SnO thin-films were deposited on Al_2O_3/HZO/degenerated Si substrates through reactive magnetron sputtering using a metal Sn target (99.999%, iTASCO) at room temperature. Al_2O_3/HZO and Si act as the gate dielectric and electrode, respectively, in a transistor. The base and working pressures in a chamber were 3×10^{-6} and 5×10^{-3} Torr, respectively. The flow rates of O_2 and Ar during the deposition were 2 and 49 sccm, respectively (O_2/Ar ratio of 3.9%). Deposited thin-films were annealed at temperatures of 100 or 250 °C for 1 h in ambient air, respectively, which will be mentioned as the first PDA temperature (T_A^{1st}) throughout this paper. Then, 100-nm-thick indium-tin-oxide (ITO) thin-films were deposited as source/drain (S/D) electrodes at room temperature through the magnetron sputtering using an ITO target (In:Sn = 9:1, 99.999%, iTASCO). Both the channel and S/D electrodes were patterned for 500 (width) and 100 (length) μm (W/L = 500/100 μm), respectively, using metal shadow masks for the bottom-gate, top-contact TFTs. The 10-nm-thick Al_2O_3 thin-films were deposited for encapsulation on top of SnO thin-films through PEALD process at 100 °C under 1 Torr. Subsequent annealing was further conducted on encapsulated thin-films at 250 °C for 1 h in ambient air, which will be referred to as the second PDA temperature (T_A^{2nd}). Figure 1 of the supplementary material shows a cross-sectional schematic of the TFT structure with an overall procedure of its fabrication.

X-ray diffraction (XRD) analyses were conducted on SnO thin-films with different postdeposition conditions to investigate the evolution of the crystalline structure depending on T_A^{1st} and encapsulation (Fig. 1). It was confirmed that the crystalline structure of unencapsulated SnO thin-films with T_A^{1st} of 100 °C is tetragonal Sn (JCPDS Card No. 04–0673), which is attributed to metallic Sn states that dominantly exist due to the low T_A^{1st} not enough to fully oxidize the SnO thin-film. The crystalline structure is transformed to tetragonal SnO (JCPDS Card No. 06–0395) with T_A^{1st} increasing up to 250 °C. However, an encapsulated SnO thin-film with T_A^{1st} of 100 °C consists of the mixed structure of tetragonal Sn and SnO after annealing at T_A^{2nd} of 250 °C, which can result from the anti-oxidation by an Al_2O_3 encapsulation layer. Furthermore, the tetragonal SnO crystallites with (001) surface orientation grow unlike the other conditions. Meanwhile, there is no noticeable difference originating from the intermediate Al_2O_3 encapsulation in the crystalline structure of SnO thin-films with the T_A^{1st} of 250 °C.

To examine nanoscale differences, we performed cross-sectional high-resolution transmission electron microscopy (HRTEM) analyses on the SnO thin-films [Figs. 2(a)–2(c)]. The unencapsulated SnO thin-film with a T_A^{1st} of 100 °C shows a significantly undulating shape as shown in Fig. 2 of the supplementary material. Selected area electron diffraction (SAED) patterns indicate the growth of tetragonal Sn crystals [Fig. 2(a)]. The unencapsulated SnO thin-film with T_A^{1st} of 250 °C has an undulating surface with a number of protrusions (Fig. 2 in the supplementary material). In detail, it shows a mixed structure with the amorphous and tetragonal SnO, where numerous tetragonal SnO crystals are on the amorphous phase [Fig. 2(b)]. Encapsulation greatly affects the crystalline structure of SnO thin-films with a T_A^{1st} of 100 °C, where an Al_2O_3 encapsulation layer prevents the thin-film from being fully oxidized at T_A^{2nd} of 250 °C. More importantly, it can

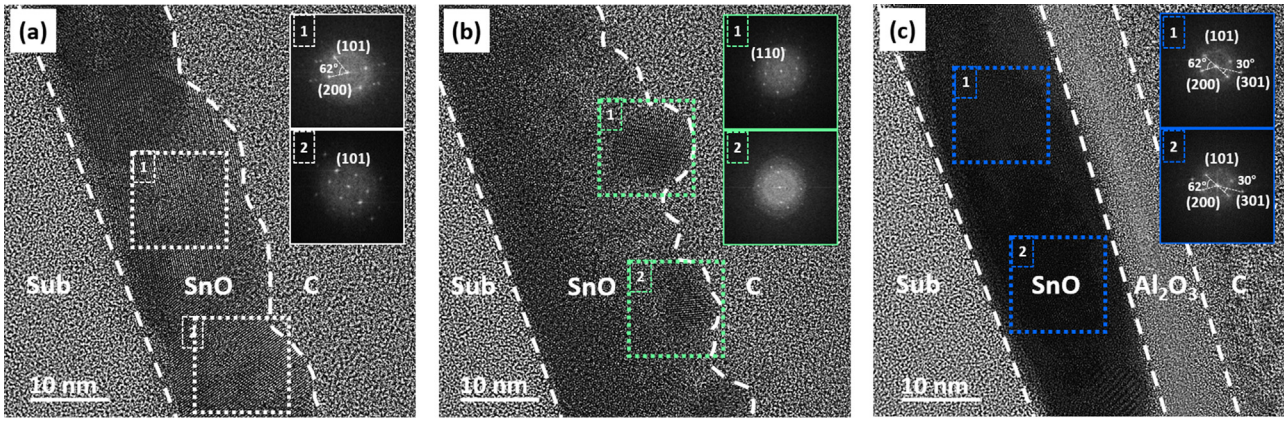

FIG. 2. Cross-sectional HRTEM images of SnO thin-films with different postdeposition conditions: (a) T_A^{1st} of 100 °C without encapsulation, (b) T_A^{1st} of 250 °C without encapsulation, and (c) T_A^{1st} of 100 °C and subsequent encapsulation followed by T_A^{2nd} of 250 °C.

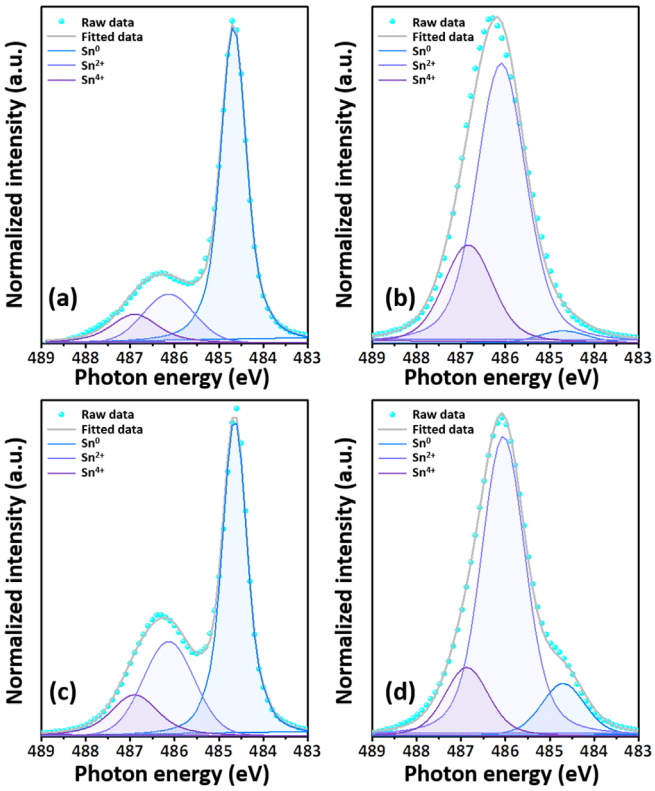

FIG. 3. Sn $3d_{5/2}$ XPS spectra of SnO thin-films with different postdeposition conditions including metallic Sn, Sn^{2+}, and Sn^{4+} states: (a) T_A^{1st} of 100 °C without encapsulation, (b) T_A^{1st} of 250 °C without encapsulation, and (c) and (d) are conditions that encapsulation, and T_A^{2nd} of 250 °C processes are further applied to (a) and (b), respectively.

stabilize the interfacial energy of thin-film surface, which facilitates the crystal growth in the thin-film.[17,18] These effects result in the lateral growth of tetragonal Sn as well as tetragonal SnO crystals [Fig. 2(c) and Fig. 3 of the supplementary material]. Moreover, the overall crystallinity is remarkably enhanced, enabling the effective intercalation of hole pathway in *VB* edge. Surface roughness also becomes smoother because of the lateral growth of crystals compared to other conditions even though it still has room to be improved [Fig. 2(c) in the supplementary material]. Note that there was no encapsulation-induced difference in the crystalline structure of SnO thin-films with T_A^{1st} of 250 °C (Fig. 1).

Figure 3 shows x-ray photoelectron spectroscopy (XPS) spectra of Sn $3d_{5/2}$ states in the SnO thin-films with different postdeposition conditions, where the binding energies for the deconvolution of three different Sn states were 484.7 ± 0.1 (Sn0) 486.1 ± 0.1 (Sn^{2+}), and 486.8 ± 0.1 (Sn^{4+}) eV, respectively.[13] With T_A^{1st} increasing from 100 to 250 °C, metallic Sn states decrease, and $Sn^{2+,4+}$ states (hereafter referred to as oxidized Sn states) increase simultaneously. Importantly, the encapsulated SnO thin-film with a T_A^{1st} of 100 °C still has a significant portion of metallic Sn states even after the T_A^{2nd} of 250 °C, which supports our explanation that the Al_2O_3 encapsulation effectively suppresses further oxidation. Note that the encapsulated SnO thin-film with T_A^{1st} of 250 °C has the lower (higher-) fraction of oxidized (metallic) Sn states compared to the unencapsulated, which could be attributed to the reduction process during the deposition of the Al_2O_3 encapsulation layer.[13] The deconvoluted portion of three different Sn states are summarized in Table 1 of the supplementary material. Furthermore, optical characteristics depending on the PDA conditions were evaluated through UV/Visible spectroscopy. Figure 4(a) shows the absorption of SnO thin-films, where it decreases with the increasing T_A^{1st}. This trend is attributed to the decrease (increase) in the metallic (oxidized) Sn states, respectively, as mentioned in the XPS results. Note that the optical characteristics of the encapsulated SnO thin-film with T_A^{1st} of 100 °C also reveals the mixed characteristics of the tetragonal Sn and SnO phases. As a result, its optical bandgap extracted using the Tauc plot is 1.2 eV, which is almost the same with the unencapsulated with T_A^{1st} of 100 °C [Fig. 4(b) and Fig. 4 of the supplementary material]. It is also worth noting that the optical characteristics of SnO thin-films with T_A^{1st} of 250 °C are almost the same irrespective of the encapsulation.

Then, SnO TFTs were demonstrated to investigate electrical characteristics depending on the PDA conditions (Fig. 5). Voltage

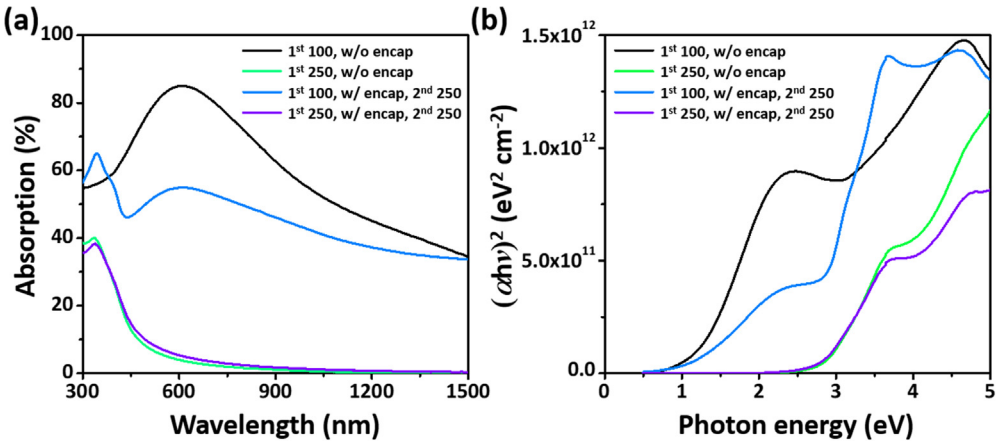

FIG. 4. Optical characteristics of SnO thin films with different postdeposition conditions: (a) absorption and (b) bandgap extraction.

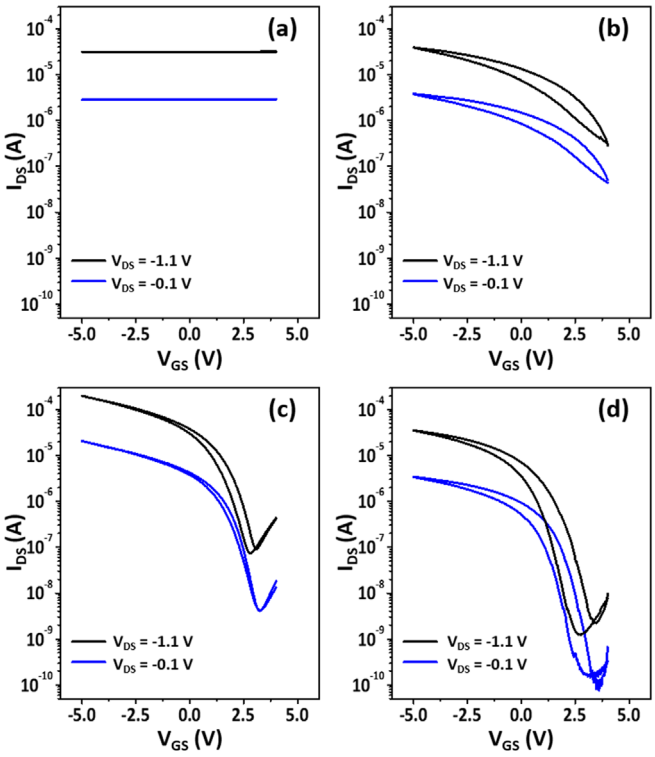

FIG. 5. Transfer characteristics of SnO TFTs with different postdeposition conditions: (a) T_A^{1st} of 100 °C without encapsulation, (b) T_A^{1st} of 250 °C without encapsulation; and (c) and (d) are conditions that encapsulation, and T_A^{2nd} of 250 °C processes are further applied to (a) and (b), respectively.

sweep rate during the measurement was 2.4 V/s. Unencapsulated SnO TFTs with T_A^{1st} of 100 °C exhibit conducting characteristics without a switching capability, which is changed to p-type semiconducting characteristics with a μ_{FE} of 1.7 ± 0.1 cm^2/Vs and an $I_{ON/OFF}$ of (8.1 ± 0.1) × 10^1 at T_A^{1st} of 250 °C. The electrical characteristics are significantly improved after the encapsulation. In particular, encapsulated SnO TFTs with T_A^{1st} of 100 °C reveal a record-high μ_{FE} of 14.6 ± 1.5 cm^2/Vs with an $I_{ON/OFF}$ of (3.4 ± 0.9) × 10^3, a subthreshold swing (*SS*) of 0.6 ± 0.1 V/dec, a threshold voltage (V_{TH}) of 1.6 ± 0.2 V, and a negligible hysteresis of 0.1 ± 0.1 V at drain–source voltage (V_{DS}) of −0.1 V. Given that the metallic Sn is considered a possible mobility booster in p-channel SnO TFTs,[12] the effective crystal intertwining by the lateral growth of tetragonal Sn as well as SnO crystals can make this prominent enhancement in device performances, especially μ_{FE}, through the encapsulation. However, the electrical characteristics are deteriorated in the encapsulated thin-films with T_A^{1st} of 250 °C, where device performances were comparable to the conventional p-channel SnO TFTs in the literature (Table I).[13] Notably, the μ_{FE} significantly decreases down to 1.8 ± 0.1 cm^2/Vs, and the hysteresis is degraded to 1.0 ± 0.2 V. The leakage current is suppressed by increasing T_A^{1st}, which could be attributed to the decrease in hole concentration resulting from the decreased (increased) metallic (oxidized) Sn states.[12] This dramatic change shows the huge implication of the low T_A^{1st} and subsequent encapsulation. It is also worth mentioning that the $I_{ON/OFF}$ of the unencapsulated SnO TFTs with T_A^{1st} of 250 °C is enhanced by more than 10^3 through the encapsulation. The high off-current in p-channel SnO TFTs could be attributed to multivalent Sn states (Sn0, Sn^{2+}, and Sn^{4+}) and narrow indirect bandgap (∼0.7 eV). Electrons can be injected from drain to source electrodes at $V_{GS} > 0$ V by Fermi-level pinning originating from its narrow bandgap, which could increase the current by electron transport in the channel at off-state.[14] The field-effect passivation via electrostatic shielding by a negative charge, such as an oxygen interstitial in the Al_2O_3 encapsulation layer, may partially constitute the reason for this improvement.[11] The encapsulation can also mitigate the ambient effect on the channel layer, which would contribute to the off-current reduction. It hints that the Fermi-level depinning technique through the metal–interlayer–semiconductor contact scheme can be effective to reduce the off-current and improve $I_{ON/OFF}$ for the encapsulated SnO TFTs with T_A^{1st} of 100 °C. The introduction of a double gate structure as well as the decreased channel thickness can be other options to improve $I_{ON/OFF}$ further due to its enhanced gate efficiency.[19]

It is also noteworthy that the hysteresis is revealed in a counterclockwise direction regardless of postdeposition conditions. It indicates that the hysteresis phenomena come from the carrier trapping at the trap sites, including SnO/dielectric interface and/or SnO bulk region rather than the migration of mobile charges in the gate dielectric. Because the encapsulated SnO TFTs with T_A^{1st} of 100 °C show the negligible hysteresis and the corresponding SnO thin-film has the significantly improved surface and crystallinity, it can be inferred that the defects in the channel could be a dominant factor on the revelation of hysteresis.

In conclusion, this study reports a simple route to fabricate high mobility p-channel SnO TFTs with hysteresis-free like behavior using PDA in two steps, especially low T_A^{1st} and intermediate encapsulation. An Al_2O_3 encapsulation layer suppresses thermodynamic oxidation of an underlying SnO thin-film, consequently leaving the significant portion of metallic Sn states. More importantly, it promotes the lateral growth of crystals by interfacial energy stabilization, enabling the

TABLE I. Device performances of SnO TFTs with different postdeposition conditions (at least five devices). Note that the encapsulated devices were subjected to T_A^{2nd} of 250 °C.

	T_A^{1st} 100 °C	T_A^{1st} 250 °C	T_A^{1st} 100 °C w/encapsulation	T_A^{1st} 250 °C w/encapsulation
μ_{FE} (cm^2/Vs)	···	1.7 ± 0.1	14.6 ± 1.5	1.8 ± 0.1
$I_{ON/OFF}$	···	(8.1 ± 0.1) × 10^1	(3.4 ± 0.9) × 10^3	(5.5 ± 0.3) × 10^4
SS (V/dec)	···	···	0.6 ± 0.1	0.7 ± 0.1
V_{TH} (V)	···	2.9 ± 0.1	1.6 ± 0.2	1.6 ± 0.1
Hysteresis (V)	···	1.5 ± 0.2	0.1 ± 0.1	1.0 ± 0.2

effective crystal intermixing of tetragonal Sn and tetragonal SnO crystals with the smooth morphology. The resultant SnO TFTs exhibit device performances with the highest μ_{FE} of $14.6 \pm 1.5\,cm^2/Vs$ and negligible hysteresis, which would contribute to the heterogeneous integration of CMOS TFTs on basis of semiconducting oxide channel layer in the advanced display and 3D semiconductor systems.

See the supplementary material for supplementary experiment methods, cross-sectional HRTEM images, summary of the portion of three different Sn states, and Tauc plot for optical bandgap extraction.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Taikyu Kim: Conceptualization (equal); Formal analysis (equal); Visualization (equal); Writing – original draft (lead). **Hochang Lee:** Conceptualization (equal); Formal analysis (equal); Methodology (equal). **Se Eun Kim:** Data curation (supporting); Formal analysis (supporting); Investigation (supporting). **Jeong-Kyu Kim:** Formal analysis (equal); Writing – original draft (equal). **Jae Kyeong Jeong:** Funding acquisition (lead); Project administration (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).
[2]T. Kim, C. H. Choi, J. S. Hur, D. Ha, B. J. Kuh, Y. Kim, M. H. Cho, S. Kim, and J. K. Jeong, "Progress, Challenges, and Opportunities in Oxide Semiconductor Devices: A Key Building Block for Applications Ranging from Display Backplanes to 3D Integrated Semiconductor Chips," Adv. Mater. 2204663 (published online 2022).
[3]A. Charnas, M. Si, Z. Lin, and P. D. Ye, Appl. Phys. Lett. **118**(5), 052107 (2021).
[4]C. H. Choi, T. Kim, S. Ueda, Y.-S. Shiah, H. Hosono, J. Kim, and J. K. Jeong, ACS Appl. Mater. Interfaces **13**(24), 28451 (2021).
[5]M. Si, Y. Hu, Z. Lin, X. Sun, A. Charnas, D. Zheng, X. Lyu, H. Wang, K. Cho, and P. D. Ye, Nano Lett. **21**(1), 500 (2021).
[6]M. Si, J. Andler, X. Lyu, C. Niu, S. Datta, R. Agrawal, and P. D. Ye, ACS Nano **14**(9), 11542 (2020).
[7]A. Charnas, Z. Lin, Z. Zhang, and P. D. Ye, Appl. Phys. Lett. **119**(25), 263503 (2021).
[8]H. J. Park, T. Kim, M. J. Kim, H. Lee, J. H. Lim, and J. K. Jeong, Ceram. Int. **48**(9), 12806 (2022).
[9]M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, Nat. Electron. **5**(3), 164 (2022).
[10]Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim, and H. Hosono, Nat. Electron. **4**(11), 800 (2021).
[11]T. Kim and J. K. Jeong, Phys. Status Solidi-Rapid Res. Lett. **16**(1), 2100394 (2022).
[12]J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, and H. N. Alshareef, ACS Nano **7**(6), 5160 (2013).
[13]T. Kim, M. J. Kim, H. Lee, H. Xu, C. H. Choi, J.-K. Kim, and J. K. Jeong, IEEE Trans. Electron Devices **68**(9), 4467 (2021).
[14]T. Kim, J.-K. Kim, B. Yoo, H. Xu, S. Yim, S.-H. Kim, H.-Y. Yu, and J. K. Jeong, J. Mater. Chem. C **8**(1), 201 (2020).
[15]S. Yim, T. Kim, B. Yoo, H. Xu, Y. Youn, S. Han, and J. K. Jeong, ACS Appl. Mater. Interfaces **11**(50), 47025 (2019).
[16]T. Kim, B. Yoo, Y. Youn, M. Lee, A. Song, K.-B. Chung, S. Han, and J. K. Jeong, ACS Appl. Mater. Interfaces **11**(43), 40214 (2019).
[17]W. D. Kingery, H. K. Bowen, and D. R. Uhlmann, *Introduction to Ceramics*, 2nd ed. (Wiley, 1975).
[18]T. Kim, C. H. Choi, P. Byeon, M. Lee, A. Song, K.-B. Chung, S. Han, S.-Y. Chung, K.-S. Park, and J. K. Jeong, npj 2D Mater. Appl. **6**(1), 4 (2022).
[19]I. Ferain, C. A. Clinge, and J.-P. Colinge, Nature **479**, 310 (2011).