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Nanoscale floating-gate characteristics of colloidal Au nanoparticles electrostatically assembled on Si nanowires have been investigated. Colloidal Au nanoparticles with ~5 nm diameters were selectively deposited onto the lithographically defined *n*-type Si nanowire surface by 2 min electrophoresis between the channel and the side gates. The device transfer characteristics measured at room temperature showed hysteresis, with the depletion mode cutoff voltage applied by the side gates shifted by as much as 1.5 V, with the source-drain bias at 1.4 V. The results demonstrate that the electrostatic assembly of colloidal Au nanoparticles is a useful method for the fabrication of Si nanowire based nanoscale floating-gate nonvolatile memory structures. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2375083]

I. INTRODUCTION

Flash memories are one of the most widely manufactured nonvolatile memory structures in today's semiconductor industry. Nanoscale processing technology has enabled flash-type floating-gate memories to be integrated at densities far exceeding gigabits per chip with feature sizes below 100 nm.[1] To increase memory density further without sacrificing device performance, the capacitance per floating gate should be reduced to minimize parasitic coupling between adjacent floating gates, and capacitive coupling between the floating gate and the channel should be enhanced. A nanoscale floating-gate nonvolatile memory structure, which was suggested to overcome this problem, was first demonstrated by Tiwari *et al.*, who used Si nanocrystals with ~5 nm diameters on top of gate oxides grown using chemical vapor deposition.[2,3] The discontinuous nanocrystals reduce leakage by reducing conduction paths and the stored charge has a local effect on channel transport, allowing injection oxides to be made thinner and the memory to be operated at lower power and higher speeds. However, growth of Si nanocrystals on oxide surfaces yields a distribution of diameters leading to different island capacitances and gate coupling. Furthermore, due to the nanoscale dimensions, the quantized energy level spacing between adjacent confined electron energy states in the Si nanocrystal may increase, leading to reduced number of charges per nanocrystal. The confinement will also elevate the quantized energy levels above that of the channel, which may increase leakage, reducing retention time.

For large scale integration and increased charge state density, it is desirable to have uniform presynthesized metallic nanocrystals for device-to-device reliability, reduced leakage, and enhanced retention time. To utilize presynthesized solution-based metallic nanocrystals as floating gates for nonvolatile memory application, a reliable method to integrate them onto lithographically defined device positions is required. Many methods have been proposed to achieve ordered colloidal nanoparticle assembly, such as colloidal deposition on chemically functionalized surfaces,[4,5] spin coating, convection-driven assembly,[6] and electrophoretic assembly,[7,8] which produce ordered layers of colloidal particles. Selective positioning of colloidal nanoparticles into lithographically defined structural templates has also been demonstrated;[9,10] this utilizes convection-driven attractive capillary forces between lithographically patterned structured surfaces and colloidal nanoparticles.

In this article, we report on the nanoscale floating-gate characteristics of colloidal Au nanoparticles assembled on Si nanowire device surfaces by electrophoresis. By applying an

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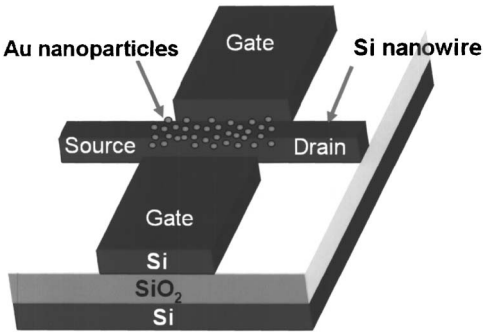

FIG. 1. Schematic diagram of the Si nanowire split side-gate transistor with colloidal Au nanoparticle floating gates.

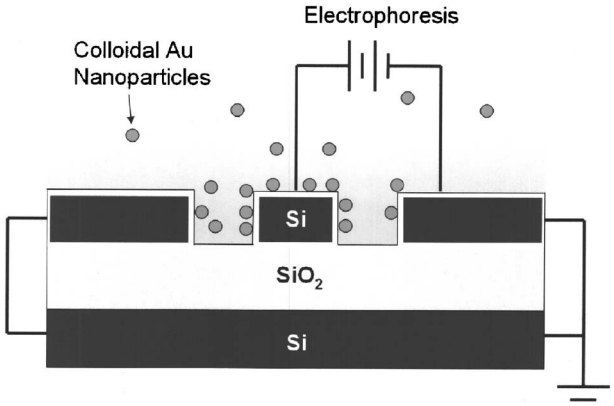

FIG. 2. Schematic diagram of the experimental setup for the electrostatic assembly of colloidal Au nanoparticles on Si nanowire surface.

electric field between the Si nanowires and the adjacent side-gate electrodes, colloidal Au nanoparticles were deposited selectively onto the oxidized Si nanowire surface (see Fig. 1). When positive voltage is applied to the side gates with respect to the *n*-type Si nanowire, electrons may tunnel from the channel on to the Au nanoparticles through the surface oxide. The stored charge on the nanoparticle acts to deplete electrons locally from the Si nanowire channel by Coulomb repulsion. Since this reduces the local electron transport channel width, the Si nanowire drain current is reduced, which in turn lowers the required side-gate voltage to pinch off the channel, thereby resulting in the reduction of the cutoff threshold voltage. The difference in the cutoff threshold voltage results in hysteresis of the transfer characteristics of the Si nanowire, enabling memory operation. The one-dimensional nature of the Si nanowire may enhance the gating effect of the charge stored on the Au nanoparticles, thereby enabling memory operation at reduced floating-gate densities. It was observed that colloidal Au nanoparticles ~5 nm in diameter assembled on ~50 nm *n*-type Si nanowire split side-gate transistor were able to produce a 1.5 V shift in the threshold voltage. The results demonstrate that electrostatic assembly presents a simple and effective method to selectively place colloidal Au nanoparticles on Si nanowire surfaces, and also that the Au nanoparticles function as nanoscale floating gates in a Si-nanowire-type one-dimensional nonvolatile memory structure.

II. DEVICE FABRICATION

We used a highly *n*-type doped (10^{14} cm^{-2}) Si-on-insulator wafer (with the top Si thickness at 70 nm and the buried oxide thickness at 100 nm) as the substrate. 4%, 950 K polymethyl methacrylate is spin coated on the wafer surface to act as the e-beam resist and dry-etch mask. High resolution electron-beam lithography was used to define the self-aligned split side-gate nanowire transistor pattern.[11] Then the pattern was transferred to the top Si layer by reactive ion etching.[12] The resist was moved by oxygen plasma ashing and the Si surface was oxidized at 1000 °C for 10 min to form a thin (~15 nm) gate oxide insulating layer. After contact definition, the solution containing the colloidal Au nanoparticles was dropped on the patterned Si nanowire structure. As shown in Fig. 2, with the substrate and the side gates grounded, 10 V dc electric field was applied between the Si nanowire anode and the side-gate cathode to assemble the nanoparticles electrostatically on the oxidized Si nanowire surface.

III. RESULTS AND DISCUSSION

Figure 3(a) shows the results of ~10 nm colloidal Au nanoparticles electrostatically assembled on an oxidized Si surface. It can be seen that after only 2 min of applied electric field, the Si surface is decorated with Au nanoparticles at a density of ~10^{11} cm^{-2}. Also, there were almost no nanoparticles deposited on the oxide surface, demonstrating that selective deposition of colloidal nanoparticles was possible using patterned electrodes. The 2 min process time was considerably lower than the several hours required for self-assembly methods used to assemble nanoparticles on chemically functionalized structured surfaces[4] and also lower than for template assisted convection-driven assembly which requires the colloidal Au nanoparticle solution to evaporate at steady state conditions.[9,10] To increase nanoparticle density, the process time was extended. However, after 10 min process time, agglomeration and growth of Au nanoparticles on the nanowire sidewall were observed, as shown in Fig. 3(b). This was attributed to current leakage through the oxide layer by prolonged application of high electric fields causing the oxide to break down, leading to effects similar to electroplating. The scanning electron microscopy image of the fabricated Si nanowire split side-gate transistor structure with ~5 nm Au nanoparticles is shown in Fig. 3(c). The nanowire transport channel was ~50 nm and the self-aligned split gates form ~50 nm gaps with the nanowire.

The device transfer characteristics were measured in vacuum at room temperature and are shown in Fig. 4. Initially without Au nanoparticle deposition, the threshold voltage shift ΔV_T was measured to be ~0.14 V [see Fig. 4(a)], which was attributed to the effect of charge trap sites on the exposed Si nanowire surface. The measurements taken after Au nanoparticle assembly, shown in Fig. 4(b), clearly show that the hysteretic behavior to applied side-gate voltages has

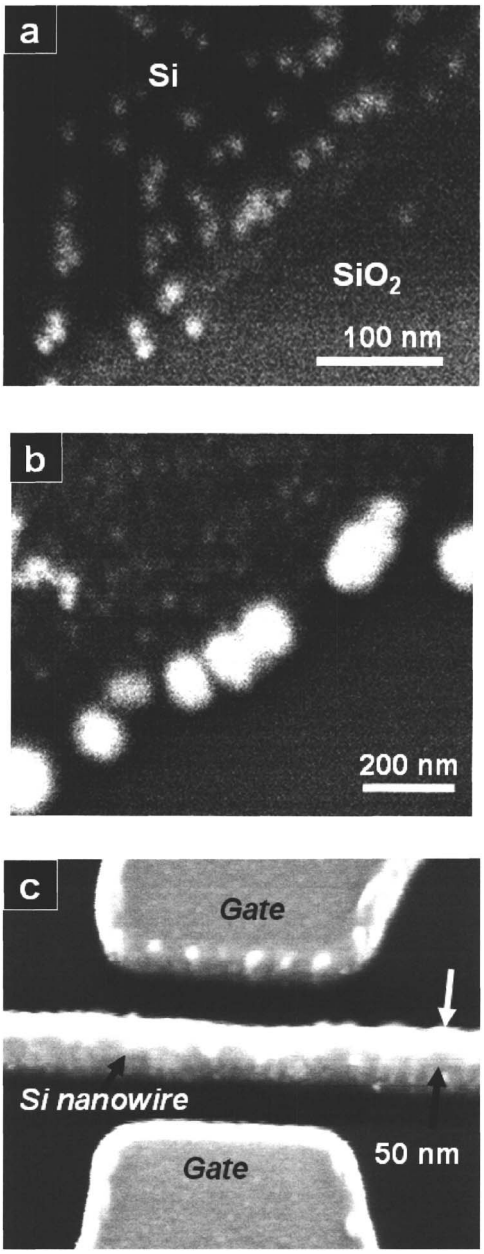

FIG. 3. Scanning electron micrographs of (a) 10 nm Au nanoparticles assembled on oxidized Si surface with 2 min electrophoresis, (b) 10 nm Au nanoparticles assembled with 10 min electrophoresis, and (c) completed device structure using 5 nm Au nanoparticles.

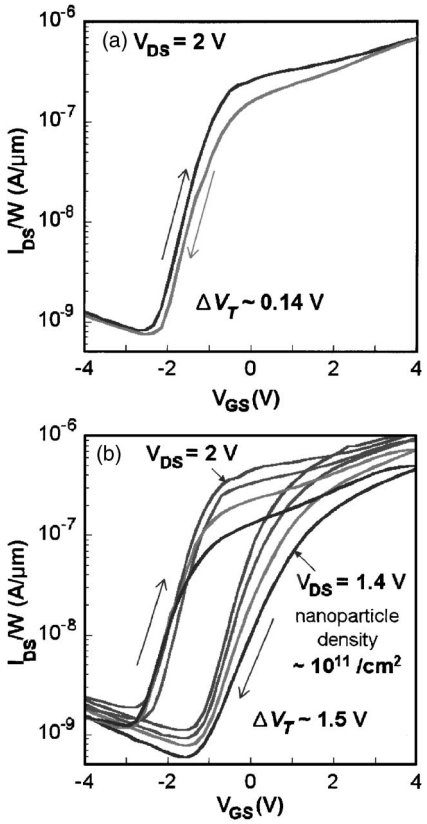

FIG. 4. Dependence of drain current on applied side-gate voltage (a) before Au nanoparticle electrophoresis and (b) after Au nanoparticle assembly. The source-drain bias was changed from 1.4 to 2 V in 0.2 V steps. The two side gates were shorted. The measurements were taken at room temperature.

increased significantly. As the voltage initially increases from a high negative value, which depletes the channel of carriers, the channel width increases and the drain current increases accordingly until the depletion region disappears. Further increase in gate voltage results in band bending and accumulation of electrons at the Si surface. When higher gate voltage was applied, electrons may tunnel through the surface oxide layer onto the Au nanoparticles. Upon reduction of the side-gate voltage, the corresponding drain current was reduced due to the added gating effect of the stored charges on the Au nanoparticles. From Fig. 4(b), it can be seen that ΔV_T has increased to $\sim$1.5 V. The high ΔV_T may be due to the one-dimensional nature of the Si nanowire, where increased ratio of channel surface area of channel cross section resulted in the charged Au nanoparticles having enhanced scattering effect on the channel transport.[12] Below threshold, leakage currents in the $\sim 10^{-12}$ A ($\sim 10^{-10}$ A/μm) range were detected and these reduced the on/off current ratio ($<10^3$). This may be due to leakage through the etched Si/SiO_2 interface. The retention time measurements showed (see Fig. 5) that

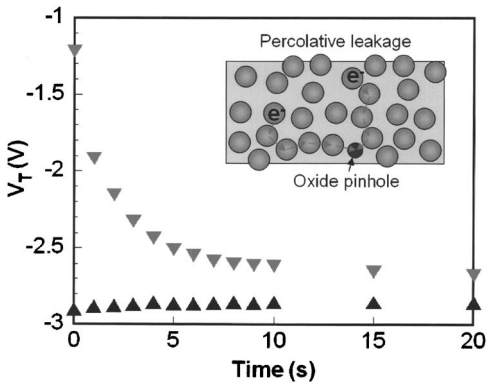

FIG. 5. Time dependence of the threshold voltage. The threshold voltages were measured after application of 1 s and $V_G = +10$ V to program (▼) and $V_G = -10$ V to erase (▲). The inset shows an illustration of the percolative leakage.

ΔV_T was exponentially reduced to ~0.24 V after 10 s and saturates to ~0.18 V. The poor retention characteristics are attributed to percolative leakage caused by assembled Au nanoparticles forming a leakage path to the channel through possible pinholes in the oxide layer. Although the average distance between nanoparticles at a density of 10^{11} cm^{-2} is ~25 nm, there is no way to prevent Au nanoparticles from sticking to each other. Also, the adhesion is mediated only by van der Waals forces and the applied gate potential creates high electric fields which may allow the adhered nanoparticles to migrate on the surface to lower potential sites. To reduce leakage, a core/shell-type nanoparticle, where a Au core is insulated by a SiO_2 insulating shell, may be utilized to prevent charge percolation.[13] Also further incorporation of a top surface insulation layer may help stabilize the adhered nanoparticles.

IV. CONCLUSION

We have investigated the nanoscale floating-gate characteristics of colloidal Au nanoparticles electrostatically assembled on Si nanowire split-gate transistor surfaces. The 5 nm Au nanoparticles on the surface oxide of 50 nm Si nanowires enabled the threshold voltage to shift by more than 1.5 V. The enhanced gating effect may be due to the narrow channel cross section increasing the gate dependent scattering. It may be possible to utilize the electrostatic assembly of colloidal Au nanoparticle on Si nanowire device structure for future nanoscale nonvolatile memory applications.

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[1]Al Fazio, MRS Bull. **29**, 814 (2004).
[2]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Carbbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996); S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, *ibid.* **69**, 1232 (1996).
[3]H. Kim *et al.*, Appl. Phys. Lett. **83**, 4619 (2003).
[4]T. Sato and H. Ahmed, Appl. Phys. Lett. **70**, 2759 (1997).
[5]D. L. Klein, R. Roth, A. K. L. Lim, A. P. Alivisatos, and P. L. McEuen, Nature (London) **389**, 699 (1997).
[6]P. Jiang, J. F. Bertone, K. S. Hwang, and V. L. Colvin, Chem. Mater. **11**, 2132 (1999).
[7]M. Trau, D. A. Saville, and I. A. Aksay, Science **272**, 706 (1996).
[8]R. C. Hayward, D. A. Saville, and I. A. Aksay, Nature (London) **404**, 56 (2000).
[9]Y. Yin, Y. Lu, B. Gates, and Y. Xia, J. Am. Chem. Soc. **123**, 8718 (2001).
[10]Y. Cui, M. T. Bjolrk, J. A. Liddle, C. Sonnichsen, B. Boussert, and A. P. Alivisatos, Nano Lett. **4**, 1093 (2004).
[11]R. A. Smith and H. Ahmed, Appl. Phys. Lett. **71**, 3838 (1997).
[12]G. Molas *et al.*, IEEE Trans. Nanotechnol. **3**, 42 (2004).
[13]Y. Lu, Y. Yin, Z.-Y. Li, and Y. Xia, Nano Lett. **2**, 785 (2002).